Comprehensive Modeling of a Back-to-Back Diodes-Based Linear Variable Capacitor

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***Abstract*—The parasitic nonlinear capacitance of diodes is well-known in power electronics literature. This manuscript analytically describes how the nonlinear parasitic capacitance of two back-to-back reverse-biased diodes can act as a linear variable capacitor (LVC) when driven from an ac current or voltage source. An LVC is a bipolar symmetric structure whose conduction principle is based on the displacement current flowing through the junction capacitance of diodes, and no biasing circuit is needed. The manuscript analytically describes the LVC capacitance dependence on the circuit (current, voltage, and frequency) and diode parameters. An in-depth current- and voltage-based LVC capacitance modeling is presented, including the harmonic analysis, safe operation boundary, and the impact of parasitics. SPICE simulations were used to verify the proposed modeling methodology, followed by experiments on three LVCs made of Schottky diodes. The nonlinear capacitance of the diodes is first characterized for differential capacitance, and then, derived parameters are used to verify the proposed LVC capacitance model with current sources at 1 and 2 MHz. The proposed framework can be used to design resonant power circuits with the LVC as a passive component. An integrated LVC can be applied in high-frequency power circuits for load impedance transformation and power control.**

***Index Terms*—Device modeling, heterostructure barrier varactor (HBV), nonlinear capacitance, parasitic capacitance.**

I. Introduction

THE introduction of wide bandgap devices and soft-switching designs has boosted the operating frequencies of power converters to the megahertz range. Lee et al. [1] identify power control as one of the critical challenges of megahertz operation. The majority of reported approaches utilized sensing and active frequency-based feedback control for load regulation [1], [2]. As per Federal Communications Commission requirements, the limited bandwidth at the Industrial, Scientific, and Medical (ISM) band frequencies can cause a significant challenge to frequency-based controller implementation [3]. Moreover, utilizing a variable switching frequency complicates filter designs and worsens the converter's electromagnetic interference (EMI) performance [4]. Variable passive devices, particularly those not utilizing auxiliary switching [5] or active biasing circuits [6], [7] represent an addition or even a full alternative to frequency regulation that can mitigate load variation and enable constant frequency operation.

Manuscript received 4 April 2023; revised 30 July 2023 and 24 September 2023; accepted 11 November 2023. Date of publication 22 November 2023; date of current version 22 December 2023. Recommended for publication by Associate Editor M. Vitelli. *(Corresponding author: Zeljko Pantic.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3335344.

Digital Object Identifier 10.1109/TPEL.2023.3335344

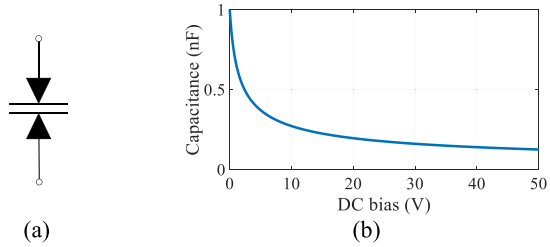

Fig. 1. (a) Symbol of an HBV/LVC (b) Typical nonlinear capacitance of a p-n junction diode.

The impedance transformation networks are used to reduce the load variation range, thus reducing the frequency variation range for power control [8], [9]. However, they increase circuit complexity and add extra losses. A solution with a single passive magnetic component has been proposed in [10] and [11] by deploying nonlinear saturable inductors as Duffing resonators to regulate power in wireless power transfer (WPT) systems operating at low frequencies (30 kHz). In the megahertz range, the core losses are often prohibitive, thus limiting the applicability of saturable inductor-based control to a sub-megahertz range. Another passive method to combat load variation is using the nonlinear parasitic capacitance of two back-to-back reverse-biased diodes [12], [13], [14], [15], [16]. The advantages of this method are that back-to-back reverse-biased diodes act as a variable capacitor, and no biasing circuit is needed for operation. The circuit has a lower footprint than magnetic devices and generates a negligible loss. An integrated back-to-back diode structure is traditionally called a heterostructure barrier varactor (HBV), and its symbol is shown in Fig. 1(a).

An HBV is a semiconductor device that demonstrates voltage- and current-dependent capacitance and does not require a biasing circuit [17]. It is made from two or more semiconductor materials layered together to form a single device. The HBV is a bipolar symmetric structure whose conduction principle is based on the displacement current flowing through the junction capacitance of diodes. A typical nonlinear capacitance profile of a p-n Junction diode is shown in Fig. 1(b). A traditional application of an HBV structure is in low-power systems (100-mW range) to generate high-frequency signals in the gigahertz range from a low-frequency input. Although the original HBV is proposed as a single semiconductor device, it can be equally implemented

TABLE I
DIFFERENT METHODS USING SOLELY PASSIVE COMPONENTS FOR MITIGATING LOAD VARIATION

Paper	Method	Contribution	Challenges
[8], [9]	Matching networks	Reduce the frequency variation range for power converter operation	Increases circuit complexity and adds extra losses. Bulky design as it requires magnetic components.
[10], [11]	Nonlinear saturable inductors	Used nonlinear inductors as Duffing resonators for WPT with wide coupling variation.	Applicability is limited to the sub-MHz range due to core losses. The variable inductor size is large compared to the optimal design.
[12]-[16]	LVC	LVC acts as compensation capacitors in WPT to stabilize power delivery in variable coupling. The variable equivalent linear capacitance of the LVC acts as negative feedback to regulate output power. The circuit is described by Duffing equation.	The analysis is based on a polynomial approximation of the diode charge model. It does not discuss how diode parameters impact LVC. Lacks accurate capacitance model.
This article	LVC	Derived accurate LVC capacitance models based on diode parameters. Discussed the impact of diode parameters on LVC linearity. Case analysis for junction gradient m=0.5. Effect of package and PCB parasitics on LVC characteristics.	An integrated device needs to be developed to leverage the parasitic capacitance model for improved characteristics.

by a back-to-back connection of two p-n or Schottky diodes. In this manuscript, the realization of an HBV-like structure using discrete diodes for high-frequency power applications is referred to as a linear variable capacitor (LVC).

In [12], [13], [14], [15], and [16], the researchers incorporated an LVC into WPT systems to stabilize the power delivery in a variable coupling environment. The proposed design improves the open-loop power transfer profile. Abdelatty et al. [12] replaced the compensation capacitance on the transmitter side of an *LC–LC*-compensated WPT system with an LVC made of two Schottky diodes. The impact of the variable capacitance is optimized to desensitize the power transferred from the coupling variation. The variable equivalent linear capacitance of the LVC acts as negative feedback to regulate output power. It was reported that the LVC doubled the acceptable misalignment range of the WPT system. In [13], the authors replaced both compensation capacitors of an *LC–LC*-compensated WPT system with an LVC. The results show that the minimum coupling coefficient required for power transfer reduced from 0.3 to 0.12.

Initial work on deploying the LVC in WPT systems indicates numerous application opportunities, as the WPT equivalent circuit consists of a high-frequency inverter connected to an equivalent load. Variations in the coupling due to the magnetic coupler misalignment, tolerance in compensation component values, component aging, or load conditions (such as the one happening during the CC–CV battery charging) can result in changes to the equivalent load. LVCs have the potential to effectively address circuit variation challenges in high-frequency resonant inverters/converters. An accurate LVC model is a prerequisite for its successful deployment in power converters, but a better understanding of the LVC from a power electronics and device perspective is needed. In [13], a high-level description of LVC's charge and capacitance features is presented with simulation results, but analytical models supporting the charge model, harmonics results, and the equivalent capacitance are not discussed. LVCs are fundamentally constructed using diode parasitic capacitance.

Capacitor models commonly express capacitance as a function of capacitor voltage or current as $C = f(V)$ or $C = f(I)$. This research aims to derive similar models for an LVC structure for a typical set of diode parameters and validate the models through experimental testing of selected LVCs. Furthermore, the authors have explored how diode parameters (C_{j0}, V_B, and m) impact LVC characteristics and their operation. As per the authors' knowledge, no existing publication describes how these device parameters relate to LVC characteristics and overall operation. Hence, this manuscript aims to bridge the research gap and offer a fundamental approach to understanding LVC current- and voltage-dependent models. Furthermore, the impact of diode parameters on LVC's linearity is studied, a simplified model is presented for diodes with a 0.5 grading coefficient, and the effect of package and printed circuit board (PCB) parasitics is analyzed. Table I summarizes different methods to mitigate load variation solely based on passive components and highlights the contribution made by this manuscript.

The rest of this article is organized as follows. To provide background, a short review of diode modeling, based on the diode parasitic capacitance model from [18], is presented in Section II-A. Current-based comprehensive capacitance modeling of an LVC is presented in Section II-B. LVC's linearity and the boundary of safe operation are discussed in the same section. Voltage-based capacitance modeling of an LVC is presented in Section III. The analysis for the special case of $m = 0.5$ junction gradient is discussed in Section IV, while the experimental results are presented in Section V. Section VI elaborates on the impact parasitic package and trace inductance have on the LVC model and operation. Finally, Section VII concludes this article. Appendix A contains a comprehensive description of the current-dependent model for case $m = 0.5$ and its underlying derivations. Finally, Appendix B explains the voltage-dependent model for $m = 0.5$, providing insights into the derivation process.

II. DIODE CAPACITANCE AND CURRENT-DEPENDENT LVC MODEL

A. Capacitance Models of p-n and Schottky Diodes

An LVC is a back-to-back connection of two reverse-biased p-n-junction or Schottky diodes. Consequently, the nonlinear capacitance of the diode junction plays a key role in conducting the ac current through the device, and it is essential to understand its model. Therefore, a brief description of the diode parasitic capacitance model adopted from [18] is presented in this section. The latter sections use the model to derive the LVC current and voltage-dependent models.

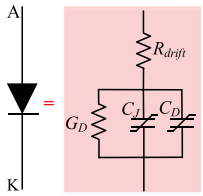

Fig. 2. AC model of a diode.

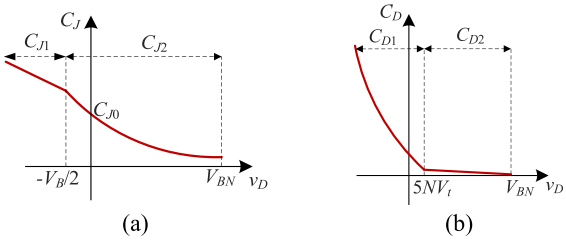

Fig. 3. Typical diode capacitances as a function of diode voltage. (a) Junction capacitance C_J. (b) Diffusion capacitance C_D.

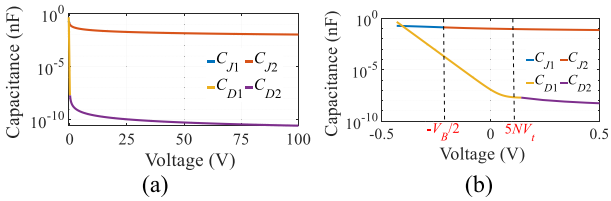

Fig. 4. (a) Capacitance of the RF601BGE2D diode. (b) Zoomed-in view of the low-voltage region. Parameters of the diode are: $C_{j0} = 100$ pF, $m = 0.41$, $V_B = 0.431$, $FC = 0.5$, $I_S = 85$ pA, $N = 1.08$, and $\tau_D = 31$ ns.

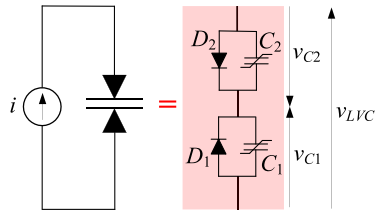

Fig. 5. Equivalent LVC circuit consisting of a diode and a nonlinear capacitor.

In Fig. 2, the ac small-signal diode model is represented by the series resistance R_{drift}, transconductance G_D, differential junction capacitance C_J, and differential diffusion capacitance C_D. The capacitance of a p-n junction diode consists of a parallel combination of C_J and C_D, with C_J dominating the reverse and C_D dominating the forward bias regions. Unlike a p-n junction diode, a Schottky diode utilizes only majority carriers, effectively eliminating C_D. The following analysis is conducted for a more general case of a p-n junction diode, and differences are highlighted where needed.

Fig. 3(a) shows that C_J capacitance depends on the diode voltage v_D. In this manuscript, the sign convention is chosen such that $v_D > 0$ for the reverse biased condition. C_j dependence on v_D can be broadly divided into two regions. In the first region covering voltages $v_D \leq -V_B/2$, the capacitance demonstrates a linear relationship with the diode terminal voltage v_D as

$$C_{J1}(v_D) = \frac{C_{J0}}{(0.5)^{(m+1)}}\left(1 - \frac{(m+1)}{2} - \frac{m v_D}{V_B}\right) \qquad v_D < -\frac{V_B}{2} \tag{1}$$

where V_B is the forward bias junction threshold voltage, m is the grading coefficient, and C_{J0} is a zero-bias junction capacitance. When the diode voltage increases over $-V_B/2$ level and up to the diode breakdown voltage V_{BN} ($-0.5V_B \leq v_D \leq V_{BN}$), the relation becomes the well-known polynomial form

$$C_{J2}(v_D) = C_{J0}(1 + v_D/V_B)^{-m} \qquad -\frac{V_B}{2} \leq v_D \leq V_{BN}. \tag{2}$$

Similarly, C_D depends on v_D, described as follows and shown in Fig. 3(b), again identifying two distinctive zones. In the zone $v_D \leq 5NV_t$ (N is the emission coefficient, and $V_t = 26$ mV at 25 °C is the thermal voltage), the diffusion capacitance increases exponentially with v_D

$$C_{D1}(v_D) = \frac{\tau_D I_S}{NV_t} e^{\left(\frac{v_D}{NV_t}\right)} \qquad -V_B \leq v_D \leq 5NV_t \tag{3}$$

where τ_D is the forward transit time and I_S is the saturation current. In zone $5NV_t < v_D \leq V_{BN}$, the capacitance declines reciprocally with v_D and approaches zero as the diode voltage approaches the breakdown voltage V_{BN} as

$$C_{D2}(v_D) = \tau_D I_S / v_D \qquad 5NV_t \leq v_D < V_{BN}. \tag{4}$$

The parameters for characterizing C_J and C_D can be extracted from a datasheet, as explained in [18]. To model a Schottky diode, one can simply adopt that the forward transit time τ_D is zero ($\tau_D = 0$), effectively eliminating C_D. As an illustration, the capacitance of the diode RF601BGE2D is shown in Fig. 4. In Fig. 4(a), it can be observed that C_J unequivocally dominates the device capacitance for most of the reverse-bias conditions ($v_D > 0$). However, C_D becomes prominent close to the forward bias region when v_D approaches $-V_B$. A similar capacitance profile can be observed in Si or SiC MOSFETs in which the output capacitance C_{oss} primarily consists of the capacitance of the p-n junction body diode C_{ds}.

B. Current-Dependent LVC Model

An LVC connected to an ideal sinusoidal current source is shown in Fig. 5. The ideal LVC diodes are replaced by the real one consisting of nonideal diodes and voltage-dependent capacitors, as described by the diode parasitic capacitance model (1)–(4) in Section II-A. The instantaneous voltage $v_{C1}(t)$ of the voltage-dependent capacitor C_1 can be derived starting from the differential equation

$$C_1(-v_{C1}(t))\, dv_{C1} = i(t)\, dt \tag{5}$$

where voltage-dependent capacitance C_1 can be expressed as

$$C_1(v_{C1}(t)) = C_J(v_{C1}(t)) + C_D(v_{C1}(t)). \tag{6}$$

Voltage v_{C1} can be solved in terms of the phase angle $\theta = \omega t$

$$\int_{-V_S}^{v_C} \left[C_J\left(v_{C1}(\theta)\right) + C_D\left(v_{C1}(\theta)\right)\right] dv_{C1} = \frac{I_m}{\omega}\int_0^{\theta} \sin(\theta) d\theta = \frac{I_m}{\omega}\left(1-\cos\theta\right). \tag{7}$$

Similarly, for v_{C2}

$$\int_{-V_S}^{v_C} \left[C_J\left(v_{C2}(\theta)\right) + C_D\left(v_{C2}(\theta)\right)\right] dv_{C2} = -\frac{I_m}{\omega}\int_{\pi}^{\theta} \sin(\theta) d\theta = \frac{I_m}{\omega}\left(1+\cos\theta\right). \tag{8}$$

When a current begins flowing through the p-n junction in a steady state, the diode voltage builds up, starting from $-V_S$. The calculation of V_S is described in Section II-A. For most high-voltage diodes, an approximation of $V_S < V_B/2$ holds. In this scenario, the diffusion capacitance C_D can be neglected compared to the junction capacitance C_J.

Consequently, voltage v_{C1} can be calculated from

$$\int_{-V_S}^{v_C} C_{j0}\left(1+\frac{v_{C1}}{V_B}\right)^{-m} dv_{C1} = \frac{I_m}{\omega}\int_0^{\theta} \sin(\theta) d\theta \tag{9}$$

resulting in the expression

$$\frac{C_{j0}V_B}{(1-m)}\left[\left(1+\frac{v_{C1}}{V_B}\right)^{1-m}\right]_{-Vs}^{vc} = \frac{I_m}{\omega}\left[-\cos\theta\right]_0^{\theta}. \tag{10}$$

The expression is simplified as

$$\left(1+\frac{v_{C1}}{V_B}\right)^{1-m} - \left(1-\frac{V_s}{V_B}\right)^{1-m} = \frac{(1-m)\,I_m}{V_B\omega C_{j0}}\left(1-\cos\theta\right) \tag{11}$$

$$1+\frac{v_{C1}}{V_B} = \left(P\left(1-\cos\theta\right) + \left(1-\frac{V_s}{V_B}\right)^{1-m}\right)^{\frac{1}{1-m}} \tag{12}$$

where P is defined as

$$P = \frac{I_m\left(1-m\right)}{\omega C_{j0}V_B}. \tag{13}$$

This is further solved for v_{C1} as

$$V_B + v_{C1} = V_B P^{\frac{1}{1-m}}\left(1-\cos\theta+P_s\right)^{\frac{1}{1-m}} \tag{14}$$

$$v_{C1}(\theta) = V_B P^{\frac{1}{1-m}}\left(1+P_S-\cos\theta\right)^{\frac{1}{1-m}} - V_B$$

where P_s is defined as

$$P_S = \frac{1}{P}\left(1-\frac{V_S}{V_B}\right)^{1-m}. \tag{15}$$

Similarly, v_{C2} can be calculated using the following expression:

$$\int_{-V_S}^{v_C} C_{j0}\left(1+\frac{v_{C2}}{V_B}\right)^{-m} dv_{C2} = -\frac{I_m}{\omega}\int_{\pi}^{\theta} \sin(\theta) d\theta \tag{16}$$

as

$$v_{C2}\left(\theta\right) = V_B P^{\frac{1}{1-m}}\left(1+P_S+\cos\theta\right)^{\frac{1}{1-m}} - V_B. \tag{17}$$

TABLE II
DIODE SPECIFICATIONS

Diode	C_{j0} (nF)	m	V_B (V)	V_K (V)
General diodes				
GD1	10	2/3	0.5	0.3
GD2	10	1/2	0.5	0.3
GD3	10	1/3	0.5	0.3
Selected practical (off-the-shelf) diodes				
RB238T150	1.6	0.50	0.50	0.26
RF601BGE2D	0.1	0.41	0.43	0.43

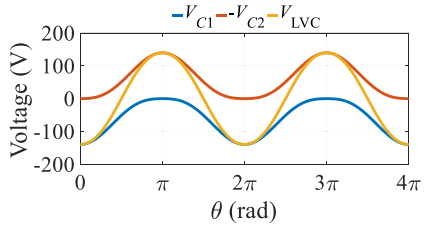

Fig. 6. Voltage across individual LVC diodes GD1 and the entire structure for $I_m = 250$ mA and $f = 1$ MHz.

The voltage of the LVC can be calculated as follows:

$$v_{\text{LVC}} = v_{C1} - v_{C2} = V_B P^{\frac{1}{1-m}}\left(\left[1+P_S-\cos\theta\right]^{\frac{1}{1-m}} - \left[1+P_S+\cos\theta\right]^{\frac{1}{1-m}}\right) \tag{18}$$

where

$$P = \frac{I_m\left(1-m\right)}{\omega C_{j0}V_B} \text{ and } P_S = \frac{1}{P}\left(1-\frac{V_S}{V_B}\right)^{1-m}. \tag{19}$$

The magnitude $V_{\text{LVC},n}$ of the nth harmonic of the LVC voltage, can be calculated as

$$V_{\text{LVC},n} = \frac{1}{\pi}\int_0^{2\pi} v_{\text{LVC}}(\theta)\cos(n\theta) d\theta \tag{20}$$

$n = 1$ corresponds to the fundamental voltage component $V_{\text{LVC},1}$. It is used to calculate the equivalent LVC capacitance as

$$C_{\text{LVC}}\left(\omega, I_m\right) = I_m/(\omega V_{\text{LVC},1}). \tag{21}$$

The normalized LVC capacitance is given as

$$C_{\text{LVC},Cj0}\left(\omega, I_m\right) = C_{\text{LVC}}\left(\omega, I_m\right)/C_{j0}. \tag{22}$$

As an illustration, an LVC made of a diode GD1 is analyzed. The parameters of GD1 are mentioned in Table II. Fig. 6 represents the time waveforms of voltages v_{C1} and v_{C2} for the operating condition $I_m = 0.25$ A and $f = 1$ MHz. It can be observed that v_{C1} and v_{C2} are distorted, indicating the presence of signal harmonics and dc bias due to the nonlinear capacitance. v_{C1} has a negative dc bias, while v_{C2} has a positive dc bias. However, the voltage across the LVC is almost sinusoidal.

The equivalent LVC capacitance can be solved numerically. To validate the modeling, an LVC made of practical diode RB238T150 from Table II is considered for simulation analysis,

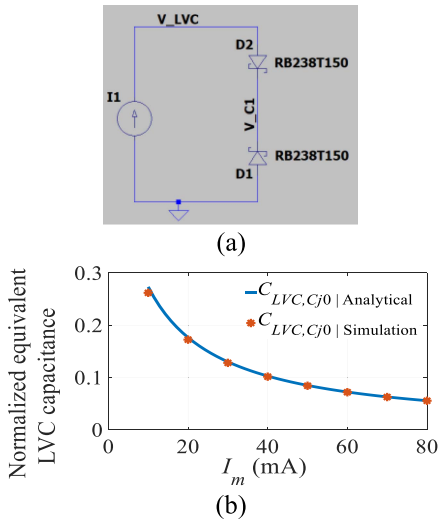

Fig. 7. Current-dependent model of LVC made of RB238T150 ($f = 1$ MHz). (a) LT-SPICE simulation model. (b) Normalized equivalent capacitance value as a function of the current magnitude.

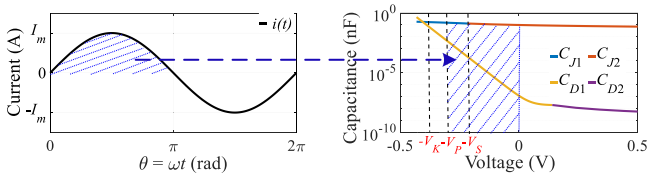

Fig. 8. Charging of the LVC capacitance during the initial phase ($V_P < V_K$ case).

as shown in Fig. 7(a). The normalized capacitance of LVC as a function of I_m is presented in Fig. 7(b). It can be observed that the simulation values agree with the analytical calculations.

1) Modeling and Calculation of V_S: V_S is the minimum voltage of the voltage-dependent nonlinear capacitor for direct-biased diodes ($v_D = v_C < 0$). In a practical case, it is different from 0 or $-V_B$. It is determined by the charge pumped into one of the p-n junctions during the first half cycle of the current.

During the first half cycle of the operation with sinusoidal current excitation, the charge from the current source is stored in C_J and C_D of D_2 until the potential reaches $-V_P$. The shaded area in Fig. 8 marks the equivalent charge in the region. Contingent upon the current magnitude and frequency, V_P can be smaller or equal to V_K, where V_K is the diode knee voltage. This charge will be distributed over time between the two LVC p-n junctions according to the charge conservation principle so that each diode reaches the same direct bias voltage $-V_S$. If V_P does not reach V_K, then the diode conduction can be neglected, and the total charge Q_P brought by the current and stored in the parasitic diode capacitances is

$$Q_P = \frac{I_m}{\omega}\int_0^{\pi} \sin(\theta)d\theta = \frac{2I_m}{\omega} \quad \text{for} \quad V_P < V_K. \tag{23}$$

V_P will reach V_K if the following is true

$$\int_0^{V_K} \left[C_J\left(v_C(t)\right) + C_D\left(v_C(t)\right)\right] dv_C < \frac{2I_m}{\omega}. \tag{24}$$

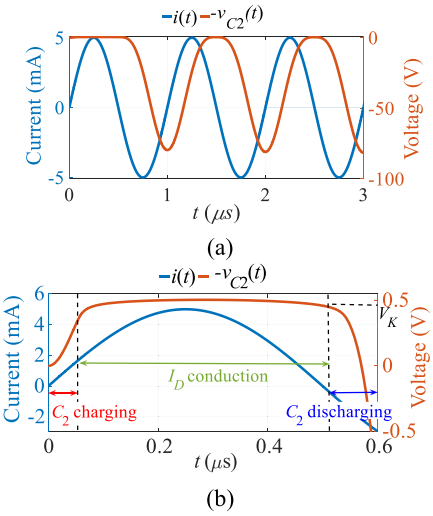

Fig. 9. Time waveforms of the diode voltage and current (Diode RF601BGE2D). (a) During the first three periods. (b) Zoomed-in view during the first half-period ($V_P = V_K$ case).

In that case, after the diode reaches V_K, the diode begins to conduct, and only a small portion will continue charging the capacitors. This is because the diode is forward biased, and diode current I_D significantly increases with a slight increase in voltage across the diode V_D as per the expression

$$I_D\left(v_D\right) = I_{S0}\left(e^{qv_D/(NkT)} - 1\right) \tag{25}$$

where I_{S0} is the saturation current, q is the charge of an electron, k is Boltzmann's constant, and T is the junction temperature in Kelvins. After the current $i(t)$ reaches its maximum and starts reducing, I_D will continue to flow, now supported partially by the recombination of the excess of minority carriers in the diode, i.e., the charges from the two capacitors. This operation is illustrated, and the time segments are marked in Fig. 9. Before $i(t)$ changes direction, the diode voltage returns to the V_K level. Consequently, the charge stored in the C_J and C_D at the end of the half-period can be approximated as follows:

$$Q_P = \int_0^{V_K} \left[C_J\left(v_C(t)\right) + C_D\left(v_C(t)\right)\right] dv_C \quad \text{for} \quad V_P \geq V_K. \tag{26}$$

According to the charge conservation principle, Q_P will be distributed over time between the two LVC p-n junctions so that each diode reaches the same direct bias voltage $-V_S$. Therefore, V_S can be calculated using the following expression:

$$\int_0^{V_S} \left[C_J\left(v_C(t)\right) + C_D\left(v_C(t)\right)\right] dv_C = \frac{Q_P}{2}. \tag{27}$$

Numerical methods can be employed to solve (27). The same V_S is achieved irrespective of the initial phase of the source current.

Fig. 10 illustrates how the initial voltage V_P and V_S change as a function of current magnitude for two LVCs. The first LVC consists of two RF601BGE2D diodes, while the second LVC consists of two RB238T150 Schottky diodes. The diode

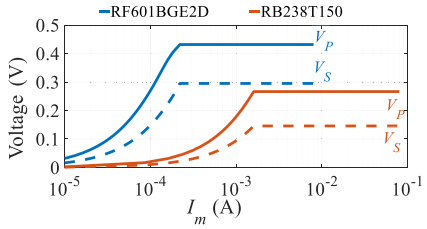

Fig. 10. V_P and V_S as a function of source current in the LVC made of the RF601BGE2D and RB238T150 diodes.

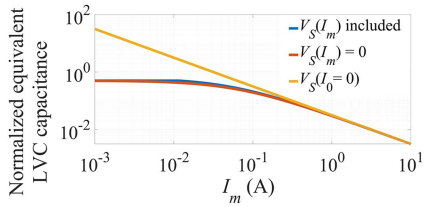

Fig. 11. Normalized equivalent capacitance as a function of I_m and V_S for LVC with GD2 at $f = 1$ MHz.

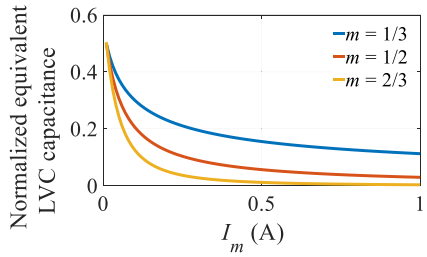

Fig. 12. Normalized equivalent capacitance value as a function of the current magnitude for $m = 1/3$ (GD3), $m = 1/2$ (GD2), and $m = 2/3$ (GD1) $f = 1$ MHz.

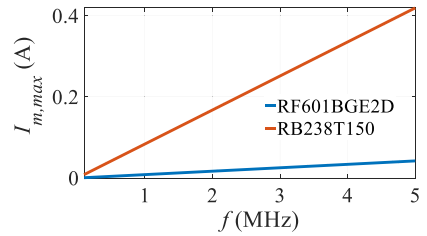

Fig. 13. $I_{m,\max}$ as a function of frequency in the LVC made of the RF601BGE2D and RB238T150.

specifications are mentioned in Table II. These two diodes are selected due to significantly different values of C_{j0}.

A typical ac current rating of a diode is very low, even for the diode rated for a high dc current. It is due to the small junction capacitance being charged quickly to the breakdown voltage of the diode, even by a small current during the reverse-biased phase. Each LVC curve in Fig. 10 is presented up to the maximum ac current it can safely handle without causing a breakdown. As expected, V_P increases with I_m but does not exceed the respective V_K.

In Fig. 11, an LVC made with diode GD2 is analyzed for normalized equivalent capacitance (22) for the following three cases:

1) accurately calculated V_S;
2) simplifying calculations by neglecting V_S ($V_S = 0$);
3) assuming $V_S = V_B$.

It is observed that the difference in values between cases 1) and 2) is small (less than 14%) for practical currents $I_m > 0.1$ A. For low-current operation, 2) is closer to accurate model 1) than 3). In summary, although the value of P_S in (19) depends on V_S, it does not significantly affect capacitance for $I_m > 0.1$ A. Therefore, for a typical range of I_m (0.1∼1 A), the $V_S = 0$ approximation is valid.

Applying $V_S = 0$ approximation, (19) turns into $P = 1/P_S$, and it can be substituted into (18)

$$v_{\text{LVC}} = V_B P_s^{\frac{1}{m-1}} \left([1 + P_s - \cos\theta]^{\frac{1}{1-m}} - [1 + P_s + \cos\theta]^{\frac{1}{1-m}} \right). \tag{28}$$

Considering the same LVC parameters, the normalized equivalent LVC capacitance is calculated for a range of currents through the device and for three gradient coefficients: $m = 1/3$ (GD3), $m = 1/2$ (GD2), and $m = 2/3$ (GD1). It can be observed in Fig. 12 that for similar characteristics and operating conditions, $m = 1/3$ (GD1) offers substantially higher capacitance.

2) LVC Current Rating: The maximum ac current of an LVC can be derived from the expression

$$\frac{I_{m,\max}}{\omega} \int_0^{\pi} \sin(\theta) d\theta = \int_{-V_S}^{V_{BN}} \left[C_J\left(v_C(t)\right) + C_D\left(v_C(t)\right) \right] dv_C. \tag{29}$$

In the zone from $-V_S$ to V_{BN}, the diffusion capacitance can typically be neglected with respect to junction one as

$$\frac{I_{m,\max}}{\omega} \int_0^{\pi} \sin(\theta) d\theta \approx \int_{-V_S}^{V_{BN}} \left[C_J\left(v_C(t)\right) \right] dv_C = \int_{-V_S}^{V_{BN}} C_{j0} \left(1 + \frac{v_{C1}}{V_B}\right)^{-m} dv_{C1}. \tag{30}$$

The expression is solved as

$$\frac{I_{m,\max}}{\omega} \left[\cos\theta\right]_0^{\pi} = \frac{C_{j0} V_B}{(1-m)} \left[\left(1 + \frac{v_{C1}}{V_B}\right)^{1-m} \right]_{-Vs}^{V_{BN}} \tag{31}$$

leading to the following expression of $I_{m,\max}$:

$$I_{m,\max} = \frac{V_B \omega C_{j0}}{2\,(1-m)} \left(\left(1 + \frac{V_{BN}}{V_B}\right)^{1-m} - \left(1 + \frac{-V_S}{V_B}\right)^{1-m} \right). \tag{32}$$

The expression reveals that the maximum current increases linearly with signal frequency and capacitance C_{j0}. Fig. 13 shows $I_{m,\max}$ as a function of frequency in the LVC made of the RF601BGE2D diodes and RB238T150 diodes. It can be noticed that $I_{m,\max}$ is linearly increasing. However, even at megahertz

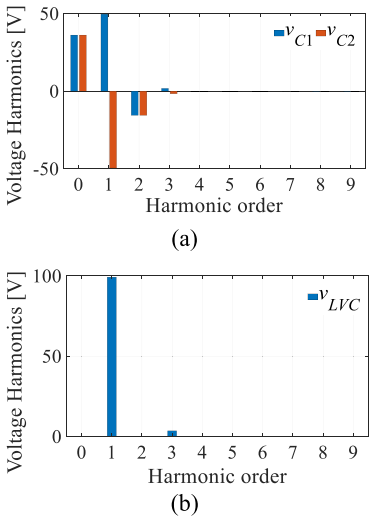

Fig. 14. LVC harmonic analysis; LVC is made of four pairs of back-to-back connected diodes GD1 for $I_m = 0.25$ A and $f = 1$ MHz. (a) v_{C1} and v_{C2}. (b) $v_{\rm LVC}$.

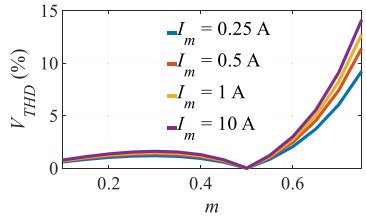

Fig. 15. THD of the voltage of a current-supplied LVC as a function of I_m and m.

operation, the values are significantly less than the conduction current rating 6 A for RF601BGE2D and 20 A for RB238T150.

3) Harmonic Analysis of Current-Dependent LVC: The harmonic content of the voltage waveform in a typical current-supplied LVC is shown in Fig. 14. The harmonic magnitudes of v_{C1} and v_{C2} are shown in Fig. 14(a), while the $v_{\rm LVC}$ harmonic content is shown in Fig. 14(b). It is visible from Fig. 14(a) that both signals v_{C1} and v_{C2} demonstrate strong dc components and the first two harmonics, while the other harmonics are smaller. Due to symmetry, the magnitudes of corresponding harmonics of the two signals are identical. However, the phases of even harmonics are shifted apart by 180°, which causes these harmonics to cancel in $v_{\rm LVC}$. The same is true with the dc components of v_{C1} and v_{C2}. The first harmonics of the two signals are in phase, appearing additively in the $v_{\rm LVC}$ signal. This qualitative analysis confirms that LVC effectively acts as a capacitor, producing minimum harmonic content, and its effective linear capacitor behavior can be utilized in many resonant converter applications.

The harmonic content of an LVC voltage depends on multiple parameters such as I_m, C_{j0}, m, V_B, and f, with m being a dominant factor. For most of the power devices in the market, m is from 0.3 to 0.6. To illustrate the impact of m and V_B on the total harmonic distortion (THD) of LVC voltage, THD is calculated and plotted in Fig. 15 for a range of m values at $f = 1$ MHz and four I_m current values (0.25, 0.5, 1, and 10 A),

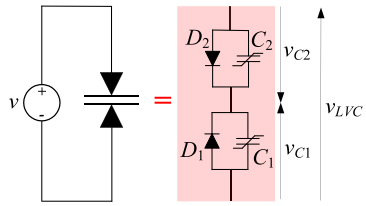

Fig. 16. Equivalent LVC circuit consisting of a diode and a voltage-dependent capacitor.

while C_{j0} is kept constant ($C_{j0} = 10$ nF). Harmonics up to an order of 20 are considered for THD calculation. It can be observed that for $V_B = 0.5$ V, THD is less than 2% up to m of approximately 0.60 and increases exponentially above that. The THD is minimum (zero) at $m = 0.5$, which could be a preferred design for many power electronic applications. The harmonics increase with the current magnitude, but the values are relatively small when $m < 0.60$.

A linear device shows an identical response when supplied from a current or voltage source, and the same device model can be used for both cases. Unfortunately, the presence of voltage harmonics for all m values different than 0.5 indicates that an LVC is a nonlinear structure. Consequently, the current-dependent model derived in Section III may not be accurate if the same LVC is supplied from a voltage source. Therefore, a voltage-dependent LVC model is discussed in the next section.

III. Voltage-Dependent LVC Model

Similar to the analysis in Section III, an analogous analysis is conducted to derive a voltage-dependent model of LVC with nonlinear voltage-dependent junction capacitance. A sinusoidal voltage source $v_{\rm LVC}(t) = V_m \cos(\omega t)$ is connected to the LVC, as shown in Fig. 16. The expression for instantaneous voltage $v_{C1}(t)$ can be obtained from the following equations:

$$i_{\rm LVC} = C_1\left(v_{C1}\right)\frac{dv_{C1}}{dt} \tag{33}$$

$$v_{\rm LVC} = v_{C1} - v_{C2}. \tag{34}$$

Substituting $\theta = \omega t$, (33) and (34) can be solved, leading to a differential equation with respect to $v_{C1}(\theta)$ as

$$\left(\left(1 - \frac{v_{\rm LVC}(\theta)}{V_B + v_{C1}(\theta)}\right)^m + 1\right)\frac{dv_{C1}}{d\theta} = \frac{dv_{\rm LVC}}{d\theta}. \tag{35}$$

For $v_{\rm LVC}(\theta) = V_m \cos(\theta)$, the general solution can be written in the form

$$\int_{p_0}^{p(\theta)} \frac{(p+1)\sqrt[m]{p}}{mp\left(\sqrt[m]{p}-1\right)\left(p+\sqrt[m]{p}\right)}dp = \int_{\theta=0}^{\theta} \cot\theta d\theta \tag{36}$$

where

$$p(\theta) = \left(1 - \frac{V_m\cos(\theta)}{V_B + v_{C1}(\theta)}\right)^m \tag{37}$$

$$p_0 = \left(1 - \frac{V_m}{V_m + V_B - V_S}\right)^m. \tag{38}$$

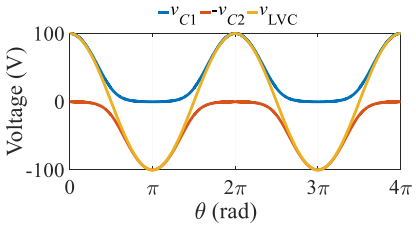

Fig. 17. Waveforms of an LVC supplied from a voltage source at $f = 1$ MHz.

A general explicit solution of $v_{C1}(\theta,m)$ cannot be derived from (36), but (36) can be solved for known values of m. For example, the solution for $m = 1/2$ is

$$\frac{\left(1+\sqrt{1-\frac{V_m\cos(\theta)}{V_B+v_{C1}(\theta)}}\right)\left(1-\sqrt{1-\frac{V_m}{V_B+V_m-V_S}}\right)}{\left(1-\sqrt{1-\frac{V_m\cos(\theta)}{V_B+v_{C1}(\theta)}}\right)\left(1+\sqrt{1-\frac{V_m}{V_B+V_m-V_S}}\right)} = \pm\sec\theta. \tag{39}$$

$v_{C1}(\theta,m)$ can be calculated from the aforementioned equation, and then, i_{LVC} can be obtained from (33). Fig. 17 shows the voltage waveform for the LVC consisting of diodes GD1 supplied by voltage $v(t) = 100\cos(\omega t)$. It can be observed that v_{C1} and v_{C2} are distorted, but the distortion cancels out to constitute the sinusoidal $v(t)$ waveform.

Once $v_{C1}(\theta)$ is known, $i_{\mathrm{LVC}}(\theta)$ can be obtained using (33). The magnitude $I_{\mathrm{LVC},n}$ of the nth harmonic of the LVC current can be calculated as

$$i_{\mathrm{LVC},n} = \frac{1}{\pi}\int_0^{2\pi} i_{\mathrm{LVC}}(\theta)\sin(n\theta)d\theta \tag{40}$$

$n = 1$ corresponds to the fundamental current component $i_{\mathrm{LVC},1}$. It is used to calculate the equivalent LVC capacitance as

$$C_{\mathrm{LVC}}(\omega, I_m) = I_{\mathrm{LVC},1}/(\omega V_m). \tag{41}$$

The normalized equivalent LVC capacitance is defined as

$$C_{\mathrm{LVC,norm}}(\omega, V_m) = C_{\mathrm{LVC}}(\omega, V_m)/C_{j0}. \tag{42}$$

The equivalent LVC capacitance can be calculated numerically. A simulation model of an LVC structure made with a diode RB238T150 and connected to a sinusoidal voltage source is shown in Fig. 18(a). The LVC normalized capacitance as a function of V_m is presented in Fig. 18(b). It can be observed that the simulation values agree with the analytical calculations. The normalized equivalent capacitances for $m = 1/3$, $m = 1/2$, and $m = 2/3$ are shown in Fig. 19. Similar to the current-dependent model, $m = 1/3$ offers substantially higher capacitance for similar characteristics and operating conditions.

IV. Harmonicless LVC

In this section, the solutions for the harmonicless case $m = 0.5$ are described and analyzed in detail for both the current- and voltage-dependent LVC models.

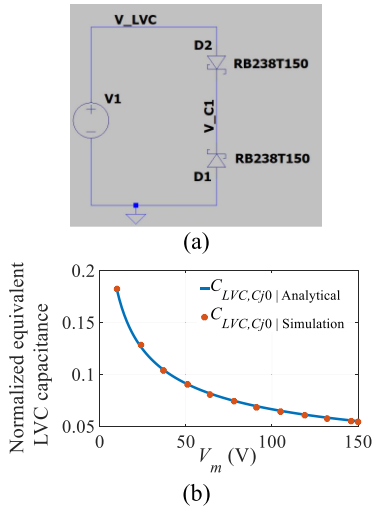

Fig. 18. Voltage-dependent model of LVC made of RB238T150 at $f = 1$ MHz. (a) LT-SPICE simulation model. (b) Normalized equivalent capacitance value as a function of V_m.

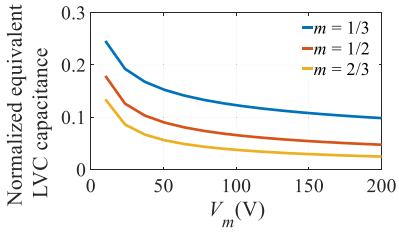

Fig. 19. Normalized equivalent capacitance value as a function of the voltage magnitude for $m = 1/3$ (GD3), $m = 1/2$ (GD2), and $m = 2/3$ (GD1), $= 2\pi \times 10^6$ rad/s.

A. Current-Dependent Model of LVC for m = 0.5

The expression for v_{LVC} in (18) is simplified for $m = 0.5$ as

$$v_{\mathrm{LVC}} = \left(\frac{I_m}{V_B\omega^2 C_{j0}^2}(I_m + I_0)\right)\sin\left(\theta - \frac{\pi}{2}\right) \tag{43}$$

$$I_0 = 2\omega C_{j0} V_B\sqrt{1 - V_S/V_B}. \tag{44}$$

It is established from (43) that v_{LVC} has only the fundamental component; no higher order harmonics exist. For a given LVC and operating frequency, I_0 represents a constant current parameter. The normalized equivalent capacitance can be calculated as follows:

$$C_{\mathrm{LVC},m=0.5,\mathrm{norm}}(\omega, I_m) = \frac{\omega V_B C_{j0}}{(I_m + I_0)}. \tag{45}$$

It is visible from (45) that the $C_{\mathrm{LVC},m\ =\ 0.5,\mathrm{norm}}$ depends on operating conditions. It is directly proportional to ω but inversely related to I_m. Approximating $V_S = 0$ in (45) results in

$$C_{\mathrm{LVC},m=0.5}(\omega, I_m) \approx \frac{\omega V_B C_{j0}^2}{I_m + 2\omega C_{j0} V_B}. \tag{46}$$

The variation of $C_{\mathrm{LVC},m\ =\ 0.5,\mathrm{norm}}$ with I_m for an LVC with parameters $C_{j0} = 10$ nF, $m = 1/2$, and $V_B = 0.5$ V is shown in

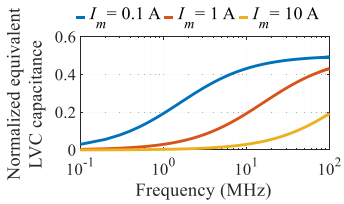

Fig. 20. Normalized equivalent capacitance as a function of frequency for LVC made of GD2 ($V_S = 0$ V).

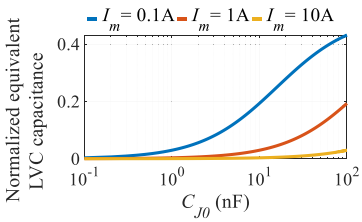

Fig. 21. Normalized equivalent capacitance as a function of C_{j0} ($m = 1/2$, $f = 1$ MHz, $V_B = 0.5$ V, $V_K = 0.3$ V, and $V_S = 0$ V).

Fig. 11, and it agrees with (45). The variation of $C_{\mathrm{LVC},m=0.5,\mathrm{norm}}$ with frequency is presented in Fig. 20, showing that it increases with frequency. Therefore, high-frequency power electronic systems can benefit more from the LVC. The relative capacitance change is higher at lower I_m. Similarly, it can be observed in Fig. 21 that increasing the C_{j0} leads to higher values of normalized capacitance.

B. Voltage-Dependent Model of LVC for m = 0.5

The simplified expression of the diode voltages v_{C1} and v_{C2} in an LVC supplied from a sinusoidal voltage source $v_{\mathrm{LVC}} = V_m \cos(\omega t)$ for $m = 0.5$ is given by

$$v_{C1} = V_m \left(\left(\frac{1}{4\beta} + \frac{\beta}{8} \right) + \frac{\cos(\theta)}{2} + \frac{\beta \cos(2\theta)}{8} \right) - V_B \tag{47}$$

$$v_{C2} = V_m \left(\left(\frac{1}{4\beta} + \frac{\beta}{8} \right) - \frac{\cos(\theta)}{2} + \frac{\beta \cos(2\theta)}{8} \right) - V_B \tag{48}$$

$$\beta = \frac{\sqrt{V_B + V_m - V_S} - \sqrt{V_B - V_S}}{\sqrt{V_B + V_m - V_S} + \sqrt{V_B - V_S}} \tag{49}$$

where β is a constant dependent on the V_S, V_B, and V_M. The voltages v_{C1} and v_{C2} contain dc bias, the first, and the second harmonic components. The expression for the v_{C1} is used to calculate the fundamental harmonic of the LVC current

$$\begin{aligned} i_{\mathrm{LVC}}(\theta) &= \omega C_1(v_{C1}) \frac{dv_{C1}}{d\theta} \\ &= -\frac{\omega C_{j0} V_m}{\sqrt{1 + \frac{V_m\left(\frac{1}{4\beta} + \frac{\cos(\theta)}{2} + \frac{\beta\cos^2(\theta)}{4}\right) - V_B}{V_B}}} \\ &\quad \times \left(\frac{\sin(\theta)}{2} + \frac{\beta \sin(2\theta)}{4} \right). \end{aligned} \tag{50}$$

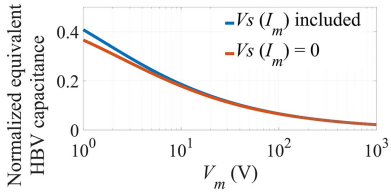

Fig. 22. Normalized equivalent capacitance as a function of V_m and V_S GD2.

TABLE III
LVC SPECIFICATIONS

Diode specifications	LVC-1	LVC-2	LVC-3
Part number	RB238T150	PDS5100	IDH20G120C5
Voltage rating	150 V	100 V	1200 V
Number of diodes used	20	30	10

This can be simplified as follows:

$$i_{\mathrm{LVC}}(\theta) = \omega C_{j0} \sqrt{\beta V_m V_B} \cos\left(\frac{\pi}{2} + \theta \right). \tag{51}$$

One can notice that the only fundamental harmonic exists. The normalized equivalent capacitance can be calculated as follows:

$$C_{\mathrm{LVC},m=0.5,\mathrm{norm}}(V_m) = \frac{1}{C_{j0}} \frac{\omega C_{j0} \sqrt{\beta V_m V_B}}{\omega V_m} = \sqrt{\frac{\beta V_B}{V_m}}. \tag{52}$$

It can be observed that the normalized capacitance depends on β, which is a function of V_S. It depends just weakly on f and C_{j0} in as much as these two parameters impact V_S, but that can be neglected in practical applications. V_S is inherently dependent on I_m. At first, β is calculated by assuming $V_S = 0$, then I_m is calculated and used to calculate V_S. This procedure is iterated until the V_S value no longer changes. The updated β is then used for capacitance calculations. Fig. 22 shows the plot of normalized equivalent capacitance calculated in two ways: applying the accurate analysis considering V_S and the approximative analysis in which V_S is nullified. It is observed that the difference is minimal for practical voltages $V_m > 10$ V.

V. EXPERIMENTAL RESULTS

Experiments are designed to test three LVCs, named LVC-1, LVC-2, and LVC-3, in the following text. Three LVCs are selected to demonstrate the applicability of the LVC model for different diode characteristics and voltage ratings, showcasing its versatility and robustness. Each LVC is symmetrical and made by combining multiple diodes, and their specifications are provided in Table III. A setup implementing the *LCR* meter-based capacitive coupling method for dc bias capacitance is used for experimental diode characterization to estimate C_{j0}, V_B, and m. Finally, a power amplifier-based current source circuit is deployed to measure C_{LVC} as a function of i_{LVC}. A custom PCB is made to test each LVC, as shown in Fig. 23. The PCB allows paralleling of LVCs and diodes to characterize the capacitance.

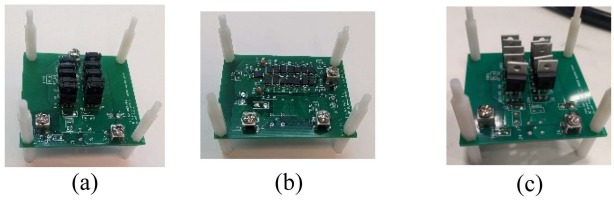

Fig. 23. Test LVC structure consisting of (a) 20 RB238T150 diodes; (b) 30 PDS5100 diodes; and (c) 10 IDH20G120C5 diodes.

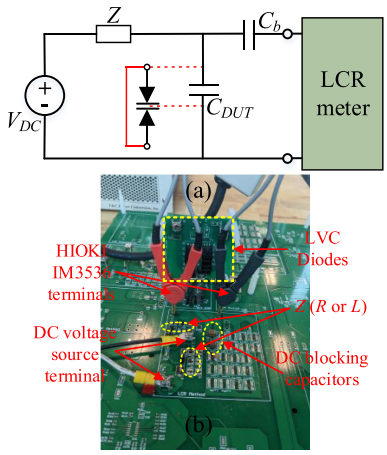

Fig. 24. *LCR* meter method. (a) Circuit diagram. (b) Experimental circuit.

TABLE IV
DC BIAS TEST SETUP PARAMETERS

Z	50 kΩ | Film resistor 0603	**LCR Meter**	Hioki IM3536
C_b	2 µF | Class I C0G	**Frequency**	1 MHz

A. Diode Differential (DC-Biased) Capacitance in an LVC

The LCR meter-based capacitive coupling method is used for the *C–V* characterization of diodes under dc bias [19], [20]. The circuit diagram is shown in Fig. 24(a). This method uses a blocking capacitor C_b (more than 50 times larger than $C_{\rm DUT}$) to protect the *LCR* meter from the applied dc voltage. A high impedance *Z*, which can be *R* or *L*, minimizes high-frequency current flow from the *LCR* meter into the dc power supply. The circuit parameters used for testing are mentioned in Table IV. All the diodes in the LVC are connected in parallel for this experiment. A detailed accuracy analysis of the *LCR* meter-based capacitive coupling method is described in [20]. The experimental circuit is shown in Fig. 24. The experiments are conducted at 1 MHz because most datasheets specify the dc bias capacitance at this frequency.

The results of the *LCR* method-based dc bias capacitances are compared with the datasheet values and presented in Fig. 25. It is observed that the measured biased capacitance differs from the datasheet values, particularly at low voltages (<1 V) but still follows the same profile. This could be due to the limited accuracy of laboratory equipment but also due to high capacitance tolerance (deviation) in practical diodes. The datasheet and

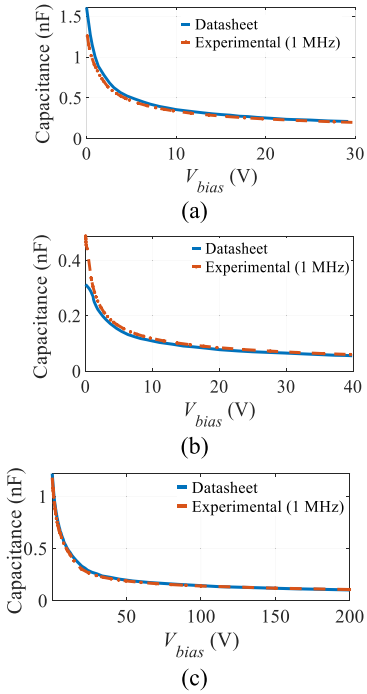

Fig. 25. Experimental differential capacitance compared with datasheet values at 1 MHz. (a) RB238T150 (LVC-1). (b) PDS5100 (LVC-2). (c) IDH20G120C5 (LVC-3).

TABLE V
DC BIASED CAPACITANCE PARAMETERS

	f=1 MHz	RB238T150	PDS5100	IDH20G120C5
C_{j0} (nF)	Datasheet	1.62	0.34	1.24
	Exp.	1.34	0.50	1.23
m	Datasheet	0.55	0.63	0.66
	Exp.	0.51	0.54	0.62
V_B (V)	Datasheet	0.68	2.09	3.50
	Exp.	0.74	0.74	3.14

experimental data are then fitted according to the expression (2), and the obtained $C_{j0,}$ *m*, and V_B values are listed in Table V. These parameters will be used to calculate $C_{\rm LVC}$ as a function of $i_{\rm LVC}$.

B. Equivalent Nonlinear LVC Capacitance

The equivalent nonlinear capacitance of the LVC is measured experimentally by connecting the LVC to a current source. The current source is created by an *LCC*-compensated circuit connected to a linear power amplifier. The circuit diagram and experimental setup are shown in Fig. 26. The equipment used and circuit parameters are mentioned in Table VI. The applied voltage $v_{\rm in}$ is varied to regulate the current through the LVC. The inductor L_P and capacitor C_P are tuned to satisfy $\omega^2 L_p C_p = 1$. L_S and *R* are connected to ensure high-quality factors and an adequate impedance for the power amplifier. L_S is appropriately adjusted for different operating frequencies using a variable air-core coupled solenoidal inductor to provide a high-quality

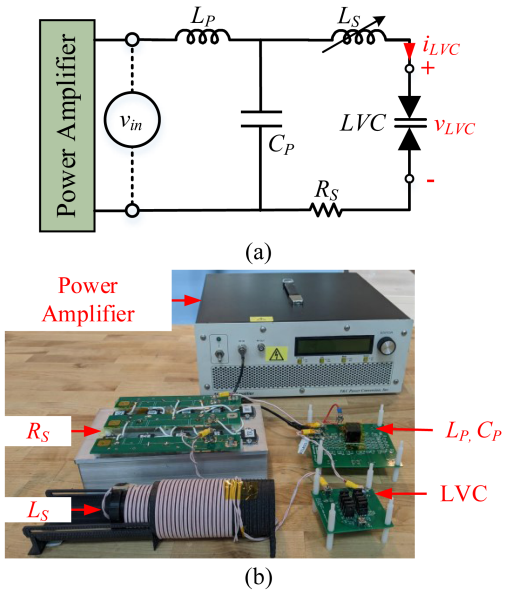

Fig. 26. C_{LVC} as a function of i_{LVC}. (a) Circuit diagram for measuring C_{LVC} and i_{LVC}. (b) Experimental setup.

TABLE VI
EXPERIMENTAL SETUP FOR LVC TESTING

Equipment		Specification	
Power Amplifier		T&C Power Conversion AG1021 100/300 W, 10 kHz-20 MHz	
Capacitor | C_P		Johnson Technology 1111 S42E-Series Capacitors	
Inductor | L_P		Core Material: Fair-rite 67 | EQ Core Wire: Magnet wire 22 AWG	
Resistor | R_S		OHMITE TGHD series 100 W, High Frequency 10 MHz	
Variable Inductor | L_S		New England Litz Wire Strand AWG 48, No. of strands 2200	
Circuit Parameters			
Frequency = 1 MHz			
L_P	4.81 µH	L_S	21 µH
C_P	5.30 nF	R_S	27.9 Ω
Frequency = 2 MHz			
L_P	5.25 µH	L_S	7.8 µH
C_P	1.22 nF	R_S	10.24 Ω

factor [21]. The current through the LVC is given by

$$i_{\mathrm{LVC}} = v_{\mathrm{in}}/(\omega L_P). \tag{53}$$

The current harmonic content on a linear scale is shown in Fig. 27, implying that the LVC current source is dominantly first harmonic. The equivalent nonlinear capacitance can be calculated by using measurements i_{LVC} and v_{LVC} as

$$C_{\mathrm{LVC}}\left(i_{\mathrm{LVC}}\right) = i_{\mathrm{LVC}}/(\omega v_{\mathrm{LVC},1}). \tag{54}$$

The experimental LVC capacitance as a function of current is shown in Fig. 28. In Fig. 28(a) and (b), the 1-MHz experimental results are plotted together with analytical results utilizing both the datasheet and experimentally measured diode parameters (see Table V). Similarly, C_{LVC} as a function of i_{LVC} for an

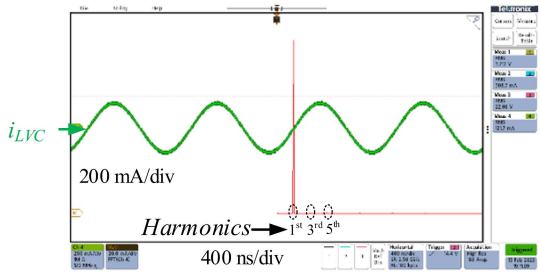

Fig. 27. i_{LVC} experimental waveform and its harmonics for LVC-1.

operating frequency of 2 MHz is shown in Fig. 28(c) and (d). It can be observed that the experimental measurements align very well with the analytical curve utilizing the measured C–V profile, which implies the accuracy of the model and the methodology. A slight discrepancy at low currents could be due to PCB parasitic inductance or an error in differential capacitance measurement. However, that is not the case with the analytical curve that utilizes the datasheet C–V profile of the diode, which deviates much more from the experimental values.

The experimental waveform across the LVC-1 is shown in Fig. 29 for 1-MHz operation. Strong harmonic content can be observed in voltage signals across the two individual diodes, but the equivalent voltage across the LVC is sinusoidal and almost free of harmonics.

To illustrate how the LVC model can be utilized in a resonant converter, a series connection of an LVC and an inductor is studied to describe the relationship between the resonant frequency of the L-LVC matching network and the current

$$f_{\mathrm{L-LVC}}\left(I\right) = \frac{1}{2\pi\sqrt{LC_{\mathrm{LVC}}\left(I\right)}}. \tag{55}$$

For illustration purposes, the aforementioned equation is calculated utilizing diode models derived in Section II-B for the three generalized diodes GD1, GD2, and GD3. Inductors for each case are selected to set the resonant frequency of 6.78 MHz for the current of 0.25 A. Fig. 30 illustrates how the resonant frequency of the three selected L-LVC resonant circuits varies with the current in the vicinity of the "nominal" resonant frequency of 6.78 MHz. These or similar profiles obtained for other types of diodes or numbers of paralleled diodes can be utilized to achieve different objectives in resonant converters, e.g., regulate the output voltage, stabilize the converter dependence on load variation, etc.

VI. EFFECT OF PACKAGE AND PCB PARACITICS ON LVC CHARACTERISTICS

Let us consider that n LVC branches are connected in parallel, as shown in Fig. 31. Each branch consists of two back-to-back discrete diodes used in the LVC, and the total package inductance is represented by $L_{\mathrm{par},n}$. The parasitic PCB inductance is denoted by $L_{\mathrm{PCB},1}$ and $L_{\mathrm{PCB},2}$. The parasitic resistances have been ignored as this analysis is focused on reactance, and no significant losses occur in the LVC as no diodes conduct in steady-state operation. The total current through the equivalent

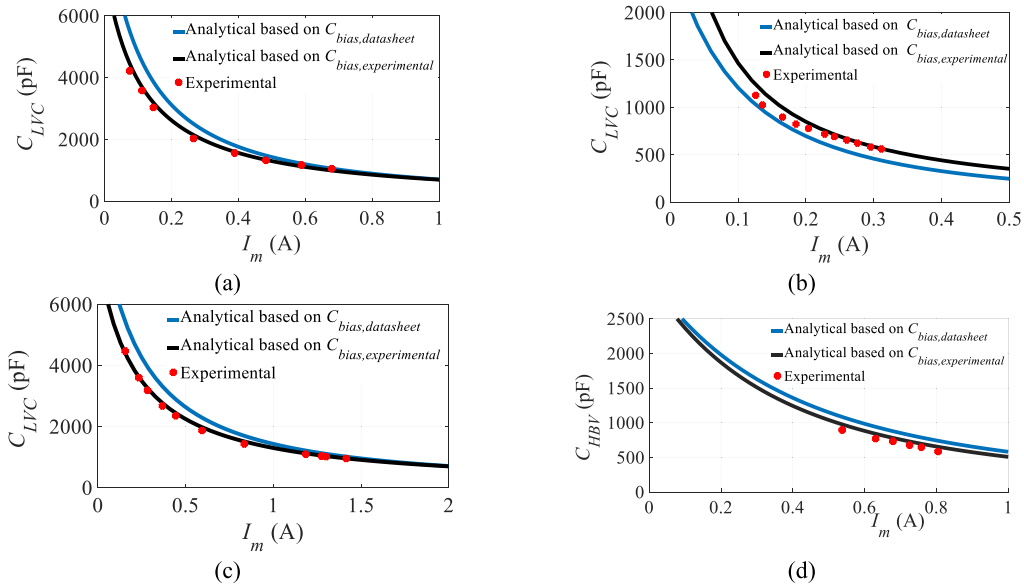

Fig. 28. C_{LVC} as a function of i_{LVC}. (a) LVC-1 (1 MHz). (b) LVC-2 (1 MHz). (c) LVC-1 (2 MHz). (d) LVC-3 (2 MHz).

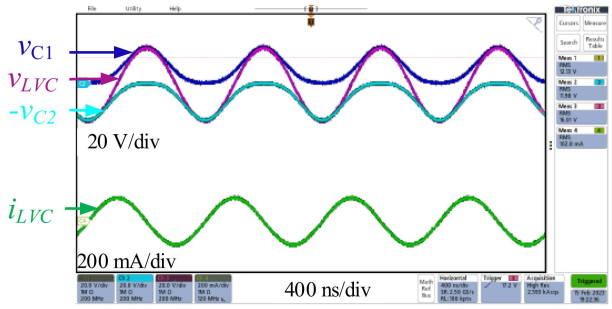

Fig. 29. Experimental waveform at 1 MHz for LVC-1: i_{LVC} and v_{LVC}.

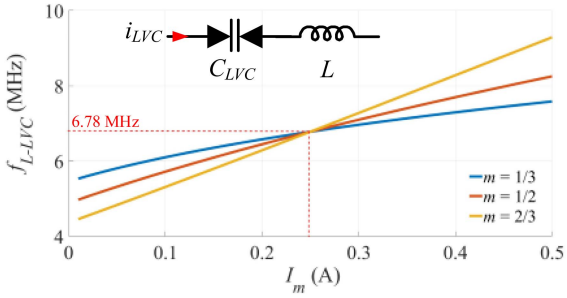

Fig. 30. Resonant frequency of an L-LVC series resonant circuit for three types of LVC devices built of GD1, GD2, and GD3 diodes.

LVC structure is i_{LVC}. For simplicity, let us consider that all the branches are symmetric

$$L_{\mathrm{par},1} = L_{\mathrm{par},2} = \ldots = L_{\mathrm{par},n} \tag{56}$$

$$L_{\mathrm{PCB}} = L_{\mathrm{PCB},1} + L_{\mathrm{PCB},2}. \tag{57}$$

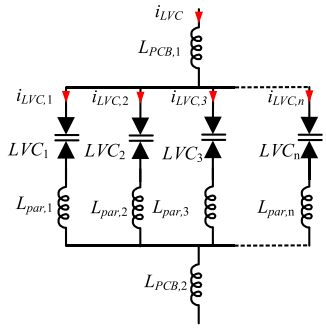

Fig. 31. Equivalent circuit of an LVC made of n parallel branches.

Consequently, i_{LVC} will be distributed equally

$$i_{\mathrm{LVC},1} = i_{\mathrm{LVC},2} = \ldots = i_{\mathrm{LVC},n} = i_{\mathrm{LVC}}/n. \tag{58}$$

The equivalent capacitance $C_{\mathrm{eq,LVC},1}$ of each branch is given by

$$C_{\mathrm{eq,LVC},1} = \frac{1}{\omega X_{C\mathrm{eq},1}} = \frac{1}{\omega}\left(\frac{1}{\omega C_{\mathrm{LVC},1}} - \omega L_{\mathrm{par},1}\right)^{-1}. \tag{59}$$

The series self-resonant angular frequency of each branch can be calculated as follows:

$$\omega_{r,\mathrm{LVC},1} = 1\Big/\sqrt{C_{\mathrm{LVC},1} L_{\mathrm{par},1}}. \tag{60}$$

It can be observed that the introduction of parasitic inductance increases the equivalent capacitance and decreases the resonant frequency. Equations (59) and (60) can be solved by deriving an explicit equation for $C_{\mathrm{LVC},1}$ using (21). $C_{\mathrm{LVC},1}$ depends on m, C_{j0}, V_B, ω, and i_{LVC}.

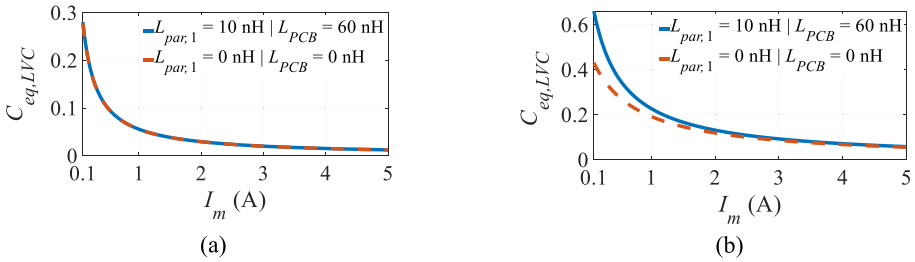

Fig. 32. $C_{\mathrm{eq,LVC}}$ as a function of I_m at (a) $f = 1$ MHz and (b) $f = 5$ MHz for LVC-1 (Diode: RB238T150).

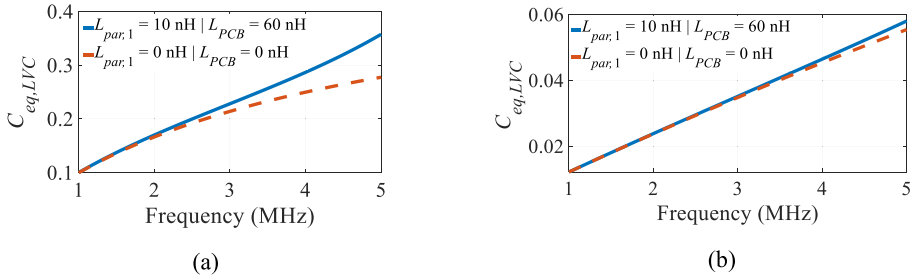

Fig. 33. $C_{\mathrm{eq,LVC}}$ as a function of frequency f for the current I_m of (a) 0.5 A and (b) 5 A for LVC-1 (Diode: RB238T150).

The equivalent capacitance $C_{\mathrm{eq,LVC}}$ of the paralleled structure, including the PCB parasitic, is given by

$$C_{\mathrm{eq,LVC}} = \frac{1}{\omega}\left(\frac{1}{\omega n C_{\mathrm{eq,LVC},1}} - \omega L_{\mathrm{PCB}}\right)^{-1} = \frac{n C_{\mathrm{eq,LVC},1}}{1 - \omega^2 n L_{\mathrm{PCB}} C_{\mathrm{eq,LVC},1}}. \quad (61)$$

Using (59) and (61), $C_{\mathrm{eq,LVC}}$ is derived as

$$C_{\mathrm{eq,LVC}} = \frac{1}{\frac{1}{n C_{\mathrm{eq,LVC},1}} - \omega^2\left(\frac{L_{\mathrm{par},1}}{n} + L_{\mathrm{PCB}}\right)}. \quad (62)$$

The series resonant frequency of the equivalent LVC can be defined as

$$\omega_{r,\mathrm{LVC}} = 1\Big/\sqrt{n C_{\mathrm{eq,LVC},1}\left(\frac{L_{\mathrm{par},1}}{n} + L_{\mathrm{PCB}}\right)} = 1\Big/\sqrt{(C_{\mathrm{eq,LVC},1} L_{\mathrm{par},1} + n C_{\mathrm{eq,LVC},1} L_{\mathrm{PCB}})}. \quad (63)$$

The self-resonating frequency of the branch depends only on $L_{\mathrm{par},1}$, while the overall resonant frequency depends on both $L_{\mathrm{par},1}$ and L_{PCB}. From (60) and (63), one can notice that $\omega_{r,\mathrm{LVC}}$ is always less than $\omega_{r,\mathrm{LVC},1}$. Therefore, for using the LVC effectively as a variable capacitor, the operating frequency ω must satisfy $\omega << \omega_{r,\mathrm{LVC}}$.

Here, a case study is presented for an LVC made of $m = 0.5$ diodes. Assuming $V_S = 0$, the capacitance is given by (46) as

$$C_{\mathrm{LVC},m=0.5}\left(\omega, \frac{I_m}{n}\right) \approx \frac{\omega V_B C_{j0}^2}{I_m/n + 2\omega C_{j0} V_B} \quad (64)$$

where I_m is the peak current value of i_{LVC}. Using (59) and (64), $C_{\mathrm{eq,LVC},1}$ of each branch is derived as

$$C_{\mathrm{eq,LVC},1} = \frac{\omega V_B C_{j0}^2}{\frac{I_m}{n} + 2\omega C_{j0} V_B - \omega^3 L_{\mathrm{par},1} C_{j0}^2 V_B}. \quad (65)$$

Using (62) and (64), $C_{\mathrm{eq,LVC}}$ is derived as

$$C_{\mathrm{eq,LVC}} = \frac{1}{\frac{I_m + 2\omega_{r,\mathrm{LVC}} C_{j0} V_B - \omega^3 L_{\mathrm{par},1} C_{j0}^2 V_B}{n\omega V_B C_{j0}^2} - \omega^2 \frac{L_{\mathrm{par},1}}{n} - \omega^2 L_{\mathrm{PCB}}}. \quad (66)$$

Combining (63) and (66) leads to the cubic equation for calculating the equivalent resonant frequency $\omega_{r,\mathrm{LVC}}$ as

$$\omega_{r,\mathrm{LVC}}^3\left(n V_B C_{j0}^2\left(\frac{L_{\mathrm{par},1}}{n} + L_{\mathrm{PCB}}\right) + L_{\mathrm{par},1} C_{j0}^2 V_B\right) - \omega_{r,\mathrm{LVC}}\left(2 C_{j0} V_B\right) - \frac{I_m}{n} = 0. \quad (67)$$

It can be commented that paralleling branches reduces the effect of package inductance by a factor of n. Developing an integrated LVC can further mitigate this issue. A typical value of package inductance for discrete semiconductor devices depends on the package and the component rating [22], [23]. LVC-1 test structure has ten branches in parallel and is used here as an example in this study. Unfortunately, the package inductance is not mentioned in the datasheet provided by the diode manufacturer [24], [25], [26]. Therefore, values of the parasitic inductance of a similarly packaged MOSFET are used. The package inductance is assumed to be 10 nH, i.e., twice the measured MOSFET's common source inductance for a similar package. The parasitic PCB inductance used in this case is measured experimentally

from the layout using an *LCR* meter as 60 nH. In Fig. 32, it can be observed that the effect of parasitics on $C_{\mathrm{eq,LVC}}$ depends on current and frequency. The effect reduces as the current is increased. Similarly, the frequency effect on $C_{\mathrm{eq,LVC}}$ is shown in Fig. 33. In a typical application, PCB parasitics will be highly reduced as the LVC will be placed together with the main circuit on the same PCB. Moreover, if an LVC is part of a series resonant circuit, both the PCB and package inductances can be merged with the inductance of the series inductor.

VII. Conclusion

This manuscript analytically confirms that the nonlinear parasitic capacitance of two back-to-back reverse-biased diodes can act as an LVC, and derives a model describing the relation between LVC capacitance and circuit and diode parameters. The current- and voltage-related models are verified through simulations and experimentally. The proposed model can be used to design circuits with the LVC for achieve objectives such as load regulations and power control. This fundamental analytical framework can also be used to develop an integrated LVC device customized for power electronic applications.

The limitations of LVCs include their restricted voltage and current handling capacity, potential harmonic generation, and parasitic reactance due to the LVC package. Low current handling capacity is caused by the voltage buildup during the half cycle of an ac signal, which may exceed the device voltage rating. To increase the current limit, one approach involves increasing the operating frequency, effectively allowing higher current amplitudes while adhering to the voltage rating. The listed limitations arise from the current state of LVC technology, which relies on the parasitic capacitance of discrete semiconductor devices like diodes or body diodes of MOSFETs. Moreover, precise control of the diffusion process is often challenging, causing m to vary around the targeted value. These semiconductor devices are primarily optimized for high-power and/or high-frequency operations, typically leading toward minimized parasitic capacitance. To address some of the listed constraints, an integrated LVC device offering high zero-bias junction capacitance and low harmonic content (through m close to 0.5) can be designed in the future. The application of the model in designing various converters will be the subject of some future publications.

Appendix A
Deriving Current-Dependent Model of LVC for $m = 0.5$

The LVC is connected to a sinusoidal current source $i_{\mathrm{LVC}} = I_m \sin(\omega t)$. The voltage across the LVC can be calculated in terms of the phase angle $\theta = \omega t$ as

$$\begin{aligned} v_{\mathrm{LVC}} &= v_{C1} - v_{C2} \\ &= V_B P^{\frac{1}{1-m}} \left([1 + P_S - \cos\theta]^{\frac{1}{1-m}} - [1 + P_S + \cos\theta]^{\frac{1}{1-m}} \right) \end{aligned} \tag{68}$$

where

$$P = \frac{I_m (1-m)}{\omega C_{j0} V_B} \text{ and } P_S = \frac{1}{P}\left(1 - \frac{V_S}{V_B}\right)^{1-m}. \tag{69}$$

Substituting $m = 0.5$ leads to

$$v_{\mathrm{LVC}} = V_B P^2 \left([1 + P_S - \cos\theta]^2 - [1 + P_S + \cos\theta]^2 \right) \tag{70}$$

where P and P_s are given by

$$P = \frac{1}{2}\frac{I_m}{\omega C_{j0} V_B} \text{ and } P_S = \frac{1}{P}\sqrt{1 - \frac{V_S}{V_B}}. \tag{71}$$

Solving (70) results in

$$v_{\mathrm{LVC}} = 4 V_B P^2 (1 + P_S)(-\cos\theta). \tag{72}$$

Substituting (71) into (72) and using trigonometric identities leads to

$$\begin{aligned} v_{\mathrm{LVC}} = 4V_B &\left(\frac{1}{2}\frac{I_m}{\omega C_{j0} V_B}\right)^2 \\ &\times \left(1 + \frac{2\omega C_{j0} V_B}{I_m}\sqrt{1 - \frac{V_S}{V_B}}\right) \sin\left(\theta - \frac{\pi}{2}\right). \end{aligned} \tag{73}$$

The aforementioned equation can be simplified and expressed as

$$v_{\mathrm{LVC}} = \left(\frac{I_m}{V_B \omega^2 C_{j0}^2}(I_m + I_0)\right) \sin\left(\theta - \frac{\pi}{2}\right) \tag{74}$$

$$I_0 = 2\omega C_{j0} V_B \sqrt{1 - V_S/V_B}. \tag{75}$$

Appendix B
Deriving Voltage-Dependent Model of LVC for $m = 0.5$

A sinusoidal voltage source $v_{\mathrm{LVC}}(t) = V_m \cos(\omega t)$ is connected to the LVC. The solution for (θ,$m = 0.5$) can be obtained by solving (35) for $m = 0.5$ as

$$\frac{\left(1 + \sqrt{1 - \frac{V_m \cos(\theta)}{V_B + v_{C1}(\theta)}}\right)\left(1 - \sqrt{1 - \frac{V_m}{V_B + V_m - V_S}}\right)}{\left(1 - \sqrt{1 - \frac{V_m \cos(\theta)}{V_B + v_{C1}(\theta)}}\right)\left(1 + \sqrt{1 - \frac{V_m}{V_B + V_m - V_S}}\right)} = \pm \sec\theta. \tag{76}$$

The following substitution is used to simplify the aforementioned equation:

$$p = \sqrt{1 - \frac{v_{\mathrm{HBV}}}{V_B + v_{C1}}} \tag{77}$$

$$p_0 = \sqrt{1 - \frac{V_m}{V_m + V_B - V_S}} \tag{78}$$

$$\beta = \frac{1 - p_0}{1 + p_0}. \tag{79}$$

Substituting (77)–(79) in (76) leads to

$$\beta \frac{(1+p)}{(p-1)} = \pm \sec\theta. \tag{80}$$

Now, (80) is solved for p as

$$p = \frac{\mp 1 - \beta\cos\theta}{\beta\cos\theta \mp 1} = \sqrt{1 - \frac{V_m \cos(\theta)}{V_B + v_{C1}}}. \tag{81}$$

Squaring both sides and solving it leads to

$$\frac{V_B + v_{C1}}{V_m \cos(\theta)} = \frac{1 + \beta^2 \cos^2(\theta) \mp 2\beta\cos(\theta)}{\mp 4\beta\cos(\theta)}. \tag{82}$$

v_{C1} is solved as

$$v_{C1} = V_m \left(\mp \frac{1}{4\beta} + \frac{\cos(\theta)}{2} \mp \frac{\beta \cos^2(\theta)}{4} \right) - V_B. \quad (83)$$

Since diode D_1 will be positively biased, the voltage across v_{c1} is given by

$$v_{C1} = V_m \left(\frac{1}{4\beta} + \frac{\cos(\theta)}{2} + \frac{\beta \cos^2(\theta)}{4} \right) - V_B. \quad (84)$$

Simplifying v_{C1} leads to

$$v_{C1} = V_m \left(\left(\frac{1}{4\beta} + \frac{\beta}{8} \right) + \frac{\cos(\theta)}{2} + \frac{\beta \cos(2\theta)}{8} \right) - V_B. \quad (85)$$

The voltage across the LVC is given by

$$v_{\text{LVC}} = v_{C1} - v_{C2} = V_m \cos(\theta). \quad (86)$$

Using (85) and (86), v_{C2} is derived as

$$v_{C2} = V_m \left(\left(\frac{1}{4\beta} + \frac{\beta}{8} \right) - \frac{\cos(\theta)}{2} + \frac{\beta \cos(2\theta)}{8} \right) - V_B \quad (87)$$

where β can be explicitly written as

$$\beta = \frac{\sqrt{V_B + V_m - V_S} - \sqrt{V_B - V_S}}{\sqrt{V_B + V_m - V_S} + \sqrt{V_B - V_S}}. \quad (88)$$

i_{LCV} can now be solved using the following equations:

$$i_{\text{LVC}}(\theta) = \omega C_1(v_{C1}) \frac{dv_{C1}}{d\theta} \quad (89)$$

$$C_1(v_{C1}) = \frac{C_{j0}}{\sqrt{1 + \frac{v_{C1}}{V_B}}} \quad (90)$$

$$\frac{dv_{C1}}{d\theta} = -V_m \left(\frac{\sin(\theta)}{2} + \frac{\beta \sin(2\theta)}{4} \right). \quad (91)$$

Using (89)–(91), i_{LVC} is expressed as

$$i_{\text{LVC}}(\theta) = - \frac{\omega C_{j0} V_m}{\sqrt{1 + \frac{V_m \left(\frac{1}{4\beta} + \frac{\cos(\theta)}{2} + \frac{\beta \cos^2(\theta)}{4} \right) - V_B}{V_B}}} \times \left(\frac{\sin(\theta)}{2} + \frac{\beta \sin(2\theta)}{4} \right). \quad (92)$$

i_{LVC} is simplified as

$$i_{\text{LVC}}(\theta) = - \frac{\omega C_{j0} V_m}{\sqrt{\frac{V_m}{\beta V_B} (1 + \beta \cos(\theta))^2}} \sin(\theta)(1 + \beta \cos(\theta)) = \omega C_{j0} \sqrt{\beta V_m V_B} \cos\left(\frac{\pi}{2} + \theta \right). \quad (93)$$

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