# An RF Power Amplifier Integrated With the Self-Health Monitor Sensor and Multisource Energy Harvesting Circuit

Min Sun and Xiaoping Liao, *Member, IEEE*

***Abstract*—This work proposes an innovative 1.76 mm × 1.76 mm circuit system, which fully integrates an radio frequency (RF) power amplifier (PA) containing a thermopile, multisource energy harvesters, and an energy combination circuit. And it is fabricated in a 0.18-$\mu$m RF complementary metal oxide semiconductor (CMOS) technology. The circuit enables self-health monitoring of the power transistor as well as multisource energy harvesting (EH) for future self-powering of the system. The input coplanar waveguide port is replaced by a three-port filter that helps reduce standing waves in the transmission line. And the PA transistor integrates a thermopile to absorb circuit-dissipated heat and monitor health status by detecting the dc output voltage of the integrated thermopile. Then, a diode chain connected parallel in the circuit is used as the electrostatic discharge protection circuit, which can also be considered as a solar cell when there is sunlight incident on the chip. In addition, standing wave energy, dissipated thermal energy, light energy, and electrostatic charge energy (when it is present) are combined and harvested by a multisource EH circuit at the same time. The tested center frequency of the RF PA is 4.3 GHz and the corresponding $S_{11}$ is −19.09 dB. When the input power is 0 dBm, the amplifier gain, the output voltage of the EH circuit, and the output voltage of the terminal power sensor are 10.6 dB, 458.88 mV, and 30 $\mu$V, respectively.**

***Index Terms*—Multisource energy harvesting (EH), radio frequency (RF) complementary metal oxide semiconductor (CMOS) integrated circuit (IC), self-health monitor.**

## I. Introduction

THE integrated circuits (ICs) for wireless sensor nodes in smart structures, medical devices, wireless communication, etc. have encountered serious challenges in terms of reliability of the power electronics systems [1], [2]. First, it is known that most of the electrical energy applied to the circuit is converted to thermal energy, which leads to the self-heating phenomenon of power transistors [3]. And the operating temperature of the transistor will affect the performance of the power devices [4]. So, it is essential to find solutions to measure the operating temperature of power devices and dissipate thermal energy. In recent studies, there are many solutions to measure the operating temperature, and the measured temperature can indicate the operating health status of the power devices.

Common solutions are optical methods, the utilization of thermal probes, and electrical methods [5]. The optical methods include optical fibers, infrared (IR) cameras, and IR microscopes, etc., which can directly display the temperature distribution [6], [7], [8]. The thermal probes are thermistors or thermocouples in contact with the chip, and the temperature of the chip can be measured from their dc outputs [9]. And many other researchers have proposed electrical methods that can be used to calculate the operating temperature by evaluating voltage and current data [10]. In addition, proper packaging to generate a heat sink under the substrate of the chip is a common way to dissipate circuit system heat [11]. The packaging solution can effectively dissipate heat, however, it always requires a relatively high cost. So, in this article, we propose a new solution to achieve temperature monitoring and simultaneously dissipate thermal energy generated in the circuit, which is based on a thermopile. Different from the thermal probes used in other works, the thermal sensor is not an external device in contact with the chip, but a thermopile monolithically integrated with the power transistor. The thermopile is designed to be very close to the transistor, which ensures that the thermopile is able to absorb as much of the thermal energy converted from the dc power supply as possible. According to the Seebeck effect, the thermopile can convert thermal energy into electrical voltage. And we can infer the operating temperature of the transistor by analyzing the output voltage of the thermopile.

The other part of this work is the multisource energy harvesting (EH) circuit to collect and reuse the energy generated in the circuit. EH technology has been widely used in wireless sensor nodes (WSNs) to provide power supply to them in place of conventional batteries [12], [13]. In general, the energy harvesters collect energy from the ambient environment [14]. Mostly, these energy sources are dependent on environmental conditions, and in order to improve the robustness of the power supply, multisource energy harvesters were proposed [15], [16], [17]. These multisource energy harvesters can collect different types of the energies in specific orders or simultaneously. Therefore, the multisource energy combining circuit proposed in this work has three input paths where the different types of energy can be

Manuscript received 6 June 2023; revised 26 September 2023; accepted 31 October 2023. Date of publication 6 November 2023; date of current version 22 December 2023. This work was supported by the National Natural Science Foundation of China under Grants 61974023 and 61674031. Recommended for publication by Associate Editor H. Hofmann. *(Corresponding author: Xiaoping Liao.)*

The authors are with the Key Laboratory of MEMS, Ministry of Education, Southeast University, Nanjing 210096, China (e-mail: min_s@seu.edu.cn; xpliao@seu.edu.cn).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3330499.

Digital Object Identifier 10.1109/TPEL.2023.3330499

harvested at the same time. The energy sources of the EH circuit are from the energy generated during the operation of the circuit itself. Among them, the first energy source is the standing wave energy that is harvested by a three-port filter. And the presence of the filter also improves the electromagnetic compatibility (EMC) rather than employing conventional EMC filtering. The second energy source is the thermal energy generated in the transistor, which is harvested by an integrated thermopile. And the third energy source is the electrostatic charges (if it exists) or the light energy collected by a diode chain. The diode chain connected in the circuit enables electrostatic discharge (ESD) protection and can also be treated as photodiodes if there is sunlight incident on the chip. And the proposed multisource EH circuit consists of two collection stages. The standing wave energy is converted into two ac signals by a transformer and combined with the dc output voltage comes from the integrated thermopile through a cross-coupled rectifier. In addition, if the electrostatic energy is present, it can be stored in a storage capacitor and added to the second stage of the energy harvester. When there is incident light, the light energy is stored in the same capacitor to be collected. Therefore, this multisource EH circuit enables the combination and simultaneous harvesting of radio frequency (RF), thermal, light, and electrostatic energy (if it occurs).

Furthermore, this work fully monolithically integrates the energy harvesters and the combining circuits with the power devices. Compared to the work presented in [9], which focuses only on the integration of energy harvesters, and in [18] and [19], which emphasizes energy combining and power management circuits, this work investigates all of the PA, the multisource energy harvesters, and energy combining circuits, as well as their full integration by a standard complementary metal oxide semiconductor (CMOS) process. In addition, the proposed PA and the integrated energy harvesters are mutually reinforcing. The three-port filter not only collects wasted RF energy but also provides a new way to eliminate the impacts of standing waves at the input port of the PA. And the thermopile integrated with the power transistor is able to absorb wasted thermal energy, as well as decreases the working temperature and improves the power gain of the amplifier. And the diode chain connected in the circuit helps to achieve ESD protection of the circuit and can collect solar energy or electrostatic charges at the same time. On the other hand, the presence of the PA also contributes to EH. Since the energy collected by the energy harvesters are the energy sources that generated in the circuit itself, they are not entirely dependent on the external environment and is ideal for powering always-on devices such as WSNs of the Internet of Things in the power system.

The rest of this article is organized as follows. In Section II, the design details of the PA integrated with the thermopile and the multisource energy harvester are illustrated. This section also includes a description of the structure of the terminal power sensor, the three-port filter, and the diode chain. The experimental performance of the PA and the outputs of the energy harvesters and the EH circuit are presented and discussed in Section III. Finally, Section IV concludes the article.

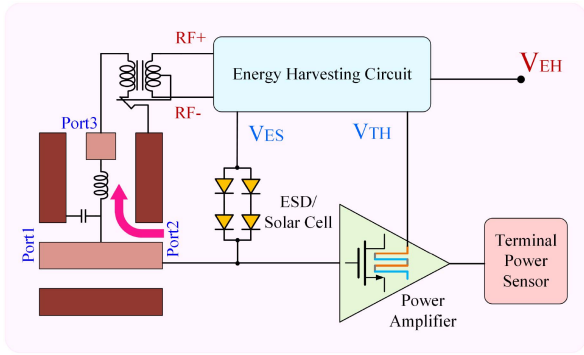
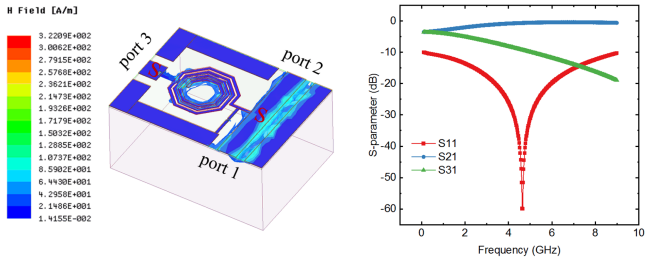



Fig. 1. Block diagram of the circuit system.




(a) (b)

Fig. 2. (a) Electromagnetic field (EMF) distribution of the three-port filter network simulated by Ansys HFSS. (b) Simulation results of the filter S-parameters.

## II. System Design and Analysis

Fig. 1 is the block diagram of the entire IC system in this work, which includes the PA, energy harvesters, and energy combining circuit. The schematic of the structures and circuits are introduced as follows.

### A. Three-Port Filter Network

Due to impedance mismatch at the input port, the existence of standing waves is a common phenomenon in RF ICs. In a transmission line, there are two main types of waves, including the traveling waves that transfer energy and the standing waves formed by the superposition of two waves transmit in opposite directions without transferring energy. Commonly, the terminal is grounded directly or through a resistance to reduce the effect of the standing waves and realize good EMC [20]. So, in this work, a filter network is designed in front of the PA to replace the conventional coplanar waveguide (CPW). It has three ports and the matching network consists of a parallel capacitor and a series octagonal inductor, whose schematic view is shown in Fig. 2(a). As a result, RF waves that can be amplified by the PA are introduced to the input port (port 2) of the PA, which are the vast majority of the initial RF energy. The other waves, including standing waves, which cannot be transmitted to the PA for amplification are passed through an additional new path with the help of the three-port filter and output from port 3. The electromagnetic simulation of this three-port filter is implemented by Ansys HFSS, and the EMF distribution is also shown in Fig. 2(a) when the input power is set to 0 dBm. And the

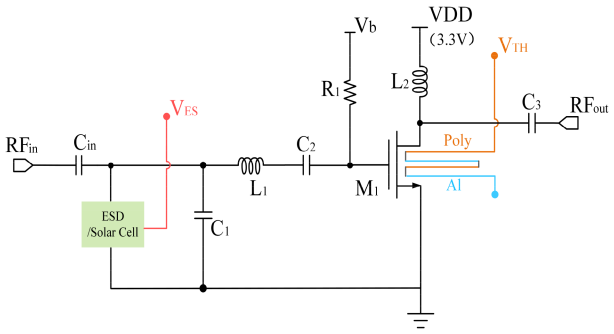



Fig. 3. Circuit schematic of the PA integrated with the thermopile.

TABLE I
PARAMETERS OF THE POWER AMPLIFIER (PA)

| Symbol | $C_{in}$ | $C_1$ | $C_2$ | $C_3$ | $R_1$ | $L_1$ | $L_2$ | $M_1$ |
|---|---|---|---|---|---|---|---|---|
| Value | 10 | 800 | 6 | 6 | 600 | 4.2 | 600 | 176/0.18 |
| Units | pF | fF | pF | pF | Ω | nH | pH | μm |

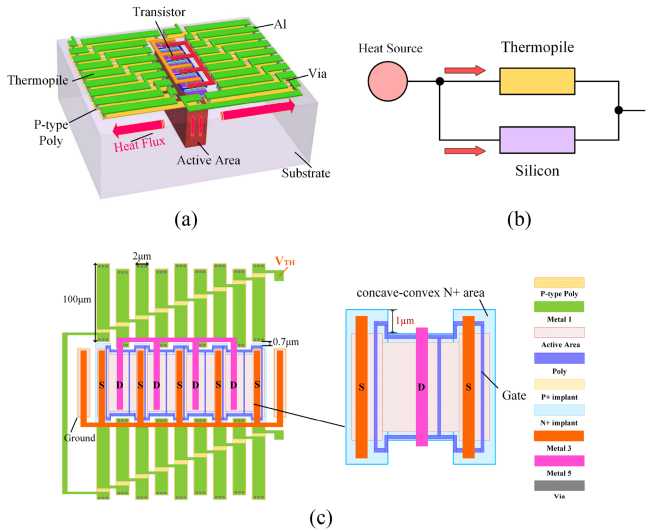



Fig. 4. (a) Structure of the transistor integrated with the thermopile. (b) Schematic of thermal conduction routes when PA is in operation. (c) Top view of the integrated thermopile and the materials in use.

S-parameter results for each of the 3 ports are shown in Fig. 2(b). At the center frequency of 4.6 GHz, the value of return loss $S_{11}$ is −60 dB, and the insertion loss $S_{21}$ and $S_{31}$ are −0.62 dB and −9 dB, respectively. Both the EMF distribution and S-parameter results indicate that the majority of the RF energy is delivered to port 2 and amplified by the PA, while the energy flowing to port 3 is a very small amount of the input energy as well as the standing wave energy.

### B. PA Integrated With the Thermopile

The circuit schematic of the PA is shown in Fig. 3. It is a basic single transistor amplifier with the novelty that the active area of the power transistor is concave and convex in shape and surrounded by a thermopile, and the output power is measured by a terminal power sensor. The parameters of the PA are listed in Table I. The three-dimensional view of the reconstructed transistor integrated with the thermopile is shown in Fig. 4(a). The thermopile is composed of aluminum and *p*-type polysilicon arms stacked on top and below. The hot and cold ends of the thermopile are placed near and away from the transistor, respectively. When the PA is in operation, much of the input dc electrical energy is converted to thermal energy in the active area of the transistor. The thermopile placed around the transistor will then drive part of the heat flow from the hot side to the cold side, which can help dissipate the thermal energy of the chip. And the presence of the thermopile also decreases the working temperature of the PA and thus improves the output performance.

Based on the law of conservation of energy, the power routing of the PA is expressed as

$$P_{\mathrm{RFin}} + P_{\mathrm{DC}} = P_{\mathrm{PAout}} + P_{\mathrm{RFout}} + P_{\mathrm{TH}} + P_{\mathrm{loss}} \tag{1}$$

where $P_{\mathrm{RFin}}$ is the input RF power of the IC, $P_{\mathrm{DC}}$ is the input dc power, $P_{\mathrm{PAout}}$ is the output power of the amplifier, $P_{\mathrm{RFout}}$ is the RF energy collected by the EH circuit. $P_{\mathrm{TH}}$ is the thermal energy absorbed by the thermopile, and $P_{\mathrm{loss}}$ is the power loss in the circuit. In this design, the vast majority of the power loss is heat dissipation, and heat conduction is the primary method of heat transfer. Therefore, when the PA is in operation, it can be assumed that a heat source is formed in the transistor channel. As shown in Fig. 4(b), a transistor with a thermopile has two main thermal conduction paths, one through the thermopile and the other through the silicon substrate. Analogies can be made between the heat system and the electrical system [21]. Among them, heat flow and thermal resistance are analogous to current and electrical resistance, respectively. Therefore, the amount of heat transferred through these two paths is related to the thermal resistance of the silicon substrate and the thermopile. The thermal amount is inversely proportional to the thermal resistance, and the ratio m of heat is as follows:

$$m = \frac{P_{\mathrm{TH}}}{P_{\mathrm{loss}}} = \frac{\Theta_{\mathrm{Si}}}{\Theta_{\mathrm{TH}}}. \tag{2}$$

And the thermal resistance $\Theta_{si}$ and $\Theta_{TH}$ of the silicon substrate and the thermopile are expressed as

$$\Theta_{\mathrm{Si}} = \frac{h_{\mathrm{si}}}{\lambda_{\mathrm{si}} A_{\mathrm{si}}} \tag{3}$$

$$\Theta_{\mathrm{TEG}} = \frac{l_{\mathrm{TH}}}{N \cdot \lambda_m A_{\mathrm{TH}}} \tag{4}$$

where $\lambda_{\mathrm{si}}$ and $\lambda_m$ are thermal conductivities of the silicon and the thermopile, respectively. And other parameters of the transistor integrated with thermopile are shown in Table II. Thus, the energy absorbed by the thermopile can be calculated as

$$P_{\mathrm{TH}} = (P_{\mathrm{RFin}} + P_{\mathrm{DC}} - P_{\mathrm{PAout}} - P_{\mathrm{RFout}}) \cdot \frac{m}{1+m}. \tag{5}$$

The value of m is calculated to be 0.41, and the proportion of the energy harvested by the thermopile is 29.08% of the total input minus the total output. Based on the analysis, the thermal energy absorbed by the thermopile can be calculated.

TABLE II
SIZE PARAMETERS OF THE INTEGRATED THERMOPILE

| Parameters | | Value | Unit |
|---|---|---|---|
| $\lambda_{si}$ | thermal conductivity of silicon | 148 | W/( m•K) |
| $\lambda_m$ | thermal conductivity of thermocouple | 90.06 | W/( m•K) |
| $h_{si}$ | height of silicon substrate | 430 | μm |
| $l_{TH}$ | length of thermocouple | 100 | μm |
| $A_{si}$ | silicon surface area of active area | 563.24 | $\mu m^2$ |
| $A_{TH}$ | cross-section of thermocouple | 2.6 | $\mu m^2$ |
| $N$ | numbers of thermocouple pairs | 34 | -- |

TABLE III
CHARACTERISTICS OF THE INTEGRATED THERMOPILE

| Parameters | | Value | Unit |
|---|---|---|---|
| $\alpha_m$ | seebeck efficient of the thermocouple | 0.1045 | mV/K |
| $R_g$ | internal resistance of the thermocouple | 13.58 | KΩ |
| $A$ | surface area of the thermopile | 215.4×71.82 | $\mu m^2$ |

According to the analysis, since part of the dc energy is harvested by the thermopile, it can be assumed that the dc energy used by the amplifier should subtract the energy collected by the thermopile. To calculate the efficiency of the PA when considering EH, the input power to the PA is turned into $P_{\text{RF-PA}}$, which is the portion coming from port 2 of the three-port filter. It is about 86% of the initial total input power according to the simulation results of the filter, and it is expressed as

$$P_{\text{RF-PA}} = 0.86 \cdot P_{\text{RFin}}. \tag{6}$$

At this point, the power added efficiency (PAE) of the PA is expressed as

$$\text{PAE} = \frac{P_{\text{PAout}} - P_{\text{RF-PA}}}{P_{\text{DC}} - P_{\text{TH}}}. \tag{7}$$

It is clear that since the dc power used by the amplifier is reduced, the PAE of the PA increases with the presence of the integrated thermopile.

In addition, the thermopile also works as a transistor health monitor based on the Seebeck Effect, which is expressed as

$$V_{\text{TH}} = N \cdot \alpha_m \cdot \Delta T \tag{8}$$

where $\alpha_m$ is the Seebeck efficient difference between aluminum and $p$-type polysilicon, $N$ is the number of pairs of the thermopile, and $\Delta T$ is the temperature difference between the hot and cold ends of the thermopile. The values and descriptions of the parameters are shown in Table III. For given materials, the value of $\alpha_m$ is constant. Hence, it can be seen that the output voltage is linearly related to the temperature gradient of the thermopile. Then, the temperature difference can be derived from the output voltage of the thermopile, which also realizes the health monitoring of the device.

To absorb more dissipated thermal energy, the transistor is designed with a concave–convex shape that allows the thermopile to be closer to the active area. Thermal simulation of the proposed transistor integrated with the thermopile as well as the normal one is performed by Ansys workbench. The transistors both have 16 fingers and are surrounded by 34 pairs of the thermocouples with a size of 2 $\mu$m × 100 $\mu$m. The detailed top view of the concave–convex transistor with the thermopile is shown in Fig. 4(c). The proposed transistor has a recessed part that allows the thermopile to be closer to the active area. And the active area of the proposed transistor is smaller compared to that of a normal transistor, which increases the silicon thermal resistance and reduces the heat loss through the silicon substrate according to (2) and (3). And the simulation results are shown in Fig. 5. It shows that when the input heat flux is the same, the temperature difference and output voltage of the proposed concave–convex transistor are larger. Fig. 6(a) and (b) shows the simulation results of the relationship between the output voltage and temperature difference of the thermopile, and it is consistent with the analysis that the output voltage and temperature difference have a linear relationship. The simulation results of the output voltage and temperature difference of the thermopile for both types of transistors at different input dc sources are shown in Fig. 6(c) and (d). The results show that the thermopile integrated with the proposed transistor has better performance than that with the normal one and the thermopile can output a significant voltage in higher power circuits. And with the increase of the dc input, the output difference between the two thermopiles becomes larger as well, which is shown in Fig. 6(e) and (f). Therefore, this research provides a guideline for the design of the thermopile-related transistor to investigate the most appropriate distance between the thermopile and the transistor to obtain the optimal performance.

Since the integrated thermopile is also a thermoelectric generator, it is necessary to analyze the energy conversion characteristics of the proposed thermopile. And the performance is

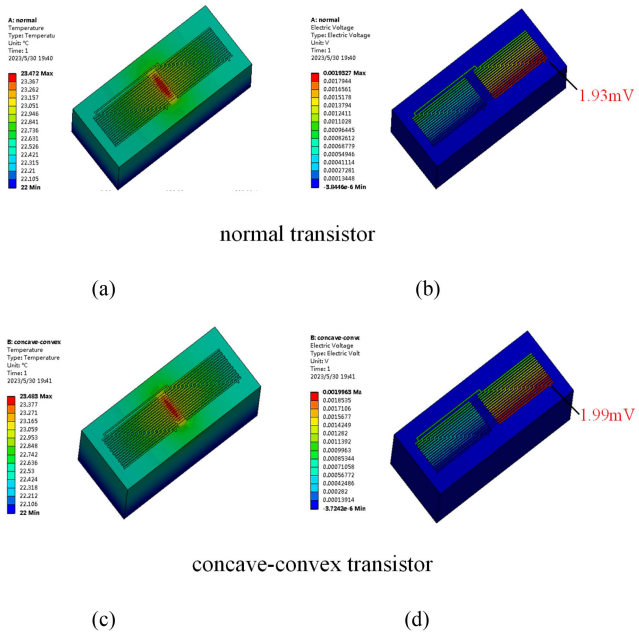



Fig. 5. (a) and (b) Thermal distribution of the integrated thermopile with normal and concave–convex active areas. (c) and (d) Output voltage of the integrated thermopile with normal and concave–convex active areas.

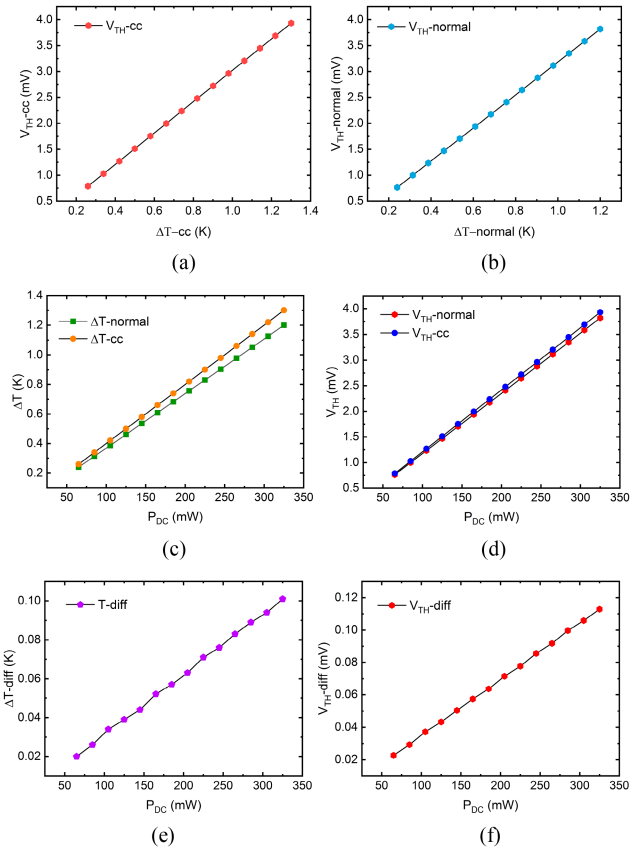



Fig. 6. Thermal simulation results of the integrated thermopiles with the normal transistor and the concave–convex transistor, respectively. (a) and (b) Relationship between temperature difference and output voltage of the thermopiles. (c) and (d) Temperature difference and output voltages of the integrated thermopiles for different dc power inputs. (e) and (f) Temperature gradient difference and output voltage difference between the two types of the thermopiles at different dc power inputs.

characterized by voltage factor (VF) and maximum power factor (PF), which are expressed as

$$\mathrm{VF} = \frac{V_{\mathrm{TH}}}{A \cdot \Delta T} \tag{9}$$

$$\mathrm{PF} = \frac{P_{\mathrm{out}}}{A \cdot \Delta T^2} \tag{10}$$

where $V_{\mathrm{TH}}$ is the open-circuit output voltage of the thermopile, $A$ is the surface area of the thermopile, $\Delta T$ is the temperature difference between the hot and cold end of the thermocouples. And $P_{\mathrm{out}}$ is the maximum output power, which is expressed as

$$P_{\mathrm{out}} = \frac{V_{\mathrm{TH}}^2}{4R_g} \tag{11}$$

where $R_g$ is the internal resistance of the thermopile.

In this work, the stacked thermopile is also used in a terminal power sensor. It consists of a CPW as the input port, two terminal resistors connected to the waveguide pads to absorb the input power to generate Joule heat and two thermopiles close to the terminal resistance. The microscope photograph and the structure of the terminal power sensor are shown in Fig. 7(a) and (b). The terminal resistors are made of 100 Ω N-type Polysilicon

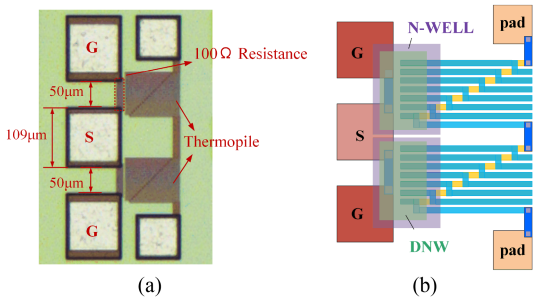



Fig. 7. (a) Microscope photograph of the terminal power sensor. (b) Schematic structure of the terminal power sensor.

to achieve the 50 Ω impedance matching at the wave port, and the thermopile is consisted of 40 pairs of the thermocouples. In [22], it was verified that the addition of the *n*-well below the termination resistors and the cold ends of the thermopile improves the sensitivity and linearity of the power sensor. Based on this, in this work, an additional *n*-well as well as a deep n-well are added at the same place, which may further improve the performance of the power sensor. When RF power is applied to the CPW port, the input power will be converted into Joule heat of the terminal resistance. The thermopile will then absorb the heat energy, and generate a temperature difference between the cold and hot ends. As a result, the input RF energy can be converted to thermal energy, which can then be converted to electrical energy through the thermopile. For the circuit system in this work, the input power of the terminal power sensor is the output power of the PA. Therefore, the output power of the amplifier can be measured and analyzed based on the output voltage of the terminal power sensor. Also, the power gain of the PA can be derived from the difference between the input power of the terminal power sensor and that of another identical independent power sensor. So, when these two power sensors have the same output voltage, the input power difference is the gain of the PA. And the design of the terminal power sensor not only improves the integration of the whole system but also enables in-line detection of the output power while the power devices are in operation.

### C. ESD Protection Circuit/Solar Cell

In this design, several diodes are connected in parallel in the circuit and it serves two purposes. First, if there are electrostatic charges at the input port, it can be discharged to ground through the diode chain or collected by a storage capacitor, which helps to realize ESD protection of the circuit. Second, the diodes can also be considered as photodiodes if there is sunlight incident into the PN junction. To be compatible with transistors in PA and EH circuit, the diodes are of *p*-diff/*n*-well construction, whose structure is shown in Fig. 8. According to the photovoltaic effect, when there is a light incident on the chip, the light energy can penetrate the P-N junction and excite holes, electrons and electron-hole pairs, and these carriers will be collected by the aluminum electrodes. Thus, the light energy can be harvested and converted to electrical energy by the diodes. In general, the

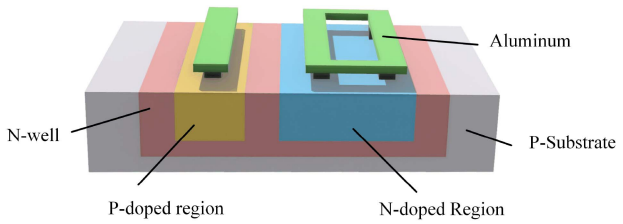



Fig. 8. Three-dimensional view of the structure of the substrate diode.

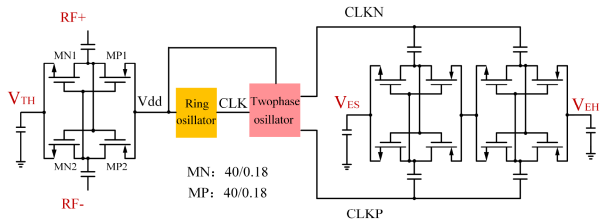



Fig. 10. Circuit schematic of the multisource energy harvester.

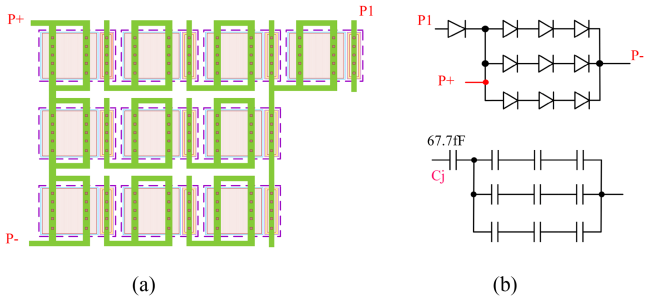



Fig. 9. (a) Top view of the diode chain used in the circuit. (b) Equivalent circuit of the diode junction capacitors.

design objectives for ESD diodes and photodiodes are not the same. In the design of ESD diodes, it is desirable to use low capacitance, low leakage current, small area diodes to minimize the impact on impedance matching and to minimize the total circuit area [23]. And factors to be considered in the design of a photodiode include exposed area, connection method, quality of the substrate, and packaging [9]. Therefore, we made a tradeoff between them. First, the area of the diodes makes the full use of the dummy area of the IC, without adding extra area to the circuit. And in order to make a trade-off between the requirements for low capacitance and more exposure area, the active area of the diode is much larger than that of a normal ESD diode, but due to the way the diodes are connected (one redundant diode in series), the total capacitance of the diode chain is still small. The diode chain is connected as shown in Fig. 9(a), and the equivalent circuit of the capacitor is shown in Fig. 9(b). According to the simulation, the capacitance of one diode is 67.7 fF, and the total capacitance is 33.8 fF. It has almost no effect on circuit matching, as confirmed by the experiment and simulation.

### D. Multisource EH Circuit

In parts A, B, and C, it illustrates that in this system, dissipated thermal energy, RF energy, electrostatic charge energy (if it is present) and light energy are all converted to electrical energy. Therefore, a multisource EH circuit is designed to combine all the electrical outputs and to enable the collection of these energies. The multisource EH circuit has three input paths, ensuring that multiple energies can be harvested at the same time. The schematic circuit of the energy harvester is shown in Fig. 10. It shows that the EH circuit is based on cross-coupled rectifiers and it has two collection stages. The first rectifier is the first stage, which collects both the RF energy and the dissipated thermal energy. When there is RF power incident from the input port, most of the energy is exported from port 2 and amplified by the PA. The standing wave flows out from port 3 of the filter is converted to ac signals with the same amplitude and the opposite phases through a balun coupler. The ac signals are the ac inputs of the first level of the rectifier and is rectified to a dc output. At the same time, since the transistor is in operation, the integrated thermopile around it can absorb the thermal energy and transform it to a dc output $V_{\mathrm{TH}}$, and is added to the rectifier as a bias. The total dc output of this rectifier is the first stage output of the EH circuit, which collects the RF energy together with thermal energy dissipated by the circuit.

The output of the first stage of the rectifier is also the driver of a ring oscillator that generates a clock signal for a two-phase oscillator. Then, a two-stage charge pump based on the same cross-coupled rectifier is driven by the positive and negative clock signals generated by the two-phase oscillator. And the dc output $V_{\mathrm{ES}}$ collected by the diodes is also added to the rectifier as another bias, then the output of this stage is raised by the charge pump to ensure sufficient voltage for subsequent power supply. The advantage of this multisource energy harvester is that all the energies can be harvested at the same time, regardless of the strength or weakness of the energy sources. Meanwhile, the EH circuit is based on the rectifier of the same structure, which will simplify the architecture and design process of the EH circuit.

### E. Fabrication Process

The IC is manufactured by a standard 0.18-$\mu$m CMOS 1-poly-6-Metal technology, and the fabrication process is shown in Fig. 11. In this design, NMOS is used as the power device and the description of the fabrication process focuses on the fabrication of NMOS transistor.

The manufacturing process starts with the preparation of the active region for the NMOS transistor. Then a sacrificial oxide layer is grown to trap the defects on the silicon surface and etched with hydrofluoric acid (HF) solution to obtain a clean silicon surface. Next, grow a gate oxide layer and deposit a polysilicon layer through chemical vapor deposition (CVD) as the gate layer of the transistor. After this, through precise photolithography and dry etching, the polysilicon layer is patterned to form the transistor gate. Then, grow a thin oxide layer, and ion-implantation is then performed to form lightly doped drain and source regions. Subsequently, a thin $Si_3N_4$ layer is deposited by CVD. Next, the horizontal surface of the $Si_3N_4$ is etched through reactive ion etching, leaving the sidewalls as spacers that serves as a

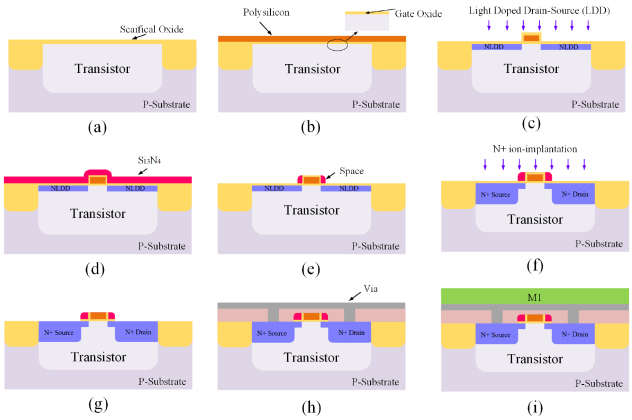



Fig. 11. Fabrication process of the IC system.

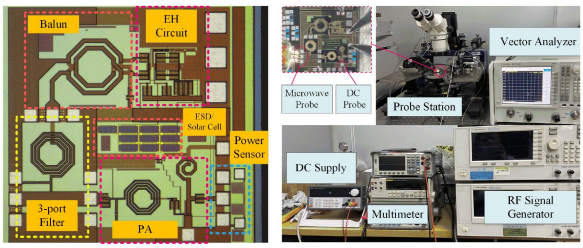



Fig. 12. (a) Microscope photograph of the chip. (b) Test platform of this work.

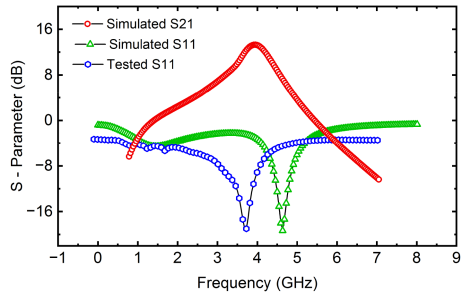



Fig. 13. Simulated and tested S-parameter of the PA.

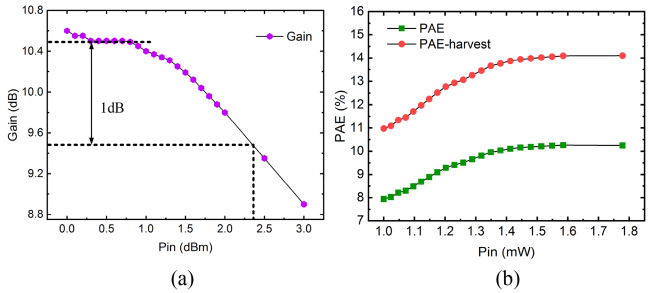



Fig. 14. (a) Tested power gain of the PA with different input power. (b) Power-added efficiency of the PA with and without EH.

barrier for subsequent ion implantation. Finally, the oxidation layer is removed by HF to expose the gate, source, and drain regions. The next steps are the preparation of through-holes and aluminum interconnections. First, deposit a $SiO_2$ layer as the passivation layer and it is selective etched to define the contacts. Then, sputter a layer of aluminum as the first layer of the metal. By repeating the above steps, the final 1-poly-6-metal device is formed.

## III. Measurement and Discussion

Fig. 12(a) is the microscope photograph of the chip, which has a size of 1.76 mm $\times$ 1.76 mm. In this section, the power gain of the amplifier, the output voltage of the integrated thermopile, the performance of the energy harvesters, and the final output of the multisource EH circuit are measured and discussed. Fig. 12(b) is the experimental setup used in this work. The chip under test is placed on the probe station. The RF signal is generated by Agilent E8257D signal generator and Agilent PNA Network Analyzer is used to measure the S-parameters of the system. The dc outputs of the chip under test are measured by a Fluke 45 multimeter.

### A. Performance of the Thermopile-Related PA

In the test of the PA, the dc power supply is set to 3.3 V. First, the S-parameter of the system is measured by the vector analyzer. Since two load resistors are connected to the output pads for absorbing the output power of the amplifier and converting the output power into thermal energy, the output power and power gain of the PA are derived from the output voltage of the terminal thermopile. Therefore, only the return loss $S_{11}$ is tested and compared with the cadence simulation results, as shown in Fig. 13. It can be seen that the tested and simulated $S_{11}$ have the same tendency. The measured center frequency of the PA is 4.3 GHz, and the tested $S_{11}$ at this point is $-19.09$ dB. Second, the power gain of the amplifier is analyzed through the terminal power sensor and the identical stand-alone power sensor. When the two power sensors have the same dc output, the input power of the stand-alone power sensor and the output power of the PA are equal. Hence, the power gain of the amplifier is the difference in the input power between the two power sensors that have the same dc output. The tested results of the power gain are shown in Fig. 14(a), which shows that the input power 1 dB compression point (IP1dB) is 2.3 dBm.

When the input power is 0 dBm, the output voltage of the terminal power sensor is 30 $\mu$V, and the corresponding power gain is 10.6 dB. As (7) shows, the PAE of the PA improves when the EH circuit is considered. Thus, Fig. 14(b) shows the PAE of the PA with and without considering EH. It shows that the PAE of the PA increases by about 3% when the initial RF power is 1 mW. The tested results also show that the PA is working properly, which means that the existence of the integrated thermopile does not impact the normal operation of the amplifier. On this basis, different thermocouples can be designed to be integrated with power devices without affecting the circuit performance.

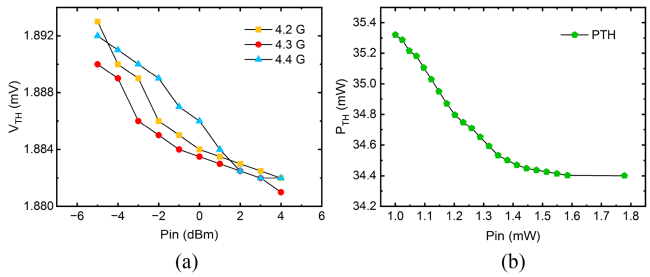



Fig. 15. (a) Output voltage $V_{\mathrm{TH}}$ of the integrated thermopile versus input power at the frequencies of 4.2, 4.3, and 4.4 GHz. (b) Thermal power absorbed by the integrated thermopile with different input RF power.

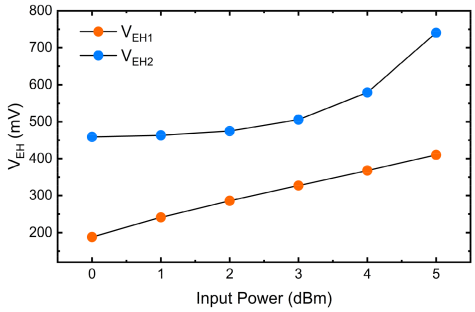



Fig. 16. Output voltage $V_{\mathrm{EH}}$ of the EH circuit with different input power.

### B. Performance of the Multisource Energy Harvester

The outputs of the energy harvesters and the multisource EH circuit are measured and discussed in this part. When a dc supply is imposed on the PA, there will be heat generated in the transistor channel, which can be absorbed by the integrated thermopile and converted to electrical energy. The outputs of the thermopile are measured at the frequencies of 4.2, 4.3, and 4.4 GHz with the same dc supply. The output voltage $V_{\mathrm{TH}}$ of the thermopile in relation to the input RF power is shown in Fig. 15(a). It indicates that the output of the thermopile is relatively noticeable, which means that the thermal energy can be successfully dissipated and collected by the integrated thermopile. It can also be seen that the dc output of the power sensor drops slightly when the input power of the amplifier increases. This can be explained by the analysis of power in (1). When the input RF power increases, output of the PA increases as well, which means more dc power is converted to the PA output power. And according to the law of conservation of energy, an increase in the dc power used for PA leads to the decrease of the thermal energy converted by it, and the power absorbed by the thermopile decreases, thus the output voltage decreases as well. Fig. 15(b) shows the thermal energy absorbed by the thermopile with different input RF power according to (5). It is consistent with the analysis that the increase of the input RF power results in the decrease the output of the integrated thermopile. This experimental phenomenon verifies that the thermopile sensor can sensitively detect the amount of the dissipated heat, thus enabling immediate health monitoring of the transistor.

Also, the dc output voltage $V_{\mathrm{TH}}$ of the thermopile will be stored in a capacitor and used as a bias voltage for the first stage of the EH circuit. Thus, it is essential to measure and analyze the performance of the thermopile that is treated as a micro-TEG. The internal resistance of the thermocouples is measured as 13.58 KΩ. And according to (8)–(11), when the input RF power is 0 dBm and the dc supply is 3.3 V, the temperature difference of the thermopile is 0.53 °C. And the measured VF and maximum PF of the thermopile are 22.87 V/cm$^2$K and 1.49 $\mu$W/cm$^2$K$^2$, respectively.

Meanwhile, the standing wave energy is converted to ac signals by a balun, which are also the ac inputs to the first level of the rectifier. As a result, the standing wave energy and the dissipated thermal energy are combined and collected. And the output dc voltage $V_{\mathrm{EH1}}$ is the first stage output of the EH circuit. The experimental results of $V_{\mathrm{EH1}}$ in different input RF power are shown in Fig. 16. When the input power is 0 dBm, the output voltage of the first stage is 188.332 mV, and the value of $V_{\mathrm{EH1}}$ increases with the increment of the input RF power.

TABLE IV
CHARACTERISTICS OF THE SOLAR CELL IN EXPERIMENT

| Area (cm$^2$) | $V_{OC}$ (V) | $I_{SC}$ (mA/cm$^2$) | $V_{max}$ (V) | $P_{max}$ (mW/cm$^2$) | Conversion Efficiency |
|---|---|---|---|---|---|
| 8.79×10$^{-4}$ | 0.191 | 3.183 | 0.11 | 0.183 | 1.5% |

* $V_{OC}$: Open-circuit output voltage; $I_{SC}$: Short-circuit current

The diode chain in the circuit is also connected to a capacitor that provides a dc bias for the second stage of the EH circuit. In the experiment, the diodes are tested as photodiodes. Since the chip is not packaged at this stage and is limited by the experimental environment, the chip is placed on the probe station and under a microscope light source for exposure with the exposure area as 370 cm$^2$ (diameter is 90 mm) and the power of 4.5 W. Therefore, the irradiance is calculated as 12 mW/cm$^2$. According to the experimental results, the maximum power density of the solar cell is 0.183 mW/cm$^2$, and the conversion efficiency is about 1.5% at this test condition. Table IV shows the tested performance of the diodes when acting as a solar cell. Similarly, when there is an electrostatic charge in the circuit, it will also be stored in the capacitor and added to the second stage of the EH circuit. The result of output voltage $V_{\mathrm{EH2}}$, i.e., the final output of the EH circuit, is also shown in Fig. 16. When the input power is 0 dBm, the final dc output voltage of the EH is 458.88 mV.

The experimental results illustrated in this part verify that the EH circuit has the capability to combine the standing wave energy, the dissipated thermal energy, light energy, and the electrostatic charge energy (if it occurs), and to convert these energies to a substantial dc output voltage, which could enable future powering of the system.

Compared with previous multisource EH circuits, this work achieves fully integration of the multisource energy harvesters, a self-health monitoring PA, and an energy combination circuit. Table V shows the comparison of this work with other multi-source EH circuits in terms of the output performance and energy

TABLE V
PERFORMANCE COMPARISON OF MULTISOURCE EH CIRCUITS

| Reference | Energy Sources | Converters | Application | Device Sizes | Output Performance | Combination Circuit |
|---|---|---|---|---|---|---|
| [15] | Indoor Light; Thermal | PVC; TEG | Indoor WSNs | PVC: 55 × 30 × 1 $mm^3$ TEG: 20 × 20 × 20 $mm^3$ | 621 $\mu$W@solar irradiance: 1010 lux and ΔT: 10K | Parallel HEH configuration |
| [16] | 2.4 GHz RF energy; Thermal | Antenna; TEG | Self-powered microsystems | Antenna: 55 × 11 $mm^2$ TEG: 20 × 20 $mm^2$ | 0.754 $\mu$W@-30 dBm | Single-diode based combiner |
| [17] | Vibration; Light; Thermal | PZT; PVC; TEG | Wearable devices | PVC: 52 × 10 × 0.3 $mm^2$ TEG: 30 × 1.5 $mm^2$ | PZT: 0.12 mW@1Hz; PVC:7.5 V@indoor TEG: 11 $\mu$W@30℃ | EMI-SECE interface circuit |
| [9] | Thermal; Light | PVC; TEG | WSNs | Chip surface: 0.32 $cm^2$ | TEG: 0.19 V/$cm^2$K PVC: 0.502 V@24.3℃ | -- |
| **This work** | Thermal; Light (Electrostatic charges); 4.3 GHz RF energy | TEG; PD; 3-port filter with a balun | Self-powered WSNs | Chip surface: 1.76 × 1.76 $mm^2$ | TEG: 22.87 V/$cm^2$K, 1.49 $\mu$W/$cm^2K^2$; PVC: 0.183 mW/$cm^2$ EH Open-circuit voltage: 458.88 mV@0 dBm | Cross-coupled rectifiers |

* PVC: Photovoltaic Cell; TEG: Thermoelectric Generator; PZT: Piezoelectric Transducer; PD: Photodiodes; HEH: Hybrid Energy Harvesting; EMI-SECE: extensible multi-input synchronous electronic charge extraction

combination circuits. With the size of the energy harvesters at only a micron scale, the output results of the energy harvesters are excellent, while the energy combining circuit also performs well.

## IV. CONCLUSION

In this article, an RF PA integrated with a self-health monitoring sensor and a multisource EH circuit is presented for the first time. A thermopile is integrated with a concave and convex-shaped power transistor, which can help dissipate heat and monitor health status of the power devices as well. The standing waves in the transmission line of the input port are directed to a specific port and collected by a three-port filter network. And a diode chain with a large area of PN junctions are designed to collect light energy and electrostatic charges. Moreover, the standing wave energy, dissipated heat energy, light energy, and electrostatic energy (if it occurs) are combined and harvested by a hybrid EH circuit based on the cross-coupled rectifiers to enable self-sustaining and self-powering of power electronics systems in the future.

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