# A Fast and Low-Cost Open-Circuit Fault Detection and Isolation Technique for Three-Phase Dual-Active-Bridge Converters Based on Finite State Machines

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***Abstract*—As one of popular high-power power interface topologies between the energy storage devices and the dc link, the three-phase dual-active-bridge (3Φ-DAB) dc–dc converter has received increasing attention. However, due to high number of semiconductor devices and multiple possible operation modes in the 3Φ-DAB converters, the reliability and healthy operation become increasingly challenging compared with traditional single-phase DAB converters. This study presents detailed waveform analyses for 3Φ-DAB converters under the normal and open-circuit faulty mode operation. Based on the analysis, a fast, cost-effective, reliable and sensor-less fault detection (FD) and fault isolation (FI) mechanism based on finite state machines for 3Φ-DAB converters is presented in this article. Specifically, switch node voltages between the primary and secondary bridges of 3Φ-DAB converters are adopted as the open-circuit fault (OCF) diagnostic signature and a low-cost OCF diagnostic circuit is utilized to perform the required signal processing. Using this technique, the open-circuit FD was achieved within 1/25th of the switching frequency and the open-circuit FI was performed within 1/6th of the switching frequency, which is the fastest FD and FI time for 3Φ-DAB converters reported so far. Experimental results were acquired from a built prototype under various OCF scenarios to validate the effectiveness of the proposed technique.**

***Index Terms*—Fault detection (FD), fault isolation (FI), three-phase dual-active-bridge (3Φ-DAB) converter.**

## NOMENCLATURE

| | |
|---|---|
| EV | Electric vehicle. |
| FD | Fault detection. |
| FI | Fault isolation. |
| FT | Fault tolerance. |
| DAB | Dual active bridge. |
| SST | Solid-state transformers. |
| 1Φ-DAB | Single-phase DAB. |
| SCF | Short circuit fault. |
| OCF | Open circuit fault. |
| 3Φ-DAB | Three-phase DAB. |
| SNV | Switch node voltage. |
| GDS | Gate driver signal. |
| R-DAB | Reconfigurable DAB. |
| PGA | Programmable gain amplifier. |
| *Other Symbols* | |
| $i_L$ | Inductor current. |
| $v_L$ | Inductor voltage. |
| $T_S$ | Switching cycle. |
| $V_{\text{DS}}$ | Drain to source voltage. |
| $V_{\text{MID}}$ | Mid-point to ground voltage. |
| $V_{\text{AUX}}$ | Auxiliary winding voltage. |
| $I_{\text{Tf-dc}}$ | Transformer phase current. |
| $i_{\text{dc-Phase}}$ | dc Component of phase current. |
| $V_C$ | Collector to ground voltage. |
| $I_{\text{LEAKAGE}}$ | Leakage inductor current. |
| $I_{C-\text{TAP}}$ | Center-tap current. |
| $+$ve | Positive. |
| $-$ve | Negative. |
| $N$ | Neutral. |

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## I. INTRODUCTION

DEVELOPMENT of cheap, compact, and more powerful electronics have ushered in a new era where electronic systems are at the heart of almost all types of critical equipment. Lifesaving medical equipment, surgical robots, automatic braking, and control systems of an EV, and nuclear power plants are some examples of these critical applications monitored and controlled by electronic systems. To ensure the high-availability factor of 99.999% for these critical applications [1], power converters, such as dc–dc converters between energy storage devices and the dc link, which are responsible for satisfying the power requirements of these applications and the components within these converters also need to achieve the same level

TABLE I
SYSTEMATIC COMPARISON AND ANALYSIS OF FAULT DIAGNOSIS SCHEMES FOR VARIOUS VARIANTS OF DAB CONVERTERS

| Ref. | DAB Topology | Fault Type | FD | FI | FT | Fault Sig. No. and type | Engineering Realization | Integration Complexity | Advantages | Limitations |
|---|---|---|---|---|---|---|---|---|---|---|
| [21] | 1Φ DAB | SW OCF | √ | X | √ | 2, SNV | No. Sim. result only | NA | -Fast detection speed | -No hardware results |
| [22] | 1Φ DAB | SW OCF Diode OCF | √ | √ | X | 8, $V_{DS}$ | Yes | High 8 detection circuits required | -Fast detection speed -SW OCF detection -Diode OCF detection | -High cost -High computational burden |
| [23] | 1Φ DAB | SW OCF Diode OCF | √ | √ | X | 4, $V_{MID}$ 1, $i_L$ | Yes | High 4 Voltage sen. required 1 Current sen. required | -Fast detection speed -SW OCF detection -Diode OCF detection | -High cost -High computational burden |
| [24] | 1Φ DAB | SW OCF | √ | √ | X | 1, $V_{AUX}$ 1, $i_L$ | Yes | High 1 Aux. winding required 1 Current sen. required | | -Slow detection speed -High cost |
| [25] | 3Φ-DAB | SW OCF | √ | √ | X | 3, Polarity of $I_{Tf-Dc}$ | No. Sim. result only | NA | | -No hardware prototype |
| [26] | 3Φ-DAB | SW OCF | √ | √ | √ | 3, $i_{dc-Phase}$ | No. Sim. result only | NA | | -No hardware results |
| [27] | 1Φ DAB with EPS | SW OCF | √ | √ | X | 4, $V_{MID}$ | Yes | High 4 Voltage sen. required | -Fast detection speed | -High cost |
| [28] | 3Φ-DAB | SW OCF | X | X | √ | 3, $i_{dc-Phase}$ | No. | High 3 current sen. required | | -High cost -Power reduced to half |
| [17] | 1Φ DAB with TPS | SW OCF | √ | √ | X | 4, $V_{MID}$ | Yes | High 4 Voltage sen. required | -Fast detection speed | -High cost |
| [8] | 1Φ DAB | SW OCF | √ | √ | X | 2, SNV | Yes | Low No sen. requirement | -Fast detection speed -Low cost | |
| [29] | 1Φ DAB | SW OCF SW SCF | √ | √ | √ | 8, $V_C$ | Yes | High 8 detection circuits required | -Fast detection speed -SCF and OCF detection | -High cost |
| [20] | 3Φ-DAB | SW OCF | X | X | √ | 3, $i_{LEAKAGE}$ | No | High 3 current sen. required | -Prevents transformer saturation | -No hardware results |
| [30] | 1Φ DAB | SW OCF | √ | √ | X | 2, $I_{C-TAP}$ | Yes | Low No sen. requirement | -Fast detection speed -Low cost | |
| [31] | 3Φ-DAB | SW OCF | √ | √ | X | 3, $i_{dc-Phase}$ | Yes | High 3 current sen. required | - Low cost current sen. | -Slow detection speed |
| [32] | 3Φ-DAB | SW OCF | √ | √ | X | 3, $i_{dc-Phase}$ | Yes | High 3 current sen. required | - Low cost current sen. | -Slow detection speed |

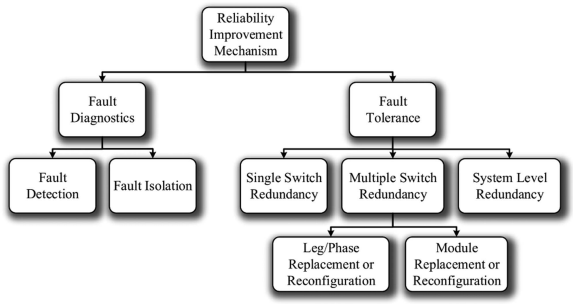


Fig. 1. Reliability improvement mechanism, including fault diagnostics and FT.

of availability. A thorough survey on the reliability of power converters has pointed out that semiconductors power electronic components are the primary cause of converter failure resulting in converter shut down and loss of service [2].

The industry and the academic community prefer dual active bridge (DAB) converters [3] for bidirectional power flow applications, such as vehicle-to-grid and vehicle-to-building charging. Apart from this, DAB converters make the central components of multilevel converters often utilized in power electronic or SST. The DAB converter is a high-performance converter due to its characteristics of galvanic isolation, high-power density [4], inherent zero voltage switching [5], [6], and bidirectional power transfer. Especially for three-phase dual-active-bridge (3Φ-DAB) converters, due to high number of semiconductor devices and multiple possible operation modes in the 3Φ-DAB converters, the reliability and healthy operation become increasingly challenging compared with traditional single-phase DAB (1Φ-DAB) converters.

High number of power switches within 3Φ-DAB converters increases the risk of failure due to short circuit faults (SCF) and open circuit faults (OCF). SCF detection and protection schemes are much more developed and often are a standard part of the gate driver circuit, such as the HCPL316. OCF occurs due to the lifting of the bond wire during thermal cycling, driver failure, or a SCF-induced failure. Its detection and remedial actions have not been given much thought because of their less severe impacts. Unlike SCF, the converter circuit can still operate abnormally under OCF in a steady state. Nevertheless, an OCF will still cause asymmetries in inductor current ($i_L$), switch node voltage (SNV), and inductor voltage ($v_L$), which results in current overshoot, capacitor voltage unbalance, and saturation of magnetic components in the DAB converter. These asymmetries stress the power components, which affect the reliability and safety of the DAB converter under long-term operation [7].

Reliability improvement mechanism within power converters usually consists of fault detection (FD), fault isolation (FI), and fault tolerance (FT) [8]. FD is the initial step of this mechanism, which detects the presence and time of the fault without pinpointing the exact fault location and type. This step then triggers the FI sequence, which identifies the precise location and type of the fault. In other words, FD and FI are the means for initial fault diagnostics [9], [10]. Once the accurate location and type of fault are determined, FT is employed to overcome the power converter failure by isolating the faulty component [11], [12], leg/phase [13], [14], [15], or entire module [16]. These faulty entities are either reconfigured or replaced with a redundant counterpart to avoid complete system failure, as illustrated in Fig. 1.

FT mechanisms for various versions of DAB converters, including the 1Φ-DAB [7], [17], 2/3 level DAB [18], the reconfigurable DAB (R-DAB) [19], and 3Φ-DAB converters [20] has been proposed. Moreover, a fair share of the prior art has also discussed the analyses of the OCF conditions and their diagnosis

in these DAB converters. Table I gives a comprehensive review about main characteristics of these FD and FI schemes for DAB converters with different variants, including FI speed, FD signatures, and the implementation cost due to added sensors.

Regarding FD and FI schemes in 1Φ-DAB converters, as listed in Table I, Ribeiro et al. [21] used two voltage sensors to measure SNV. After calculating the average value of SNV, the proposed mechanism detected the presence of switch OCF within one switching cycle ($T_S$). However, it only reported the simulation results and proposed no methodology for FI at the component level. Drain-to-source voltage ($V_{\text{DS}}$) is another FD signature for swift detection of switch OCF in 1Φ-DAB converters. In [22], the $V_{\text{DS}}$ changes were used to detect the switch and diode OCF and further isolate the power switch OCF from the diode OCF. However, an individual detection circuit requirement for each power switch inflates the total cost and increases the computational burden. Airabella et al. [23] calculated an estimated midpoint to ground voltage ($V_{\text{MID}}$) and compares it with the actual measured values acquired using four voltage sensors for FD and FI in the 1Φ-DAB converter. However, a hardware realization of the proposed FD and FI mechanism was not presented. Xie and Ge[24] utilized an additional auxiliary winding installed within the 1Φ-DAB transformer primary to measure the inductor voltage and carry out FD in $3T_S$. The polarity of dc components of the 3Φ-DAB transformer phase and magnetization current was utilized for FD and FI at the component level in [25]. However, only the simulation results were provided to validate the viability of this scheme. In [26], using simulation results, OCF in 3Φ-DAB converters was detected at the phase level by comparing the dc component of the phase currents. FT was achieved by shedding the faulty phase and allowing the converter to operate as a 1Φ-DAB converter. The difference between the mean value of the midpoint voltage and their average value calculated using four voltage sensors under normal conditions was used to detect and isolate switch OCF within one $T_S$ for a 1Φ-DAB converter operating under extended phase shift [27], and triple phase shift [17]. In [28], an FT scheme was proposed for a 3Φ current-fed DAB converter by deactivating the faulty phase within the faulty bridge and the corresponding phase in the nonfaulty bridge. Again, no information was reported on how to detect and isolate the OCF. Deviation in the SNV of 1Φ-DAB converters was effectively utilized to detect and isolate the single-switch and multiple-switch OCF within one $T_S$ in [8]. The mechanism used a simple diagnostic circuit to extract and process the fault signature without a sensor. In [29], an FT technique was proposed for SCF and OCF in power switches of 1Φ-DAB converter. The desaturation detection technique measured the collector voltage of the power switch and compared it with the gate driver signals (GDS) using logic gates. This method needs around 5 $\mu$s to detect the SCF and OCF. The proposed technique, however, requires eight logic circuits, one for each power switch for complete fault diagnostics.

Compared with the 1Φ-DAB converter, the 3Φ-DAB converter requires much smaller filter capacitors due to reduced voltage and current ripples resulting in smaller volume and weight [33]. In addition, it has the potential to realize the highest power densities due to lower filter ratings compared with its single-phase counterpart. However, with a higher switch count, the 3Φ-DAB converter is more prone to switch OCF, and isolating the exact switch fault becomes more challenging. The fault diagnostic signature must be selected to detect and isolate the fault in multiple switch locations. In the case of the 1Φ-DAB converter, a single fault diagnostic signature can be used to detect and pinpoint the switch OCF fault accurately. However, in the case of 3Φ SNV, at least three fault diagnostic signatures are required to pinpoint the fault location. This inflicts a higher financial burden and requires more processing resources to handle all the fault diagnostic signatures, which is one of the reasons the 3Φ-DAB converter has not seen much work in terms of fault diagnostics. Regarding the FD and FI techniques for the 3Φ-DAB converter, Le et al. [20] proposed an FT scheme by switching off the faulty phase of the converter and limiting the 3Φ-DAB to a 1Φ DAB converter. This research, however, did not explain the OCF detection and isolation steps. Without using any current or voltage sensor, Khan et al. [30] used the center-tap current in the modified 1Φ R-DAB converter to detect the presence of single-switch and multiple-switch OCF within 2 $\mu$s. Another effort was put forth in [31], where an FD and FI technique was presented for semiconductor OCF in 3Φ-DAB converters. The dc bias pattern of the primary phase current was obtained for all the transistor failures and was used for FD and FI in all the twelve switches in the primary and secondary bridges. The FD time, however, ranges from $7T_S$ to $10T_S$, which imposes a downside on this FD and FI technique regarding detection speed. Utilizing the same fault signature as in [31], Rastogi et al. [32] have represented the dc current bias pattern of the 3Φ-DAB converter through a single vector averaged over one switching cycle. Using this vector, they successfully detected and isolated the OCF in primary and secondary bridge within three to four switching cycles.

Albeit the research on developing more efficient FT 3Φ-DAB converters has intensified, as given in Table I, the FD and FI schemes for 3Φ-DAB converters have not been extensively studied. In most FT strategies for 3Φ-DAB converters highlighted in blue in Table I, a clear methodology to detect and isolate the switch OCF has not been established. Moreover, an explanation regarding how to implement the suggested methodology or concept in terms of a real working hardware prototype or how to realize the corresponding idea in terms of an industrial solution has not been discussed. In this article, engineering practicality evaluates the potential of a proposed scheme or idea in terms of an industrial or marketable solution. Most of the proposed FD and FI techniques are backed by the simulation analysis, and no hardware prototype or hardware results for that matter, are presented. In addition, the 3Φ-DAB converters fault diagnostic schemes in service are slow and not very cost-effective due to the requirement of extra sensors to detect fault signatures. It points to the fact that more serious work on developing novel FD and FI techniques is required that could be used alongside the already developed FT techniques. Since fault diagnostics are offered more as an additional service than a product, it must impose less or no financial burden by avoiding extra sensors and additional computational resources. Table I categorizes the cost-effectiveness of the fault diagnostic scheme based on the

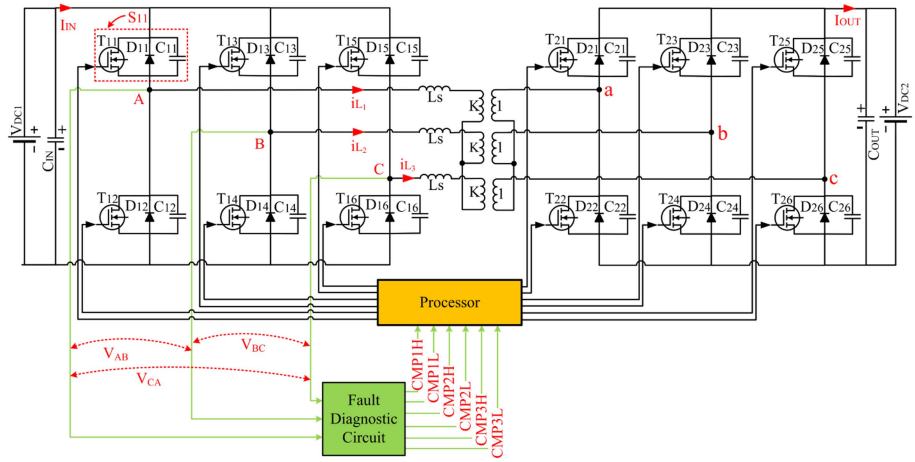


Fig. 2. 3Φ-DAB converters with a 3Φ Y–Y transformer configuration. The processor provides GDS to the corresponding switches. SNV $V_{AB}$, $V_{BC}$, and $V_{CA}$ are extracted from points A–C and fed to the fault diagnostic circuit. The fault diagnostic circuit converts the three duo-binary SNVs into six binary signals, with each duo-binary SNV represented as CMPXH: CMPXL. The processor uses these binary signals to detect and isolate switch OCF.

usage of extra voltage and current sensors or modification in the design elements, such as core size. Any scheme using two or more sensors is considered as high cost. Similarly, any scheme suggesting changes in the design element is also added to this category. Although all of the FD schemes are able to detect and isolate faults before any damage to the main converter, still the detection speed is relatively categorized as slow and fast because it is imperative to detect and isolates the fault in the minimum possible time to stop the seepage of OCF effects to the rest of the converter, after which the damages due to the fault are irrevocable. Any detection mechanism that detects and isolate a fault within one switching cycle is labeled as fast. Otherwise, they are categorized as slow. In addition, the ideal diagnostic scheme must be able to integrate into the already deployed system with minimum or no modifications, which refers to the integration complexity. If the fault diagnostic scheme is able to integrate with the main converter design and requires no modifications, it will be more cost-effective and will have less integration complexity.

All these issues have not been adequately addressed till now, and therefore, it would be highly beneficial to address the lack of research on the FD and FI schemes for 3Φ-DAB converters. The current mechanism, therefore, proposes effective FD and FI techniques using switch SNV that can be integrated with any FT technique to create more robust, fast, cost-effective FT 3Φ-DAB converters. To reach this goal, detailed waveform analyses for 3Φ-DAB converters under the normal and open-circuit faulty mode operation are presented in this article. Based on the analysis, a fast, cost-effective, reliable, and sensor-less FD and FI mechanism based on finite state machines for 3Φ-DAB converters is presented. Specifically, SNV between the primary and secondary bridges of 3Φ-DAB converters are adopted as the OCF diagnostic signature and a low-cost OCF diagnostic circuit is utilized to perform the required signal processing.

The rest of this article is organized as follows. Section II describes the regular operation of a 3Φ-DAB converter. Section III gives the analysis of the 3Φ-DAB converter under OCF. Section IV describes the proposed fault diagnostic mechanism. Section V lays out the hardware realization procedures and experimental results on switch OCFs. Finally, Section VI concludes this article.

## II. 3Φ-DAB Under Normal Operation

The 3Φ-DAB converter illustrated in Fig. 2 consists of a primary and secondary bridge. A combination of a 3Φ Y-Y transformer configuration and a leakage inductor configuration provides galvanic isolation and leakage inductance requirements for rated power transfer at a specified operating frequency. The processor generates the GDS for every switch $(S_{XX})$, and each switch can be represented as a combination of three components, namely, the MOSFET $(T_{XX})$, diode $(D_{XX})$, and the parasitic capacitance $(C_{XX})$ illustrated in Fig. 2 for switch $S_{11}$. The main processor generates the GDS at the required moment and provides a phase shift between the primary and secondary bridge to deliver the required power at the output. Switches in each leg operate in active high complementary mode, and each leg in the primary and secondary bridge lags its predecessor leg by 120°. So leg2 lags the leg1 by 120°, leg3 lags the leg2 by 120°, and leg1 by 240°. The GDS for the secondary side is phase shifted from the primary side to transfer the required power from the primary to the secondary side. For opposite power flow, i.e., from the secondary side to the primary side, a negative phase shift is applied, in which the secondary side leads the primary side.

Points A–C are the three switching nodes on the primary side, whereas a–c are the three switching nodes on the secondary side. The differential voltage between the adjacent switching nodes is called the differential SNV. $V_{AB}$ is the differential voltage on point A with respect to point B. $V_{BC}$ is the differential voltage on point B with respect to point C and $V_{CA}$ is the differential voltage on point C with respect to point A. Similar voltages can be obtained on the secondary side between points a, b, and c and are termed $V_{ab}$, $V_{bc}$, and $V_{ca}$. These voltages

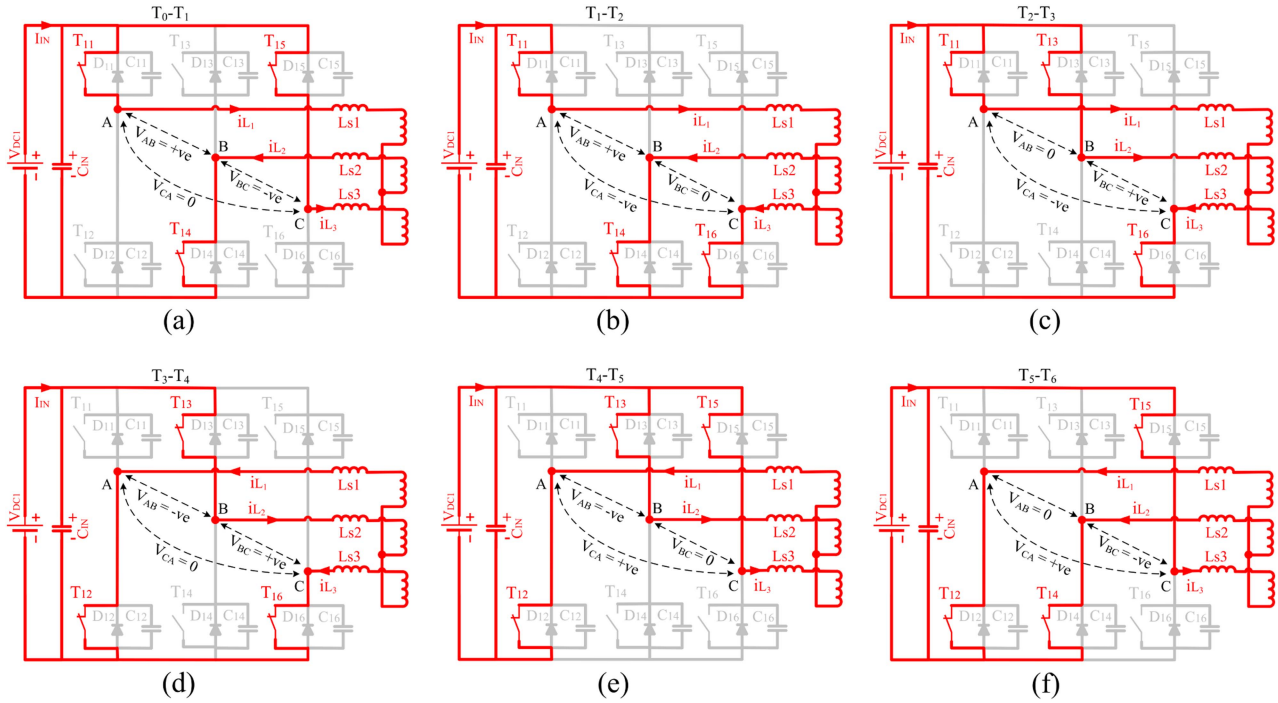


Fig. 3. Detailed analysis of the primary bridge of 3Φ-DAB converter under normal operating conditions. One $T_S$ is divided into six subintervals. SNV and $i_L$ during each subinterval are illustrated. The current path and active components are also highlighted in red. (a) Subinterval $T_0 - T_1$. (b) Subinterval $T_1 - T_2$. (c) Subinterval $T_2 - T_3$. (d) Subinterval $T_3 - T_4$. (e) Subinterval $T_4 - T_5$. (f) Subinterval $T_5 - T_6$.

are duo-binary voltages with levels shifting between positive (+ve), negative (−ve), and neutral (N) depending upon the switching sequences of the semiconductor switches. Fig. 3 gives a detailed analysis of the primary side of the 3Φ-DAB converter during normal operation. To help understand the behavior of the SNV during normal operation, one $T_S$ is divided into six subintervals. The SNV during each subinterval changes due to the activation/deactivation of the GDS of the power switches. Fig. 4 illustrates the GDS for the primary side of the 3Φ-DAB converter, which includes $S_{11}$–$S_{16}$. It also gives the differential SNV on the primary side of the 3Φ-DAB converter.

A detailed analysis of the workings of the primary side of the 3Φ-DAB converter is given below by explaining the transition of SNV conditions and $i_L$ during these subintervals.

*1) Subinterval $T_0$–$T_1$:* During this subinterval, illustrated in Fig 3(a), the GDS for $S_{11}$, $S_{14}$, and $S_{15}$ is active. The inductor current through $L_{s1}$ is given as $i_{L1} = i_{L2} - i_{L3}$ whereas the SNV $V_{AB}$ is +ve, $V_{BC}$ is −ve, and $V_{CA}$ is N. This subinterval ends with the activation of GDS for $S_{16}$ and deactivation of the same for $S_{15}$.

*2) Subinterval $T_1$–$T_2$:* During this subinterval, the GDS for $S_{11}$, $S_{14}$, and $S_{16}$ is active. The inductor current is given as $i_{L1} = i_{L2} + i_{L3}$ whereas the SNV $V_{AB}$ is +ve, $V_{BC}$ is N, and $V_{CA}$ −ve. Fig. 3(b) illustrates the active components and the inductor current active path for this subinterval.

*3) Subinterval $T_2$–$T_3$:* This subinterval begins with the activation of the GDS for $S_{13}$, and deactivation of the same for $S_{14}$. During $T_2$–$T_3$, GDS for $S_{11}$, $S_{13}$, and $S_{16}$ is active. The inductor current is given as $i_{L1} = i_{L3} - i_{L2}$, whereas the SNV $V_{AB}$ is N, $V_{BC}$ is +ve, and $V_{CA}$ is −ve. Fig. 3(c) represents the working conditions of this subinterval.

*4) Subinterval $T_3$–$T_4$:* During this subinterval, the GDS for $S_{12}$, $S_{13}$, and $S_{16}$ is active. The inductor current is $i_{L1} = i_{L2} - i_{L3}$ whereas the SNV $V_{AB}$ is −ve, $V_{BC}$ is +ve, and $V_{CA}$ is N. Fig. 3(d) illustrates the active components and the inductor current active path for this subinterval.

*5) Subinterval $T_4$–$T_5$:* During this subinterval, illustrated in Fig 3(e), the GDS for $S_{12}$, $S_{13}$, and $S_{15}$ is active. The inductor current for $L_{s1}$ is given as $i_{L1} = i_{L2} + i_{L3}$ whereas the SNV $V_{AB}$ is −ve, $V_{BC}$ is N, and $V_{CA}$ is +ve. This subinterval concludes with the activation of GDS for $S_{14}$ and deactivation of the same for $S_{13}$.

*6) Subinterval $T_5$–$T_6$:* During this subinterval, the GDS for $S_{12}$, $S_{14}$, and $S_{15}$ is active. The inductor current is $i_{L1} = i_{L3} - i_{L2}$, whereas the SNV $V_{AB}$ is N, $V_{BC}$ is −ve, and $V_{CA}$ is +ve. Fig. 3(f) illustrates the active components and the inductor current active path for this subinterval. It can be observed that at a single instant and under correct operating conditions, the three SNVs can never share the same voltage level in a certain state. If represented in this particular order and under correct operating conditions, these values for $V_{AB}$, $V_{BC}$, and $V_{CA}$ repeat after one $T_S$. Subintervals $T_0$–$T_6$ represents one complete $T_S$. A $T_S$ is divided into six subintervals, and during each subinterval or state, the three SNVs never exhibit the same voltage level. From Fig. 4 we can see that during $T_0$–$T_1$, $V_{AB}$ is +ve, $V_{BC}$ is −-ve, whereas $V_{CA}$ is N. After $T_1$, $V_{AB}$ is still +ve, $V_{BC}$ becomes N and $V_{CA}$ become −ve. Since the operational sequence of the 3Φ-DAB converter repeats itself after every $T_S$, it can be

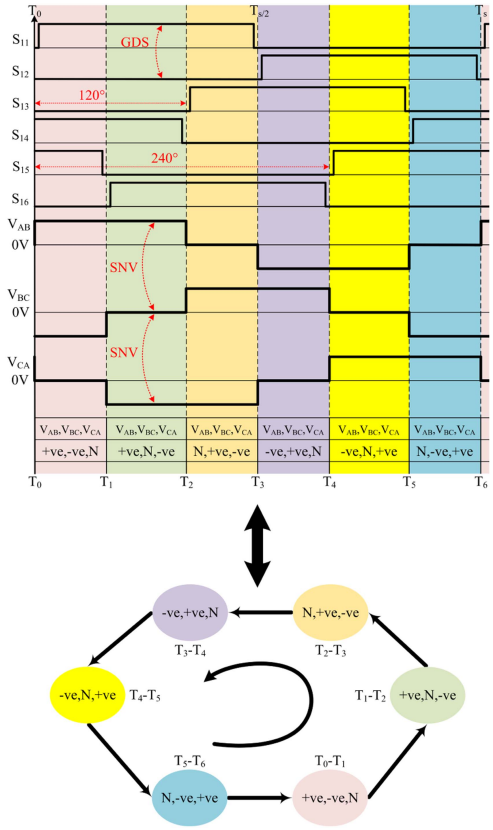


Fig. 4. GDS for all switches on the primary side of the 3Φ-DAB converter. SNV $V_{AB}$, $V_{BC}$, and $V_{CA}$ extracted from points A–C are duo-binary signals with values changing between +ve, -ve, and neutral. The sequence of SNV repeats itself after one $T_S$ and can be represented as a state diagram that follows a specific sequence and repeats itself after $T_S$.

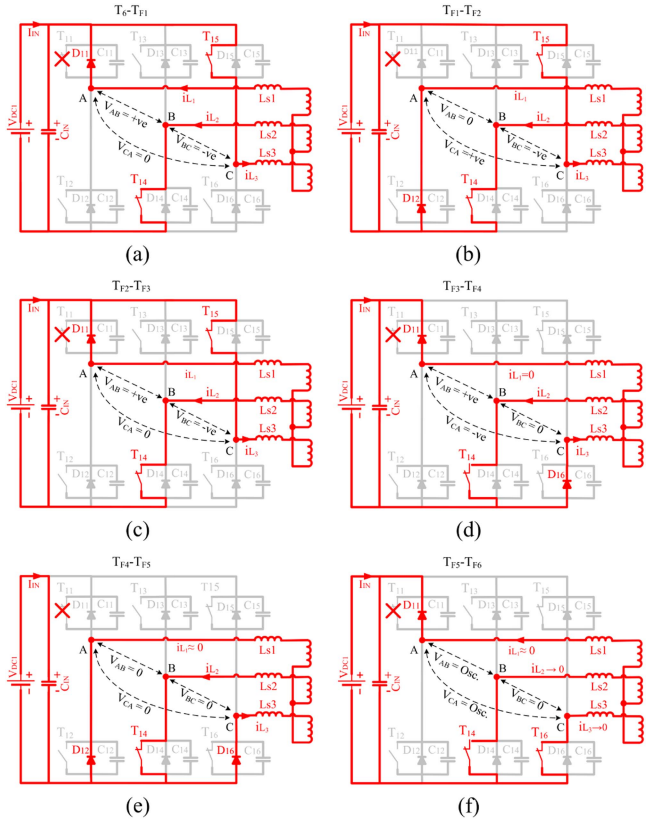


Fig. 5. Mode analysis of the primary side of the 3Φ-DAB converter under $S_{11}$ OCF. $i_L$ and SNV during each state are detailed with the current path and the active components illustrated in red. Analysis of only six subintervals relevant to the fault diagnostic mechanism is presented from $T_6$ to $T_{F6}$. (a) Subinterval $T_6$–$T_{F1}$. (b) Subinterval $T_{F1}$–$T_{F2}$. (c) Subinterval $T_{F2}$–$T_{F3}$. (d) Subinterval $T_{F3}$–$T_{F4}$. (e) Subinterval $T_{F4}$–$T_{F5}$. (f) Subinterval $T_{F5}$–$T_{F6}$.

represented using a state diagram as illustrated at the bottom of Fig. 4. Every state in this state diagram represents a subinterval in one $T_S$. This state diagram represents the working of a 3Φ-DAB converter under normal operating conditions.

## III. 3Φ-DAB Under OCF

The OCF condition of a converter is defined as when one or more than one of its semiconductor switches experiences a fault either due to the lifting of the bond wire during thermal cycling or due to the failure of the gate driver circuitry [34]. Complete analysis of the primary side of the 3Φ-DAB converter in terms of inductor currents and the 3Φ SNV is necessary, especially during OCF conditions. What follows is a mode analysis for the primary side of the 3Φ-DAB converter under $S_{11}$ OCF. Due to space limitations, an analysis of the case 1 of $S_{11}$ OCF is discussed. Analysis for all the other cases of $S_{11}$ OCF follows the same logical explanation.

### A. Mode Analysis of 3Φ-DAB Converter Under $S_{11}$ Fault

During the normal operation of the 3Φ-DAB converter, the three duo-binary SNVs behave in a predefined sequence. However, under OCF conditions, the SNVs deviate from this sequence. Complete mode analysis of the primary bridge of the 3Φ-DAB converter under $S_{11}$ OCF is given in Fig. 5, whereas Fig. 6 illustrates the behavior of the 3Φ SNV and the inductor currents during OCF. From Fig. 6, it can be observed that $S_{11}$ switch is active during $T_0$–$T_1$, $T_1$–$T_2$, and $T_2$–$T_3$. For the rest of the three subintervals from $T_3$–$T_6$, the $S_{11}$ is inactive and $S_{11}$ OCF effects on the SNV and inductor currents cannot be observed. Therefore, there are three different cases for $S_{11}$ OCF, or $S_{11}$ OCF can affect the outcome of the SNVs in three different ways. They are classified as cases 1–3, depending upon the position of occurrence of the $S_{11}$ OCF. Fault mode analysis of case 1 will be made here, and the remaining two cases follow the same logical explanation. However, a state flow diagram including all cases of $S_{11}$ OCF is provided in Fig. 7, illustrating the complete sequence of the flow of the state machine for $S_{11}$ OCF.

The following section gives a detailed analysis of the $S_{11}$ OCF for case1 by explaining the transition of SNV condition during various fault subintervals.

*1) Subinterval $T_6$–$T_{F1}$:* To simulate $S_{11}$ OCF for case1, the GDS of the $S_{11}$ is ceased during the subinterval $T_5$–$T_6$. The SNV during this subinterval are N,-ve, and +ve for $V_{AB}$, $V_{BC}$, and $V_{CA}$, respectively. The capacitors $C_{11}$ and $C_{12}$ are charged and discharged to $V_{dc1}$ and 0 V, respectively. As the converter enters the next state represented by the subinterval $T_6$–$T_{F1}$, only

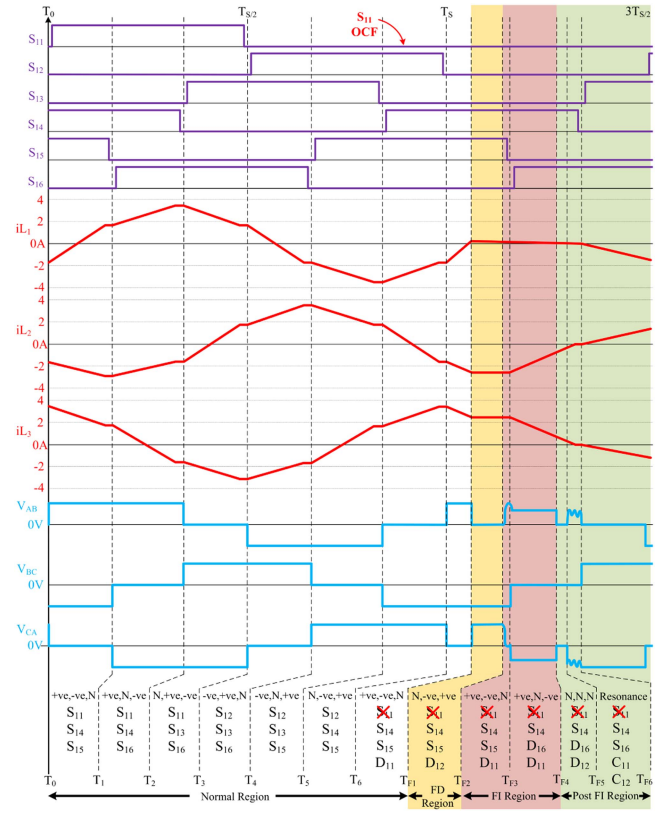


Fig. 6. Complete analysis of inductor currents $i_{L1}$, $i_{L2}$, and $i_{L3}$ and SNVs $V_{AB}$, $V_{BC}$, and $V_{CA}$ under $S_{11}$ OCF. GDS for $S_{11}$ switch is deactivated during subinterval $T_5$–$T_6$. The corresponding changes in the inductor currents and the SNVs are illustrated with the list of active components at the bottom.

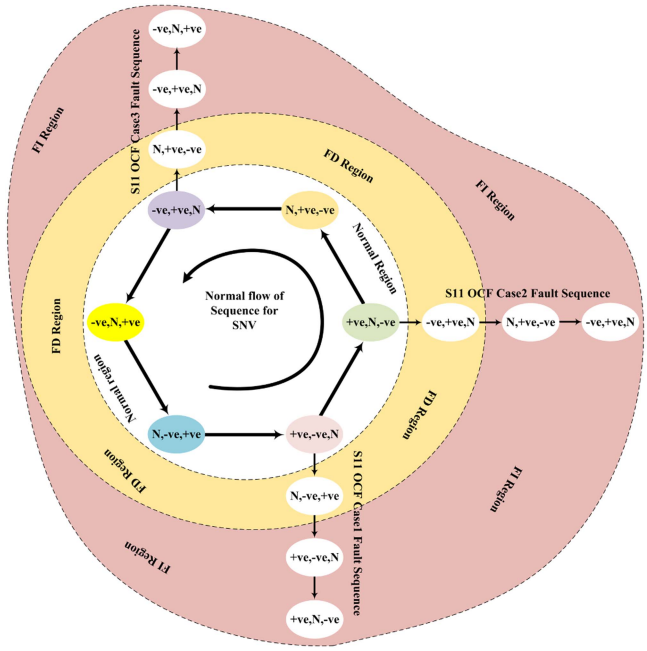


Fig. 7. Sequence of flow of state machine under $S_{11}$ OCF conditions for YY and $\Delta\Delta$ configuration. There are three cases for $S_{11}$ OCF, depending upon the occurrence of the fault at a specific location. The clear area illustrates SNVs under normal operation. Under OCF, the flow of sequence transfers from the normal region to the FD region. For $S_{11}$ OCF, there are three sequences in the normal region from where the flow of the state machine can transition from the normal region to the FD region. Identification of the fault location is carried out in the FI region.

the GDS for $S_{14}$ and $S_{15}$ are activated, while the GDS for $S_{11}$ is inhibited to simulate the $S_{11}$ OCF. Equation (1) is utilized to calculate the inductor current $i_{L1}$ at this point [35]

$$i_{L1(0)} = \begin{cases} \dfrac{nV_{\text{dc2}} - V_{\text{dc1}}2\pi - 3nV_{\text{dc2}}\varphi}{9\omega L_S} \; \forall 0 < \varphi < \dfrac{\pi}{3}. \end{cases} \quad (1)$$

This subinterval ends when the inductor current $i_{L1}$ becomes zero and the state of the 3Φ SNV changes to N,-ve, and +ve for $V_{AB}$, $V_{BC}$, and $V_{CA}$, respectively, which is different from the normal transition of the current state to the next state. Time taken by the current to become zero and cause a change in the SNV is given by $\Delta$t

$$\Delta t = \frac{(L_S \times \Delta i)}{V_{LS}}. \quad (2)$$

*2) Subinterval $T_{F1}$–$T_{F2}$:* During $T_{F1}$–$T_{F2}$, the capacitor $C_{12}$ is discharged to zero, forcing the diode $D_{12}$ to commutate. This scenario changes the state of the SNV to N,-ve, and +ve for $V_{AB}$, $V_{BC}$, and $V_{CA}$, respectively, which is different from the normal transition of the current state to the next state. The next state during the normal transition of the state diagram is +ve, N, and $-$ve for $V_{AB}$, $V_{BC}$, and $V_{CA}$, respectively. This anomaly in the transition sequence of the state diagram is effectively used to detect the fault. In response, an FD signal is asserted to indicate the fault's presence, and the same impulse is used to initiate the FI mechanism.

*3) Subinterval $T_{F2}$–$T_{F3}$:* During this subinterval, a resonant circuit between the capacitors $C_{11}$, $C_{12}$, and the inductor $L_{S1}$ forces the $D_{11}$ to commutate and $D_{12}$ to stop. This change the states of the SNV to +ve, $-$ve, and N for $V_{AB}$, $V_{BC}$, and $V_{CA}$, making it the first step in the FI mechanism. This subinterval ends when the GDS for $S_{15}$ is deactivated, and the same for $S_{16}$ is activated as per the normal switching sequence of the primary bridge.

*4) Subinterval $T_{F3}$–$T_{F4}$:* At the beginning of this subinterval, GDS for $S_{16}$ is activated and the same is deactivation for $S_{15}$. The current direction $i_{L3}$ forces $D_{16}$ to commutate and it changes the states of the SNV to +ve, N, and $-$ve for $V_{AB}$, $V_{BC}$, and $V_{CA}$, making it the second and the final step in the FI mechanism.

*5) Subinterval $T_{F4}$–$T_{F5}$:* During this subinterval, a resonant circuit develops between the parasitic capacitors $C_{11}$ and equivalent leakage inductors constituting $Ls1$, $Ls2$, and $Ls3$. This forces the diode $D_{12}$ to commutate and the 3Φ SNV $V_{AB}$, $V_{BC}$, and $V_{CA}$ become zero. The resonance frequency is given by the following:

$$\omega_{\text{res}} = \frac{1}{\sqrt{C_{\text{Paracitic}} \times L_{\text{eq}}}} \quad (3)$$

where $C_{\text{Paracitic}}$ is the MOSFET parasitic capacitance and $L_{\text{eq}}$ is the equivalent leakage inductance.

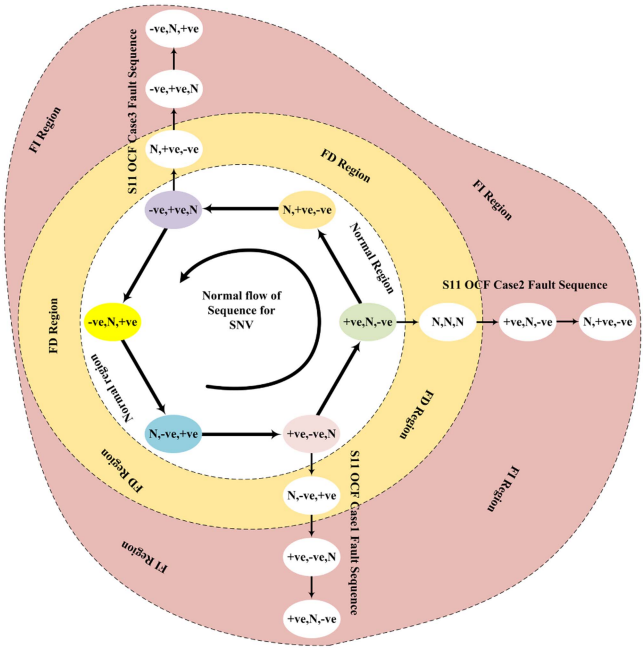


Fig. 8. Sequence of flow of state machine under $S_{11}$ OCF conditions for Y$\Delta$ configuration. There are three cases for $S_{11}$ OCF, depending upon the occurrence of the fault at a specific location. The clear area illustrates SNVs under normal operation. Under OCF, the flow of sequence transfers from the normal region to the FD region. For $S_{11}$ OCF, there are three sequences in the normal region from where the flow of the state machine can transition from the normal region to the FD region. Identification of the fault location is carried out in the FI region.

*6) Subinterval $T_{F5}$–$T_{F6}$:* The resonant circuit developed during the previous subinterval continues to operate during this subinterval, causing the SNV $V_{AB}$ and $V_{CA}$ to oscillate. During these oscillations, the inductor current in all three phases becomes zero. This subinterval continues until the deactivation of GDS for $S_{14}$ and activation of GDS for $S_{13}$.

The exact sequence of the SNVs for all three $S_{11}$ OCF cases can be ascertained using a similar analysis, and a transition sequence from the normal to the faulty condition can be established. The state diagram in Fig. 7 illustrates all the cases of transition sequences of 3$\Phi$ SNV due to $S_{11}$ OCF from the normal operation to the FD and then the FI stage for YY and $\Delta\Delta$ configuration, whereas the state diagram in Fig. 8 illustrates the same for Y$\Delta$ configuration. This difference in state diagram is because of the change in the behavior of the inductor currents, which occurs because of changes in the transformer turns ratios for Y$\Delta$ configuration to achieve the same power output at the designated leakage inductance $L_S$ [35]. It does not cause any change in the normal operating sequence of 3$\Phi$ SNV for all three winding configurations. However, under fault conditions, the 3$\Phi$ SNV operating sequence changes its behavior for Y$\Delta$ configuration because the 3$\Phi$ SNV are driven based on the inductor currents during the resonance period under fault conditions. Therefore, the behavior of the 3$\Phi$ SNV for Y$\Delta$ configurations is different from the YY and $\Delta\Delta$ under fault, and the same is reflected with in the state diagram.

The inner circle represents the states of SNV during the normal operation of the converter. However, in the case of OCF, the state machine initially transitions from the normal region to the FD region represented by subinterval $T_{F1}$–$T_{F2}$ in Figs. 5 and 6. All the states in this region are FD states and are the initial stage of the fault diagnostic procedure during, which the presence of the fault is detected. It also changes the status of the state machine from the normal state to the FD state. However, the actual location of the fault is unknown. The exact location of the fault is identified within the FI region and is represented by the subinterval $T_{F2}$–$T_{F3}$ and $T_{F3}$–$T_{F4}$ in Figs. 5 and 6, and also illustrated in Fig. 7.

A complete state diagram for all the switches fault cases in the primary bridge illustrating the transition of the state machine flow from the normal to the faulty condition is given in Fig. 9.

## IV. Proposed FD and FI Algorithm for 3$\Phi$-DAB Converters

The following assumptions have been made to ease the understanding of the proposed technique.

1) FD and FI analyses have been made for the 3$\Phi$-DAB converter operating only in the forward operating mode. The same analysis is valid for reverse power flow direction.
2) OCF is introduced by ceasing the GDS; for example, to simulate the $S_{11}$ OCF, GDS for the $S_{11}$ switch is ceased.
3) The antiparallel diode and the parasitic capacitor work normally under the switch OCF condition.

OCF in the 3$\Phi$-DAB converter causes asymmetries in $i_L$, SNV, and inductor voltages, resulting in current overshoot, capacitor voltage unbalance, and saturation of magnetic components. This stresses the power components, affecting the DAB converter's reliability under long-term operation. Therefore, a cost-effective, fast, and robust fault diagnostic strategy is required for switch OCF detection in the 3$\Phi$-DAB converter. The SNV, as a fault diagnostic signature, can provide excellent FD and FI characteristics. The behavior of 3$\Phi$ differential SNV can be effectively utilized for fault diagnostics. The state diagram in Fig. 9 illustrates all the possible sequences of transitions of the primary side SNVs during normal and OCF conditions. A finite state machine is implemented in the main processor to detect the sequence of transitions in accordance with the state diagram illustrated in Fig. 9. All the possible cases of normal and OCF transition sequences are added to the state machine. Therefore, with the current state known, the state machine knows all the possible following states of 3$\Phi$-DAB SNV under normal and OCF conditions. The regular operation of the 3$\Phi$-DAB converter includes only six states, which repeat in a specific order. For example, in Fig. 9 considers that the state machine is in the normal region with the state of 3$\Phi$ SNV, $V_{AB}$, $V_{BC}$, and $V_{CA}$ represented by +ve, $-$ve, and N, respectively. The current value of the state machine becomes +ve, $-$ve, and N. According to the state diagram, there could be three possible next states. If the state machine transitions to +ve, N, and $-$ve, the converter remains in the normal region. However, if the state machine transitions to either N, N, and N, or N, $-$ve, and +ve, then it means that the converter has encountered an OCF fault and has transitioned to the FD region. If the current state of the converter is N, N, and N in the FD region, then there could be only one

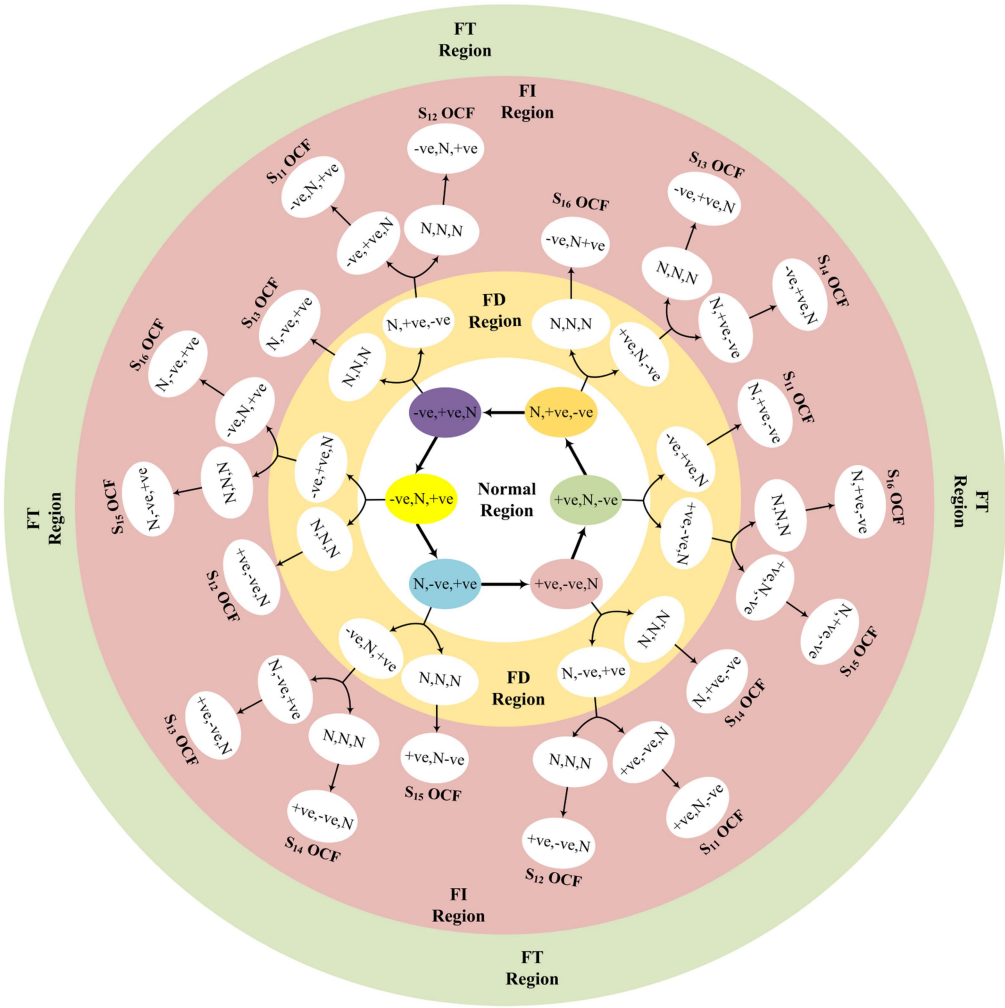


Fig. 9. Final state machine which represents transition sequences of the SNV during the normal and OCF conditions of all the switches on the primary side of the 3Φ-DAB converter.

outcome as $S_{14}$ OCF. This is confirmed by the state machine transition to N, +ve, and −ve, during the FI state. Alternatively, if the state machine transitions from +ve, −ve, and N in the normal region to N, −ve, and +ve in the FD region, then there could be two possible OCF conditions. If the state of the SNV changes to N, N, and N, then the state machine's current state becomes N, N, and N indicating the presence of $S_{12}$ OCF in the initial FI stage. $S_{12}$ OCF is confirmed in the second FI stage when the state machine transitions to +ve, −ve, and N from its current state. Alternatively, if the state of the SNV changes from N, −ve, and +ve in the FD stage to +ve, −ve, and N, the state machine enters the initial FI stage indicating the presence of $S_{11}$ OCF. The $S_{11}$ OCF is confirmed when the state machine enters the second and final FI stage characterized by +ve, N, and −ve SNV values. In a similarly manner, the OCF conditions for all the switches in the primary and the secondary bridge can be identified by knowing the current value of the 3Φ SNV, and following the transition of SNV from the normal region to the FD region and then to the FI region. Since the fault diagnostic scheme is a precursor for an FT procedure, after FI, the FT procedure will decide the next course of action and the state machine will be adjusted accordingly. For example, if the faulty phase of the 3Φ-DAB converter is deactivated [20], the 3Φ-DAB converter will be modified to a 1Φ DAB converter. In this case, the next normal state would consist of 1Φ SNV rather than 3Φ SNV as the converter configuration has changed.

## V. Experimental Evaluation

### A. Hardware Prototype

A 3Φ-DAB hardware prototype is designed and developed along with the fault diagnostic circuit to check the viability of the fault diagnostic mechanism. The specifications for the hardware prototype are given in Table II, and the corresponding prototype is illustrated in Fig. 10. In addition, Fig. 11 illustrates the simulation and the experimental results for the 3Φ-DAB converter under normal and all cases of $S_{11}$ OCF; for example, the upper portion of Fig. 11(a) represents the simulation results consisting of 3Φ SNV and the GDS for the primary switches under the normal operation of the converter. The lower portion represents the experimental results from the prototype. The experimental waveform clearly matches the simulation results. Fig. 11(b)–(d)

TABLE II
PARAMETERS FOR THE HARDWARE PROTOTYPE

| Parameters | Symbols | Value | Unit |
|---|---|---|---|
| Primary MOSFET switches | $T_{11}$–$T_{16}$ | IRF640N(200/18) | V/A |
| Secondary MOSFET switches | $T_{21}$–$T_{26}$ | IRF640N(200/18) | V/A |
| Transformer turns ratio | K:1 | 2:1 | |
| Input capacitor | $C_{\text{IN}}$ | 220 | $\mu$F |
| Output capacitor | $C_{\text{OUT}}$ | 220 | $\mu$F |
| Switch paracitic capacitors | $C_{11} - C_{16}$ $C_{21} - C_{26}$ | 125 for 30V $V_{DS}$ | pF |
| Auxiliary inductance | $L_S$ | 45 | $\mu$H |
| Switching frequency | $F_S$ | 20 | kHz |
| Max. output power | $P_O$ | 100 | W |
| PWM and FD controller | DSP | TMS320F280049C | - |

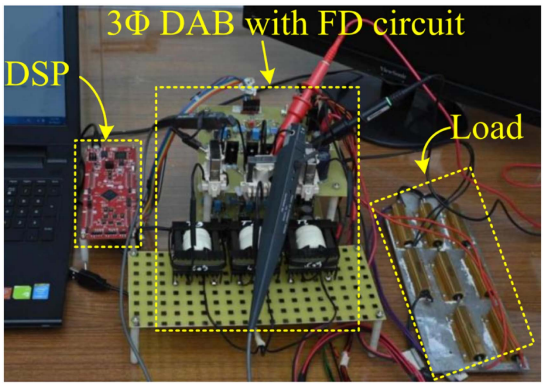


Fig. 10. Hardware prototype for the 3Φ-DAB converter.

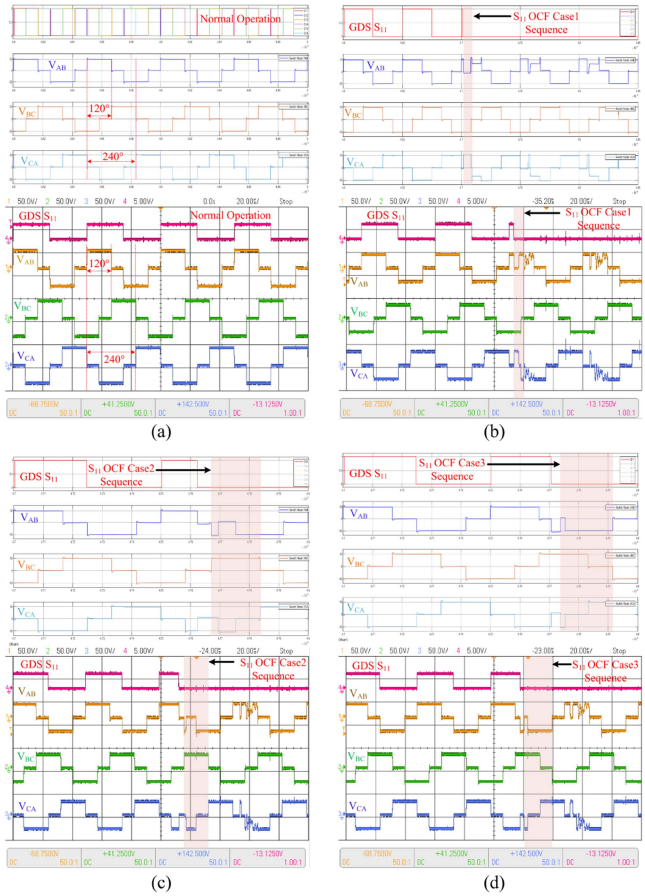


Fig. 11. Simulation and experimental representation of the normal and three cases for $S_{11}$ OCF. (a) Upper portion of the figure represents the simulation results for the normal operation of the 3Φ-DAB converter in terms of all GDS and 3Φ SNV. The lower portion is the prototype's experimental waveform, which resembles the simulation results. (b) $S_{11}$ OCF case1. The upper portion represents simulation results for $S_{11}$ OCF in terms of GDS for $S_{11}$ and the 3Φ SNVs. The lower portion is the prototype's experimental waveform, which resembles the simulation results. (c) $S_{11}$ OCF case2. (d) $S_{11}$ OCF case3.

represents the simulation and experimental results of $S_{11}$ OCF for cases 1–3, respectively. It can be seen that just like the normal operation of the 3Φ-DAB converter, the simulation and experimental results for the all cases of $S_{11}$ OCF matches. This gives the designer the confidence that the simulation model can be effectively used to develop the normal and fault conditions for the fault diagnostic state machine without resorting to hardware prototype. Introducing faults in hardware prototype at higher voltage can be dangerous and could cause hardware damage or even serious accidents. Using the simulation model to study the different fault conditions can be a very safe way to develop the fault and normal states for the fault diagnostic state machines.

### B. Fault Diagnostic Circuit

Before the SNV can be utilized for processing and information retrieval, it must be processed to make it compatible with the main controller. For this purpose, the 3Φ SNV are extracted from points A–C, illustrated in Fig. 2 and fed to the fault diagnostic circuit. The main aim of the fault diagnostic circuit illustrated in Fig. 12 is to attenuate, isolate, and convert the duo-binary 3Φ SNV into a binary representation. SNV is a differential duo-binary high-voltage signal that cannot be fed directly to the processor. It needs to be attenuated, isolated, filtered, and finally encoded to make it ready for the main processor.

The initial section of the fault diagnostic circuit constitutes a pair of matched attenuators with an input attenuation ratio of 1:50. This voltage conversion ratio has been selected to make the output of the attenuator section low enough to be within the input common-mode range of the op-amps of the following stage of the fault diagnostic circuit, which is an instrumentation amplifier. With this attenuation ratio, the attenuator section converts the maximum 3Φ SNV from ±50 V to ±1 V. Moreover, the fault diagnostic circuit can be imported to any voltage or power level by modifying the attenuator section to limit the $V_{\text{attern}}$ to the input voltage range of OP1 and OP2, which are realized using an LM318 N operational amplifier. The high input impedance, high common mode rejection ratio, and variable differential gain of the instrumentation amplifier stage cancel out the unwanted noise from the attenuated differential signal and amplify it for further processing. The instrumentation amplifier section converts the differential 3Φ SNV signal into a ground-referenced ac signal termed as $V_{\text{diff}}$ just before the isolation section illustrated in Fig. 12. The main objective of this stage is to acquire an attenuated, and filtered ground references ac signal, which imitates the 3Φ SNV $V_{AB}$, $V_{BC}$, and $V_{CA}$.

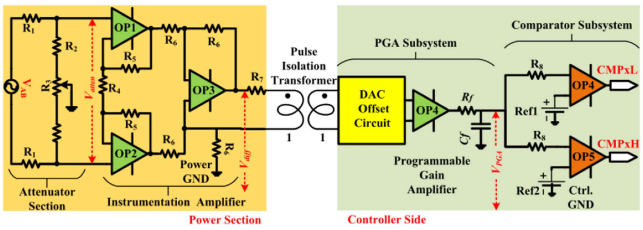


Fig. 12. Fault diagnostic circuit attenuates, filters, isolates, amplifies, and converts the duo-binary signal into a binary signal compatible with the main processor. It consists of a simple attenuator and an instrumentation amplifier on the high-voltage side. The controller side includes an offset circuit, a programmable gain amplifier, and a comparators section. After the pulse isolation transformer, the submodules, including the DAC offset stage, the programmable gain amplifier, and the comparator subsystem, are implemented within the processors.

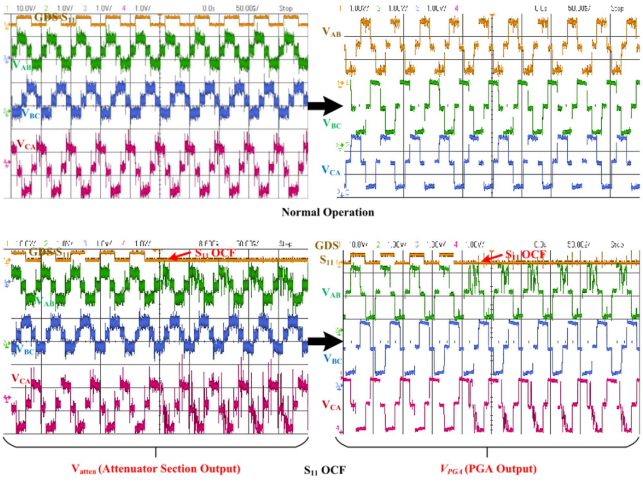


Fig. 13. Comparison between the output waveforms at various sections of fault diagnostic circuit. $V_{\text{atten}}$ is filtered and isolated to produce $V_{\text{PGA}}$. The deviation in the 3Φ SNV in the case of $S_{11}$ OCF can be observed in the case of output from the PGA.

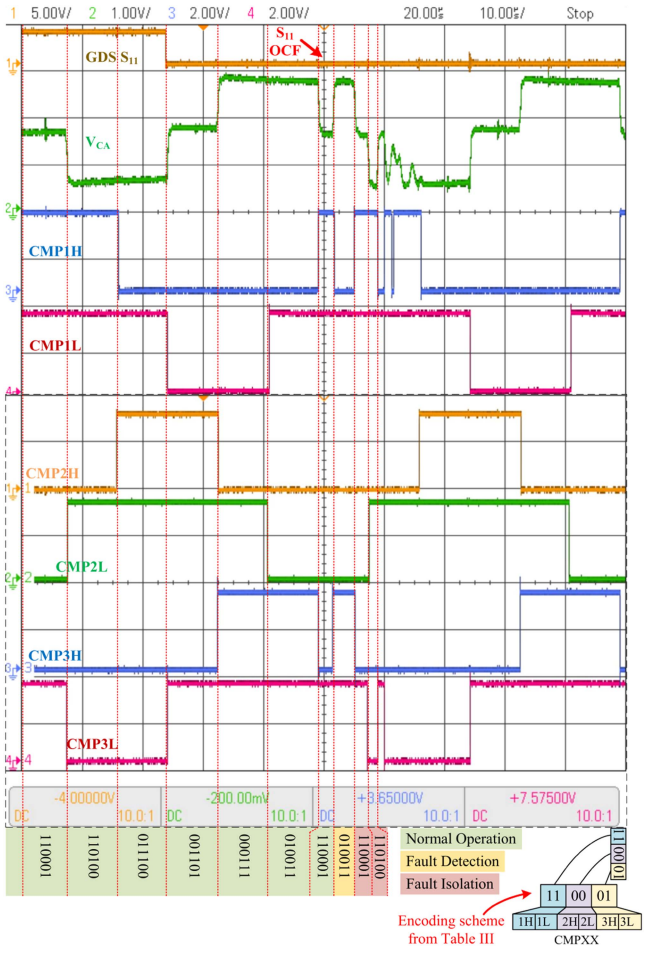


Fig. 14. Illustration of performance of comparator subsection in representing the 3Φ SNV under $S_{11}$ OCF case1. GDS for $S_{11}$ is inhibited to simulate the $S_{11}$ OCF. Deviation in SNVs caused due to $S_{11}$ OCF is ultimately reflected in the comparators output CMP1H:CMP1L and CMP3H:CMP3L. The output at the bottom represents the values of six comparator outputs. The encoding scheme from Table III can be utilized to confirm the values of SNV for case1 of $S_{11}$ OCF, in accordance with the main state diagram.

The 3Φ SNV at this stage is a duo-binary signal $V_{\text{diff}}$ with voltage levels shifting between +ve, −ve, and N. A 1:1 isolation pulse transformer is used to provide the galvanic isolation between the power section and the controller side. The isolated $V_{\text{diff}}$ signal is fed to an offset circuit to convert the ac signal into its dc counterpart. A programmable gain amplifier (PGA) in the next section ensures that the 3Φ SNV is compatible with the downstream comparator subsystem. Fig. 13 gives a comparison of the $V_{\text{atten}}$, which is the output waveform of the attenuator section, to the $V_{\text{PGA}}$, which is the output waveform from the PGA section. All three SNVs comprising $V_{AB}$, $V_{BC}$, and $V_{CA}$ are filtered, noise-free dc waveforms.

Noise rejection becomes more critical for FD cases. It can be observed from Fig. 13 that the output of attenuator section $V_{\text{atten}}$ cannot be used for $S_{11}$ open circuit FD and FI due to excessive noise. Therefore, signal conditioning from the instrumentation amplifier on the power side and the programmable gain amplifier on the controller side help mitigate this problem by removing unwanted noise. The output from the PGA contain clear information regarding the deviation of SNV due to switch OCF.

TABLE III
DUO-BINARY SNV SIGNAL CONVERSION SCHEME

| SNV Value\SNV Type | $V_{AB}$ | | $V_{BC}$ | | $V_{CA}$ | |
|---|---|---|---|---|---|---|
| | CMP1H (Bit1) | CMP1L (Bit0) | CMP2H (Bit1) | CMP2L (Bit0) | CMP3H (Bit1) | CMP3L (Bit0) |
| +ve | 1 | 1 | 1 | 1 | 1 | 1 |
| -ve | 0 | 0 | 0 | 0 | 0 | 0 |
| N | 0 | 1 | 0 | 1 | 0 | 1 |

The comparator subsystem converts the filtered and isolated SNV termed as $V_{\text{PGA}}$ into two bits binary signal (CMPxH : CMPxL). Each SNV is extracted from the 3Φ-DAB converter and transformed into a two-bit signal. So 3Φ SNV will be converted to six binary signals, as illustrated in Fig. 14, and will be used by the processor for decision-making. Table III gives the conversion scheme of the duo-binary SNVs into binary signals. Fig. 14 also illustrates the performance of the comparator section in representing the 3Φ SNV into six bit binary signal for case 1 of $S_{11}$ OCF. By inhibiting the GDS for $S_{11}$, OCF is introduced. Due to space constraints, only $V_{CA}$ is illustrated, whereas the outputs of all the comparators are displayed. Due to $S_{11}$ OCF, deviation

TABLE IV
CODING SCHEME FOR IDENTIFYING THE SWITCH FAULT USING FI_BIT1:FI_BIT0

| Semiconductor switch | FI_Bit1 | FI_Bit0 |
|---|---|---|
| No Fault | 0 | 0 |
| $S_{11}$ OCF | 1 | 0 |
| $S_{12}$ OCF | 1 | 1 |
| $S_{14}$ OCF | 0 | 1 |

in SNV $V_{AB}$ (not displayed) and $V_{CA}$ causes deviation in the output of the comparators CMP1H:CMP1L and CMP3H:CMP3L, respectively. SNV $V_{BC}$ (not displayed) remains unaffected and can be confirmed by observing CMP2H:CMP2L, which shows no deviation from its original behavior.

Output from these six comparators is fed to the FD state machine in the main processor. The comparator outputs are arranged in a specific order. The output from the comparator three makes the least significant byte whereas, the output from the comparator one becomes the most significant byte. Using a simple polling technique, the state machine observes the outputs from the comparator section and decides the new course of action.

### C. FD and Isolation Results

The FD state machine continuously monitors the comparator output, and depending upon the current state, it decides the system's health. When the converter encounters an OCF, the SNV behaves abnormally, which ultimately effects the output of the comparator subsection. Using simple comparison of the present state of the output of the comparator subsystem with the main state diagram, the FD state machine is able to detect the presence of the OCF and is able to pinpoint the exact location of the faulty switch. The FD state machine was implemented in the main processor, and different conditions of switch OCF were introduced to check the performance of the proposed scheme.

Fig. 15 illustrates the performance of the fault diagnostic scheme in terms of accuracy and detection speed by exemplifying case 1 of $S_{11}$ OCF. The GDS for $S_{11}$ is ceased to simulate the switch OCF. The abnormality in $V_{AB}$ and $V_{CA}$ produces deviations in CMP1H:CMP1L and CMP3H:CMP3L, respectively, whereas CMP2H:CMP2L remains the same since $V_{BC}$ is unaffected due to $S_{11}$ OCF. The six comparator signals are fed to the fault diagnostic state machine for final decision-making. Based on the present state, the next state is ascertained. Since the converter has encountered an OCF, the values of the 3Φ SNV deviate from its normal behavior, and the fault is detected instantly. In response, a FD signal is asserted within 1.8 $\mu$s, indicating the presence of the fault. With the converter switching frequency of 20KHz ($T_S$=50 $\mu$s), the fault is detected within 1/25 ($T_S$). The FI_Bit1 and FI_Bit0 are used to represent the encoded description of the exact faulty switch in the primary bridge. Table IV tabulates the coding sequence representing the semiconductor switch under OCF based on the values of FI_Bit1 and FI_Bit0. Two bit encoding has been carried out due to space limitations for displaying the results. It can be further converted to 3 or 4 b to include all switches on the primary and secondary sides. For this specific case, 2 b encoding is used to detect the fault in various legs of the primary bridge. Using the state machine, the exact location of the fault has been identified within 7.4 $\mu$s after which FI_Bit0 remains zero, and FI_Bit1 is set indicating, the coding sequence of $S_{11}$ OCF. The fault, therefore, has been identified within 1/6 ($T_S$).

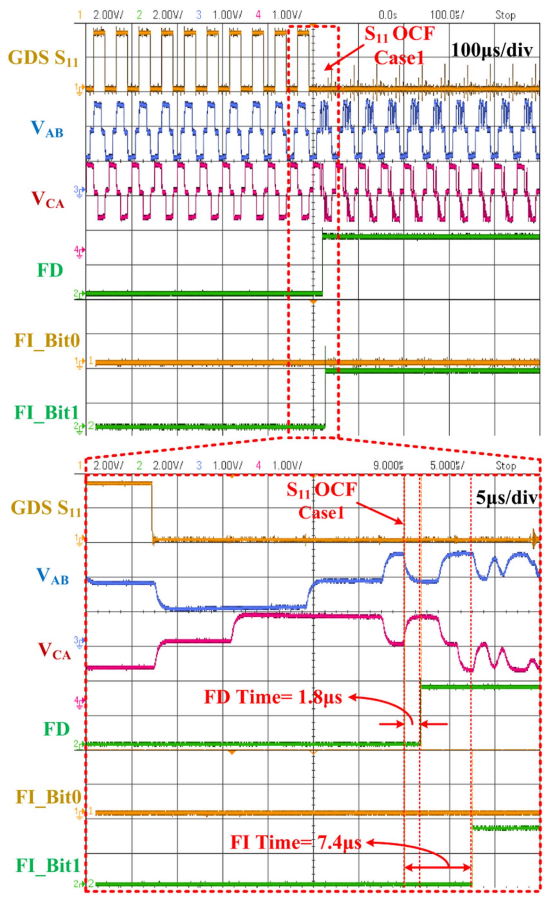


Fig. 15. $S_{11}$ OCF case1 performance results. SNV $V_{AB}$, and $V_{CA}$ deviates from its original behaviors caused due to $S_{11}$ OCF. FD is the FD signal indicating the presence of a fault. The combination of FI_Bit1 and FI_Bit0 represents the encoded information (from Table IV), giving the exact faulty switch. A zoomed portion below illustrates that the FD time is 1.8 $\mu$s and the FI time is 7.4 $\mu$s.

Fig. 16 illustrates the performance of the fault diagnostic scheme using case 2 of $S_{11}$ OCF. The GDS for $S_{11}$ is ceased to simulate the switch OCF. In this specific case, the FD signal is asserted within 5.1 $\mu$s, indicating the presence of the fault. Using the state machine, the exact location of the fault has been identified within 7.2 $\mu$s, after which FI_Bit0 remains zero, and FI_Bit1 is set, indicating the coding sequence of $S_{11}$ OCF. The fault, therefore, has been identified within less than (1/6)$T_S$.

Another illustration of the results is given in Fig. 17, which shows the performance of the fault diagnostic scheme for identifying and isolation case 1 of $S_{14}$ OCF. The GDS for $S_{14}$ is ceased to simulate the switch OCF. The abnormality in $V_{AB}$ and $V_{BC}$ produces deviations in CMP1H:CMP1L and CMP2H:CMP2L, respectively, whereas CMP3H:CMP3L remains the same since $V_{CA}$ is unaffected due to $S_{14}$ OCF. The six comparator signals

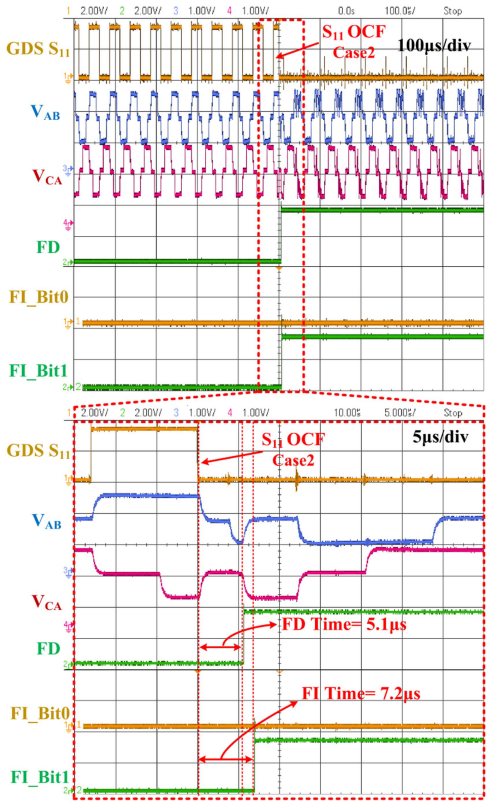


Fig. 16. Illustration of $S_{11}$ OCF case2 performance results. GDS for $S_{11}$ is inhibited to simulate the $S_{11}$ OCF under case2. $S_{11}$ OCF causes a deviation in SNVs $V_{AB}$, and $V_{CA}$. FD is the FD signal indicating the presence of a fault, whereas the combination of FI_Bit1 and FI_Bit0 represents the encoded information about the exact faulty switch (See Table IV). The zoomed portion below illustrates that the FD time is 5.1 $\mu$s and the FI time is 7.2 $\mu$s.

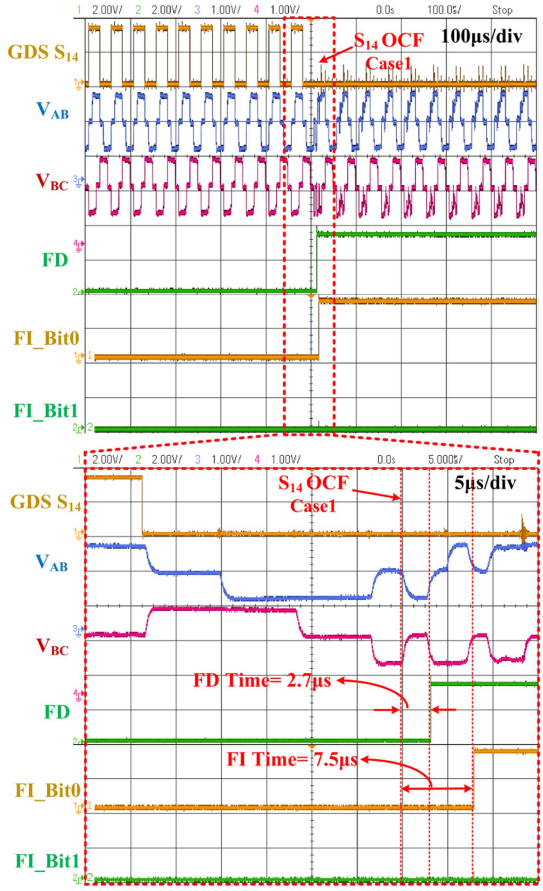


Fig. 17. Illustration of $S_{14}$ OCF case1 performance results. GDS for $S_{14}$ is inhibited to simulate the $S_{14}$ OCF. Deviation in SNV $V_{AB}$, and $V_{BC}$ caused due to $S_{14}$ OCF is also evident. FD is the FD signal indicating the presence of a fault. Whereas, the combination of FI_Bit1 and FI_Bit0 represents the encoded information about the exact faulty switch (see Table IV). The zoomed portion below illustrates that the FD time is 2.7 $\mu$s and the FI time is 7.5 $\mu$s.

are fed to the fault diagnostic state machine for final decision-making. Based on the present state, the next state is ascertained. Since the converter has encountered, and OCF, the values of the 3$\Phi$ SNV deviate from its normal behavior and the fault is detected instantly. In response, the FD signal is asserted within 2.7 $\mu$s, indicating the presence of the fault. Using the fault diagnostic state machine, the exact location of the fault has been identified within 7.5 $\mu$s, after which FI_Bit0 is set, and FI_Bit1 remains zero, indicating the coding sequence of $S_{14}$ OCF. The fault, therefore, has been identified within 1/6 ($T_S$).

Fig. 18 illustrates the performance of the fault diagnostic scheme by exemplifying case 3 of $S_{14}$ OCF. The GDS for $S_{14}$ is ceased to simulate the switch OCF. In this specific case, the FD signal is asserted within 5.1 $\mu$s, indicating the presence of the fault. Using the fault diagnostic state machine, the exact location of the fault has been identified within 11.5 $\mu$s after which FI_Bit0 is set, and FI_Bit1 remains zero indicating the coding sequence of $S_{14}$ OCF.

## VI. Performance Evaluation Under Different Conditions

A brief discussion regarding the maximum allowable operating frequency, variation in leakage inductance, and output transients on the proposed fault diagnostic scheme is presented in this section. As illustrated in Fig. 19, the fault diagnostic state machine is implemented as an interrupt service routine (ISR) in the main processor along with the main control algorithm to detect the presence of the fault. With the complete fault diagnostic state machine implemented within the ISR, the time for ISR completion is 400 ns in the proposed prototype with the F280049 C DSP processor. The polling scheme used in the algorithm triggers the fault diagnostic state machine ISR at 1 MHz to oversample the output from the comparator subsystems every 1 $\mu$s, during which it detects the changes in the comparator outputs. In order for the fault diagnostic state machine ISR to clearly assess the changes and not miss a deviation in 3$\Phi$ SNV, the maximum running time of the ISR must be smaller than the minimum time, during which the 3$\Phi$ SNV changes its sequence after the introduction of switch OCF and can be calculated using (1) and (2). Fig. 20 illustrates a plot for the minimum detection time versus the operating frequency. It can be observed that the existing setup could be utilized to detect OCF fault for 3$\Phi$-DAB operating upto 120KHz at different leakage inductances. The only limitation in frequency is due to the main processor capability and can be overcome by using faster

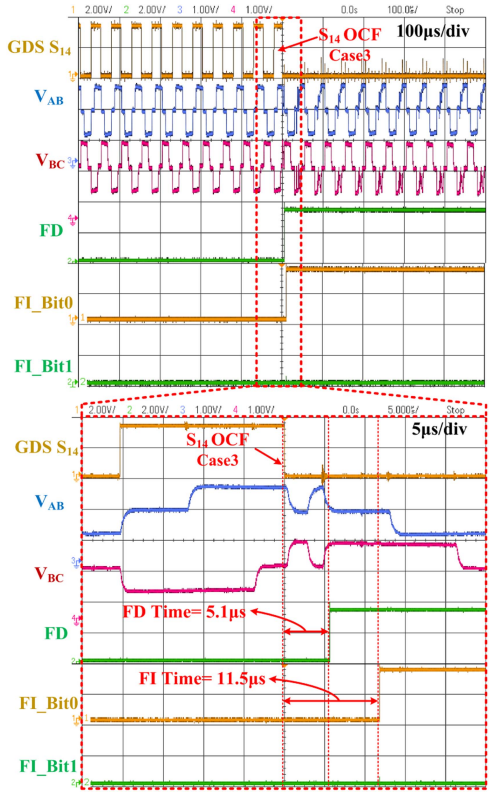


Fig. 18. Illustration of $S_{14}$ OCF case3 performance results. GDS for $S_{14}$ is inhibited to simulate the $S_{14}$ OCF. Deviation in SNVs $V_{AB}$, and $V_{BC}$ caused due to $S_{11}$ OCF is illustrated. FD is the FD signal indicating the presence of a fault. Whereas, the combination of FI_Bit1 and FI_Bit0 represents the encoded information about the exact faulty switch (see Table IV). The zoomed portion below illustrates that the FD time is 5.1 $\mu$s and the FI time is 11.5 $\mu$s.

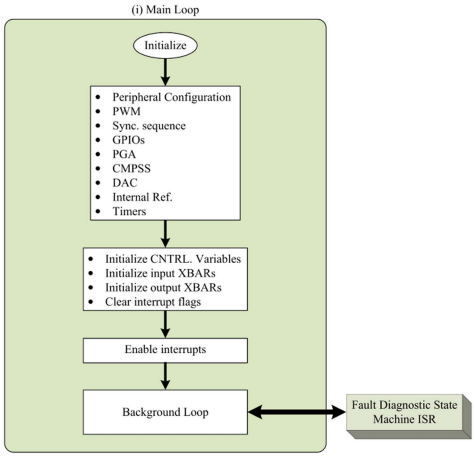


Fig. 19. Fault diagnostic scheme software control structure.

DSP processors of FPGAs. Fig. 21 also illustrates the robustness of the proposed scheme to voltage and load variations. After comparing Fig. 21(a) and (b), it can be stated that the proposed fault diagnostic mechanism can accurately detect and isolate the switch OCF under different load conditions and voltage levels.

One of the most powerful features of this technique is that the mechanism can be updated with extreme ease by modifying the fault diagnostic state machine to include new states of 3Φ

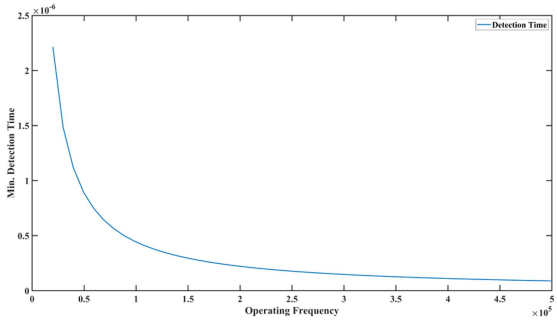


Fig. 20. Minimum detection time versus the operating frequency.

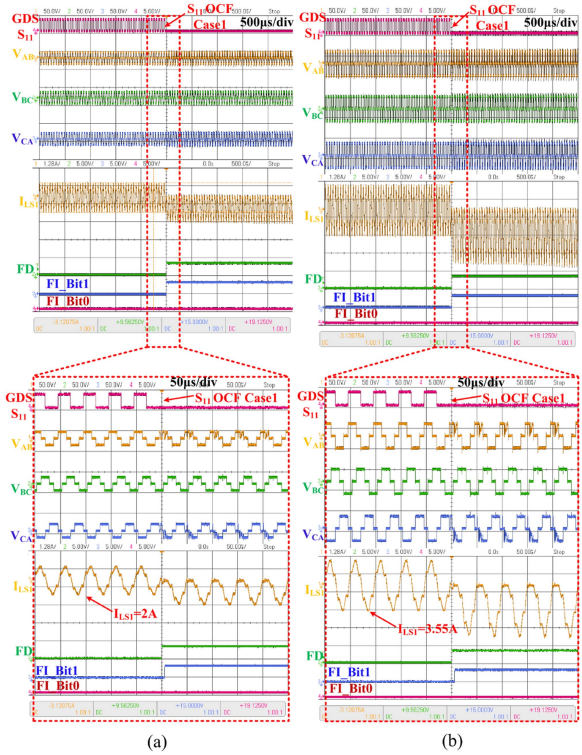


Fig. 21. Performance evaluations of the proposed scheme under different output voltage conditions. (a) $S_{11}$ OCF illustrations under $V_{DC2}$ = 8 V, and inductor current $I_{L1}$=2 A. (b) $S_{11}$ OCF illustrations under $V_{DC2}$ = 14 V, and inductor current $I_{L1}$ = 3.55 A.

SNV for additional normal and fault conditions introduced due to changes in the switching sequence. As the fault diagnostic state machine is implemented within software along with the main control algorithm, all the developer needs is to identify the new normal and faulty states using either simulation results or experimental analysis and add these stages to the state machine software.

## VII. Conclusion

FT mechanisms are indispensable to a highly reliable electronic system, and FD and FI are the initial step to these mechanisms. Owing to this fact, this research is focused on the much-neglected fault diagnostic schemes for the 3Φ-DAB converter. The duo-binary SNVs from the three phases are the fault signature used for FD and FI. This signature is extracted from the

3Φ-DAB converter and processed using a low cost, simple fault diagnostic circuit. The fault diagnostic circuit filters, isolates, and processes the 3Φ SNV. Using a simple state machine and the current state of the 3Φ SNV, the fault diagnostic mechanism can effectively detect and isolate the switch OCF without using costly current and voltage sensors. Various experimental results were presented using a low-power prototype that prove this technique's accuracy. Compared with previously presented techniques, the proposed FD and FI technique is superior in various aspects and can also be utilized to detect and isolate the switch SCF. One novelty of this approach is that it does not utilize any costly voltage and current sensor or any expensive transducers. The FD time is robust to circuit parameter variations, such as leakage inductance, input and output voltages, and is as low as 1.8 $\mu s$, which can be further reduced if a more powerful DSP processor or an FPGA is utilized, and the overall FI time is as less as 7.2 $\mu$s.

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