A Cascaded H-Bridge-Based Multilevel Converter With Low Energy Pulsation for High-Power Grid Applications

Daniel Bernet, *Member, IEEE*, and Marc Hiller, *Member, IEEE*

***Abstract*—The ongoing transformation of power supply is leading to an increasing penetration of electrical grids with power converters, which are used in high-volume applications such as grid integration of renewable energy sources, energy storage systems, charging infrastructure for electric vehicles, and industrial electric drives. This results in significant and novel challenges for power quality and supply stability, which will likely result in further increasing demands on the converters used in the aforementioned applications. To address these challenges, this article presents a novel multilevel converter system for high-power grid applications, which is characterized by high output power and voltage quality, low energy pulsation, and high scalability and modularity. These characteristics are achieved by a novel concept of operation for the combination of a high-power main converter and a low-power cascaded H-bridge converter, which is derived based on the modeling and control design carried out for the proposed converter system. Simulation and experimental results verify the potential of the multilevel converter system and show that, compared to full-power multilevel converters, it allows high output voltage quality at high output power while maintaining low current load and low energy pulsation within the cells of the cascaded H-bridge converter.**

***Index Terms*—Active filter, active front-end, cascaded H-bridge converter, hybrid converter system, multilevel converter.**

I. Introduction

CURRENT changes in the electrical energy supply and the structure of electrical grids as a result of the large-scale grid integration of renewable energy sources, charging infrastructure for electric vehicles, and energy storage systems pose significant and novel challenges for energy quality and supply stability. It is to be expected that power electronics, as an important base technology for these developments, will take on a significantly increasing share in the conversion and distribution of electrical energy in the future.

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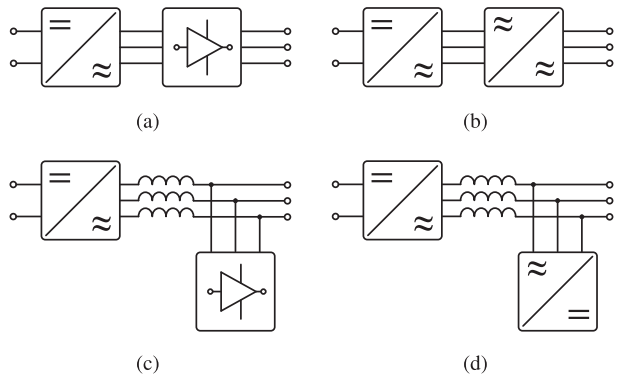

Fig. 1. Hybrid converter topologies with a DC and a three-phase AC connection for grid applications. (a) SHPA. (b) SHC. (c) PHPA. (d) PHC.

As a result of these development trends, a significant increase in converter-induced harmonics is to be expected, which cause additional losses and can also lead to harmonic instabilities and power supply interruptions due to resonance excitation and interaction with other grid equipment [1]. In order to achieve stable operation and high voltage quality even under these conditions, future grid standards are likely to include reduced harmonic limits. For this reason, passive filtering efforts to reduce harmonics are expected to increase for conventional two- and three-level converters [2L-VSC and three-level neutral point clamped VSC (3L-NPC-VSC)], which are widely used in commercial applications in the low-voltage (LV) and lower medium-voltage (MV) range due to their competitive cost, high robustness, and high efficiencies. To reduce the passive components of the output filter, multilevel converters such as the modular multilevel converter (MMC) [2], [3] and the cascaded H-bridge voltage source converter (CHB-VSC) are possible alternatives to the widely used two-level and three-level converters. However, the significantly increased power semiconductor and capacitive energy storage requirements and, in the case of the CHB-VSC, the complex transformer are major drawbacks of these topologies, which imply higher costs and lower power density. Quasi-two-level modulation of multilevel converters, introduced in [4] for a five-level converter, is one way to reduce capacitively stored energy. This modulation strategy uses the additional voltage levels only to balance the semiconductor series connections, leading approximately to a two-level output voltage. This allows a substantial reduce in capacitance and has been investigated primarily for medium- and high-voltage

TABLE I
SELECTED CONTRIBUTIONS ON HYBRID CONVERTERS CLASSIFIED BY APPLICATION FOR INCREASING THE POWER OF LINEAR AMPLIFIERS, TWO-LEVEL CONVERTERS (2L), AND MULTILEVEL CONVERTERS (ML)

Appl.	SHPA	SHC	PHPA	PHC
Grids	/	[19]	/	[23]^{2L}, [24–27]^{ML}
Drives	/	[20]	/	[28–30]^{2L}
PHIL	[13, 14]	[13, 21]	[13]	[13, 31–33]^{ML}
Other	[12, 15–18]	[22]	[12, 16, 34, 35]	[36, 37]^{2L}

applications, including application to the flying capacitor converter (FLC-VSC) [5], [6], [7], [8] and MMC [9], [10], [11].

Hybrid converter topologies are another alternative for reducing the effort of multilevel converters. These typically use a conventional two- or three-level main converter, which is characterized by an advantageous relation between attainable output power and costs as well as by a high robustness and power density. To improve the output voltage quality and, thus, reduce the required filtering effort, an additional low-power auxiliary converter with high output voltage quality, such as a multilevel converter or linear amplifier, is used. Hybrid power converters for grid applications with a dc and a three-phase ac connection can be connected in a series or parallel structure, as shown in Fig. 1. Yundt [12] provides an overview of series and parallel hybrid power converter configurations that are investigated in a number of research contributions for single-phase and three-phase applications. An overview of recent research activities on the application of hybrid converters for power-hardware-in-the-loop (PHIL) applications can be found in [13]. Table I summarizes selected contributions on hybrid converters depending on their topologies and applications.

According to Fig. 1(a) and (b), series hybrid converters (SHCs) are composed of a series connection of the high- and low-power converters. This topology with linear amplifiers as shown in Fig. 1(a), called series hybrid power amplifier (SHPA), has been investigated in [13] and [14] for PHIL applications and furthermore in [15], [16], [17], and [18] as a general single-phase power supply. The series connection of a high-power main converter and a fast-switching full-bridge cell based on Fig. 1(b) was proposed in [19] for grid applications and in [20] for feeding an electric drive. Furthermore, the concept is used in [13] and [21] for a PHIL emulation converter and in [22] as a general power supply for a three-phase load. In parallel hybrid converter topologies, the main and auxiliary converters are connected in parallel, which requires an additional inductor for voltage decoupling according to Fig. 1(c) and (d). The principle in Fig. 1(c) was introduced in [12] to increase the output power of linear power amplifiers and was further investigated for this purpose in [16], [34], and [35]. An investigation regarding the application as PHIL emulation converter can be found in [13]. In [23], [24], [25], [26], and [27], we proposed the use of a parallel hybrid converter with a switching auxiliary converter as shown in Fig. 1(d) for the three-phase grid and PHIL applications. In this context, the combination of a silicon (Si) insulated-gate bipolar transistor (IGBT)-based two-level main converter with a silicon-carbide (SiC) MOSFET-based two-level auxiliary converter is presented in [23]. In [24], [25], [26], and [27], the potential of a 3L-NPC-VSC main converter with a CHB-VSC as an auxiliary converter for reducing the passive filter size and, thereby, increasing the utilization of high-power MV converters is investigated.

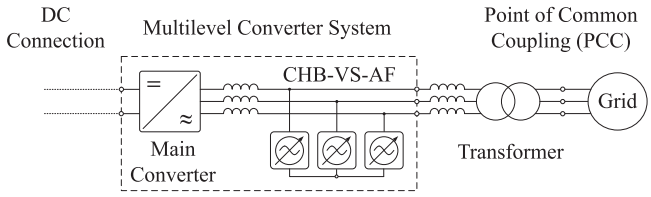

Fig. 2. Proposed grid-connected multilevel converter system composed of a high-power main converter and a voltage-forming CHB-VS-AF.

The combination of a Si-IGBT-based two-level main converter and a SiC-MOSFET-based two-level auxiliary converter is investigated in [36] and [37] as a three-phase general-purpose power supply. In [28] and [29], the so-called tandem converter is introduced for electric drives, which is composed of a 2L-VSC as an auxiliary converter and a current-source converter (CSI) as the main converter. Therein, the implemented hysteresis control of the auxiliary converter allows the compensation of the substantial low-frequency current harmonics of the CSI, which is used to control an induction machine. Modeling of semiconductor losses and a comparison of the tandem converter to a 2L-VSC as a full-power converter are presented in [30] for the possible use of Si and SiC semiconductors. Due to the use of a CSI as the main converter, the tandem converter does not require coupling inductors while on the other hand, the size and weight of the inductive dc-link are important disadvantages of this topology.

To reduce the capacitively stored energy in grid-connected multilevel converters, this article presents the multilevel converter system shown in Fig. 2, which is based on the work in [23], [24], [25], [26], and [27] and corresponds to a parallel hybrid converter according to Fig. 1(d). It is composed of a conventional main converter and a CHB-VSC connected in parallel to the converter output without coupling impedance. Since the CHB-VSC is only intended to provide the output voltage and to mitigate the current harmonics of the main converter, it will be referred to as the cascaded H-bridge voltage-source active filter (CHB-VS-AF). The introduced operating principle ensures a very low energy pulsation and installed semiconductor power of the presented hybrid multilevel converter as compared to full-power multilevel converters with comparable performance characteristics.

The rest of this article is organized as follows. Section II presents, for the first time, the complete modeling of the multilevel converter system shown in Fig. 2. Based on the derived model, the control design is carried out in Section III with the aim of limiting the load current of the CHB-VS-AF to harmonics of the main converter at steady-state and transient operation in order to minimize the additional effort for the CHB-VS-AF. Furthermore, a part of this control strategy is an energy control that allows the CHB-VS-AF to operate without a power supply or connection to the main converter dc-link. In Section IV, the presented concept of operation is verified by simulation results. The energy pulsation and installed semiconductor power are

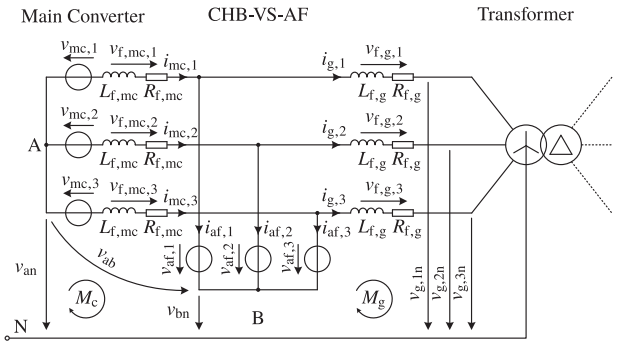

Fig. 3. Generalized equivalent circuit diagram of the main converter, voltage-forming CHB-VS-AF, and transformer.

examined in Section V and compared with full-power multilevel converters. Finally, the potential of the proposed multilevel converter configuration is confirmed by experimental results presented in Section VI.

II. Modeling

Since the characteristics and requirements are fundamentally different from conventional multilevel converters, physical modeling of the proposed converter configuration is carried out in this section. This contributes to the understanding of the energy conversion process between the grid, CHB-VS-AF, and main converter and provides the basis for the control design in Section III.

For a generally valid and topology-independent modeling, main converter and CHB-VS-AF are considered as adjustable three-phase voltage sources in star connection in the equivalent circuit of the overall system in Fig. 3. Since the CHB-VS-AF provides only reactive power and therefore does not require a dc voltage supply, consideration is given to the power components of the CHB-VS-AF (see Section II-C) impacting the energy stored in its capacitances. The converter-side and grid-side filter inductors are modeled by a series connection of their inductance and winding resistance. With respect to a practical implementation, the primary voltage of the transformer is defined as the grid voltage, since this is typically used by the grid-side converter control for grid synchronization.

The overall system can be divided into a grid side (see Section II-A), consisting of the grid-side filter inductor, transformer, and point of common coupling (PCC), and a converter side (see Section II-B), consisting of the main converter and its filter inductor. The aim of deriving the converter model is to separately describe all power components of the converter system formed by currents and voltages of the main converter, CHB-VS-AF, and the grid. The modeling strategy used was proposed in [38] for the control of an MMC and can also be applied to other MMC topologies such as the modular multilevel matrix converter (M3C), as shown in [39].

A. Grid-Side Model

According to the generalized equivalent circuit in Fig. 3, applying Kirchhoff's voltage law (KVL) to the grid-side mesh

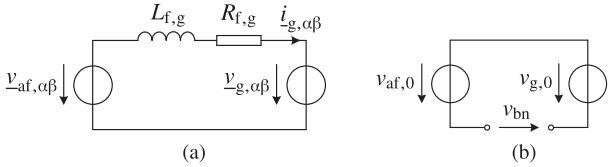

Fig. 4. $\alpha\beta 0$ equivalent circuits of the grid side. (a) $\alpha\beta$-components. (b) 0-component.

M_g yields the following system of equations:

$$\begin{bmatrix} v_{\mathrm{af},1\mathrm{n}} \\ v_{\mathrm{af},2\mathrm{n}} \\ v_{\mathrm{af},3\mathrm{n}} \end{bmatrix} = R_{\mathrm{f,g}} \begin{bmatrix} i_{\mathrm{g},1} \\ i_{\mathrm{g},2} \\ i_{\mathrm{g},3} \end{bmatrix} + L_{\mathrm{f,g}} \frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} i_{\mathrm{g},1} \\ i_{\mathrm{g},2} \\ i_{\mathrm{g},3} \end{bmatrix} + \begin{bmatrix} v_{\mathrm{g},1\mathrm{n}} \\ v_{\mathrm{g},2\mathrm{n}} \\ v_{\mathrm{g},3\mathrm{n}} \end{bmatrix}. \quad (1)$$

In (1), $\boldsymbol{i_\mathrm{g}} = [i_{\mathrm{g},1}\ i_{\mathrm{g},2}\ i_{\mathrm{g},3}]^\mathrm{T}$, $\boldsymbol{v_{\mathrm{g,n}}} = [v_{\mathrm{g},1\mathrm{n}}\ v_{\mathrm{g},2\mathrm{n}}\ v_{\mathrm{g},3\mathrm{n}}]^\mathrm{T}$, and $\boldsymbol{v_{\mathrm{af,n}}} = [v_{\mathrm{af},1\mathrm{n}}\ v_{\mathrm{af},2\mathrm{n}}\ v_{\mathrm{af},3\mathrm{n}}]^\mathrm{T}$ are the grid current, the line-to-neutral grid voltage, and the line-to-neutral voltage of the CHB-VS-AF, respectively. The latter is composed of the phase voltage $\boldsymbol{v}_\mathrm{af} = [v_{\mathrm{af},1}\ v_{\mathrm{af},2}\ v_{\mathrm{af},3}]^\mathrm{T}$ and the neutral point voltage v_bn of the CHB-VS-AF

$$\begin{bmatrix} v_{\mathrm{af},1\mathrm{n}} \\ v_{\mathrm{af},2\mathrm{n}} \\ v_{\mathrm{af},3\mathrm{n}} \end{bmatrix} = \begin{bmatrix} v_{\mathrm{af},1} \\ v_{\mathrm{af},2} \\ v_{\mathrm{af},3} \end{bmatrix} + \begin{bmatrix} v_\mathrm{bn} \\ v_\mathrm{bn} \\ v_\mathrm{bn} \end{bmatrix}. \quad (2)$$

The transformation from three-phase to $\alpha\beta 0$-coordinates can be achieved by using the Clarke transformation from (23)

$$\begin{bmatrix} v_{\mathrm{af},\alpha} \\ v_{\mathrm{af},\beta} \\ v_{\mathrm{af},0} \end{bmatrix} = \mathbf{C} \cdot \begin{bmatrix} v_{\mathrm{af},1\mathrm{n}} \\ v_{\mathrm{af},2\mathrm{n}} \\ v_{\mathrm{af},3\mathrm{n}} \end{bmatrix} - \mathbf{C} \cdot \begin{bmatrix} v_\mathrm{bn} \\ v_\mathrm{bn} \\ v_\mathrm{bn} \end{bmatrix} \quad (3)$$

$$= R_{\mathrm{f,g}} \begin{bmatrix} i_{\mathrm{g},\alpha} \\ i_{\mathrm{g},\beta} \\ 0 \end{bmatrix} + L_{\mathrm{f,g}} \frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} i_{\mathrm{g},\alpha} \\ i_{\mathrm{g},\beta} \\ 0 \end{bmatrix} + \begin{bmatrix} v_{\mathrm{g},\alpha} \\ v_{\mathrm{g},\beta} \\ v_{\mathrm{g},0} \end{bmatrix} - \begin{bmatrix} 0 \\ 0 \\ v_\mathrm{bn} \end{bmatrix}. \quad (4)$$

Using the grid-side mesh (4), the equivalent circuits of the $\alpha\beta$- and common-mode components in Fig. 4 can be derived. In Fig. 4(a), it can be seen that the grid current $\alpha\beta$-components are determined exclusively by the $\alpha\beta$-components of the grid and CHB-VS-AF voltages as well as the impedance of the grid-side filter inductor while they have no dependencies on current or voltage components of the main converter. This decoupling of grid current and main converter current results from the impedanceless connection of the CHB-VS-AF to the converter output and represents an important characteristic of the proposed converter configuration. In (4), $v_{\mathrm{g},0}$ corresponds to a possible common-mode component of the grid voltage, which can occur, for example, in converter-fed grids and is connected in antiseries to the common-mode voltage $v_{\mathrm{af},0}$ of the CHB-VS-AF in the associated equivalent circuit in Fig. 4(b). Therein, the open terminals, between which the neutral point voltage v_bn drops, take into account the impossibility of a common-mode current according to (4).

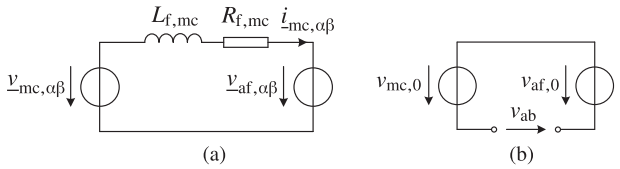

Fig. 5. $\alpha\beta0$ equivalent circuit of the converter side. (a) $\alpha\beta$-components. (b) 0-component.

B. Converter-Side Model

The converter-side mesh M_{c} of the investigated converter configuration in Fig. 3 results in a system of equations whose structure corresponds to the grid-side mesh (1)

$$\begin{bmatrix} v_{\mathrm{mc,1n}} \\ v_{\mathrm{mc,2n}} \\ v_{\mathrm{mc,3n}} \end{bmatrix} = R_{\mathrm{f,mc}} \begin{bmatrix} i_{\mathrm{mc},1} \\ i_{\mathrm{mc},2} \\ i_{\mathrm{mc},3} \end{bmatrix} + L_{\mathrm{f,mc}} \frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} i_{\mathrm{mc},1} \\ i_{\mathrm{mc},2} \\ i_{\mathrm{mc},3} \end{bmatrix} + \begin{bmatrix} v_{\mathrm{af,1n}} \\ v_{\mathrm{af,2n}} \\ v_{\mathrm{af,3n}} \end{bmatrix}. \tag{5}$$

In (5), $\boldsymbol{i}_{\mathrm{mc}} = [i_{\mathrm{mc},1}\ i_{\mathrm{mc},2}\ u_{\mathrm{mc},3}]^{\mathrm{T}}$ denotes the output current and $\boldsymbol{v}_{\mathbf{mc,n}} = [v_{\mathrm{mc,1n}}\ v_{\mathrm{mc,2n}}\ v_{\mathrm{mc,3n}}]^{\mathrm{T}}$ the line-to-neutral voltage of the main converter. In the same way as the line-to-neutral voltage of the CHB-VS-AF in (2), the latter is composed of the phase voltage $\boldsymbol{v}_{\mathrm{mc}} = [v_{\mathrm{mc,1n}}\ v_{\mathrm{mc,2n}}\ v_{\mathrm{mc,3n}}]^{\mathrm{T}}$ and the neutral point voltage v_{an} of the main converter

$$\begin{bmatrix} v_{\mathrm{mc,1n}} \\ v_{\mathrm{mc,2n}} \\ v_{\mathrm{mc,3n}} \end{bmatrix} = \begin{bmatrix} v_{\mathrm{mc},1} \\ v_{\mathrm{mc},2} \\ v_{\mathrm{mc},3} \end{bmatrix} + \begin{bmatrix} v_{\mathrm{an}} \\ v_{\mathrm{an}} \\ v_{\mathrm{an}} \end{bmatrix}. \tag{6}$$

The Clarke transformation of (6) into $\alpha\beta0$-coordinates results in

$$\begin{bmatrix} v_{\mathrm{mc},\alpha} \\ v_{\mathrm{mc},\beta} \\ v_{\mathrm{mc},0} \end{bmatrix} = \mathbf{C} \cdot \begin{bmatrix} v_{\mathrm{mc,1n}} \\ v_{\mathrm{mc,2n}} \\ v_{\mathrm{mc,3n}} \end{bmatrix} - \mathbf{C} \cdot \begin{bmatrix} v_{\mathrm{an}} \\ v_{\mathrm{an}} \\ v_{\mathrm{an}} \end{bmatrix} \tag{7}$$

$$= R_{\mathrm{f,mc}} \begin{bmatrix} i_{\mathrm{mc},\alpha} \\ i_{\mathrm{mc},\beta} \\ 0 \end{bmatrix} + L_{\mathrm{f,mc}} \frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} i_{\mathrm{mc},\alpha} \\ i_{\mathrm{mc},\beta} \\ 0 \end{bmatrix} + \begin{bmatrix} v_{\mathrm{af},\alpha} \\ v_{\mathrm{af},\beta} \\ v_{\mathrm{af},0} \end{bmatrix} - \begin{bmatrix} 0 \\ 0 \\ v_{\mathrm{ab}} \end{bmatrix}. \tag{8}$$

In (8), v_{ab} denotes the voltage drop between the converter star points A and B in Fig. 3

$$v_{\mathrm{ab}} = v_{\mathrm{an}} - v_{\mathrm{bn}}. \tag{9}$$

The consistency of the equation system structure with the grid side also transfers to the converter-side $\alpha\beta0$ equivalent circuits in Fig. 5. In the $\alpha\beta$ equivalent circuit in Fig. 5(a), it can be seen that the output current $\alpha\beta$-components of the main converter are determined solely by the voltage $\alpha\beta$-components of the main converter and CHB-VS-AF, as well as the impedance of the filter inductor on the converter side. In the equivalent circuit of the common-mode components in Fig. 5(b), the common-mode voltage of the main converter $v_{\mathrm{mc},0}$ is connected in antiseries to the common-mode voltage of the CHB-VS-AF $v_{\mathrm{af},0}$. Analogous to the grid side, no common-mode current is possible on the converter side according to (8), which is taken into account in the equivalent circuit by open terminals A and B between which the neutral point voltage v_{ab} drops.

C. Power Components of the CHB-VS-AF

The desired operation of the CHB-VS-AF without an external voltage supply requires control and monitoring of the energy stored in it. To achieve this, the power components of the CHB-VS-AF leading to changes in the energy state are derived in the following. Considering Kirchhoff's current law (KCL), the power input or output from each phase of the CHB-VS-AF is described by the three-phase power in

$$\begin{bmatrix} p_{\mathrm{af},1} \\ p_{\mathrm{af},2} \\ p_{\mathrm{af},3} \end{bmatrix} = \begin{bmatrix} v_{\mathrm{af},1} \\ v_{\mathrm{af},2} \\ v_{\mathrm{af},3} \end{bmatrix} \circ \begin{bmatrix} i_{\mathrm{mc},1} - i_{\mathrm{g},1} \\ i_{\mathrm{mc},2} - i_{\mathrm{g},2} \\ i_{\mathrm{mc},3} - i_{\mathrm{g},3} \end{bmatrix}. \tag{10}$$

Since converter- and grid-side current control in three-phase 123-coordinates is disadvantageous, a description of the electrical quantities in (10) in $\alpha\beta0$-coordinates is derived first. The inverse Clarke transformation according to (24) gives the phase voltage of the CHB-VS-AF

$$\begin{bmatrix} v_{\mathrm{af},1} \\ v_{\mathrm{af},2} \\ v_{\mathrm{af},3} \end{bmatrix} = \mathbf{C^{-1}} \cdot \begin{bmatrix} v_{\mathrm{af},\alpha} \\ v_{\mathrm{af},\beta} \\ v_{\mathrm{af},0} \end{bmatrix} = \begin{bmatrix} v_{\mathrm{af},\alpha} + v_{\mathrm{af},0} \\ -\frac{1}{2} v_{\mathrm{af},\alpha} + \frac{\sqrt{3}}{2} v_{\mathrm{af},\beta} + v_{\mathrm{af},0} \\ -\frac{1}{2} v_{\mathrm{af},\alpha} - \frac{\sqrt{3}}{2} v_{\mathrm{af},\beta} + v_{\mathrm{af},0} \end{bmatrix}. \tag{11}$$

Under consideration of KCL, the output current of the CHB-VS-AF results in

$$\begin{bmatrix} i_{\mathrm{af},1} \\ i_{\mathrm{af},2} \\ i_{\mathrm{af},3} \end{bmatrix} = \mathbf{C^{-1}} \cdot \begin{bmatrix} i_{\mathrm{af},\alpha} \\ i_{\mathrm{af},\beta} \\ 0 \end{bmatrix} = \begin{bmatrix} i_{\mathrm{mc},\alpha} - i_{\mathrm{g},\alpha} \\ -\frac{1}{2}\left(i_{\mathrm{mc},\alpha} - i_{\mathrm{g},\alpha}\right) + \frac{\sqrt{3}}{2}\left(i_{\mathrm{mc},\beta} - i_{\mathrm{g},\beta}\right) \\ -\frac{1}{2}\left(i_{\mathrm{mc},\alpha} - i_{\mathrm{g},\alpha}\right) - \frac{\sqrt{3}}{2}\left(i_{\mathrm{mc},\beta} - i_{\mathrm{g},\beta}\right) \end{bmatrix}. \tag{12}$$

Substituting (11) and (12) into (10) gives the three-phase power of the CHB-VS-AF as a function of the $\alpha\beta0$-components. A subsequent Clarke transformation of this power into $\alpha\beta0$-coordinates yields

$$\begin{bmatrix} p_{\mathrm{af},\alpha} \\ p_{\mathrm{af},\beta} \\ p_{\mathrm{af},0} \end{bmatrix} = \frac{1}{2} \begin{bmatrix} v_{\mathrm{af},\alpha}\, i_{\mathrm{mc},\alpha} - v_{\mathrm{af},\beta}\, i_{\mathrm{mc},\beta} \\ -v_{\mathrm{af},\alpha}\, i_{\mathrm{mc},\beta} - v_{\mathrm{af},\beta}\, i_{\mathrm{mc},\alpha} \\ v_{\mathrm{af},\alpha}\, i_{\mathrm{mc},\alpha} + v_{\mathrm{af},\beta}\, i_{\mathrm{mc},\beta} \end{bmatrix}$$

$$+ \frac{1}{2} \begin{bmatrix} -v_{\mathrm{af},\alpha}\, i_{\mathrm{g},\alpha} + v_{\mathrm{af},\beta}\, i_{\mathrm{g},\beta} \\ v_{\mathrm{af},\alpha}\, i_{\mathrm{g},\beta} + v_{\mathrm{af},\beta}\, i_{\mathrm{g},\alpha} \\ -v_{\mathrm{af},\alpha}\, i_{\mathrm{g},\alpha} - v_{\mathrm{af},\beta}\, i_{\mathrm{g},\beta} \end{bmatrix} + \begin{bmatrix} v_{\mathrm{af},0}\, i_{\mathrm{hs},\alpha} - v_{\mathrm{af},0}\, i_{\mathrm{g},\alpha} \\ v_{\mathrm{af},0}\, i_{\mathrm{mc},\beta} - v_{\mathrm{af},0}\, i_{\mathrm{g},\beta} \\ 0 \end{bmatrix}. \tag{13}$$

The common-mode power component $p_{\mathrm{af},0}$ from (13) leads to a uniform energy change in all phases and thus to a change in the total energy $w_{\mathrm{af},0}$ stored in the CHB-VS-AF. In contrast, the $\alpha\beta$-power $\boldsymbol{p}_{\mathbf{af},\boldsymbol{\alpha\beta}} = [p_{\mathrm{af},\alpha}\ p_{\mathrm{af},\beta}]^{\mathrm{T}}$ can cause or compensate for

TABLE II
CHB-VS-AF POWER COMPONENTS

No.	Source/Sink	Parameter	$\boldsymbol{v_{\alpha\beta}}$	$\boldsymbol{i_{\alpha\beta}}$	$\boldsymbol{p_{af,\alpha\beta}}$		$\boldsymbol{p_{af,0}}$
I	Grid	amplitude	$\hat{v}_{af}$	$\hat{i}_g$	$-\frac{1}{2}\hat{v}_{af}\hat{i}_g$		$-\frac{1}{2}\hat{v}_{af}\hat{i}_g$
		phase angle	$\omega_g t+\varphi_{af,v}$	$\omega_g t+\varphi_{g,i}$	$2\omega_g t+\varphi_{af,v}+\varphi_{g,i}$		$\varphi_{af,v}-\varphi_{g,i}$
II	Grid	amplitude	$\hat{v}_{af,0}$	$\hat{i}_g$	$-\frac{1}{2}\hat{v}_{af,0}\hat{i}_g$	$-\frac{1}{2}\hat{v}_{af,0}\hat{i}_g$	
		phase angle	$\omega_g t+\varphi_{af,v}$	$\omega_g t+\varphi_{g,i}$	$2\omega_g t+\varphi_{af,0}+\varphi_{g,i}$	$\varphi_{g,i}-\varphi_{af,0}$	
III	Main Converter	amplitude	$\hat{v}_{af}$	$\hat{i}_{mc}$	$\frac{1}{2}\hat{v}_{af}\hat{i}_{mc}$		$\frac{1}{2}\hat{v}_{af}\hat{i}_{mc}$
		phase angle	$\omega_g t+\varphi_{af,v}$	$\omega_g t+\varphi_{g,i}$	$-2\omega_g t-\varphi_{af,v}-\varphi_{mc,i}$		$\varphi_{af,v}-\varphi_{mc,i}$
IV	Main Converter	amplitude	$\hat{v}_{af,0}$	$\hat{i}_{mc}$	$\frac{1}{2}\hat{v}_{af,0}\hat{i}_{mc}$	$\frac{1}{2}\hat{v}_{af,0}\hat{i}_{mc}$	
		phase angle	$\omega_g t+\varphi_{af,0}$	$\omega_g t+\varphi_{mc,i}$	$2\omega_g t+\varphi_{af,0}+\varphi_{mc,i}$	$\varphi_{mc,i}-\varphi_{af,0}$	

an uneven energy distribution $\boldsymbol{w_{af,\alpha\beta}}=[w_{af,\alpha}\ w_{af,\beta}]^T$ in the three phases of the CHB-VS-AF

$$\begin{bmatrix} w_{af,\alpha} \\ w_{af,\beta} \\ w_{af,0} \end{bmatrix} = \begin{bmatrix} w_{af,t0,\alpha} \\ w_{af,t0,\beta} \\ w_{af,t0,0} \end{bmatrix} + \int_{t_0}^{t} \begin{bmatrix} p_{af,\alpha} \\ p_{af,\beta} \\ p_{af,0} \end{bmatrix} \mathrm{d}t. \tag{14}$$

To determine the power components impacting the energy stored in the CHB-VS-AF, fundamental frequency electrical quantities are considered according to

$$x=\hat{x}\cos\left(\omega_g t+\varphi_x\right) \tag{15}$$

where $\hat{x}$ and φ_x are the amplitude and phase angle, respectively. Substituting these quantities into (13) gives the power components of the CHB-VS-AF, the most important of which is summarized in Table II. Therein, all active power components that lead to a permanent change in the energy state of the CHB-VS-AF are marked in blue.

The power component I marked in blue results from the injection of a grid current and impacts the total energy stored in the CHB-VS-AF. On the converter side, III corresponds to the equivalent power component, which has a negative sign due to KCL. In the same way, the blue marked equivalent power components II and IV with an impact on the energy distribution among the CHB-VS-AF phases are obtained, which are caused by the grid-side and converter-side fundamental currents and the fundamental CHB-VS-AF common-mode voltage. For operation with coupled control of the main converter and CHB-VS-AF, e.g., by using a common control unit, the reference of one of these equivalent power components can be freely specified. Consequently, the respective power component remaining can be used to compensate the preset power component and thus to control the total energy and energy distribution. This shows that with the power components highlighted in blue in Table II, there are sufficient degrees of freedom available for the control design described in the next section.

III. CONTROL

The control scheme handles the operational management and provides the basis for the implementation of the proposed multilevel converter configuration. Important requirements for the control design result from the objectives formulated in Section I and include compensation of current harmonics up to the kilohertz range with simultaneously limited control bandwidth (see Section III-A), grid current control (see Section III-B) with current limitation of the CHB-VS-AF in steady-state and transient operations (see Section III-C), and control of the energy stored in the CHB-VS-AF (see Section III-D). Fig. 6 shows the coupled fundamental frequency control scheme for the main converter and CHB-VS-AF developed based on the modeling in Section II. In the following, the functional units and features of the control system are described according to the requirements to be met.

A. Limited Control Bandwidth

The coupled fundamental frequency control of the multilevel converter system is performed in dq-coordinates. As in conventional grid-side control strategies in rotating coordinates, the phase angle of the positive sequence grid voltage is used for the Park transformation, so that the positive sequence of the controlled variables corresponds to dc-components and the negative sequence and harmonic components correspond to alternating components. This allows the use of conventional fundamental frequency current control schemes, where the grid-side current is controlled based on Fig. 4(a) by the CHB-VS-AF and the converter-side current is controlled based on Fig. 5(a) by the main converter. Since fundamental frequency currents and voltages, as shown in Section II, are also sufficient for energy control of the CHB-VS-AF, and since no identification or active compensation of the current harmonics of the main converter is required [23] due to the exclusive dependence of the grid current on the CHB-VS-AF according to Fig. 4(a), no electrical quantities with frequencies above fundamental frequency need to be controlled and a high control bandwidth can be avoided.

B. Grid Current Control

Based on (4) and Fig. 4(a), the CHB-VS-AF performs the grid current control using conventional PI-controllers and a sampling frequency of $f_{s,af}$ [23]. The widely used double-decoupled synchronous reference frame phase-locked-loop (DDSRF-PLL) [40] allows a determination of the positive and negative sequence in dq-coordinates as well as the phase angle of the measured three-phase grid voltage. In addition to the grid voltage in dq-coordinates $\underline{v}_{g,dq}=[v_{g,d}\ jv_{g,q}]^T$, the grid current $\underline{i}_{g,dq}=[i_{g,d}\ ji_{g,q}]^T$, transformed into dq-coordinates using the

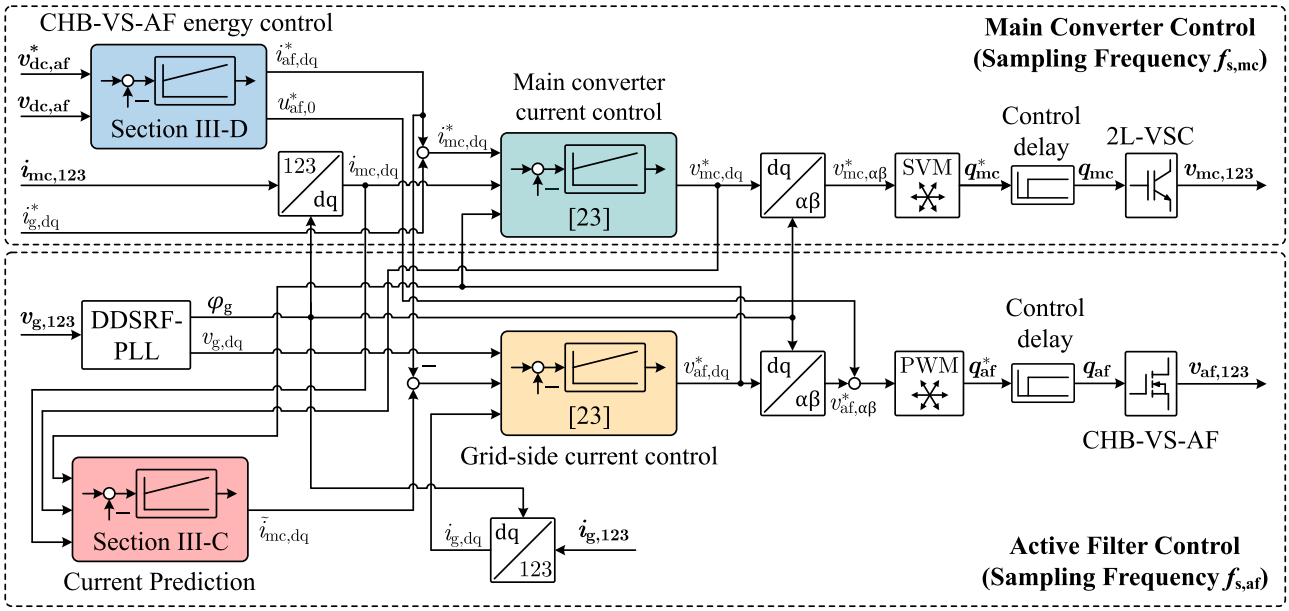

Fig. 6. Fundamental frequency multilevel converter control in the rotating dq-frame (underlines indicate complex numbers). The control scheme uses a DDSRF-PLL, current prediction, current control loops of the main converter and CHB-VS-AF, CHB-VS-AF energy control, space vector modulation, and PWM.

grid angle φ_g, and the positive sequence grid current reference, typically specified by the application, represent input variables of the grid current control loop. The latter determines the reference output voltage of the CHB-VS-AF, which is passed both to the control of the main converter for voltage feedforward and, after an inverse Park transformation, to the modulation scheme. With the switching signals thus obtained, the CHB-VS-AF, represented in Fig. 6 by the symbol of a MOSFET, generates the three-phase output voltage of the multilevel converter system due to the parallel connection to the output without a coupling impedance (see Figs. 2 and 3).

C. Limitation of the CHB-VS-AF Output Current

In order to achieve that the CHB-VS-AF leads to a high-quality voltage-source output characteristic of the multilevel converter system at only a small share of the total power, a reliable limitation of the CHB-VS-AF output current to current harmonics of the main converter is required under all operating conditions. According to KCL, the current of the CHB-VS-AF is equal to the difference between the main converter current and the grid current

$$\boldsymbol{i}_{\mathrm{af}} = \boldsymbol{i}_{\mathrm{mc}} - \boldsymbol{i}_{\mathbf{g}}. \tag{16}$$

For this reason, the use of equal current references for the converter-side and grid-side current control loops initially seems obvious. In steady-state operation, this would result in precise output current limitation of the CHB-VS-AF due to the use of PI-controller-based current control loops in dq-coordinates without permanent control deviation. When the current reference is changed, however, the ratio of main converter and grid current is determined by the dynamic characteristics of the converter- and grid-side current control loops, so that a limited output current of the CHB-VS-AF in both steady-state and transient operating points would require an alignment of the reference variable behavior of the current control loops when using the same current reference. For this purpose, the combination of conventional fundamental frequency controls with different sampling frequencies and back electromotive force (EMF) voltages of the main converter and CHB-VS-AF represent an important disadvantage of using equal references for the current control loops. In particular, the volatility of the CHB-VS-AF output voltage, corresponding to the back EMF voltage of the main converter, and the delayed feedforward of its reference due to the calculation dead times result in a substantial challenge for the adaptation of the reference variable behavior of the main converter control.

In order to, nevertheless, achieve a high match of grid current and main converter current in steady-state and transient operations and, thus, avoid an increased current load on the CHB-VS-AF, e.g., in the event of reference step changes, a predictive determination of the reference of the grid-side current control, shown in red in Fig. 6, is carried out. Although the actual value $\underline{i}_{\mathrm{mc,dq}}$ measured by the main converter, which corresponds in good approximation to the fundamental current when symmetrical or asymmetrical sampling is used, is available as an input variable for identification of $\underline{\tilde{i}}_{\mathrm{mc,dq}}$, a determination of $\underline{\tilde{i}}_{\mathrm{mc,dq}}$ by the CHB-VS-AF is still necessary between the sampling instants of the main converter due to the higher sampling and control frequency of the CHB-VS-AF. Due to the control coupling of the main converter and CHB-VS-AF, model-based current prediction is a promising possibility, for which the output voltages of the main converter and CHB-VS-AF can be used according to Fig. 6. The voltage across the filter inductor on the converter side corresponds to the difference between the output voltages of the main converter and the CHB-VS-AF

$$\underline{v}_{\mathrm{f,mc}} = \underline{v}_{\mathrm{mc}} - \underline{v}_{\mathrm{af}}. \tag{17}$$

Assuming the ratio $\omega_g L_{f,mc} \gg R_{f,mc}$ typical for high-power applications, this voltage drops to a good approximation across the filter inductance $L_{f,mc}$

$$\underline{v}_{f,mc} = L_{f,mc}\frac{d\underline{\tilde{i}}_{mc,dq}}{dt} + j\omega_g L_{f,mc}\underline{\tilde{i}}_{mc,dq}. \quad (18)$$

Since neglecting $R_{f,mc}$ leads to a linear change of $\underline{\tilde{i}}_{mc,dq}$ at assumed constant output voltages of the main converter and CHB-VS-AF within a sampling period $T_{s,af}$, a discretization of the model by a discrete first-order Taylor series is feasible

$$\underline{\tilde{i}}_{mc,dq}(k+1) = \underline{\tilde{i}}_{mc,dq}(k) + \left.\frac{d\underline{\tilde{i}}_{mc,dq}}{dt}\right|_k T_{s,af}. \quad (19)$$

Rearranging (18) and substituting it into (19), the main converter current to be expected after one sampling period is obtained

$$\underline{\tilde{i}}_{mc,dq}(k+1) = \underline{\tilde{i}}_{mc,dq}(k) + \underbrace{\frac{T_{s,af}}{L_{f,mc}}}_{G_{sp,af}(z)} \left(\underline{v}_{mc}(k) - \underline{v}_{af}(k) - \underbrace{j\omega_g L_{f,mc}}_{G_{x,af}(z)} \underline{\tilde{i}}_{mc,dq}(k) \right). \quad (20)$$

Since the main converter and the CHB-VS-AF are operated with a common control unit, a current prediction according to (20) is promising. However, it should be noted that the output voltages $\underline{v}_{mc}$ and $\underline{v}_{af}$ may change in the next sampling period and thus lead to a deviation of the predicted current. Due to the significantly lower sampling and control frequency compared to the CHB-VS-AF, only minor impairments of the current prediction caused by the main converter voltage $\underline{v}_{mc}$ are to be expected in this case, especially since its voltage reference for the next sampling period $\underline{v}_{mc}(k+1)$ can be forwarded for the calculation in (20) depending on the required computation time of the main converter control. In contrast, the future output voltage of the CHB-VS-AF $\underline{v}_{af}(k+1)$ has a direct dependence on the predicted current $\underline{\tilde{i}}_{mc,dq}(k)$, since this is used as the reference for the grid current control and the output voltage of the CHB-VS-AF $\underline{v}_{af}(k+1)$ corresponds to its actuating variable. Nevertheless, by selecting a high sampling and control frequency of the CHB-VS-AF, it can be assumed that the resulting deviation can be sufficiently reduced.

The prediction of the main converter current by the CHB-VS-AF based on (20) is shown in Fig. 7. Therein, the control delay time of the CHB-VS-AF is taken into account by the transfer function $G_{d,af}$

$$G_{d,af}(z) = z^{-1}. \quad (21)$$

To minimize the resulting total deviation of the predicted current $\underline{\tilde{i}}_{mc,dq}(k+1)$ from the actual value $\underline{i}_{mc,dq}(k+1)$ after the next sampling period, the current $\underline{i}_{mc,dq}(k)$ measured by the main converter is used as the actual value $\underline{\tilde{i}}_{mc,dq}(k)$ for the current prediction according to (20) at each sampling instant of the main converter. For the sampling instants of the CHB-VS-AF where no updated value of the main converter is detected by comparison with the previous measured value, the current predicted in the previous sampling instant is used for $\underline{\tilde{i}}_{mc,dq}(k)$. This procedure ensures that the deviations caused by the single-step current prediction can propagate only until the next sampling instant of the main converter.

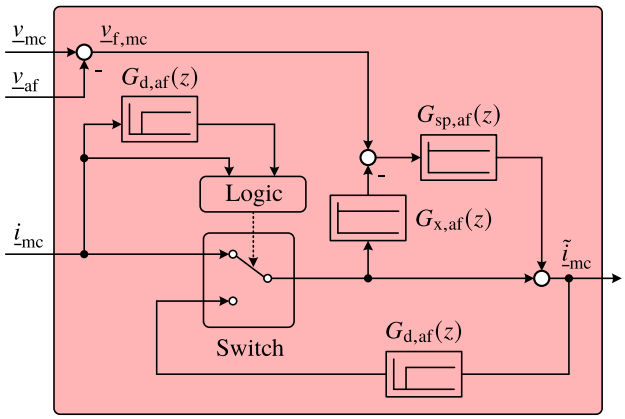

Fig. 7. Method for predicting the main converter current by the CHB-VS-AF.

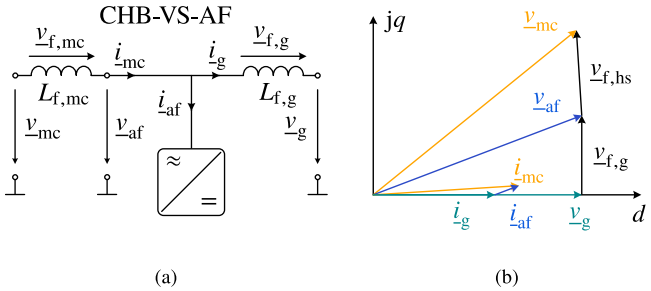

Fig. 8. (a) Single-phase equivalent circuit diagram of the CHB-VS-AF connected to the converter output. (b) Fundamental frequency complex vector diagram for operation with loss coverage.

The resulting current and voltage ratios when using the prediction of the main converter current by the CHB-VS-AF can be understood from Fig. 8. Therein, Fig. 8(b) shows the fundamental frequency complex vector diagram for an exemplary operating point for the single-phase equivalent circuit of the converter output in Fig. 8(a). By using the grid synchronous DDSRF-PLL, the grid voltage v_g is therein located on the d-axis. According to Fig. 6, the main converter uses a PI-controller to set its output current i_{mc} [based on (7) and Fig. 5(a)] to its reference value i^*_{mc}, which is composed of the grid current reference i^*_g and the fundamental current i^*_{af} required for loss coverage of the CHB-VS-AF. The latter predicts the current i_{mc} controlled by the main converter according to the procedure in Fig. 7 and uses it, minus the current required for loss coverage, as the reference value for the control of the grid current i_g according to Fig. 6. This operating principle ensures that the CHB-VS-AF carries the minimum possible fundamental frequency current in steady state and transient operations and, beyond that, only compensates the current distortions of the main converter.

D. CHB-VS-AF Energy Control

The energy control of the CHB-VS-AF is responsible for its loss coverage and energy balancing. The requirement is to maintain defined energy in the phases of the CHB-VS-AF

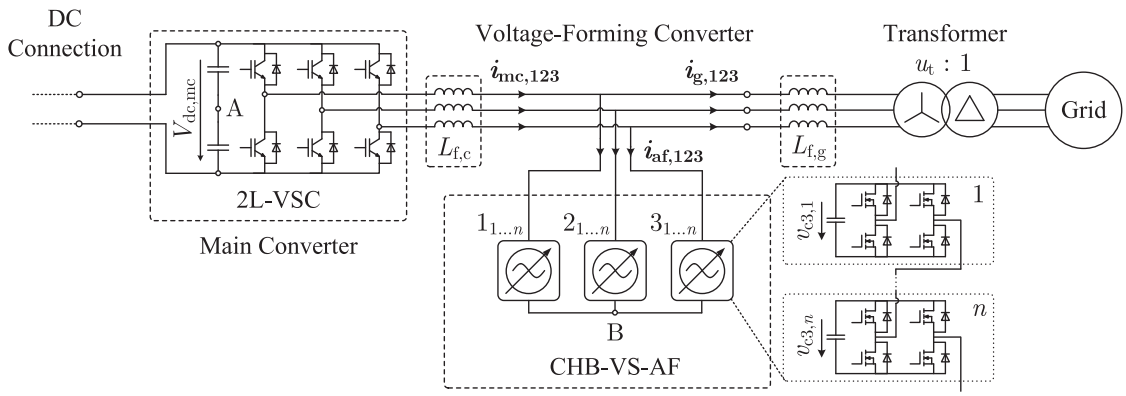

Fig. 9. Grid-connected multilevel converter system composed of a conventional 2L-VSC with Si-IGBTs as main converter and a parallel CHB-VS-AF with Si-MOSFETs as a voltage-forming converter.

under all operating conditions by exchanging power with the main converter or the grid, thus enabling stable operation of the converter system. The control scheme used in this article is based on the CHB-VS-AF power components shown in blue in Table II, which are derived in Section II. It represents an advancement of the work in [23] and [26] and uses a fundamental current $\underline{i}^*_{\mathrm{af,dq}}$ of the CHB-VS-AF for energy control, which is according to Figs. 6 and 8(b) added to the reference of the main converter current control loop. Furthermore, to balance an unequal energy distribution among the phases of the CHB-VS-AF, a fundamental common mode voltage $v^*_{\mathrm{af},0}$ is used.

IV. Simulation Results

In this section, the control strategy developed for the proposed converter configuration is verified with a simulation model implemented in MATLAB/Simulink. The simulative investigations are carried out for application in the LV range and include the generation of a multilevel output voltage at a small energy pulsation occurring in the phases of the CHB-VS-AF, mitigation of current distortions by the CHB-VS-AF, the energy control and the load current limitation of the CHB-VS-AF at steady-state and transient operating points.

The simulative verification of the proposed grid-connected multilevel converter system is carried out for the converter configuration shown in Fig. 9. It is designed according to the harmonic limits of the IEEE 519-2014 grid standard [41] for use in the 690 V grid, as this voltage level is widely used in high-power solar and wind power plants. Due to its high importance for LV applications, a Si-IGBT-based 2L-VSC is used as the main converter, operating with a dc-link voltage of 1100 V and a switching frequency of 3 kHz, which is common for wind turbines. For the simulation, the use of the 1.7 kV half-bridge module *FF1500R17IP5R* from INFINEON with a maximum continuous dc current of 1500 A is assumed. The coupling inductance is chosen to be 5.3% to allow a current ratio of CHB-VS-AF to the main converter of less than 15%. The design and control of CHB-VSC topologies without a dc power supply, which is used in star configuration as CHB-VS-AF, is the subject of numerous research contributions (e.g., [42], [43], [44], [45]) and it is commercially available in delta configuration for application as static synchronous compensator, e.g., as *SVC PLUS* by Siemens [46] and *SVC Light* by ABB [47]. The CHB-VS-AF is composed of seven cascaded full-bridge cells per phase with a cell voltage of 100 V and, thus, can generate a 15-level output voltage. The semiconductors used in the simulation are the *IRF200P222* Si-MOSFETs from Infineon with a maximum drain–source voltage of $V_{\mathrm{DS}} = 200\,\mathrm{V}$ and a continuous dc current $I_{\mathrm{D}} = 182\,\mathrm{A}$. A cell capacitance of 3.1 mF is selected so that the cell voltage deviations occurring in rated operation due to energy pulsation in the phases are around 10%. The parameters of the converter configuration are summarized in Table III.

TABLE III
Simulation Parameters

	Parameter	Symbol	Value
System p.u. base values	Power	S_{r}	1 MVA
	Voltage	V_{r}	690 V
	Current	I_{r}	837 A
Main converter	IGBT volt. rating	V_{CES}	1.7 kV
	IGBT curr. rating	$I_{\mathrm{C,nom}}$	1500 A
	DC-link voltage	V_{dc}	1100 V
	Switching frequency	$f_{\mathrm{sw,mc}}$	3 kHz
CHB-VS-AF	MOSFET volt. rating	V_{DS}	200 V
	MOSFET curr. rating	I_{D}	182 A
	Cells per phase-leg	n	7
	Cell voltage	v_{C}	100 V
	Cell capacitance	C_{af}	3.1 mF
	Switching frequency	$f_{\mathrm{sw,af}}$	30 kHz
Converter-side filter	Inductance	$L_{\mathrm{f,c}}$	81 µH
	Inductance (p.u.)	$L'_{\mathrm{f,c}}$	5.3 %
Grid-side filter	Inductance	$L_{\mathrm{f,g}}$	30 µH
	Inductance (p.u.)	$L'_{\mathrm{f,g}}$	2 %
Transformer	Voltage ratio	u_{t}	1
Grid	Voltage	V_{g}	690 V
	Frequency	f_{g}	50 Hz

A. Concept of Operation

Fig. 10 shows the simulation results of the current and voltage waveforms of the main converter, CHB-VS-AF, and grid. The

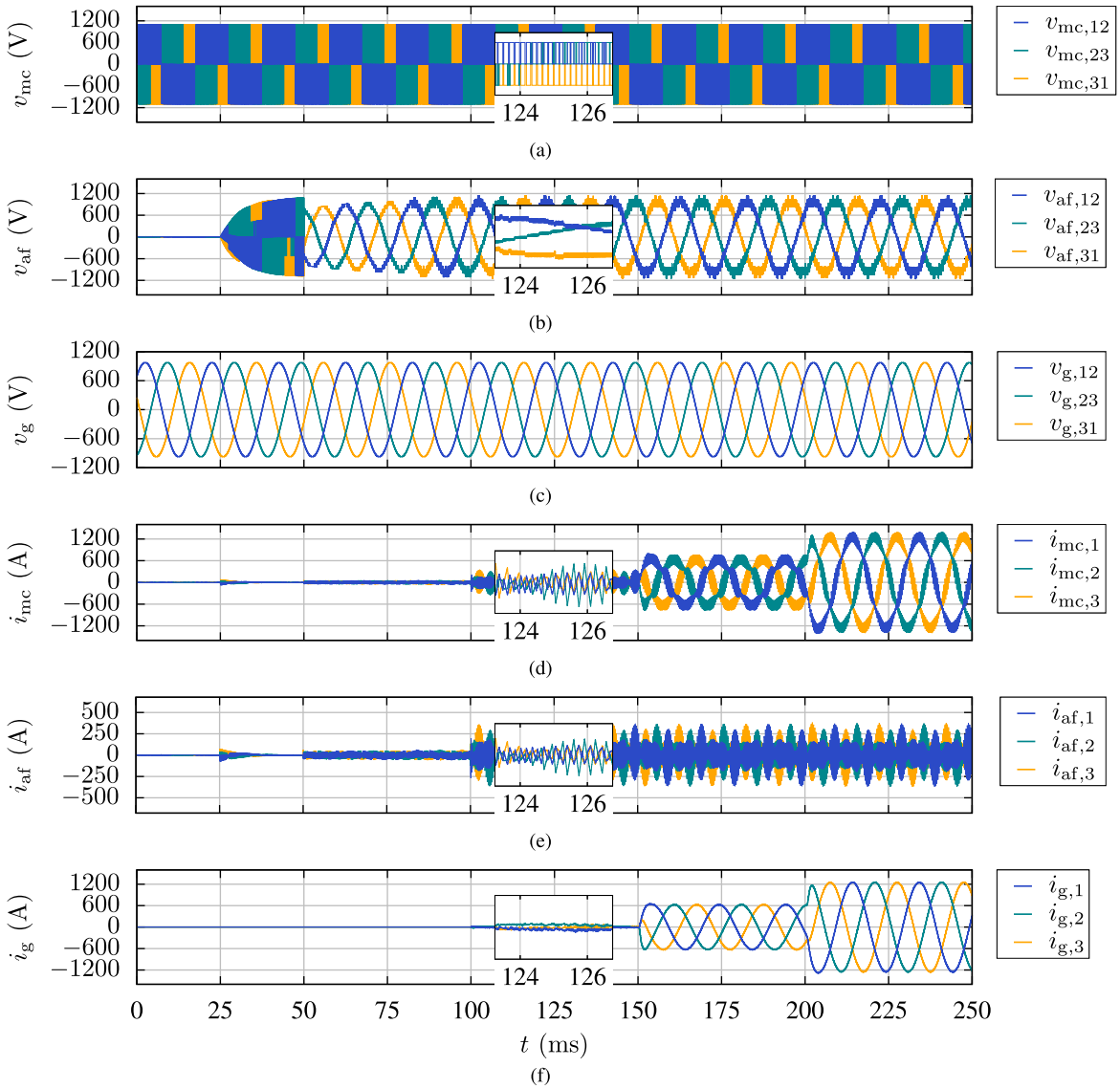

Fig. 10. Simulation results of the grid-connected multilevel converter system of precharging and step changes of the current reference. (a) Line-to-line voltages of the main converter. (b) Line-to-line voltages of the CHB-VS-AF. (c) Line-to-line grid voltages. (d) Main converter currents. (e) CHB-VS-AF currents. (f) Grid currents.

capacitive energy storage of the CHB-VS-AF is initially discharged and the converter configuration is disconnected from the grid. At $t = 25\,\mathrm{ms}$, the cell capacitances of the CHB-VS-AF are passively charged via precharging resistors, which are connected in series to the CHB-VS-AF and are not shown in Fig. 9 for better clarity. After $t = 50\,\mathrm{ms}$, the pulses of the CHB-VS-AF are enabled and an active precharging begins, for which the number of cells per phase-leg contributing to voltage generation is initially fixed at five and then increased to seven as a function of the dc-link voltages. At $t = 100\,\mathrm{ms}$, the precharging resistors are bypassed and the converter configuration is connected to the grid. Subsequently, after the converter configuration is initially operated at no-load, the active current reference changes to half the value of the rated current at $t = 150\,\mathrm{ms}$ and to the rated current at $t = 200\,\mathrm{ms}$. It can be clearly seen that the low switching frequency and small number of output voltage levels of the main converter according to Fig. 10(a) result in significant current distortions in Fig. 10(d), causing a total harmonic distortion (THD) of 11.6% at the rated output power of $1\,\mathrm{MW}$. Due to the high effective switching frequency and high number of voltage levels of the CHB-VS-AF shown in Fig. 10(b), the grid current injected by the multilevel converter system has only low harmonic distortions, resulting in a THD of only 0.4% at $1\,\mathrm{MW}$. According to the KCL in (16), the CHB-VS-AF compensates for all harmonic components of the main converter that are not included in the grid current [23], thus avoiding identification of individual harmonics or precise measurement and control of the total high-frequency current distortion.

During operation at rated power beginning at $t = 200\,\mathrm{ms}$, the main converter is operated at an average power of $1\,\mathrm{MW}$, with maximum instantaneous power values of about $1.5\,\mathrm{MW}$. The maximum instantaneous power of the CHB-VS-AF, which

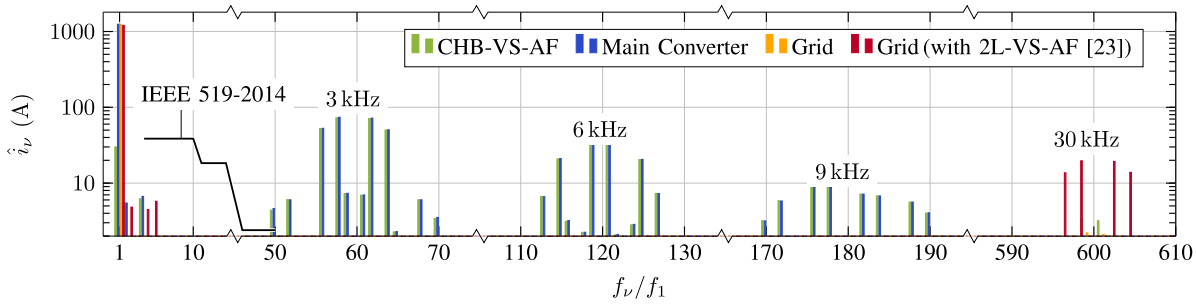

Fig. 11. Harmonic current spectra for an output power of 1 MW with the fundamental frequency $f_1 = f_g = 50\,\text{Hz}$ and the harmonic frequency $f_\nu = \nu \cdot f_1$. The THDs of the currents are 11.6% for the main converter (blue), 0.4% for the grid (yellow), and 3.3% for the grid using a 2L-VS-AF according to the work in [23] (red).

compensates only distortion reactive power to a good approximation, is 170 kVA, corresponding to about 11.3% of the maximum instantaneous power of the main converter. The ratio of the rms currents of CHB-VS-AF (104 A) and the main converter (890 A) of 11.7% is in good agreement with the power ratio. The increase in the rms current of the main converter compared to the value given in Table III is caused, in particular, by the superimposed current distortions and the loss coverage of the CHB-VS-AF. The decoupling of the conventional high-power component, the main converter, and the voltage-forming low-power component, the CHB-VS-AF, leads to a high efficiency of the converter system of $\eta = 98.3\%$, with the total losses of the main converter and CHB-VS-AF being 12.9 kW and 4.4 kW, respectively. Even taking into account filter inductance losses combined in a series equivalent resistance of 0.2% [48], the efficiency is $\eta = 98.24\%$.

B. Mitigation of Current Distortions

Since the fundamental active current required for energy control is negligible, the load current of the CHB-VS-AF in Fig. 10(e) corresponds to the current distortion of the main converter to a very good approximation. This is also evident from the harmonic current spectra at rated operation shown in Fig. 11: The presented multilevel converter configuration allows the CHB-VS-AF to compensate for the current distortions of the main converter in the carrier bands around the switching frequency of 3 kHz and its multiples (6 kHz, 9 kHz,...). Moreover, compared to the use of a 2L-VS-AF [23], the CHB-VS-AF even avoids notable grid current harmonics in the range of its switching frequency $f_{\text{sw,af}}$.

C. Limitation of the CHB-VS-AF Output Current

In Fig. 10(e), it can be seen that the control strategy limits the load current of the CHB-VS-AF to a very good approximation to current distortions of the main converter. This applies for steady-state operating points as well as transitions between no load, part-load, and rated load. This is achieved by the used prediction of the main converter current by the CHB-VS-AF described in Section III-C, which is illustrated in Fig. 12 for the operating point transitions according to Fig. 10. Therein, the fundamental current $i_{\text{mc,d}}$ measured and transformed into

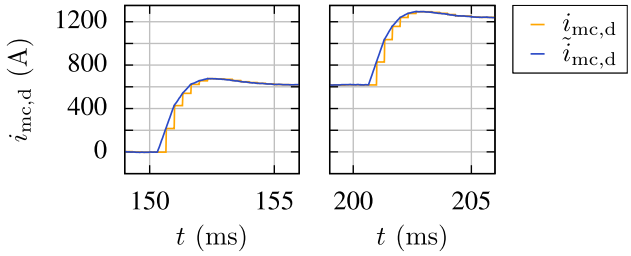

Fig. 12. Prediction of the fundamental converter current by the CHB-VS-AF for the transition between no-load, part-load, and rated operation.

dq-coordinates by the main converter with the sampling frequency $f_{\text{s,hs}} = f_{\text{sw,hs}} = 3\,\text{kHz}$ is shown in yellow. The blue waveform shows the predicted current $\tilde{i}_{\text{mc,d}}$, which is used as the reference by the grid-side current control of the CHB-VS-AF. It can be seen that the sampled current waveform can be very well determined by the prediction, and thus, a high match between the main converter current and the grid current can be achieved, resulting in a limitation of the CHB-VS-AF load current to current distortions of the main converter. This clearly illustrates the advantages of the proposed multilevel converter concept: A conventional IGBT-based main converter allows a high power rating, high robustness, and high power density of the overall converter system at competitive costs. At the same time, a parallel CHB-VS-AF leads to a high-quality output voltage at only a small share of the total power. This highlights the potential of the proposed multilevel converter configuration as an attractive alternative to conventional converters with *LCL* filters, full-SiC converters, or full-power multilevel converters with comparable harmonic performance.

D. Performance of the CHB-VS-AF Energy Control

To control the energies stored in the phases of the CHB-VS-AF, an energy control according to Section III-D is used, which avoids a costly cell power supply. Fig. 13 shows the resulting waveforms of the accumulated cell voltages in the three phases

$$v_{\text{dc,af,x}} = \sum_{m=1}^{7} v_{\text{cx},m}. \tag{22}$$

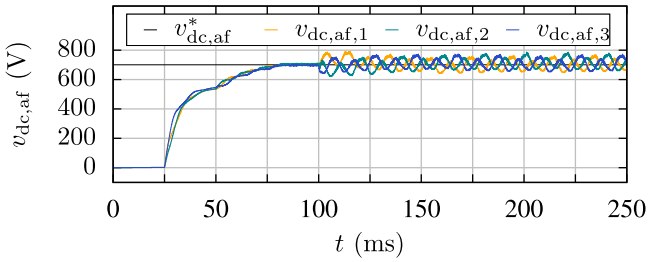

Fig. 13. Waveforms of the reference and actual dc-link voltages of the CHB-VS-AF during precharging and step changes of the current reference.

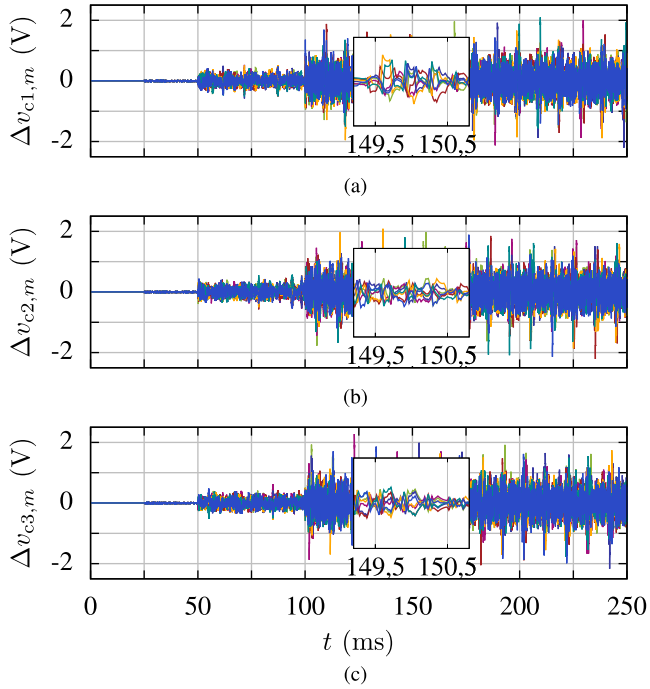

Fig. 14. Cell voltage deviation of the CHB-VS-AF. (a) Phase 1. (b) Phase 2. (c) Phase 3.

Following the passive precharging of the cells, starting at $t = 25\,\mathrm{ms}$, active precharging begins at $t = 50\,\mathrm{ms}$ by pulse enabling of the CHB-VS-AF and reduction of the number of cells contributing to voltage generation, resulting in a visibly higher slew rate of the accumulated cell voltages. After bypassing the precharging resistors and grid connection at $t = 100\,\mathrm{ms}$, significant voltage harmonics with twice the fundamental frequency of $100\,\mathrm{Hz}$ occur, resulting from the power components of the fundamental currents required for energy control and the fundamental component of the output voltage of the CHB-VS-AF derived in Section II. These voltage harmonics are also characteristic of other modular multilevel converter topologies such as the MMC [38] and the M3C [39] and are caused by the fact, that, in contrast to converter topologies with a common dc-link, the capacitive energy storage devices distributed over the three phases carry the phase currents before their harmonic components compensate for each other. Fig. 13 shows that the total energy control allows a constant sum of all cell voltages to be set, and the control for energy balancing also allows a uniform energy distribution among the phases of the CHB-VS-AF, so that the average cell voltages of a phase correspond to the reference value of $700\,\mathrm{V}$ in a very good approximation. Due to the superimposed alternating components, maximum deviations of 11.4% occur during grid operation, which, however, do not lead to any impairment of the converter behavior.

To balance the power distribution within the phases of the CHB-VS-AF, full sorting is used, where the converter cells are sorted according to their cell voltages and considered or excluded depending on the power sign of the respective phase for the voltage generation in the next sampling period. It should be noted that for voltage generation a certain number of cells are switched on statically in each sampling period and only one cell is operated with a pulsewidth modulation (PWM). The resulting voltage deviations of the cells from the average cell voltage of each phase are shown in Fig. 14, with only very slight differences between the cell voltages of a phase.

V. Comparison to Full-Power Multilevel Converters

The simulation results in Section IV show promising converter characteristics that limit the CHB-VS-AF current in steady-state and transient operations, allowing a CHB-VS-AF power share of less than 15% while achieving a high-quality 15-level output voltage of the multilevel converter system. For further potential analysis, this section provides a comparison to full-power multilevel converters with respect to other important criteria such as the energy pulsation as well as the installed semiconductor power and its influence on the achievable power rating. For better distinction, the presented multilevel converter system is referred to as the hybrid converter in this section.

A. Energy Pulsation

Since the load current of the CHB-VS-AF corresponds to a very good approximation to the current ripple of the main converter, the currents $\boldsymbol{i_{\mathrm{af}}} = [i_{\mathrm{af},1}\ i_{\mathrm{af},2}\ i_{\mathrm{af},3}]^{\mathrm{T}}$ have much smaller current time areas compared to a full-power multilevel converter designed for the same performance characteristics (see Table III), which would carry a fundamental current of several hundred amperes in each phase. Fig. 15 shows the peak-to-peak energy pulsations resulting from the combination of CHB-VS-AF output voltage $\boldsymbol{v}_{\mathrm{af}}$ and CHB-VS-AF output current $\boldsymbol{i}_{\mathrm{af}}$ (solid, blue) and CHB-VS-AF output voltage $\boldsymbol{v}_{\mathrm{af}}$ and grid current $\boldsymbol{i}_{\mathbf{g}}$ (solid, yellow) as a function of the current fed into the grid. It is seen that the energy pulsation caused by the output current of the CHB-VS-AF in the proposed converter configuration has approximately no dependence on the grid current due to the low dependence of the main converter current ripple on the modulation index. If, on the other hand, a full-power CHB-VSC were to supply the grid current in this application, the resulting energy pulsation shown in yellow would, as expected, be very dependent on the grid current and would already be many times the energy pulsation of the CHB-VS-AF shown in blue at low output currents, as can be seen in Fig. 16. The same applies to the application of the proposed converter configuration in the

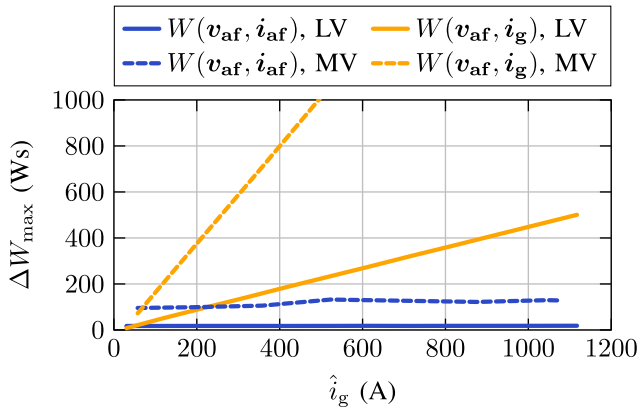

Fig. 15. Peak-to-peak energy pulsations as a function of the grid current: The results for the combination of a 2L-VSC and CHB-VS-AF (see Table III) are shown for the energy pulsation resulting from $\boldsymbol{v}_{\mathrm{af}}$ and $\boldsymbol{i}_{\mathrm{af}}$ in solid blue and $\boldsymbol{v}_{\mathrm{af}}$ and $\boldsymbol{i}_{\mathbf{g}}$ in solid yellow. The results for the combination of a 3L-NPC-VSC and CHB-VS-AF [25] are shown for the energy pulsation resulting from $\boldsymbol{v}_{\mathrm{af}}$ and $\boldsymbol{i}_{\mathrm{af}}$ in dashed blue and $\boldsymbol{v}_{\mathrm{af}}$ and $\boldsymbol{i}_{\mathbf{g}}$ in dashed yellow.

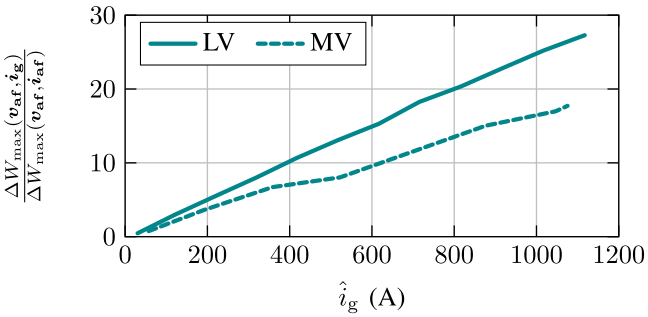

Fig. 16. Ratio of energy pulsations caused by $\boldsymbol{v}_{\mathrm{af}}$ in combination with $\boldsymbol{i}_{\mathrm{af}}$ and $\boldsymbol{i}_{\mathbf{g}}$ for the LV and MV use cases.

MV level: By combining a 3L-NPC-VSC with a CHB-VS-AF for application in the lower MV grid according to the work in [25] (3.3 kV, 5 MVA), the energy pulsation can also be significantly reduced compared to a full-power multilevel converter, as shown in Figs. 15 and 16. This allows the CHB-VS-AF used in the MV converter in [25] to have capacitive stored energy of only $0.41\ \frac{\mathrm{Ws}}{\mathrm{kVA}}$ related to the output power. Considering relative energy stored in the dc-link of the 3L-NPC-VSC used as the main converter of $5.2\ \frac{\mathrm{Ws}}{\mathrm{kVA}}$ [49], [50], [51], [52], the total stored energy per output power in the proposed converter configuration is $5.61\ \frac{\mathrm{Ws}}{\mathrm{kVA}}$. In comparison, a full-power MMC designed in [53] and [54] for use in a similar voltage and power range (4.16 kV, 4.3 MVA) has a stored energy of about $13\ \frac{\mathrm{Ws}}{\mathrm{kVA}}$, even when optimized internal currents are applied.

B. Installed Semiconductor Power and Power Rating

Another important advantage of the proposed multilevel converter configuration is that it only slightly increases the installed semiconductor power [25], [49], [53] compared to two- and three-level main converters with *LCL* filters. Considering the CHB-VS-AF investigated in Section IV with the converter characteristics given in Table III, the total installed semiconductor power is 26 related to the output power of 1 MVA (2L-VSC: 22.95 MVA; CHB-VS-AF: 3.05 MVA, corresponding to a 13.3% increase in installed semiconductor power which, according to Section IV, is in good approximation with the current ratio of CHB-VS-AF and 2L-VSC). The MV converter in [25] has a total installed semiconductor power of 25.3 related to the output power of 5 MVA (3L-NPC-VSC: 113.4 MVA; CHB-VS-AF: 13 MVA, corresponding to an 11.4% increase in installed semiconductor power). In comparison, the MMC designed in [53] and [54] for a similar voltage and power rating has an installed semiconductor power of 40 related to the output power of 4.3 MVA.

TABLE IV
COMPARISON OF THE INSTALLED SEMICONDUCTOR POWER AT THE SAME POWER RATING AND THE ACHIEVABLE POWER RATING WITH MATCHED INSTALLED SEMICONDUCTOR POWER

	Topology	Semiconductor power at equal power rating	Power rating at equal semiconductor power
LV	2L-VSC with 15L-CHB-VS-AF	26 MVA 100 %	1 MVA 100 %
	3L-NPC-VSC	41.4 MVA 159 %	628 kVA 63 %
	5L-(A)NPC-VSC	53.2 MVA 205 %	488 kVA 49 %
	15L-MMC	70.9 MVA 273 %	365 kVA 37 %
MV	3L-NPC-VSC with 9L-CHB-VS-AF	126.4 MVA 100 %	5 MVA 100 %
	3L-NPC-VSC	113.4 MVA 90 %	5.58 MVA 112 %
	5L-(A)NPC-VSC	145.8 MVA 115 %	4.33 MVA 87 %
	9L-MMC	194.4 MVA 154 %	3.25 MVA 65 %

The results of the comparison to full-power multilevel converters of the same power or the same installed semiconductor power are shown in Table IV. This is carried out in the LV and MV range for the above-mentioned hybrid LV and MV converters and the 3L-NPC-VSC, the five-level neutral point clamped VSC and five-level active neutral point clamped VSC [55], [56], [57], and an MMC with the same number of output voltage levels as the hybrid converter presented. It is noted that NPC VSCs with more than five voltage levels have significant disadvantages with regard to practical implementation, such as the difficulty of the low-inductance design of all commutation paths and in the voltage balancing of the dc-link capacitors [49] and are, therefore, not considered here. The designs for a power rating of 1 MVA in the LV range and 5 MVA in the MV range are made with scaled semiconductor data, calculating the commutation voltages of the semiconductors for all topologies and determining their blocking voltage, which is used to calculate the installed semiconductor power, while maintaining the voltage utilization factor [49], [57] of the respective hybrid converter. To compare the converter topologies for an equal installed semiconductor power, the designs maintain the voltage ratings of the semiconductors while adjusting the current rating so that the resulting

installed semiconductor power is equal to that of the respective hybrid converter.

In the LV range, taking into account the assumptions made, the results in Table IV show that by using a high-power 2L-VSC as main converter, a rated power of 1 MVA can be achieved by the hybrid converter with a significantly reduced installed semiconductor power compared to full-power multilevel converters. The three- and five-level (A)NPC-VSC topologies require more than 1.5 and 2 times the installed semiconductor power while having only one-fifth and one-third the output voltage levels of the hybrid converter, respectively, which substantially impacts the THD of the output voltage. A 15L-MMC, whose output voltage quality is comparable to that of the hybrid converter, requires 2.7 times the installed semiconductor power to achieve a rated power of 1 MVA. As expected, equalizing the installed semiconductor power requires a significant reduction in the power rating. For the three- and five-level NPC-VSC topologies, this results in power ratings of 628 kVA and 488 kVA while for the 15L-MMC, a reduction to 365 kVA is required.

In the MV range, the differences are smaller than in the LV range due to the use of a 3L-NPC-VSC as main converter in the hybrid converter. While, as expected, to achieve an output power of 5 MVA, a reduction of 10% in the total installed semiconductor power can be achieved when omitting the CHB-VS-AF, which is, however, accompanied by a significant reduction in the number of output voltage levels of the converter system, the 5L-(A)NPC-VSC topologies as well as a 9L-MMC, nevertheless, require installed semiconductor powers increased by 15% and 54%, respectively. Considering the assumptions made earlier, equalizing the installed semiconductor power ratings results in a 12% increase in power rating for the 3L-NPC-VSC while reducing it by 13% for the 5L-(A)NPC-VSC topologies and by approximately one third for the 9L-MMC. Based on the results, it is clear that in terms of energy conversion between a dc side and a three-phase ac side, the presented hybrid converter topology enables the design of multilevel converters with a high number of output voltage levels while significantly reducing the required installed semiconductor power compared to conventional full-power multilevel converters. This is made possible, in particular, by the control decoupling of the conventional high-power component, the main converter, and the voltage-forming low-power component, the CHB-VS-AF, described in Sections II and III.

VI. Experimental Results

This section describes the experimental verification of the proposed grid-connected multilevel converter system. The test setup used for the experimental verification corresponds to the converter configuration shown in Fig. 9. It uses the two-level main converter platform shown in Fig. 17, which includes a dc-link with a capacitance of 200 µF, the 1.2 kV Si-IGBT power module *FS75R12KT4_B15* from Infineon with a continuous dc current of 75 A, gate drivers, and a *MAX-10*-based FPGA unit. Three of the CHB-VS-AF phase-leg modules shown in Fig. 18 are used as the voltage-forming converter, the design of which can be found in [27]. Every phase-leg module contains a *MAX-10*-based FPGA unit and $n = 12$ cascaded full-bridge cells, each using four *SQJQ960EL* Si-MOSFETs from Vishay with a maximum drain–source blocking voltage of 60 V and a maximum continuous dc current of 36 A, gate drivers as well as cell capacitors with a capacitance of 6 mF. Unlike the two-level main converter in Fig. 17, the phase-leg modules of the CHB-VS-AF have no dc power supply, as it is designed to provide reactive power only. The parameters of the test setup used for the experimental verification can be found in Table V.

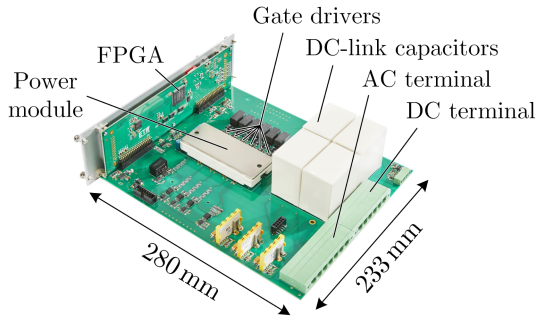

Fig. 17. Two-level main converter with Si-IGBTs.

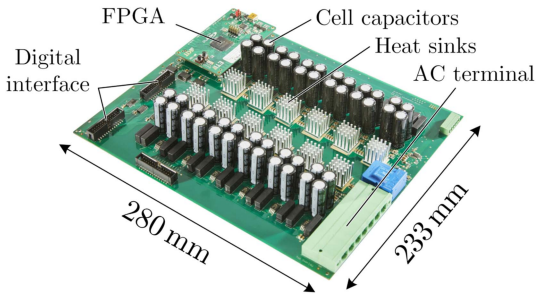

Fig. 18. 25L-CHB-AF phase-leg module with Si-MOSFETs.

TABLE V
Parameters of the Test Setup

	Parameter	Symbol	Value
System p.u. base values	Power	S_r	10 kVA
	Voltage	V_r	200 V
	Current	I_r	28.3 A
Main converter	IGBT volt. rating	V_CES	1.2 kV
	IGBT curr. rating	$I_\mathrm{C,nom}$	75 A
	DC-link voltage	V_dc	350 V
	DC-link capacitance	C_mc	200 µF
	Switching frequency	$f_\mathrm{sw,mc}$	3 kHz
CHB-VS-AF	MOSFET volt. rat.	V_DS	60 V
	MOSFET curr. rat.	I_D	36 A
	Cells per phase-leg	n	12
	Cell voltage	V_C	15 V
	Cell capacitance	C_af	6 mF
	Switching frequency	$f_\mathrm{sw,af}$	12 kHz
Filter Inductors	Inductance	$L_\mathrm{f,c/g}$	1 mH
	Inductance (p.u.)	$L'_\mathrm{f,c/g}$	7.9 %
	Resistance	$R_\mathrm{f,c/g}$	48 mΩ
Transformer	Voltage ratio	u_t	0.5
Grid	Voltage	V_g	400 V
	Frequency	f_g	50 Hz

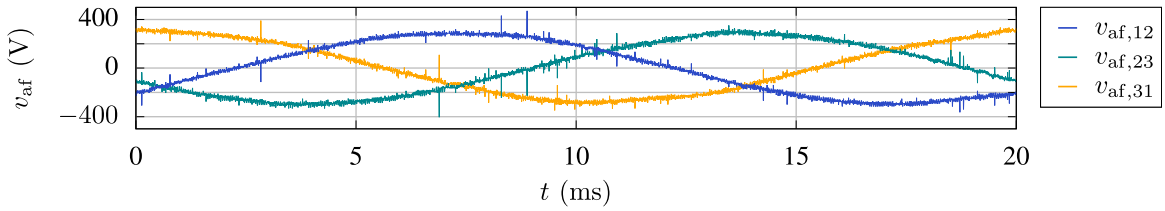

Fig. 19. Measured waveforms of the CHB-VS-AF line-to-line output voltages corresponding to the output voltages of the multilevel converter system.

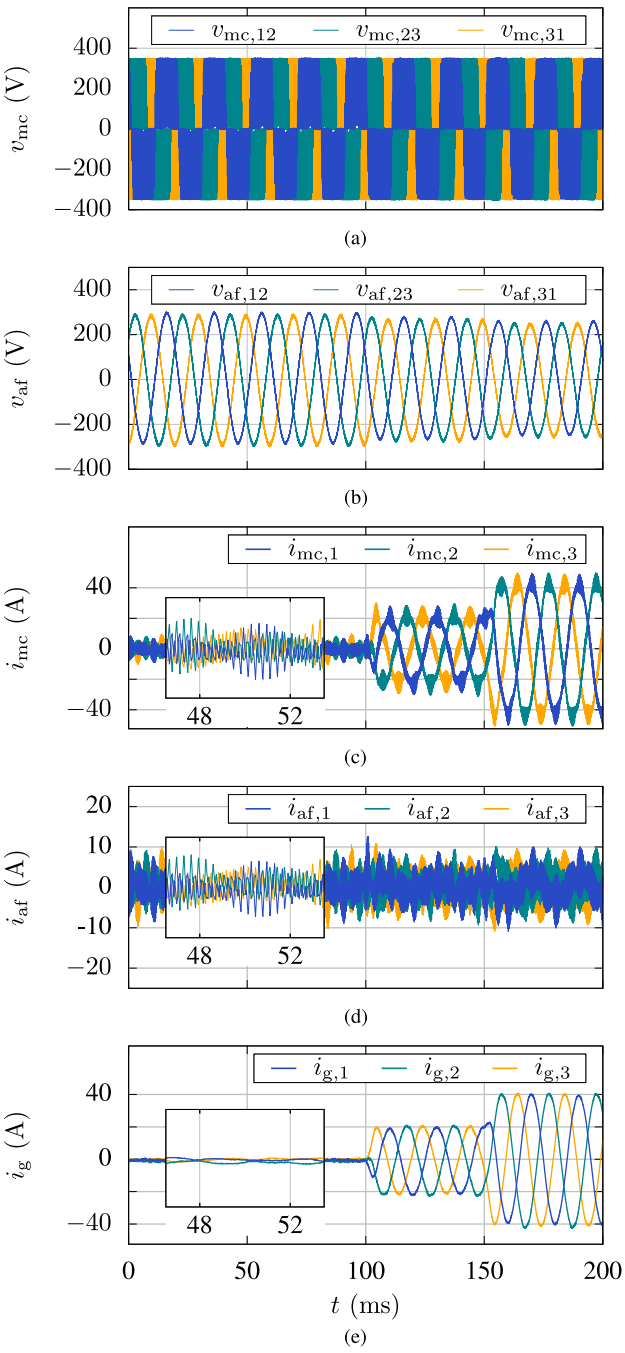

Fig. 20. Experimental results of the grid-connected multilevel converter system for step changes of the current reference. (a) Line-to-line voltages of the main converter. (b) Line-to-line voltages of the CHB-VS-AF. (c) Main converter currents. (d) CHB-VS-AF currents. (e) Grid currents.

The experimental results are shown in Fig. 20. After the converter configuration is initially operated on the grid at no-load, the active grid current reference initially increases to half the value of the rated current at $t = 100\,\mathrm{ms}$ and to the rated current at $t = 150\,\mathrm{ms}$. In Fig. 20(c), it can be seen that the main converter causes significant current distortion due to its low switching frequency, resulting in a THD of 21% for an output power of 5 kVA. In contrast, due to the quadruple switching frequency and multilevel voltage of the 25L-CHB-VS-AF in Fig. 20(b), which is shown in higher resolution in Fig. 19, a nearly sinusoidal current with a THD of only 2.2% is injected into the grid according to Fig. 20(e). In very good agreement with the simulation results, the fundamental current required for loss coverage of the 25L-CHB-VS-AF is negligible, so that the CHB-VS-AF current in Fig. 20(d) corresponds in good approximation to the harmonic currents of the main converter in steady-state and transient operation. This is also illustrated by the current spectra shown in Fig. 21. It can be seen that the 25L-CHB-VS-AF significantly reduces the current distortions in the carrier frequency range of 3 kHz and, moreover, approximately eliminates them in the double and triple carrier frequency range (6 kHz and 9 kHz). As expected and in close agreement with the simulation results, a significant reduction of the harmonic currents in the range around the 25L-CHB-VS-AF switching frequency of $f_{\mathrm{sw,af}} = 12\,\mathrm{kHz}$ to below 0.1 A can be achieved compared to the current spectra when using a 2L-VS-AF according to the work in [23] (red in Fig. 21).

The experimental results once again demonstrate the advantages of the unique combination of conventional and modern power electronics technologies in the proposed converter system: While the complex CHB-VS-AF, with a load current limited to below 15 A even in transient operation according to Fig. 20(d) and, therefore, with low energy pulsation in the cell capacitors, produces the nearly sinusoidal output voltage in Fig. 19, a conventional two-level main converter supplies all the active power exchanged with the grid. Since the latter operates with a switching frequency of 3 kHz according to Table V—a frequency widely used in high-power applications—the CHB-VS-AF shown in Fig. 18 could instead be used with a much more powerful two-level main converter without changing its specifications. In addition, the CHB-VS-AF could be extended for use at a higher voltage level by increasing the number of cells per phase-leg, e.g., by connecting multiple phase-leg modules in series. This high degree of scalability and modularity makes the proposed multilevel converter system easily adaptable to a wide range of grid applications and requirements.

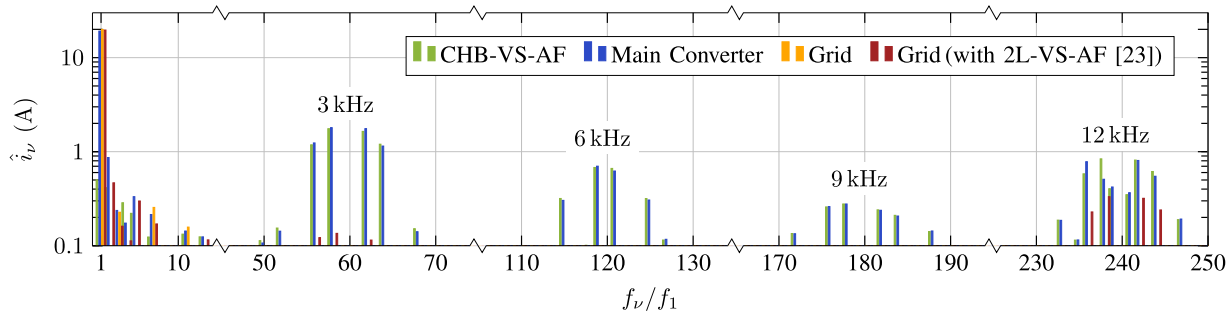

Fig. 21. Harmonic current spectra for an output power of 5 kVA with the fundamental frequency $f_1 = f_g = 50$ Hz and the harmonic frequency $f_\nu = \nu \cdot f_1$. The THDs of the currents are 21% for the main converter (blue), 2.2% for the grid (yellow), and 4% for the grid using a 2L-VS-AF according to the work in [23] (red).

VII. Conclusion

This article presents a novel multilevel converter system composed of a conventional main converter and a parallel CHB-VS-AF with low energy pulsation for high-power grid applications. As shown by simulation and experimental results, decoupling of the high-power unit (main converter) and the voltage-forming unit (CHB-VS-AF) can be achieved by the proposed concept of operation, which is based on the presented modeling and control design. By using a conventional IGBT-based two-level or three-level converter as the high-power main converter and a low-power CHB-VS-AF, it is possible to simultaneously achieve a high power rating and high-quality output voltage of the converter system while the increase in total installed semiconductor caused by the additional voltage-forming converter is below 15%. Since the output current of the latter corresponds in very good approximation to the current ripple of the main converter, whose frequencies are in the range around the main converter carrier frequency and its integer multiples, only very low energy pulsations occur in the phases of the CHB-VS-AF. As a result, the proposed multilevel converter system is an attractive alternative to full-power multilevel converters with distributed dc-links, where limiting the energy pulsation caused by high fundamental frequency currents in the phases may require significant internal currents and impact the converter design. Compared to multilevel converter topologies with common dc-links, a significant reduction in the required installed semiconductor power can be achieved for the same power rating, while conversely, a significantly higher output power results when the installed semiconductor power is equal. Further advantages are given by the high modularity and scalability, which makes the multilevel converter easily adaptable to the requirements of a wide range of applications. Therefore, it has a high potential to contribute to the solution of challenges such as power quality or power-electronics-based grid forming, which arise with the increasing penetration of power converters in modern grids.

Appendix

Clarke transformation using the matrix $\mathbf{C}$

$$\begin{bmatrix} x_\alpha \\ x_\beta \\ x_0 \end{bmatrix} = \mathbf{C} \cdot \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} = \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ 0 & \frac{1}{\sqrt{3}} & -\frac{1}{\sqrt{3}} \\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3} \end{bmatrix} \cdot \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix}. \quad (23)$$

Inverse Clarke transformation using the matrix $\mathbf{C^{-1}}$

$$\begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} = \mathbf{C^{-1}} \cdot \begin{bmatrix} x_\alpha \\ x_\beta \\ x_0 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & 1 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & 1 \end{bmatrix} \cdot \begin{bmatrix} x_\alpha \\ x_\beta \\ x_0 \end{bmatrix}. \quad (24)$$

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