A 95.4% Hybrid Always-Dual-Path Recursive Step-Down Converter Using Adaptive Switching Level Control With 288 mΩ Large-DCR Inductor

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Abstract*—This article proposes a hybrid always-dual-path recursive (ADPR) step-down converter to achieve high efficiency using a small-volume inductor with large dc resistance (DCR). The ADPR step-down converter utilizes only low-voltage transistors (1.5 or 3.3 V) for power switches. The converter has adopted adaptive switching level control, which includes adaptive mode transition (AMT) and adaptive duty modulation (ADM), based on one dual-flipped saw-tooth waveform. AMT and ADM enable a wide range operation and ensure flying capacitor charge balance while leading to higher efficiency. In addition, a complementary switch guarantees the reliable operation at lower input voltage to 2.8 V. The 130-nm prototype converter used a small-volume 4.7 μH inductor with 288 mΩ DCR, a 10 μF output capacitor, and two 4.7 μF flying capacitors to verify highly efficient always-dual-path recursive operation. The measurement results show that the ADPR step-down converter can be suitable for converting Li-ion battery (2.8–4.2 V) to 0.7–1.1 V while the ratio of the inductor current over the load current (I_{LOAD}) can be set between 0.42 and 0.66 at all range. The peak efficiency was measured up to 95.4% at $V_{\mathrm{IN}} =$ 3.7 V and $I_{\mathrm{LOAD}} =$ 75 mA. When $V_{\mathrm{OUT}} =$ 1 V and $I_{\mathrm{LOAD}} =$ 100 mA, the efficiencies were higher than 92.9% at whole input voltage ranges, ensuring small efficiency variation of 1.6%.

***Index Terms*—Always-dual-path recursive, buck converter, hybrid multilevel converter, large dc resistance (DCR) inductor, stacked power stage.**

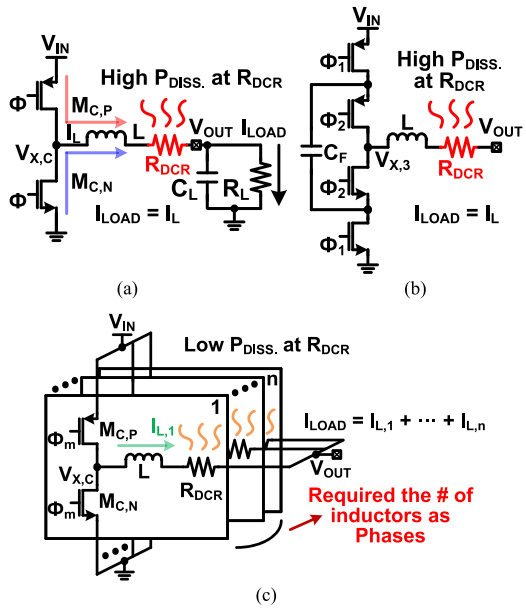

Fig. 1. Conceptual topologies of (a) a conventional two-level buck converter, (b) a three-level buck converter, and (c) a multiphase buck converter.

I. Introduction

OPERATION voltages for mobile and wearable systems have been decreased to around 1 V as the CMOS process scaled down, while they are powered by higher voltages such as Li-ion battery voltage of 2.8–4.2 V [1], [2], [3]. For those systems, a step-down converter with low voltage conversion ratio (VCR $= V_{\mathrm{OUT}}/V_{\mathrm{IN}}$) is highly required [4]. The power efficiency is also an important factor to maximize the battery usage time. Since the sizes of mobile and wearable devices are getting smaller and thinner, the external components (e.g., inductor) are tightly limited to have low height (e.g., <1 mm) and small volume [5]. However, small-volume inductors have noticeable issues such as large dc resistance (DCR) up to several hundred milliohms. The large DCR increases conduction loss, which is one of the major factors to degrade the power efficiency and leads to heat dissipation.

The power consumption in the step-down converters mainly results from conduction and switching losses. In conventional buck converters (CBC) in Fig. 1(a) [6], [7], [8], [9], [10], the conduction losses can be expressed as [11]

$$P_{\mathrm{LOSS},COND} = [D \times I_{L,\mathrm{rms}}^2 \times R_{\mathrm{ON},P}] + [(1-D) \times I_{L,\mathrm{rms}}^2 \times R_{\mathrm{ON},N}] + [I_{L,\mathrm{rms}}^2 \times R_{\mathrm{DCR}}] \quad (1)$$

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where D is duty ratio, $R_{\text{ON},P}$ and $R_{\text{ON},N}$ are the ON-resistances of $\text{M}_{\text{C,P}}$ and $\text{M}_{\text{C,N}}$, respectively, and $I_{L,\text{rms}}$ is the root-mean-square (rms) current of the inductor. The $I_{L,\text{rms}}$ can be expressed as

$$I_{L,\text{rms}} = \sqrt{I_{L,\text{dc}}^2 + \Delta I_L^2/12} \tag{2}$$

where $I_{L,\text{dc}}$ is an average dc current of the inductor, and ΔI_L is an inductor current ripple. The switching losses at power switches are affected by parasitic gate capacitance V_{IN}, and switching frequency, which can be expressed as

$$P_{\text{LOSS},SW} = (C_{G,N} + C_{G,P}) \times V_{\text{IN}}^2 \times f_{SW} \tag{3}$$

where $C_{G,N}$ and $C_{G,P}$ are the gate capacitance of $\text{M}_{\text{C,N}}$ and $\text{M}_{\text{C,P}}$, respectively, and f_{SW} is the switching frequency.

For higher efficiency, total P_{LOSS} should be decreased. In (1) and (3), $P_{\text{LOSS},COND}$ and $P_{\text{LOSS},SW}$ have a trade-off relationship due to ON-resistances and gate capacitances, which depend on the size of power switches. Thus, it limits to improve the efficiency with controlling switch size. The alternative solution can be found from (2). First, if $I_{L,\text{dc}}$ or ΔI_L decrease, $I_{L,\text{rms}}$ also decreases leading to reduction in $P_{\text{LOSS},COND}$ without affecting the other losses. Second, power switches can compose of low-voltage transistors (e.g., 1.5 or 3.3 V). The low-voltage transistors have low gate capacitances and are driven by low gate driving voltage, which reduce $P_{\text{LOSS},SW}$. This also enables to use the cost-effective low-voltage process for battery-powered integrated converters.

In switched-inductor converters, CBC has the identical inductor current (I_L) to I_{LOAD}. Thus, it suffers from large $I_{L,\text{rms}}$, which leads to high power dissipation at R_{DCR}. Multilevel buck converters can decrease ΔI_L by reducing the switching voltage level at $V_{X,3}$ with an additional flying capacitor (C_F) like Fig. 1(b) [12], [13], [14], [15], [16], [17], [18], [19], but whole I_{LOAD} still flows through the inductor. To address this issue, several topologies to decrease I_L and $I_{L,\text{rms}}$ such as multiphase buck converters (MPBC) and dual-path hybrid converter (DPHC) have been reported. Although MPBC divides I_L, it needs the same number of inductors as the phases of MPBC, as shown in Fig. 1(c) [20], [21], [22], [23]. The multiple inductors increase the size and cost of the system while they still suffer from inherent R_{DCR}. Another solution is DPHC which transfers I_{LOAD} through both an inductor and a capacitor in parallel, as shown in Fig. 2(a) [5], [24], [25], [26], [27], [28], [29], [30]. External capacitors (e.g., surface mount device) have smaller series resistance (R_{ESR}) and lower price than inductors. Thus, DPHC divides $I_{L,\text{dc}}$ with capacitors to minimize conduction loss by R_{DCR}. The DPHC in [5] shows improved efficiencies than CBC up to 3.95% but I_L/I_{LOAD} is always higher than 0.7 and become worse at low VCR. For example, I_L/I_{LOAD} becomes 0.88 at VCR = 0.24, which means most load current flows through inductor resulting in large conduction loss. As more reduced I_L/I_{LOAD} topologies, the DPHC in [25] has I_L/I_{LOAD} of 0.5 but low-voltage transistors are not available. Other DPHCs with lower I_L/I_{LOAD} in [26] and [27] have the ranges of 0.4–0.71 or 0.4–0.65, respectively. However, V_{IN} ranges of the above

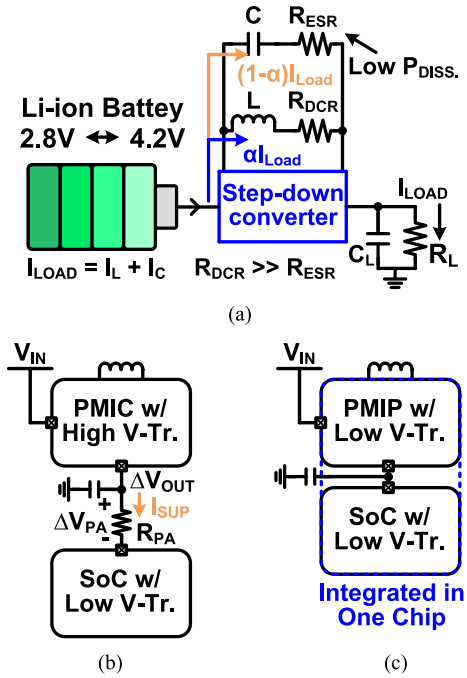


Fig. 2. (a) Conceptual diagram of the dual-path hybrid converter and the SoC powered (b) by an additional PMIC chip, and (c) an integrated PMIP.

DPHCs are still less compatible for the Li-ion battery [5], [25], [26], [27].

Power management ICs (PMIC) supplied by batteries require high-voltage process ($\geq$5 V), so they are typically placed as a separate chip as Fig. 2(b). However, the separate PMIC chip results in larger supply voltage ripples ($\Delta V_{\text{OUT}} + \Delta V_{PA}$) to SoCs and efficiency reduction due to parasitic resistance of PCB lines (R_{PA}) [29]. To solve these issues, a power management IP (PMIP), which is integrated on the low-voltage SoC chip, is highly desired by adopting high-voltage tolerant converters.

This article proposes the hybrid always-dual-path recursive (ADPR) step-down converter that can not only reduce $I_{L,\text{dc}}$ with always-dual-path topology but also minimize ΔI_L using recursive switching control (RSC). RSC leads to the lower switching voltage level across the inductor compared to three-level converters, while enabling high-voltage-tolerant always-dual-path operation for achieving higher power efficiency. This article is an extended version of [30], and the following contents are added: 1) theoretical analysis of $V_{\text{OUT}}/V_{\text{IN}}$ and I_L/I_{LOAD}; 2) detailed circuit implementations including the complementary switch; 3) derivation about how to set the duty cycle depending on the operation mode; 4) additional measurements for load transient response in both modes and output voltage ripples; 5) additional measured efficiencies and comparison with 0402 and 0805 sized flying capacitors; 6) analysis and comparison of the inductor DCR values according to inductor volumes.

The rest of this article is organized as follows. Section II explains the ADPR step-down converter, and Section III describes its circuit details. Measurement results and discussions with state-of-the- arts are presented in Section IV. Finally, Section V concludes this article.

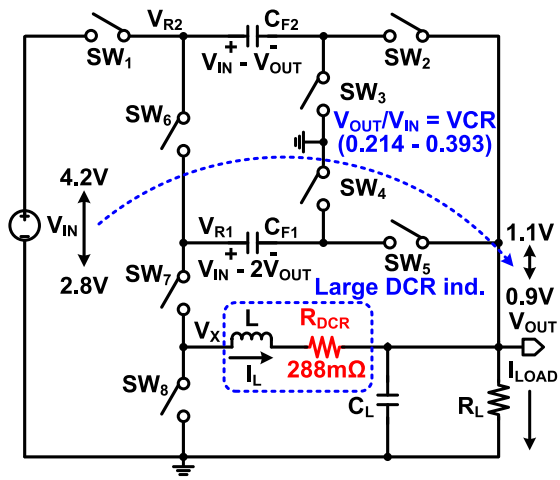


Fig. 3. Conceptual diagram of the proposed hybrid ADPR step-down converter.

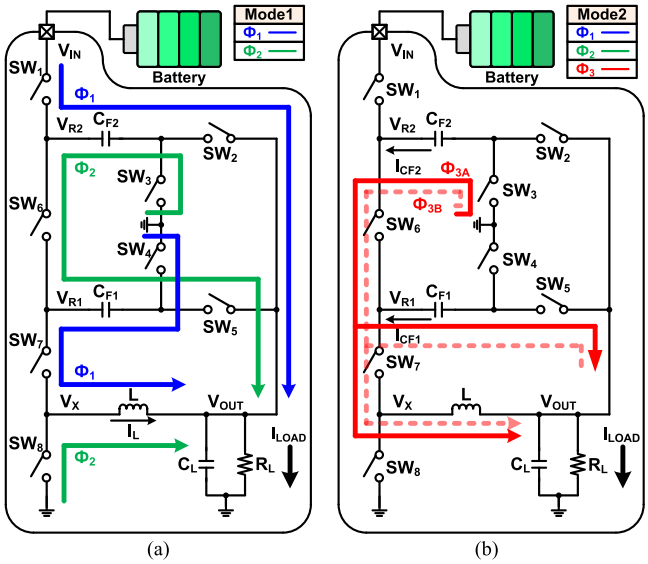


Fig. 4. Operation principles of the proposed ADPR step-down converter at (a) mode1 and (b) mode2.

II. Proposed Hybrid Always-Dual-Path Recursive Converter

Fig. 3 shows the conceptual diagram of the proposed high-voltage-tolerant ADPR step-down converter that consists of power switches ($SW_{1\text{-}8}$) with low-voltage transistors (1.5 V or 3.3 V transistors), two flying capacitors (C_{F1} and C_{F2}), one small-volume inductor (L), and one output capacitor (C_L). The proposed converter has two operation modes (mode1 and mode2) depending on V_{IN}. In both modes, C_{F1} and C_{F2} are automatically self-balanced to V_{IN} - 2 V_{OUT} and V_{IN} - V_{OUT}, respectively. Two modes also enable a wide input range operation and guarantee sufficient self-balancing time for C_{F1} and C_{F2} as the duty ratio (D) varies. Mode change schemes are mostly adopted to have wide range operation [25], [26]. Figs. 4 and 5 depict the operation sequences along with VCR, I_L/I_{LOAD}, and duty ratio definition.

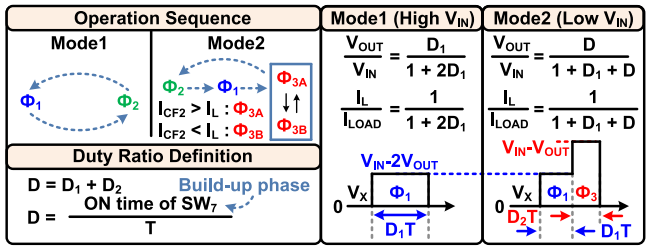


Fig. 5. Operation sequence and analysis of mode1 and mode2.

The overall block diagram of the proposed ADPR step-down converter with high-voltage tolerant power stages, which can operate at high V_{IN} of a Li-ion battery range, is on Fig. 6. M_{L1}–M_{L5} (1.5 V transistors) and M_{H1}–M_{H4} (3.3 V transistors) are used as power switches. The high-voltage tolerant power stages need to be designed with the consideration of voltage stress for power transistors, which maintains lower than break down voltage. An adaptive pulse gate controller (APGC) generates the gate logic signals (S_{L1}–S_{L5} and S_{H1}–S_{H4}) for both modes by utilizing dual-flipped saw-tooth generator (DFSG) outputs (V_{RP} and V_{RN}) and type-3 compensator output (V_E). The mode selector generates timing signals (V_{TAC} and V_{TB}) with using Q and QB from APGC. The timing signals play key roles to adaptively determine the operation mode and duty ratio. V_{LOW} ($=1$ V) and L_{VDD} ($=2.2$–2.5 V) are supplied by LDOs for the controllers as well as gate drivers for $M_{L2\text{-}5}$ and M_{H4}. The details will be explained in the sections including operation principle, adaptive mode transition (AMT), and adaptive duty modulation (ADM).

A. Mode1 Operation Principle

Fig. 4(a) shows the mode1 operation of the ADPR converter for higher V_{IN} levels. It repeats two phases Φ_1 ($=D_1T$) and Φ_2, and V_X becomes V_{IN} - $2V_{OUT}$ and 0, respectively, as depicted in Fig. 5. In Φ_1, $SW_{1,2}$ are closed for a capacitor (C_{F2}) path, SW_4 and SW_7 are closed for build-up with C_{F1}, and the other switches are open. C_{F2} is self-balanced to V_{IN} - V_{OUT}, flowing the current to the load in parallel with the inductor.

The other phase Φ_2 has the opposite current flow through C_{F1} and C_{F2} for capacitor charge balance. In Φ_2, $SW_{3,56}$ are closed for capacitor (C_{F1} and C_{F2} in series connection) paths, SW_8 are closed for free-wheeling, and the other switches are open. Thus, V_X is 0 V, and C_{F1} is self-balanced to V_{IN} - $2V_{OUT}$. C_{F1} forms the dual path in Φ_2 as C_{F2} does in Φ_1. It is noticeable that the series-connected switches for each current path in $\Phi_{1,2}$ are one to three, which is similar numbers of switches to three or four level buck converters.

During each phase, C_{F1} and C_{F2} are charged in a recursive way by subtracting V_{OUT} from V_{IN} - V_{OUT} and V_{IN}, respectively. Then, the switching voltage at V_X, 0 to V_{IN} - $2V_{OUT}$, are mostly lower than $V_{IN}/2$, leading to smaller ΔI_L and rms loss. RSC also ensures that the inductor and the flying capacitors

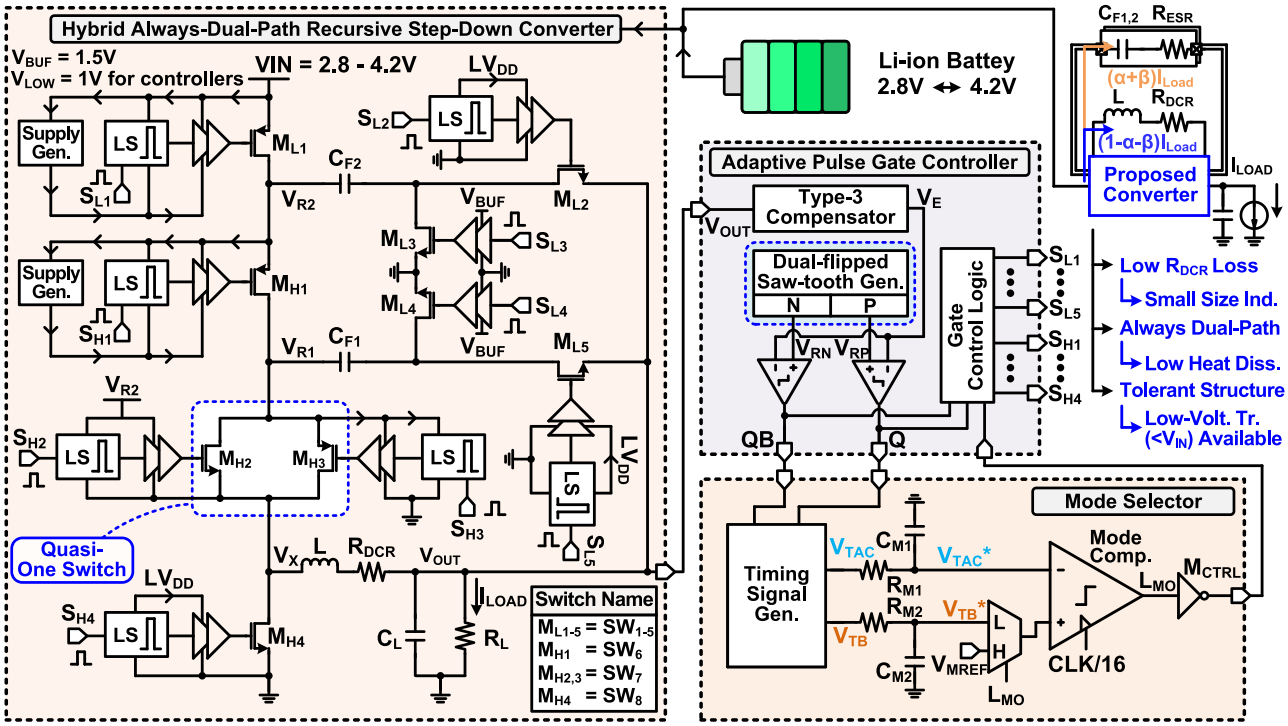


Fig. 6. Overall system diagram of the proposed ADPR converter with emphasis on the high-voltage tolerant power stages.

are connected in parallel from V_{IN} to V_{OUT} for both phases, enabling highly efficient always-dual-path operation.

To analyze VCR ($=M$), the voltage-second balance is applied to the inductor as

$$D_1(V_{\mathrm{IN}} - 2V_{\mathrm{OUT}} - V_{\mathrm{OUT}}) + (1 - D_1)\,(-\ V_{\mathrm{OUT}}) = 0. \quad (4)$$

Then, (4) can be rearranged to

$$M_1 = \frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}}} = \frac{D_1}{1 + 2D_1} \quad (5)$$

where M_1 is the conversion ratio at mode1, V_{IN} is the input voltage, V_{OUT} is the output voltage, and D_1 is the duty ratio when V_X is V_{IN} - $2V_{\mathrm{OUT}}$.

The average inductor current can be also found by applying capacitor charge balance to C_{F1}, C_{F2}, and C_L in one periodic steady state. The analysis starts from C_{F1} and C_{F2} as

$$CF1: D_1 I_{L,1} - (1 - D_1)\, I_{CF1,\Phi 2} \quad (6)$$

$$C_{F2}: D_1 I_{CF2,\Phi 1} + (1 - D_1)\, I_{CF1,\Phi 2} \quad (7)$$

where $I_{CFn,\Phi m}$ is the current flowing through C_{Fn} during Φ_m, n and m are 1 or 2. The charge balance at C_L can be express as

$$C_L: D_1(I_{L,1} + I_{CF2,\Phi 1} - I_{\mathrm{LOAD}})$$
$$+(1 - D_1)(I_{L,1} + I_{CF1,\Phi 2} - I_{\mathrm{LOAD}}) = 0. \quad (8)$$

By substituting (6) and (7) to (8), $I_{L,1}$ in mode1 becomes

$$I_{L,1} = \frac{1}{1 + 2D_1}\, I_{\mathrm{LOAD}}. \quad (9)$$

It shows that D_1 and I_{LOAD} are divided by a factor of $(1 + 2D_1)$ in mode1 comparing to CBC. Accordingly, $I_{L,1}$ is obviously lower than that of CBC and becomes less than 0.5 when D_1 is over 0.5. DCR loss can be reduced by the square of $1 + 2D_1$.

When VCR increases, D_1 may be close to 1. If V_{IN} decreases at a fixed load condition, the converter with flying capacitors typically suffers from insufficient time for flying capacitor balancing and large currents of $I_{CF1,2}$ at Φ_2. Thus, when V_{IN} becomes low (e.g., $D_1 > 0.75$), a higher voltage than V_{IN} - $2V_{\mathrm{OUT}}$ is required at V_X to build-up a larger inductor current, which can provide an extended time for free-wheeling. In other words, a higher switching voltage for V_X reduces D_1 even when V_{IN} decreases, which is realized in the mode2 for lower V_{IN} levels.

B. Mode2 Operation Principle

The mode2 adopts an additional phase (Φ_3) that provides higher V_X as V_{IN} - V_{OUT} while still enabling always-dual-path operation like Fig. 4(b). In Φ_3, $\mathrm{SW}_{3,5\text{-}7}$ are closed for capacitor (C_{F1} and C_{F2} in series connection) paths and inductor build-up with C_{F2}, and the other switches are open. The series-connected switches for the current paths in Φ_3 are three. The mode2 operates repeatedly in order of Φ_2 for 1-D ($V_X = 0$), Φ_1 for D_1T ($V_X = V_{\mathrm{IN}}$ - $2V_{\mathrm{OUT}}$), and Φ_3 for D_2T ($V_X = V_{\mathrm{IN}}$ - V_{OUT}), where $D = D_1 + D_2$. In addition, Φ_3 consists of $\Phi_{3\mathrm{A}}$ and $\Phi_{3\mathrm{B}}$ depending on I_{CF2} and I_L conditions, as shown in Fig. 5($\Phi_{3\mathrm{A}}$ for $I_{CF2} > I_L$ and $\Phi_{3\mathrm{B}}$ for $I_{CF2} < I_L$). The higher V_X of V_{IN} - V_{OUT} is only utilized for the limited period of D_2T during Φ_3 to ensure the sufficient capacitor balancing time while still achieving high efficiency by minimizing ΔI_L.

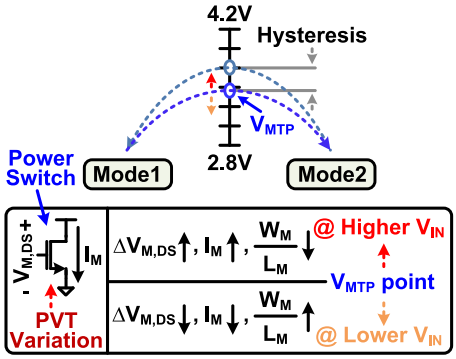


Fig. 7. Adaptive V_{MTP} control depending on operation conditions for AMT between mode1 and mode2.

To analyzing VCR in mode2, the duty ratio should be separated as the phases while the other procedures are the same as mode1

$$D_1(V_{\mathrm{IN}} - 2V_{\mathrm{OUT}} - V_{\mathrm{OUT}}) + D_2(V_{\mathrm{IN}} - V_{\mathrm{OUT}} - V_{\mathrm{OUT}}) + (1 - D_1 - D_2)(-V_{\mathrm{OUT}}) = 0. \tag{10}$$

Then, (10) can be simplified as

$$M_2 = \frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}}} = \frac{D}{1 + D_1 + D} \tag{11}$$

where M_2 is the conversion ratio at mode2, D_1 and D_2 are the duty ratio matched with Φ_1 and Φ_3, respectively, and D is the summation of D_1 and D_2.

To find the average inductor current, capacitor charge balance is applied to C_{F1}, C_{F2}, and C_L in one periodic steady state

$$C_{F1} : D_1 I_{L,2} - D_2 I_{CF1,\Phi3} - (1 - D_1 - D_2) I_{CF1,\Phi2} = 0 \tag{12}$$

$$C_{F2} : D_1 I_{CF2,\Phi1} - D_2 I_{CF2,\Phi3} + (1 - D_1 - D_2) I_{CF2,\Phi2} = 0 \tag{13}$$

$$C_L : D_1 (I_{L,2} + I_{CF2,\Phi1} - I_{\mathrm{LOAD}}) + D_2 (I_{L,2} + I_{CF1,\Phi3} - I_{\mathrm{LOAD}}) - (1 - D_1 - D_2)(I_{L,2} + I_{CF1,\Phi2} - I_{\mathrm{LOAD}}) = 0 \tag{14}$$

where $I_{CFn,\Phi m}$ is the current flowing through C_{Fn} during Φ_m, n is 1 or 2, m is 1, 2, or 3. By substituting (12) and (13) to (14), $I_{L,2}$ can be found as

$$I_{L,2} = \frac{1}{1 + D_1 + D} I_{\mathrm{LOAD}}. \tag{15}$$

D and I_{LOAD} are scaled by $1/(1 + D_1 + D)$ in mode2 comparing to CBC. It is obviously noticed that $I_{L,2}$ is still lower than the inductor current of CBC, resulting in smaller DCR loss.

C. Adaptive Mode Transition

The ADPR step-down converter adopts the AMT, which adaptively sets the transition point (V_{MTP}) from mode1 to mode2. AMT utilizes the mode selector in Fig. 6 to determine V_{MTP} depending on operation conditions. Fig. 7 shows the adaptive V_{MTP} level control that automatically set V_{MTP} against various

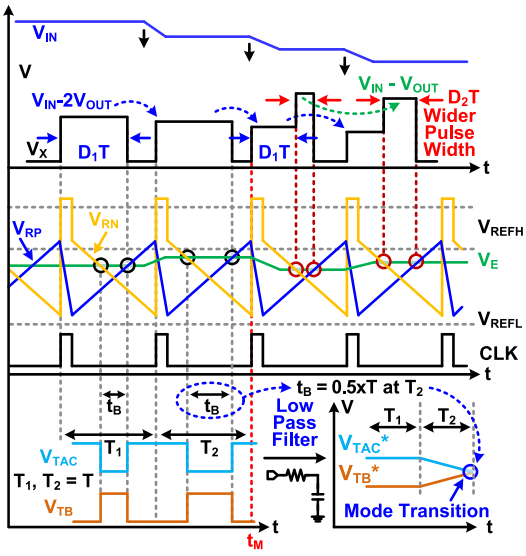


Fig. 8. Operation waveforms focusing on adaptive mode transition and adaptive duty modulation as V_{IN} drops.

factors affecting V_{CF1} and V_{CF2}, such as PVT variations, current variations flowing through power switches, and variation of total resistance on current paths. For example, if total resistance in current paths increases at fixed I_{LOAD}, V_{MTP} becomes higher. i.e., mode2 starts at higher V_{IN} to ensure sufficient time for capacitor charge balancing and stable V_{OUT}. On the contrary, when I_{LOAD} decreases, V_{MTP} can be adaptively set to lower V_{IN} for mode2. Since mode1 with two phases and lower dc current of I_L can be more efficient than mode2 with three phases, AMT adaptively sets the ADPR step-down converter to operate in mode1 for longer time. A mode comparator uses the divided frequency which is 16 times slower than clock (*CLK*) to prevent multiple mode transitions by providing sufficient time until the steady state condition.

The detailed AMT operation is depicted in Fig. 8. V_{MTP} for mode1-to-2 is adaptively set when D_1 exceeds 0.75 considering capacitor balancing for stable operation. D_1 in mode1 is determined by the point where V_{RP} reaches V_E, while V_{RP} and V_{RN} are symmetric when $CLK = 0$. The timing when D_1 exceeds 0.75 is found with V_{TAC} and V_{TB}. When the low-pass filtered V_{TAC} and V_{TB} ($V_{TAC}{}^*$ and $V_{TB}{}^*$) in the mode selector reach $0.5V_{\mathrm{LOW}}$, it indicates that D_1 becomes 0.75. As an example, when V_{IN} is getting lower from 4.2 V, V_E, and D_1 continuously increase. This finally leads to slightly lower $V_{TAC}{}^*$ and higher $V_{TB}{}^*$ than $0.5V_{\mathrm{LOW}}$, resulting in mode1-to-2 transition, which is synchronized to the mode comparator. Then, the positive input of the mode comparator changes to V_{MREF} for providing the hysteresis in AMT. The overall transition waveforms for mode1-to-2 and mode2-to-1 with hysteresis to protect continuous mode change at the boundary are described in Fig. 9 in detail.

D. Adaptive Duty Modulation

The ADPR step-down converter also adopts the ADM. ADM continuously adjusts D_1 and D_2 in mode2 with V_{TAC} and V_{TB}

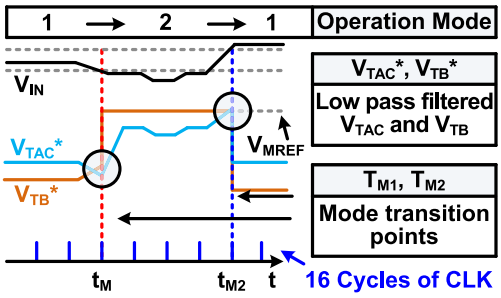


Fig. 9. Operation waveforms showing mode transition with hysteresis.

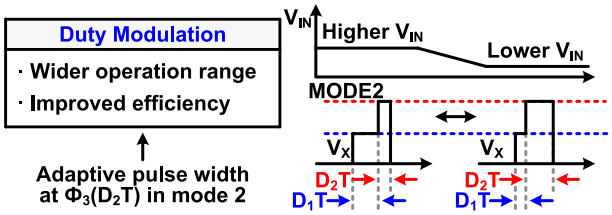


Fig. 10. Mechanism of the proposed adaptive duty modulation.

to allocate variable time for D_1 and D_2 considering power efficiency and VCR. D_2 provides higher voltage at V_X for low $V_{\rm IN}$ operation but increase inductor current ripple. Therefore, D_2 needs to be allocated only as necessary. Fig. 10 shows the mechanism of ADM that adaptively changes the ratio between D_1 and D_2 depending on VCR. When $V_{\rm IN}$ becomes lower, D_2 increases while D_1 decreases. This limits the increase of D ($= D_1 + D_2$) in mode2 by controlling the ratio between D_1 and D_2. Additionally, V_X has a longer time for D_1 when $V_{\rm IN}$ is high, leading to low ΔI_L. Therefore, ADM can provide wider operation range and higher efficiency compared to the other topologies.

The operation waveforms of ADM are also depicted in Fig. 8. ADM shares the control signals, which are used for AMT. The mode transition occurs at t_M and mode2 operation starts. The period before the crossing of V_{RN} and V_E is D_1T, and the period until the crossing of V_{RP} and V_E is D_2T. As $V_{\rm IN}$ is getting lower, V_E increases, which decrease D_1T and increases D_2T. In this way, two adaptive control loops (AMT and ADM) can operate by sharing the same signals of V_{RP}, V_{RN}, and V_E.

III. Circuit Details and Implementation

A. Complementary Switch for Power Stages

Hybrid dual-path step-down converters commonly have issues with the range of VCR because flying capacitors reduce voltage levels to energize the inductor. To solve this issue, the ADPR converter adopted two modes and complementary switch. The proposed ADPR converter can be employed for battery-powered low-power devices such as IoT applications. In Fig. 6, $\rm M_{H2}$ and $\rm M_{H3}$ operate as a complementary switch (i.e., quasi-one switch) for a wide input range operation. Fig. 11 shows the operation principles and waveforms of the complementary switch including the gate driver voltages of $\rm M_{H2}$ and $\rm M_{H3}$ at

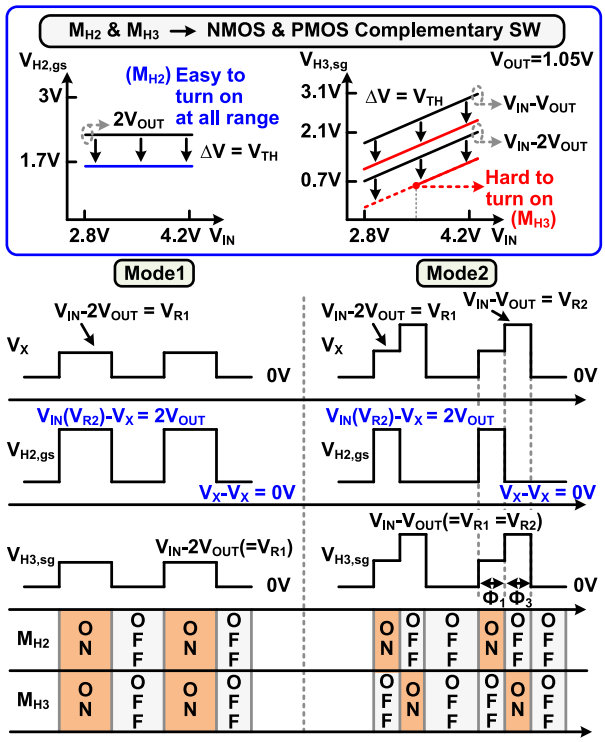


Fig. 11. Operation principles and waveforms of the complementary switch depending on $V_{\rm IN}$ and mode.

$V_{\rm OUT} = 1.05$ V. $\rm M_{H2}$ is powered by V_{R2}, and $\rm M_{H3}$ is powered by V_{R1}, which is $V_{\rm IN}$ - $2V_{\rm OUT}$ at the lowest. When $V_{\rm IN}$ is low (e.g., < 3 V) in Φ_1, $\rm M_{H3}$ is hard to turn on because V_{GS} of $\rm M_{H3}$ is near or below V_{TH}. Nonetheless, V_{R1} can be still connected to V_X through $\rm M_{H2}$ of the complementary switch, which gate is driven up to the V_{R2} level.

Regarding the operation mode, both $\rm M_{H2}$ and $\rm M_{H3}$ can properly operate in mode1 since $V_{\rm IN}$ is higher than 3 V. In mode2, $V_{\rm IN}$ may be lower than 3 V, and $\rm M_{H2}$ and $\rm M_{H3}$ operate in complementary fashion to connect V_{R1} and V_X. $\rm M_{H3}$ is OFF because $V_{\rm IN}$ - $2V_{\rm OUT}$ is not enough for turning ON, while $\rm M_{H2}$ turns ON in Φ_1 instead. In Φ_3, V_X becomes $V_{\rm IN}$ - $V_{\rm OUT}$, and V_{GS} of $\rm M_{H2}$ is 0 V whereas V_{R1} becomes $V_{\rm IN}$ - $V_{\rm OUT}$. Thus, $\rm M_{H2}$ turns OFF, and $\rm M_{H3}$ turns ON. Consequently, the complementary switch with $\rm M_{H2}$ and $\rm M_{H3}$ can ensure wide range operation including low $V_{\rm IN}$ conditions while minimally affecting the design complexity by reusing the existing timing signals.

B. Dual-Flipped Saw-Tooth Generator

The circuit diagram of the DFSG generator is depicted in Fig. 12. It generates two flipped ramp signals (V_{RP} and V_{RN}) by inserting and subtracting a certain ratio of currents based on current mirrors to C_{C1} and C_{C2}. When *CLK* is 1, C_{C1} is charged to $V_{\rm LOW}$ - V_D and C_{C2} is discharged to V_D in short time. When *CLK* becomes 0, the bottoms of C_{C1} and C_{C2} are connected to GND, and they are gradually discharged and charged by current mirrored I_{BIAS1} and I_{BIAS2}, respectively. Fig. 13 shows the output and control waveforms of DFSG.

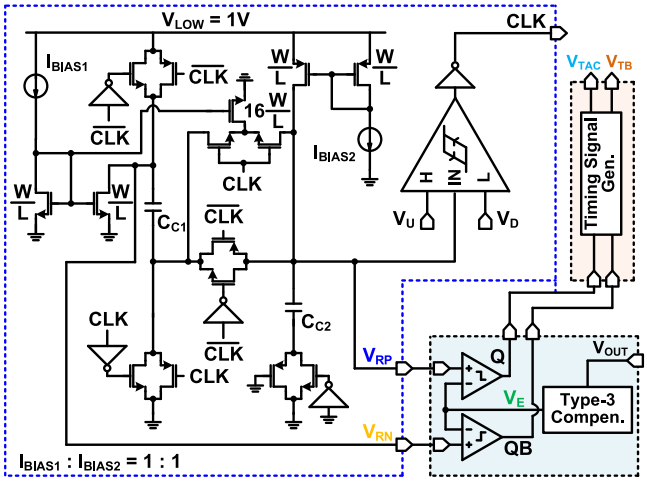


Fig. 12. Circuit diagram of the dual-flipped saw-tooth generator.

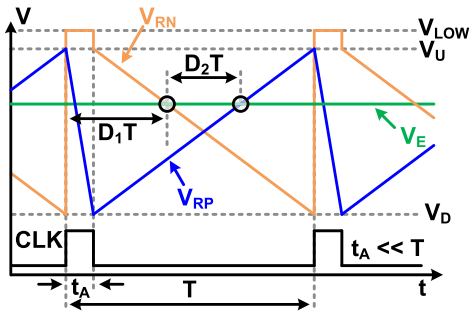


Fig. 13. Operation waveforms of the dual-flipped saw-tooth generator.

The decision relationship of the ratio between D_1 and D_2 is derived as follows with assumption of $t_A << T$ for simplification:

$$V_U + V_D = V_{\text{LOW}} \tag{16}$$

where V_U and V_D are high and low reference voltages of the hysteresis comparator in DFSG, respectively. Equation (16) can be guaranteed by connecting C_{C1} and C_{C2} in series at every cycle when *CLK* is 1. Then, V_{RN} and V_{RP} including the terms of time can be expressed as

$$V_{RN}(t) = -(V_U - V_D)/\text{T} \times t + V_U \tag{17}$$

$$V_{RP}(t) = -(V_U - V_D)/\text{T} \times t + V_U \tag{18}$$

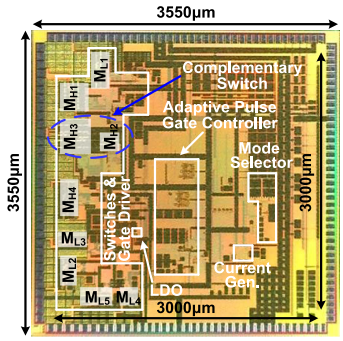
when $t_A < t < T$, $V_{RN}(t)$ and $V_{RP}(t)$ consist of voltage slopes at C_{C1} and C_{C2}, and the dc component V_U and V_D, respectively. Substituting V_E to $V_{RN}(t)$ and $V_{RP}(t)$, expressions about D_1 and D ($= D_1 + D_2$) are derived as follow:

$$D_1 = (V_U - V_E)/(V_U - V_D) \tag{19}$$

$$D = \frac{V_E - V_D}{V_U - V_D}. \tag{20}$$

Then, VCR can be expressed by combining (19) and (20) with (11) as

$$\text{VCR} = M_2 = \frac{D}{1 + D_1 + D} = \frac{V_E - V_D}{2(V_U - V_D)} \tag{21}$$



Switch	Type
M_{L1}	1.5V P-CMOS
M_{L2}	1.5V N-CMOS
M_{L3}	1.5V N-CMOS
M_{L4}	1.5V P-CMOS
M_{L5}	1.5V N-CMOS
M_{H1}	3.3V P-CMOS
M_{H2}	3.3V P-CMOS
M_{H3}	3.3V P-CMOS
M_{H4}	3.3V N-CMOS
Area w/o Pads : 9mm^2 Active Area : 2.55mm^2	

Fig. 14. Chip micrograph.

$$V_E = 2VCR(V_U - V_D) + V_D \tag{22}$$

where V_E is the type-3 compensator output. Using (22) at a specific VCR, V_E is decided. Finally, D_1 and D are acquired by substituting the V_E to (19) and (20). To sum up, DFSG provides two flipped saw-tooth waveforms which repeat at every T. Combining the desired VCR with (22) decides the output voltage of the type-3 compensator (V_E). Then, D_1 and D are obtained from (19) and (20) with V_E.

IV. Measurement Results

The proposed ADPR step-down converter was fabricated in a 0.13-μm CMOS occupying the silicon area of 3.55 × 3.55 mm^2 including power and monitoring pads, and decoupling capacitors, as shown in Fig. 14. The active of 2.55 mm^2 is estimated along the white line, which is related to the performance of the ADPR converter including each 45 pF decoupling capacitors for supply generators of M_{L1} and M_{H1}. Fig. 15 shows the measured waveforms related to the operation modes and phases when $V_{\text{OUT}} = 1.05$ V. In mode1 on Fig. 15(a), V_X is switching between 0 and V_{IN} - $2V_{\text{OUT}}$ while affected by small voltage drop of 80 mV through switches. The charging voltages of C_{F1} ($V_{CF1} = V_{\text{IN}}$ - $2V_{\text{OUT}} = 1.62$ V) and C_{F2} ($V_{CF2} = V_{\text{IN}}$ - $V_{\text{OUT}} = 2.7$ V) can be verified with the switching waveforms of V_X and V_{R1}, respectively. When V_{IN} is lower than 3.5 V, the mode2 operates with additional Φ_3, which leads V_X switching levels up to V_{IN} - V_{OUT} (= 2.4 V), as depicted in Fig. 15(b). To verify that D_1 and D_2 are adaptively adjusted by V_{IN} levels, V_{IN} is changed to 3 V like Fig. 15(c). Then, D_2 for Φ_3 increases from 220 ns to 440 ns since ADM controls D_1 and D_2 depending on VCR. Fig. 16 shows the measured inductor current (I_L) waveform depending on operation modes. $I_{L,\text{dc}}$ is less half of I_{LOAD} in mode1, as shown in Fig. 16(a). In mode2 with Fig. 16(b) and (c), $I_{L,\text{dc}}$ is about half of I_{LOAD}. The inductor current ripples (ΔI_L) were measured as 64.8 mA in mode1 and 77.6 mA to 88.8 mA in mode2. It shows that always-dual-path and RSC can work effectively to reduce $I_{L,\text{dc}}$ and ΔI_L.

Fig. 17 depicts mode transitions with hysteresis. Mode1-to-2 transition was measured by varying V_{IN} from 3.7 to 3.6 V, and the mode transition occurred at $V_{\text{IN}} = 3.62$ V. Mode2-to1 transition was tested by sweeping V_{IN} from 3.7 to 3.8 V, and the transition happened at $V_{\text{IN}} = 3.78$ V. Fig. 18 shows the load

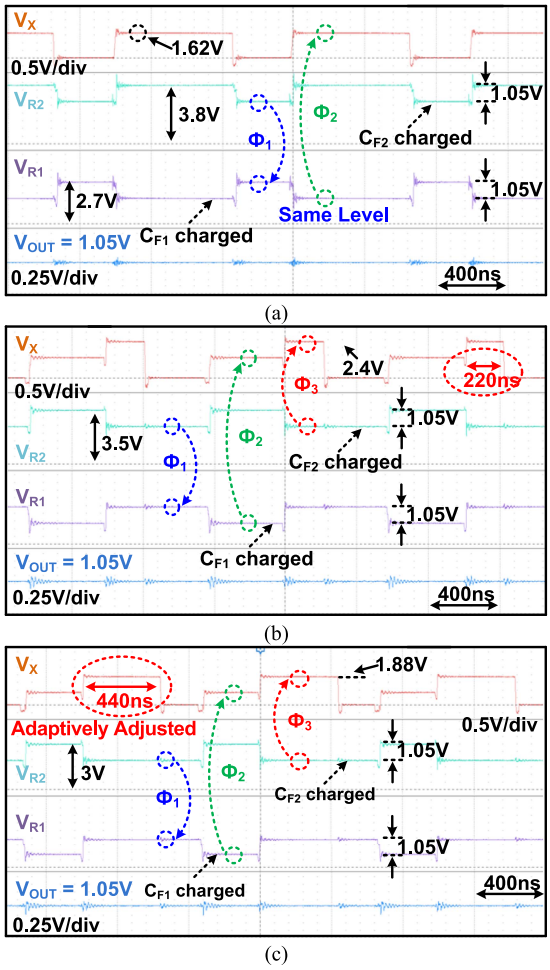


Fig. 15. Measured waveforms with $I_{\mathrm{LOAD}} = 100$ mA at mode1 (a) when $V_{\mathrm{IN}} = 3.8$ V, and at mode2, (b) when $V_{\mathrm{IN}} = 3.5$ V, and (c) when $V_{\mathrm{IN}} = 3$ V.

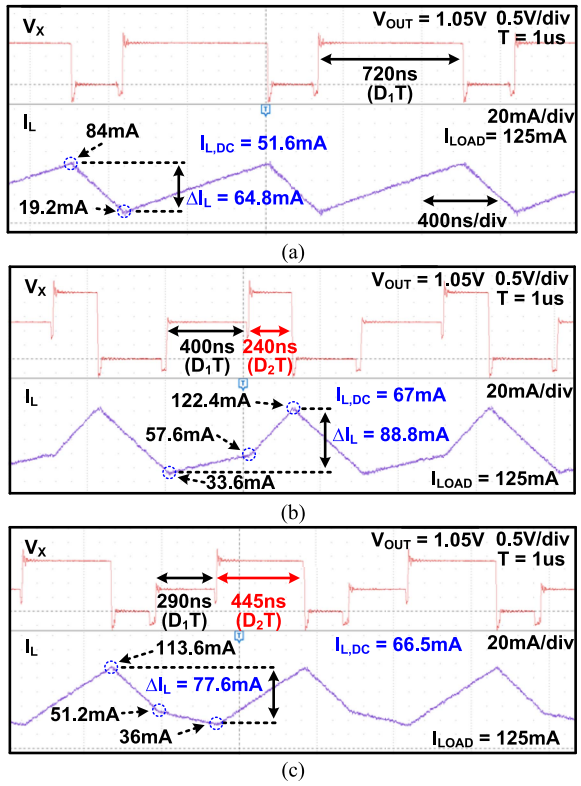


Fig. 16. Measured inductor current waveforms when (a) $V_{\mathrm{IN}} = 3.7$ V in mode1, (b) $V_{\mathrm{IN}} = 3.5$ V in mode2, and (c) $V_{\mathrm{IN}} = 3$ V in mode2.

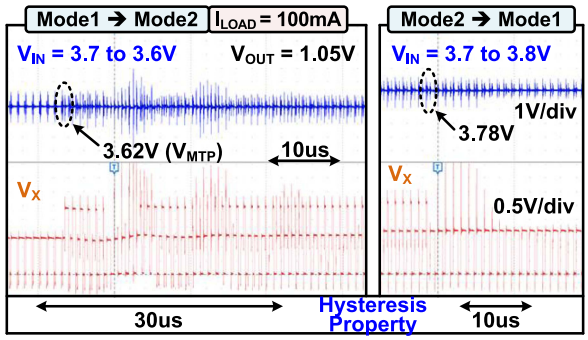


Fig. 17. Measured waveforms showing mode transition with hysteresis.

transient responses depending on operation modes. Fig. 18(a) and (b) plots the transient responses in mode1 when $V_{\mathrm{IN}} = 3.8$ V and $V_{\mathrm{OUT}} = 1$ V with $\Delta I_{\mathrm{LOAD}} = 300$ mA, and the output voltage undershoot and overshoot were measured as 35 mV and 45 mV, respectively. Fig. 18(c) and (d) shows the transient responses in mode2 when $V_{\mathrm{IN}} = 3.4$ V and $V_{\mathrm{OUT}} = 1$ V with $\Delta I_{\mathrm{LOAD}} = 150$ mA, and the output undershoot and overshoot were 10 mV and 11 mV, respectively. The output voltage ripples were between 5 mV to 10 mV in both modes from the enlarged waveform of Fig. 18, verifying that RSC enables low output voltage ripples.

Fig. 19 shows the comparison of the power efficiencies with different footprint size of flying capacitors, which are 0805 and 0402 sizes in inch. The ADPR converter with 0805-sized C_F achieves the peak efficiency of 95.4% at $V_{\mathrm{IN}} = 3.7$ V and $I_{\mathrm{LOAD}} = 75$ mA even with a large inductor DCR of 288 mΩ, as shown in Fig. 19(a). The V_{MTP} line indicates that the mode transition points are adaptively set depending on operation conditions thanks to AMT. The ADPR converter with 0402-sized C_F in Fig. 19(b) also plots the similar efficiencies up to 95% with AMT, showing that the footprint size of C_F has little effects to the ADPR converter.

In Fig. 20, the power efficiencies were measured by sweeping I_{LOAD}, V_{IN}, and V_{OUT}. Mode1 has higher efficiencies than mode2 because rms loss and I_L/I_{LOAD} are lower at mode1, as shown in Fig. 20(a), while I_{LOAD} can be up to 800 mA. The simulated power efficiencies of CBC with 5 V transistors occupying same power switches area were added to fully compare the efficiency improvement of the proposed ADPR converter. The ADPR converter has higher power efficiencies over all the load range and achieves 9% higher efficiency than that of the conventional converter when $V_{\mathrm{IN}} = 4.1$ V, $V_{\mathrm{OUT}} = 1$ V, and $I_{\mathrm{LOAD}} = 650$ mA. The ADPR converter can also operate at no load condition by absorbing or releasing I_L with C_{F1} and C_{F2}. When sweeping V_{IN} with $V_{\mathrm{OUT}} = 1$ V and $I_{\mathrm{LOAD}} = 100$ mA, as shown in Fig. 20(b), the ADPR converter achieves

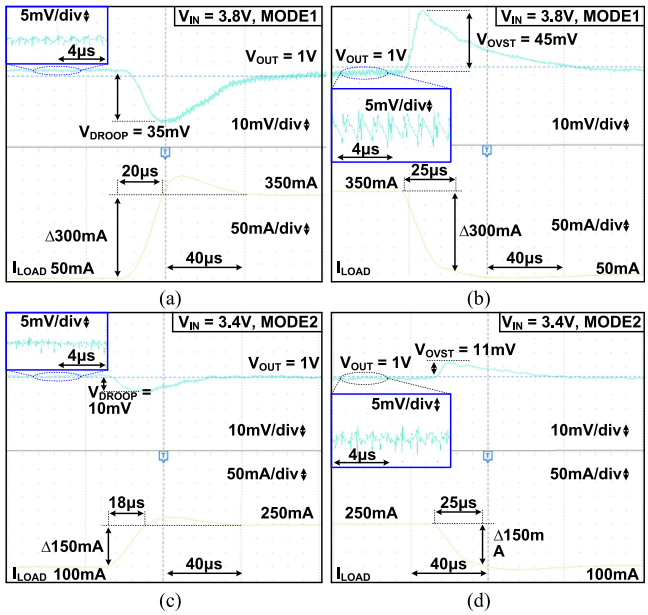


Fig. 18. Load transient responses in mode1 at (a) low-to-high and (b) high-to-low with $\Delta I_{\mathrm{LOAD}} = 300$ mA, and in mode2 at (c) low-to-high and (d) high-to-low with $\Delta I_{\mathrm{LOAD}} = 150$ mA.

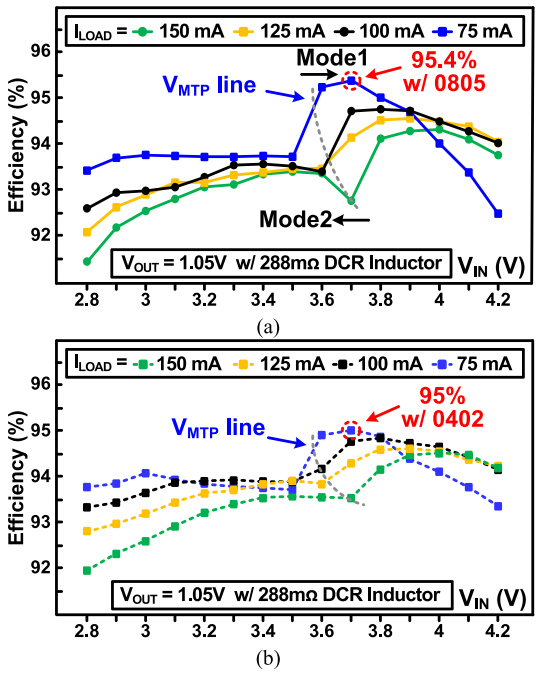


Fig. 19. Measured power efficiencies at different I_{LOAD} with (a) the large-sized C_F (0805) and (b) the small-sized C_F (0402).

high efficiencies between 92.9% and 94.5% at all V_{IN} ranges from 2.8 to 4.2 V, resulting in small efficiency variation of 1.6% thanks to always-dual-path and ADM, which is effective in mode2. In addition, the ADPR converter in mode2 has less than 0.5% efficiency variation when V_{IN} is higher than 3 V. Fig. 20(c) verifies that V_{MTP} moves effectively by AMT to achieve higher power efficiencies. When V_{OUT} is 0.9 V or higher at $V_{\mathrm{IN}} = 2.8$ V

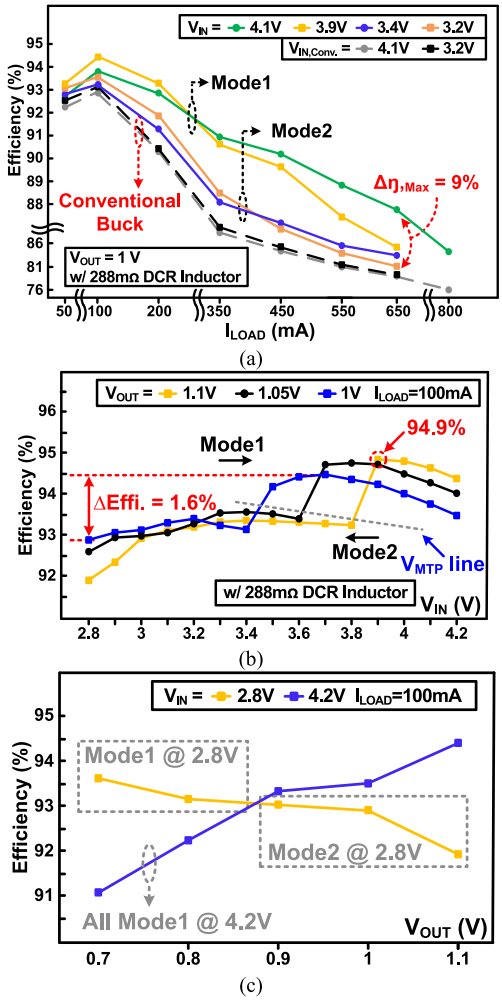


Fig. 20. Measured power efficiencies at different (a) I_{LOAD}, (b) V_{IN}, and (c) V_{OUT}.

and $I_{\mathrm{LOAD}} = 100$ mA, AMT sets the ADPR converter to operate in mode2 for generating stable V_{OUT}. On the other hand, when V_{OUT} is lower than 0.9 V at $V_{\mathrm{IN}} = 2.8$ V and $I_{\mathrm{LOAD}} = 100$ mA, V_{MTP} becomes lower than 2.8 V leading the ADPR converter to operate in mode1 with higher efficiency. When $V_{\mathrm{IN}} = 4.2$ V, D decreases at lower V_{OUT}, which increases $I_{L,\mathrm{dc}}$ and degrades power efficiencies. It is noted that the power efficiencies were measured by including LDO losses.

The comparison of normalized losses (DCR loss, R_{ON} loss, and gate switching loss) is depicted in Fig. 21 along with specification of the inductor. All converters in Fig. 21(a) used the same switching frequency of 1 MHz and inductor of 4.7 μH. The proposed ADPR converter has smaller DCR loss and R_{ON} loss when D $>$ 0.5 than [25], which has larger I_L/I_{LOAD} and the terms of $2I_LI_C$. Also, the ADPR converter has smaller DCR loss and similar R_{ON} loss than [28] which has larger I_L/I_{LOAD}. In the normalized loss comparison, on-resistance of all power switches and DCR of the inductor are assumed to be the same value as R_{ON} and R_{DCR}, respectively. ESR of the SMD capacitors (R_{ESR}) can be ignored since R_{ESR} is much smaller than R_{ON}. It can be also observed that the ADPR

TABLE I
PERFORMANCE COMPARISON WITH STATE-OF-THE-ART WORKS

	TPEL 2018 [2]	VLSI 2018 [14]	JSSC 2020 [18]	VLSI 2021 [25]	ISSCC 2022 [26]	TCAS-I 2022 [27]	JSSC 2023 [28]	This work
Process	130 nm	250 nm	65 nm	180 nm	65 nm	65 nm	180 nm	130 nm
Topology	SC	3-Level	Hybrid (Dickson SC)	Hybrid (ADP)	Hybrid (CPL)	Hybrid (Tri-Path)	Hybrid (SDBBC)	Hybrid (ADPR)
V_{IN} [V]	3.2 - 4	2.6 - 5	3.4 - 4.2	3.4 - 4.5	3 - 4.2	3.3 - 4	2.9 - 4.2	2.8 - 4.2
V_{OUT} [V]	1.07	0.34 - 4.5	0.3 - 0.9	0.3 - 1.7	0.6 - 1	0.7 - 1	3.3	0.7 - 1.1
V_{IN}/V_{OUT}	3 - 3.73	1.11 - 14.7	3.78 - 14	2 - 15	3 - 7	3.3 - 5.7	0.88 - 1.27	2.45 - 6
Available for Whole Range of Li-ion Battery Voltage	☹	☺	☹	☹	😐	☹	😐	☺
LV Process Integration[E]	☺	☺	☺	☹	☺	☺	☹	☺
Adaptive Control for Efficiency Improvement	☹	☹	☹	☹	☹	☹	☹	☺ (ADM)
Inductor [μH] (DCR) / Volume	-	0.22	0.18	4.7 (250mΩ) / 4mm^3	0.47 / 1 mm^3	1 (80mΩ) / 3.8mm^3	4.7 (175mΩ)	4.7 (288mΩ) / 3.2mm^3
Flying Cap. [μF] (# of Cap.)	0.00012[A] (6, Integ.)	1 (1)	4.7 - 22 (3)	10 (2)	4.7 (2)	0.47 (2)	10 (2)	4.7 (2)
Freq. [MHZ]	10 - 100	4.4 - 11.8	0.3 - 0.5	1	2	5	1	1
Inductor Current ($I_{L,DC}$)	-	I_{LOAD}	I_{LOAD}	0.5·I_{LOAD} (fixed)	0.4·I_{LOAD} to 0.71·I_{LOAD}	0.4·I_{LOAD} to 0.65·I_{LOAD}[A]	0.7-0.81[A]	0.42·I_{LOAD} to 0.66·I_{LOAD}
Max. Load [A]	0.045	0.8	1.5	1.6	1.2	0.3	1	0.8
Peak Efficiency @ VCR[B], (V_{IN}, I_{LOAD})	80% @ 0.29, (3.7V, 9.4mA[A])	92.8% @ 0.9, (3.3V, 300mA)	92.6% @ 0.214, (4.2V, 500mA)	91.5% @ 0.38, (4.5V, 400mA)	92.9% @ 0.267, (3V, 400mA)	84% @ 0.25, (3.6V, 160mA)	93.6% @ 1, (3.3V, 400mA)	95.4% @ 0.284, (3.7V, 75mA)
Efficiency @ Similar (VCR, V_{IN}, I_{LOAD}=300mA)	N/A (Max. I_{LOAD} = 45mA)	79%[A] (0.3, 4.2V, 300mA)	89%[A] (0.214 ,4.2V, 300mA)	86%[A] (0.245, 4.5V, 300mA)	91.5%[A] (0.263, 3.8V, 300mA)	81%[A] (0.225, 4V, 300mA)	N/A (Min. VCR = 0.785)	91.7% (0.244, 4.1V, 300mA)
Current Density (mA/mm^2)	115[D]	166[D]	375[D]	392[D]	300	361	215[D]	313[D]

[A] Calculated from reported data, [B]VCR = V_{OUT}/V_{IN}, [C]size = 3.2mm^3, [D]active chip area, [E]possible to use transistors lower than maximum V_{IN} level

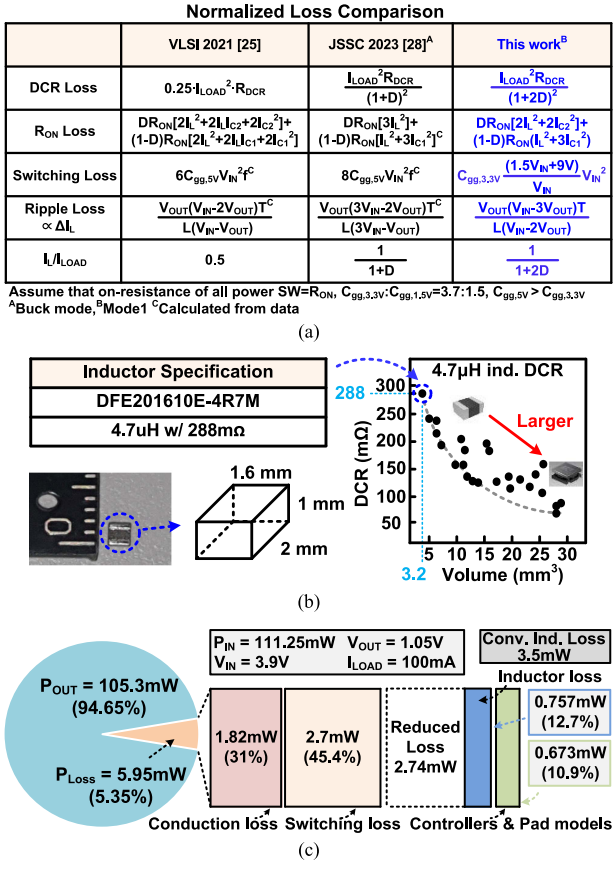


Fig. 21. Power loss analysis with (a) comparison of normalized losses, (b) inductor DCR comparison, and (c) simulated power pie chart.

converter has the smallest switching loss in Fig. 21(a) because $C_{gg,3.3V}$ is smaller than $C_{gg,5V}$. The inductor used for test has 4.7 μH with 288 mΩ occupying 1.6×2×1 mm^3. The output component capacitors tested for both cases of 0805 and 0402, which are commonly adopted sizes. The volume of inductor and the number of output component capacitors, which are related to the cost of products, compared with other converters on Table I. The ADPR converter aims to maximize the efficiencies even with the small-volume inductor with larger DCR, as described in Fig. 21(b). The simulated power pie chart in Fig. 21(c) shows the detailed power losses of the converter. When $V_{\rm IN} = 3.9$ V, $V_{\rm OUT} = 1.05$ V, and $I_{\rm LOAD} = 100$ mA, the efficiency is 94.65%. The simulated result is well matched with the measured result, and most power losses resulted from conduction and switching losses. The large inductor DCR (288 mΩ) dissipates the small power loss of 0.757 mW, which is only 0.68% of the input power and saved 2.74 mW when compared to CBC with loss of 3.5 mW under same conditions.

Table I shows the performance summary and comparison with state-of-the-art converters. The proposed ADPR converter has 2.45–6 of $V_{\rm IN}/V_{\rm OUT}$, which is similar or wider than [26], [27] and narrower than [18], [25] due to their low output voltage levels down to 0.3 V. However, the proposed ADPR converter has the widest input operate range of $V_{\rm IN} = 2.8$–4.2 V and $V_{\rm OUT} = 0.7$–1.1 V thanks to ADM, which is helpful to increase power efficiency in mode2 by adaptively adjusting $D_{1,2}$ and the complementary switch. As the result, the proposed ADPR converter is most compatible for Li-ion battery (2.8–4.2 V) while the other hybrid converters cannot use the whole range of Li-ion battery voltages [18], [25], [26], [27], [28]. The proposed ADPR converter achieves considerably higher power

efficiencies up to 95.4% at VCR condition of 0.284 comparing to other dual-path hybrid converter [25], [26], [27] while having lower or similar VCR and even adopting the small-volume inductor with the largest DCR of 288 mΩ thanks to always dual-path and a relatively low $I_L/I_{\rm LOAD}$ of 0.43 at the VCR of the peak efficiency. Especially, $I_L/I_{\rm LOAD}$ of the proposed ADPR step-down converter is lower than [25], [28] and similar level to [26], [27] leading to lower conduction loss for $R_{\rm DCR}$. For the comparisons about a different load condition when $I_{\rm LOAD} =$ 300 mA, the proposed ADPR converter still shows the highest power efficiency of 91.7% than the other converters in Table I. The proposed ADPR converter does not require a large value inductance and adopted a 4.7 μH inductor with 288 mΩ, which is a commonly used inductance value like [25], [28] but higher dc resistance because of smaller volume (3.2 mm^3). The proposed ADPR converter has higher efficiencies under most load current conditions than [27], which uses smaller value and larger volume of inductor (1 μH with 80 mΩ and 3.8 mm^3). This means that small volume inductor with large inductance is also an effective solution. In addition, Ko et al. [25] adopted 25% larger volume of inductor with 4.7 μH leading to lower DCR (250 mΩ) but this converter shows lower power efficiency for the peak and the same load condition ($I_{\rm LOAD} = 300$ mA) than the proposed ADPR converter due to DCR loss and $R_{\rm ON}$ loss as explained on Fig. 21(a). Cai et al. [26] has more power transistors in current path by configuring power switches in series connection of transistors resulting in higher R_{ON} loss. In addition, Cai et al. [26] adopted 10x smaller inductor which is 0.47 μH and 2x higher switching frequency, which is 2 MHz leading to higher rms loss while the ADPR converter has 4.7 μH, 1 MHz, and the same VCR at the peak efficiency as [26]. For the reasons, the ADPR converter can achieve higher power efficiencies while [26] has 3x smaller volume of inductor which is 1 mm^3, which is the smallest volume on Table I. The current density of most converters including the proposed ADPR converter on Table I are between 300 and 400 mA/mm^2 but [2], [14], [28] are lower than 300 mA/mm^2.

V. Conclusion

The proposed ADPR step-down converter has the advantages of both dual-path hybrid converters and multilevel converters. The ADPR converter adopts the efficient high-voltage tolerant topology, so it can operate with the Li-ion battery despite of using only low-voltage transistors as power switches. In other words, the ADPR converter can be integrated in SoCs with low-voltage process, which can improve the performance and cost for overall systems, while still ensuring high power efficiencies. The adaptive mode transition and adaptive duty modulation enable the converter to operate at wide input ranges while achieving high efficiencies up to 95.4% and small efficiency variation of 1.6%.

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