# Spread Spectrum Modulation to Reduce EM Noise for *LLC* Resonant Converter Using Partial Power Processing Concept

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***Abstract*—This article proposes a method to obtain tight output voltage regulation under the spread spectrum modulation (SSM) using a partial power processing (PPP) concept. The *LLC* resonant converter performs the SSM by handling most of the power as a dc transformer without output voltage regulation. In contrast, a buck converter processes only partial power to regulate the output voltage and to compensate for the output voltage fluctuations caused by the SSM. Since the output voltage fluctuation can be compensated by the PPP, high power conversion efficiency, electromagnetic (EM) noise reduction, and tight output voltage regulation can be obtained simultaneously. Furthermore, the proposed method has high cost-effectiveness compared with the conventional methods which process the full power to compensate for the output voltage fluctuation due to the SSM. The effectiveness of the proposed method is experimentally verified with a 500-W prototype. The output voltage is tightly regulated under the steady-state operations and transient-state within 1.24 $V_{pp}$ (2.5%) and within 1.7 $V_{pp}$ (3.5%) under the rated power. The EM noises are reduced by 26 dB$\mu$V (more than 45%) compared with the no SSM case. The maximum power conversion efficiency is 95.49% under the nominal input voltage of 400 V.**

***Index Terms*—Electromagnetic noise reduction, *LLC* resonant converter, output voltage regulation, partial power processing, spread spectrum modulation.**

## I. Introduction

THE *LLC* resonant converter is widely used in home and industrial applications, which require high power conversion efficiency and high power density [1], [2], [3], [4], [5]. It can obtain zero voltage switching (ZVS) and zero current switching (ZCS) capabilities in the primary switches and the secondary rectifiers, respectively, which enables high-speed switching operations. In addition, it can easily obtain buck and boost operations using a pulse frequency modulation (PFM). However, when the *LLC* resonant converter operates far from the series resonant frequency, it results in low power conversion efficiency due to increased circulating current and switching loss.

To overcome those issues, the dc transformer (DCT) concept is proposed [6], [7]. When the *LLC* resonant converter operates at the series resonant frequency where the circulating current is minimized, the power conversion efficiency becomes maximum. However, since the converter cannot regulate the output voltage at this fixed operating frequency, the DCT cannot be adopted in many applications that require various load responses and tight output voltage regulation. Several studies have been conducted to enhance the power conversion efficiency of the *LLC* resonant converter and to obtain the output voltage regulation capability, simultaneously.

In [8], [9], the *LLC* resonant converter operates as the DCT, and a dc/dc converter is connected in series to regulate the output voltage. However, since the full power is processed by the two conversion stages, it decreases power conversion efficiency and power density. In [10], [11], [12], [13], [14], and [15], the *LLC* resonant converters combined with partial power processing (PPP) converters have been proposed. An additional dc/dc converter handles partial power to regulate the output voltage. In [10] and [11], the output voltage of the entire power conversion system can be regulated by configuring the output stage of the PPP converter connected to the output of the main converter in series. Using the structure, the wide output voltage range, and the elimination of the second harmonic generated from the ac source can be obtained [11]. In [12], output voltage regulation is obtained by adjusting the amplitude of the square wave applied to the resonant network by the PPP converter. In the case of [13], the dual-active-bridge converter operates as the PPP converter, which regulates the output voltage and supports the ZVS of the secondary side switches. In [14], a three-port *LLC* DCT converter consists of two input ports and one output port. The PPP converter is connected in series at one of the input ports to regulate the output voltage, which can obtain a

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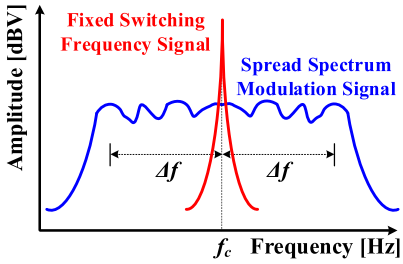


Fig. 1. Principle of the spread spectrum modulation.

TABLE I
COMPARISON BETWEEN CONVENTIONAL METHODS

| | PFM only | PFM + PSM [23] | Phase-shifted PFM [24] |
|---|---|---|---|
| Output voltage regulation | X | O (Step-load X) | O |
| Complexity | Simple | Complex | Simple |
| Applicable structures | Half & Full bridge | Full-bridge only | Multiple converter configuration only |
| Cost-effectiveness | - | Middle | Low |
| Light load efficiency | Low | | |

wide input voltage range. In [15], the PPP converter composed of full-bridge and push–pull converters is connected to the *LLC* DCT with input parallel and output series. It enables bipolar regulation capability and obtains the ZVS in the PPP converter. These papers [10], [11], [12], [13], [14], [15] achieved high power conversion efficiency by regulating the output voltage through PPP operations.

The *LLC* resonant converters are preferred to operate with switching frequencies ranging from several hundred kHz to several MHz to obtain high power density. However, the fast switching operation can generate electromagnetic (EM) noises, which cause the malfunction of various electrical and electronic circuits. Therefore, the electromagnetic interference (EMI) standards prescribe the criteria for electrical products to be released to the market [16]. To meet those standards, EM noise reduction methods such as printed circuit board (PCB) layout changes, groundings, shieldings, and EMI filters have been developed [17], [18], [19], [20], [21], [22]. However, those methods reduce the power density of power converters and increase their cost.

As an alternative solution, a spread spectrum modulation (SSM) can be a good technical choice. The SSM can reduce the EM noise by modulating the switching frequency with a preshaped modulation pattern. The frequency modulation of the SSM can be expressed as follows [16]:

$$s(t) = A_o \cos\left[2\pi f_c t + 2\pi\Delta f \int_{-\infty}^{t} \xi(\tau)d\tau\right] \quad (1)$$

where $A_o$ is the amplitude, $\xi(\tau)$ $(-1 \le \xi(\tau) \le 1)$ is the modulated frequency pattern of the frequency $f_m$, $f_m$ is the modulation frequency, $f_c$ is the center frequency, and $\Delta f$ is the frequency variation of the SSM. When the switching frequency varies within the range of $[f_c - \Delta f, f_c + \Delta f]$ with the preshaped modulation pattern, the narrow band EM noise signal is dispersed to the adjacent frequency band. As a result, the peak EM noise can be effectively reduced as shown in Fig. 1. However, since the voltage gain of the *LLC* resonant converter depends on the switching frequency, its variation caused by the SSM can induce high output voltage fluctuation [23].

To overcome those issues, output voltage regulation methods have been proposed to compensate for the output voltage fluctuation. In [23], a hybrid control method using the PFM and phase-shift modulation (PSM) is proposed. However, it can only be applied to the full-bridge structure and the SSM cannot be performed under the transient state. In addition, it has a complicated control scheme. In [24], the output voltage fluctuation is compensated by the phase-shifted SSM operation using two *LLC* resonant converters with a series-connected output stage. It has a simple control scheme. However, it is limited to the multiple converter structure which can increase the production cost. Both the previous methods are less cost-effective and less efficient in power conversions because they tried to handle full power to compensate for the output voltage fluctuation. Furthermore, since both methods are based on PFM, they have poor efficiency at the light load due to increased reactive power and circulating current. A comparison between the conventional methods is summarized in Table I.

In this article, an output voltage regulation method using the PPP concept is proposed for the *LLC* resonant converter to mitigate the output voltage fluctuations due to the SSM. The *LLC* resonant converter operates as the DCT, which performs the SSM to mitigate the EM noise without regulating the output voltage. In contrast, a buck converter, as the PPP converter, regulates the entire output voltage by compensating for the output voltage fluctuation caused by the SSM. Since the buck converter handles only partial power, the power delivered by the two-stage conversion is minimized. Therefore, high power conversion efficiency, EM noise reduction, and tight output voltage regulation can be obtained simultaneously. Furthermore, the buck converter uses lower-rating switching devices and passive components, which is more cost-effective than previous research. The proposed method is experimentally verified by a 500 W prototype.

This article is an extension version of the conference paper [25] and includes improvements in five aspects as follows:

1) *Power Analysis*: For a detailed explanation of the proposed method, the power analysis under the SSM with the proposed method is conducted in Section II.
2) *Application-oriented design methodology*: This article considers the input voltage variations. The target application is a step-down isolated converter for data centers, which have the specification of 400 V nominal input voltage and 48 V output voltage [1]. The converter should be able to cope with various input voltage situations [12]. Therefore, the input voltage range is assumed to be ± 5% ([380 V, 420 V]) of the nominal voltage, and an application-oriented design methodology is presented in Section III.

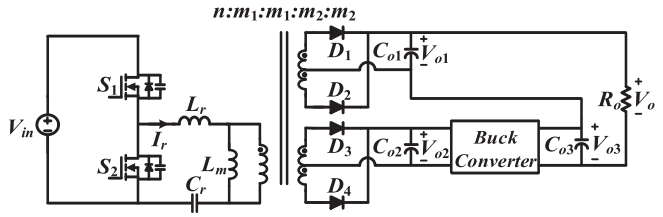


Fig. 2. Circuit diagram of the PPP *LLC* resonant converter.

3) *Optimization of power conversion efficiency*: This article shows improved power conversion efficiency. It is obtained by designing the PPP converter to process only the minimum partial power to compensate for only the output voltage fluctuations caused by the SSM in Section III.
4) *Verification of the power conversion efficiency*: To verify and analyze the power conversion efficiency improvements in PPP *LLC* resonant converter, power loss analysis according to three alternative converter types are presented in Section IV.
5) *Direct comparison with previous research papers*: To show the technical contributions of the proposed method, this article presents a direct comparison of the proposed method with [23] and [24] in terms of cost-effectiveness and power conversion efficiency in Section V.

## II. Operating Principles of PPP *LLC* Resonant Converter

Fig. 2 shows the circuit diagram of the PPP *LLC* resonant converter composed of an *LLC* resonant converter and a buck converter. The *LLC* resonant converter operates as the DCT, which delivers most of the power and performs the SSM without the output voltage regulation to mitigate EM noises with a fixed 50% duty ratio. $L_r$ is the resonant inductance implemented by the leakage inductance of the transformer, $L_m$ is the magnetizing inductance, and $C_r$ is the resonant capacitor. The buck converter is configured at the tertiary winding of the transformer for the output voltage regulation, and its output stage is connected in series to $V_{o1}$. Unlike the *LLC* DCT, the buck converter handles partial power.

### A. Power Distribution

Based on the structure shown in Fig. 2, the output voltage of the PPP *LLC* resonant converter can be derived as follows:

$$V_o = V_{o1} + V_{o3} = V_{o1} + DV_{o2} \tag{2}$$

where $D$ is the duty ratio of the buck converter. In addition, (2) can be expressed as an equation for the input voltage, as follows:

$$\begin{cases} V_{o1} = \frac{m_1}{2n} M_1 V_{\text{in}} \\ V_{o2} = \frac{m_2}{2n} M_2 V_{\text{in}} \end{cases} \tag{3}$$

where $n$, $m_1$, and $m_2$ are the primary, secondary, and tertiary turn numbers, respectively. In this article, $m_2$ is assumed to be one. $M_1$ and $M_2$ are the resonant network's voltage gains of

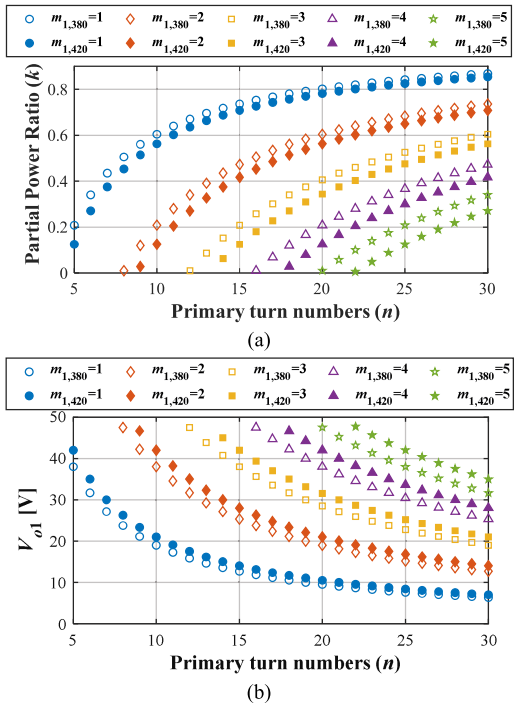


Fig. 3. Parameters according to primary turn numbers at the maximum and minimum input voltages. (a) Partial power ratio. (b) $V_{o1}$.

the secondary and the tertiary side considering the primary side, respectively. As the *LLC* resonant converter operates as the DCT, $M_1$ and $M_2$ are assumed to be the unity voltage gain. Therefore, the voltage gain of the PPP *LLC* resonant converter is obtained as follows:

$$M = \frac{V_o}{V_{in}} = \frac{\frac{m_1}{2n} M_1 V_{in} + D\frac{m_2}{2n} M_2 V_{in}}{V_{in}} \simeq \frac{1}{2n}(m_1 + D) \tag{4}$$

when the turn numbers are determined, the required duty ratio to regulate the output voltage can be derived by using (4).

Since $V_{o1}$ and $V_{o3}$ are connected in series and $V_{o3}$ can be expressed in terms of $V_{o1}$ using (2) and (3), the partial power ratio can be derived as follows:

$$k = \frac{P_{o3}}{P_{\text{Total}}} = \frac{V_{o3}}{V_{o1} + V_{o3}} = \frac{DV_{o1}/m_1}{V_{o1} + DV_{o1}/m_1} = \frac{D}{m_1 + D} \tag{5}$$

where $P_{o3}$ is the partial power processed by the buck converter, and $P_{\text{Total}}$ is the total power transferred by both the *LLC* resonant converter and the buck converter. By using (4) and (5), the relationship between the partial power ratio and the turn numbers can be expressed as follows:

$$k = 1 - \frac{m_1}{2nM}, \quad 0 \le k \le 1. \tag{6}$$

Fig. 3 shows the partial power ratio and $V_{o1}$ according to the primary turn numbers at the maximum and minimum input voltages. As the primary turn numbers decrease, the partial power ratio decreases. In addition, the higher the input voltage, the higher the output voltage of the *LLC* resonant converter operating as the DCT, reducing the partial power handled by the buck converter. When the output voltage of the *LLC* DCT is

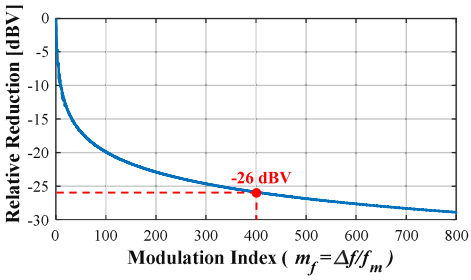


Fig. 4. Peak relative EM noise reduction according to $m_f$ under triangular modulation.

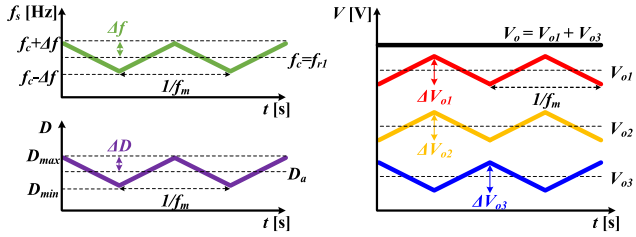


Fig. 5. Output voltage fluctuation waveforms with the SSM.

greater than the nominal voltage, the output voltage cannot be regulated by the buck converter. Therefore, the turn ratio should be selected by considering the maximum input voltage.

### B. Correlation Between Power Conversion Efficiency and Partial Power Ratio

The PPP *LLC* resonant converter delivers the power using two paths. One is the single-stage path by the *LLC* DCT, and the other is the two-stage path composed of the *LLC* DCT and the buck converter. The output power delivered by two paths can be expressed as follows:

$$\begin{cases} P_{o1} = (1-k)\cdot P_o = \eta_1 \cdot P_{in1} \\ P_{o2} = k \cdot P_o = \eta_2 \cdot P_{in2} \end{cases} \tag{7}$$

where $\eta_1$ and $\eta_2$ are the power conversion efficiency when power is transferred through the single-stage and the two-stage path, respectively. $P_{in1}$ and $P_{in2}$ are the input powers transferred to the secondary and tertiary sides, respectively. Using (7), the total power conversion efficiency is derived as follows:

$$\eta_{\text{Total}} = \frac{P_o}{P_{\text{in1}} + P_{\text{in2}}} = \frac{\eta_1\eta_2}{k\,(\eta_1 - \eta_2) + \eta_2}. \tag{8}$$

As the partial power ratio increases, the total conversion efficiency decreases to approach the two-stage power conversion efficiency of $\eta_2$. Therefore, the partial power should be minimized to obtain high power conversion efficiency close to $\eta_1$.

### C. Spread Spectrum Modulation

To reduce EM noises, the *LLC* DCT performs the SSM. The EM noise reduction performance by the SSM is determined by the modulation index of $m_f$ expressed as $\Delta f/f_m$. The periodic triangular modulation pattern is adopted as the modulated switching frequency pattern of the SSM. Fig. 4 shows the peak relative EM noise reduction according to $m_f$ under the triangular modulation. Large $m_f$ can effectively reduce the peak EM noise, and its performance is determined by designing $\Delta f$ and $f_m$. The modulation frequency of $f_m$ should be greater than or equal to the resolution bandwidth (RBW) of measurement equipment [26]. In this article, a spectrum analyzer (9320B manufactured by Keysight) with the RBW of 100 Hz is used, where $f_m$ is selected to 100 Hz. In addition, to obtain the peak EM noise reduction of –26 dBV compared with the case of non-SSM, $\Delta f$ is selected to 40 kHz.

### D. Proposed Output Voltage Regulation Method

Using the first harmonic approximation (FHA), the *LLC* resonant converter has frequency-dependent voltage gain expressed as follows [24]:

$$G(f_s) = \left| \frac{L_n (f_s/f_{r1})^2}{(L_n+1)(f_s/f_{r1})^2 - 1 + j((f_s/f_{r1})^2 - 1)(f_s/f_{r1})QL_n} \right| \tag{9}$$

where $f_s$ $(= 1/T_s)$ is the switching frequency, $f_{r1}$ is the series-resonant frequency, $L_n$ is the ratio of the magnetizing inductance to the resonant inductance, and $Q$ is the quality factor. From (9), high switching frequency variation caused by the SSM can induce high output voltage fluctuation. The voltage fluctuations of $V_{o1}$ and $V_{o2}$ can be derived as follows:

$$\begin{cases} \Delta V_{o1} = \frac{m_1}{n} \cdot V_{\text{in}} \cdot [G(f_c - \Delta f) - G(f_c + \Delta f)] \\ \Delta V_{o2} = \frac{1}{n} \cdot V_{\text{in}} \cdot [G(f_c - \Delta f) - G(f_c + \Delta f)] \end{cases}, \; f_c = f_{r1}. \tag{10}$$

The center frequency of the SSM is aligned to the series-resonant frequency to operate the converter at an optimal power conversion efficiency point. The total output voltage fluctuation of the converter can be derived as follows:

$$\begin{cases} \Delta V_o = \Delta V_{o1} + \Delta V_{o2} + \Delta V_{\text{ripple}} \\ \Delta V_{\text{ripple}} = \frac{\pi}{2} I_o R_{\text{esr}} + \frac{\Delta Q}{C_{o1}} \end{cases} \tag{11}$$

where $\Delta V_{\text{ripple}}$ is the output voltage ripple on $V_{o1}$ by the switching operation, $C_{o1}$ and $R_{\text{esr}}$ are the output capacitance and equivalent series resistance (ESR), respectively, $I_o$ is the load current, and $\Delta Q = 0.105\, I_o T_s$. Since the buck converter handles only a small portion of the total output voltage, the switching ripple on $V_{o3}$ can be ignored.

Output voltage fluctuations due to the SSM can be compensated for by changing the duty ratio of the buck converter. When $V_{o3}$ has the same amplitude with 180° out of phase as $V_{o1}$, the output voltage of the PPP *LLC* resonant converter can be tightly regulated, as illustrated in Fig. 5. The voltage fluctuation of $V_{o3}$ and the variation of the duty ratio which are required to

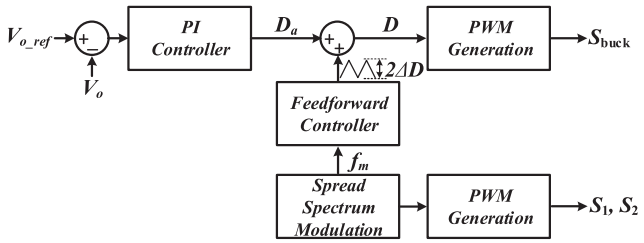


Fig. 6. Control block diagram of the PPP *LLC* resonant converter.

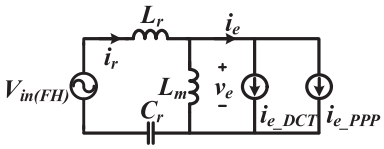


Fig. 7. Equivalent circuit of the PPP *LLC* resonant converter.

compensate for $V_{o1}$ can be derived as follows:

$$\begin{cases} \Delta V_{o3} = \frac{V_{in}}{n} \cdot [G(f_c+\Delta f) \cdot D_{\max} - G(f_c-\Delta f) \cdot D_{\min}] \\ \Delta D = \frac{2[G(f_c-\Delta f)-G(f_c+\Delta f)]\cdot(m_1+D_a)}{G(f_c-\Delta f)+G(f_c+\Delta f)} \end{cases} \tag{12}$$

where $D_a$ is the average value of the duty ratio, $D_{\max}$ and $D_{\min}$ are $D_a + \Delta D$ and $D_a - \Delta D$, respectively. Fig. 6 shows the control block diagram of the PPP *LLC* resonant converter. A PI controller and a feedforward controller are configured, which can compensate for the steady-state error and output voltage fluctuation, respectively. To synchronize with the SSM operation, $f_m$ of the SSM is input to the feedforward controller. A feedforward controller changes the duty ratio with a period of $1/f_m$ according to the designed $\Delta D$, which is added to the PI controller's output value of $D_a$. Therefore, the duty ratio of the buck converter swings within the range of $[D_a - \Delta D, D_a + \Delta D]$. As a result, the controlled $\Delta V_{o3}$ with the same magnitude as $\Delta V_{o1}$ can compensate for the output voltage fluctuation.

### *E. Power Analysis*

To conduct the power analysis under the SSM with the proposed method, the equivalent circuit of PPP *LLC* resonant is derived by FHA from Fig. 2, which is shown in Fig. 7. $i_{e\_DCT}$ and $i_{e\_PPP}$ are primary side equivalent currents reflected from the secondary side and the tertiary side, respectively. Since the fundamental component of the square wave is applied to the primary side, $v_e$(t) can be derived from the output voltage of $V_{o1}$(t) as follows:

$$v_e(t) = \left(\frac{n}{m_1}\right)\frac{4}{\pi} V_{o1}(t) \sin[2\pi f_s(t) \cdot t]. \tag{13}$$

Using (5), (13) can be expressed in terms of the duty ratio and turn numbers as follows:

$$v_e(t) = \frac{4}{\pi} \cdot \frac{n}{m_1 + D(t)} \cdot V_o \sin[2\pi f_s(t) \cdot t] \tag{14}$$

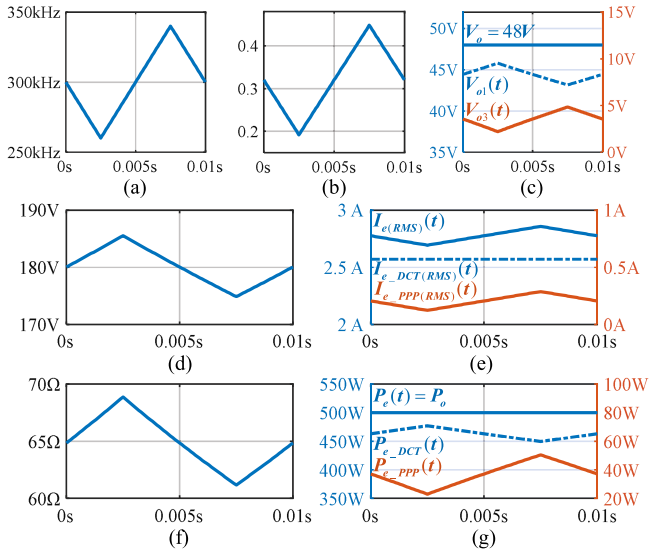


Fig. 8. Power analysis of the PPP *LLC* resonant converter at a period of $1/f_m$. (a) $f_s$. (b) $D$. (c) Output voltage. (d) $V_{e(\mathrm{RMS})}$. (e) $I_{e(\mathrm{RMS})}$. (f) $R_e$. (g) Output power.

where $V_o$ is the nominal output voltage of 48 V. When the output voltage is tightly regulated with $V_o$ by the PPP converter, the load current has a constant value of $I_o$ under a fixed load resistance ($R_o$). Therefore, $i_e$(t) can be obtained from the secondary and tertiary side rectified currents as follows:

$$i_e(t) = \frac{\pi}{2n} I_o \cdot (m_1 \sin[2\pi f_s(t) \cdot t] + D(t) \sin[2\pi f_s(t) \cdot t]) \tag{15}$$

$v_e$(t) and $i_e$(t) are assumed to be in phase, indicating that all the power transferred by the transformer is delivered to the output. Because $k$(t) and $D$(t) change slowly with $f_m$ (100 Hz), while $f_s$ changes quickly, the RMS values of $v_e$(t) and $i_e$(t) are approximated as follows:

$$\begin{cases} V_{e(\mathrm{RMS})}(t) \simeq \frac{2\sqrt{2}}{\pi} \cdot \frac{n}{m_1+D(t)} V_o \\ I_{e(\mathrm{RMS})}(t) \simeq \underbrace{\frac{\pi}{2\sqrt{2}n} m_1 I_o}_{Ie\_\mathrm{DCT(RMS)}} + \underbrace{\frac{\pi}{2\sqrt{2}n} D(t) I_o}_{Ie\_\mathrm{PPP(RMS)}}. \end{cases} \tag{16}$$

From the $V_{e(\mathrm{RMS})}$(t) and $I_{e(\mathrm{RMS})}$(t), the equivalent ac resistance of $R_e$(t) and $P_e$(t) are can be obtained as follows:

$$R_e(t) = \frac{V_{e(\mathrm{RMS})}(t)}{I_{e(\mathrm{RMS})}(t)} = \frac{8n^2}{\pi^2 m_1 [m_1 + D(t)]^2} R_o \tag{17}$$

$$P_e(t) = V_{e(\mathrm{RMS})}(t) \cdot I_{e(\mathrm{RMS})}(t) = V_o I_o = P_o \,(\text{constant}). \tag{18}$$

Fig. 8 shows the power analysis of the PPP *LLC* resonant converter at a period of $1/f_m$, using the turn ratio of 18:4:4:1:1, $f_{r1}$ of 300 kHz, which are designed parameters in Section III. $R_o$ is fixed to the rated load. The switching frequency changes within the range of [260, 340 kHz] under a nominal input voltage of 400 V. When the switching frequency is lower than the center frequency (300 kHz) ([0, 0.005 s]), $V_{e(\mathrm{RMS})}$ increases, and the power delivered through the single-stage path ($P_{e\_\mathrm{DCT}}$)

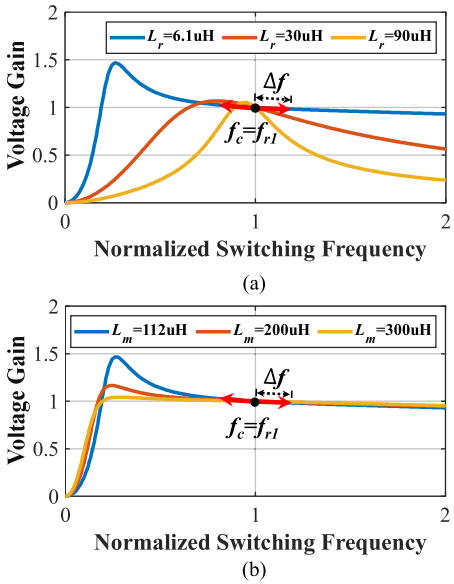


Fig. 9. Voltage gain curves. (a) According to resonant inductances. (b) According to magnetizing inductances under $L_r = 6.1\ \mu$H.

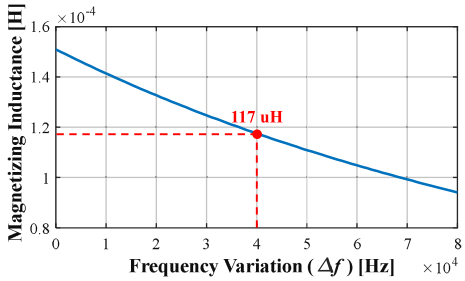


Fig. 10. Maximum magnetizing inductance curve according to the operating frequency variation.

increases. To compensate for the power increment ($V_{o1}$ increment), the duty ratio is reduced which decreases $V_{o3}$ and $I_{e(\mathrm{RMS})}$ by (5) and (16). $R_e$ is increased due to a reduction in $I_{e(\mathrm{RMS})}$. As a result, the power transmitted through the two-stage path ($P_{e\_\mathrm{PPP}}$) is diminished as shown in Fig. 8(g). In contrast, at ([0.005, 0.01 s]), the duty cycle is increased, which $I_{e(\mathrm{RMS})}$ increases. Therefore, $R_e$ decreases, and the power transmitted through the two-stage path increases. Since $V_{e(\mathrm{RMS})}$ and $I_{e(\mathrm{RMS})}$ change in inverse proportion according to duty ratio variation in both cases, the power delivered to the load is constant by (18). It means that the output voltage is tightly regulated.

## III. Power Stage Design

### A. Resonant Inductance Design

To minimize the output voltage fluctuation due to the SSM, the change in voltage gain should be insensitive to the switching frequency variations. Therefore, a small quality factor is required to get a flat voltage gain change. The quality factor of the PPP *LLC* resonant converter can be derived as follows:

$$Q = \frac{\sqrt{L_r/C_r}}{R_e} \tag{19}$$

where $R_e$ is assumed to be the equivalent ac resistance at the rated load resistance, where the quality factor is maximum.

Fig. 9(a) shows the voltage gain curves of the PPP *LLC* converter according to the resonant inductances where $f_{r1}$ is 300 kHz and $L_m$ and turn numbers are the values designed in Section III-B and C, respectively. As $L_r$ increases, the slope of the voltage gain at $f_{r1}$ becomes steeper due to the increment of the quality factor. It can result in large output voltage fluctuation. Therefore, small $L_r$ is effective to mitigate the output voltage fluctuation. The small $L_r$ can be obtained by the high coupling coefficient among the windings. By manufacturing the transformer, $L_r$ is determined, then $C_r$ can be selected according to the measured $L_r$ for obtaining a targeted resonant frequency. Therefore, the quality factor can be determined.

### B. Magnetizing Inductance Design for ZVS Capability

Fig. 9(b) shows the voltage gain curves according to the magnetizing inductance under the fixed resonant inductance. As the magnetizing inductance increases, the difference between the series and parallel resonant frequencies increases due to the parallel resonant frequency decrement. It induces the flat voltage gain variation at the series resonant frequency. Therefore, it is effective to use large magnetizing inductance. However, the *LLC* DCT can lose the ZVS capability due to the magnetizing current decrement.

To ensure the ZVS capability of the *LLC* DCT, the magnetizing current should be designed to discharge the output capacitance of the power switches during the dead time. The ZVS condition is expressed as follows:

$$\begin{cases} I_{m,\mathrm{peak}} \cdot t_d \geq 2C_{oss} \cdot V_{\mathrm{in}} \\ I_{m,\mathrm{peak}} \simeq \frac{V_{\mathrm{in}}(T_s/2 - t_d)}{4L_m} \end{cases} \tag{20}$$

where $I_{m,\mathrm{peak}}$ is the peak magnetizing current, $t_d$ and $C_{oss}$ is the dead time and the output capacitance of the power switch, respectively. The dead time of $t_d$ has 5% of the switching period. During the SSM operation, the magnetizing current changes due to the switching frequency variation. The peak current of the magnetizing current is minimized at $f_c + \Delta f$. Therefore, the maximum magnetizing inductance to ensure the ZVS capability can be derived as follows:

$$L_m \leq \frac{(T_{s,\min}/2 - t_d)\, t_d}{8C_{oss}} = L_{m,\max} \tag{21}$$

where $T_{s,\min} = 1/(f_c + \Delta f)$. Fig. 10 shows the maximum magnetizing inductance curve according to frequency variation. Since $T_{s,\min}$ decreases according to the increment of $\Delta f$, the lower maximum magnetizing inductance is required under the higher $\Delta f$.

### C. Transformer Turn Number and $\Delta D$ Design

Since the quality factor can be determined using the $L_r$ and $L_m$ under each turn number, $\Delta V_{o1}$ can be calculated by (10) and (19). Therefore, the turn number of the transformer can be selected considering power conversion efficiency and output

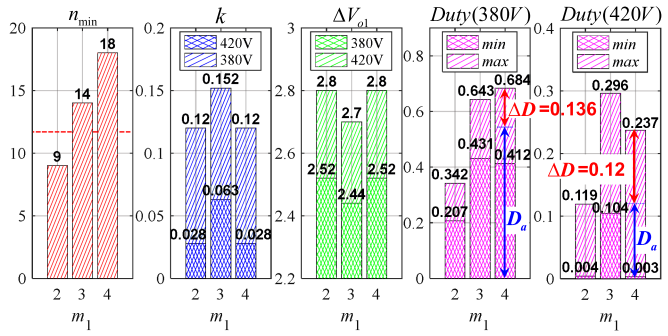


Fig. 11. Parameters at the minimum $n$ according to $m_1$.

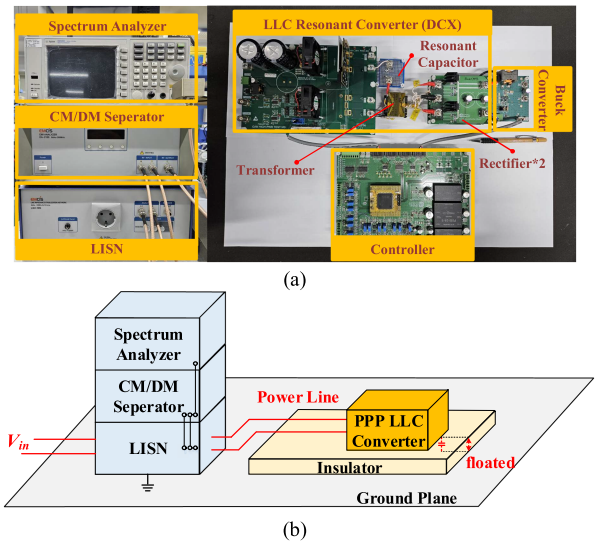


Fig. 12. Experimental setup of the 500 W prototype PPP *LLC* resonant converter. (a) Experimental setup. (b) EM noise measuring setup.

voltage regulation performance. As analyzed in Section II-B, the turn ratio with the minimum partial power ratio should be selected to obtain high power conversion efficiency.

However, the minimum partial power ratio does not guarantee compensation for voltage fluctuations due to the SSM. Therefore, it is necessary to determine whether the voltage fluctuation can be compensated within the duty ratio. Fig. 11 shows the parameters at the minimum $n$ according to $m_1$, which is selected at the minimum $k$ under the maximum voltage of 420 V as shown in Fig. 3. Only $m_1 = 2$ to $m_1 = 4$ are considered because a small $k$ of 0.5% at $n = 22$, $m_1 = 5$ cannot compensate for voltage fluctuations by the SSM, and $n = 5$, $m_1 = 1$ has high $k$. At each turn number, the duty variations to compensate for $\Delta V_{o1}$ in the maximum and minimum voltage conditions are all within the buck converter control range. Therefore, the turn numbers can be selected between $n = 9$, $m_1 = 2$, and $n = 18$, $m_1 = 4$, which results in the minimum partial power ratio. Considering the minimum turn numbers to avoid the transformer saturation shown in Fig. 11 with the red line, $n = 18$, $m_1 = 4$ is selected. The condition of the primary turn number can be expressed as follows:

$$N_{p,\min} = \frac{V_{\text{in,max}}}{2} \cdot \frac{1}{4B_{\max}A_e f_{s,\min}} \tag{22}$$

where $V_{\text{in,max}}$ is the maximum input voltage, $B_{\max}$ is the maximum flux density, $f_{s,\min}$ is the minimum switching frequency, and $A_e$ is the effective cross-sectional area of the transformer. At this point, the buck converter can obtain tight output voltage regulation capability under SSM with partial power control from 2.8 to 12% according to the input voltage.

Since $\Delta V_{o1}$ changes according to the input voltage, an effective $\Delta D$ selection is required to compensate for the voltage fluctuation caused by the SSM. If $\Delta D$ is designed by considering the maximum or minimum voltage given by (12), the compensation performance of the output voltage fluctuation according to the input voltage can be degraded. For example, if $\Delta D$ of 0.12 is designed based on 420 V, $\Delta V_{o1}$ of 2.8 V can be compensated. However, since the required $\Delta D$ is higher than the 420 V case in the 380 V case, the output voltage cannot be compensated entirely. Therefore, $\Delta D$ should be designed based on the nominal voltage of 400 V to minimize the difference in voltage compensation performance depending on the input voltage. $\Delta D$ of 0.128 is required for a 400 V, which is the middle value of $\Delta D$ at 380 and 420 V.

## IV. Experimental Results

Fig. 12 shows the experimental setup of a 500-W prototype PPP *LLC* resonant converter, which includes a digital controller (TMS320F28379D, TI), a spectrum analyzer (9320B, Keysight), a common mode (CM)/differential mode (DM) noise separator (EA-2100, EMCIS), a line impedance stabilization network (LISN) (LN-16N, EMCIS). The PPP *LLC* converter is floated from the ground plane by an insulator, allowing conducted noise to flow through parasitic components as shown in Fig. 12(b) [27]. A LISN is connected to the ground plane and provides the conducted noise measured with respect to the ground plane as a reference. In addition, the power analyzer (WT5000, YOKOGAWA) is used to measure the efficiency of the prototype converter. The specifications and parts numbers are described in Table II.

Fig. 13 shows the experimental waveforms of the PPP *LLC* resonant converter in the steady state at 500 W under the nominal input voltage. Under no SSM, the *LLC* DCT operates with a fixed switching frequency. The output voltage of the PPP *LLC* resonant converter maintains 48 V with a small voltage fluctuation of 0.55 $V_{pp}$ (1.1%). In contrast, under the SSM without the output voltage compensation, the switching frequency changes by 40 kHz based on a center frequency of 300 kHz. It induces high output voltage fluctuation with 3.68 $V_{pp}$ (7.7%) due to the frequency-dependent voltage gain characteristics of the *LLC* resonant converter. However, under the SSM with the output voltage compensation by the PPP buck converter, since $\Delta V_{o1}$ is compensated by the feedforward controller, the output voltage is tightly regulated within 1.24 $V_{pp}$ (2.5%).

Fig. 14 shows the experimental voltage and current waveforms of the *LLC* DCT according to load variations at the maximum and minimum input voltages. The switching frequency

TABLE II
SPECIFICATIONS AND PARTS NUMBER OF COMPONENTS

| Parameter | | LLC DCT | PPP LLC | Two-Stage |
|---|---|---|---|---|
| $V_{in}$ | | 400 V | 380-420 V | 400 V |
| $V_o$ | | 48 V | | |
| $R_o$ | | 4.608 Ω (500 W) ~23.04 Ω (100 W) | | |
| $L_r$ | | 6.1 μH | | 5 μH |
| $L_m$ | | 112 μH | | |
| $C_{oss}$ | | 207 pF | | |
| $L_{buck}$ | | 22 μH | | |
| $\Delta f$ | | - | 40 kHz | - |
| $f_m$ | | - | 100 Hz | - |
| $f_c$=$f_{r1}$=$f_{buck}$ | | 300 kHz | | |
| Turn ratio | | 18:4:4 | 18:4:4:1:1 | 18:5:5 |
| Controller | $P$ gain | - | 0.2 | |
| | $I$ gain | - | 187 | |
| | $\Delta D$ | - | 0.128 | - |
| $C_r$ | | 56 nF | | 46 nF |
| $C_{o1}$ | | 272 uF | | - |
| $C_{o2}$ | | - | 240 uF | |
| $C_{o3}$ | | - | | |

| Components | LLC DCT | PPP LLC | Two-Stage |
|---|---|---|---|
| LLC Converter's switch | GS66516B-MR | | |
| Buck Converter's switch | GS61008P | | |
| Transformer core | PQ 40/40, N97 | | |
| Secondary rectifier | NTST30100CTG | | DST20150C |
| Tertiary rectifier | - | DSTF4050C | - |
| $C_r$ | B32652A7223J, B32652A7333J | | B32653A0473J |
| $C_{o1}$ | 50SVPF68M | | - |
| $C_{o2}$ | - | 35SVPF120M | |
| $C_{o3}$ | - | | |

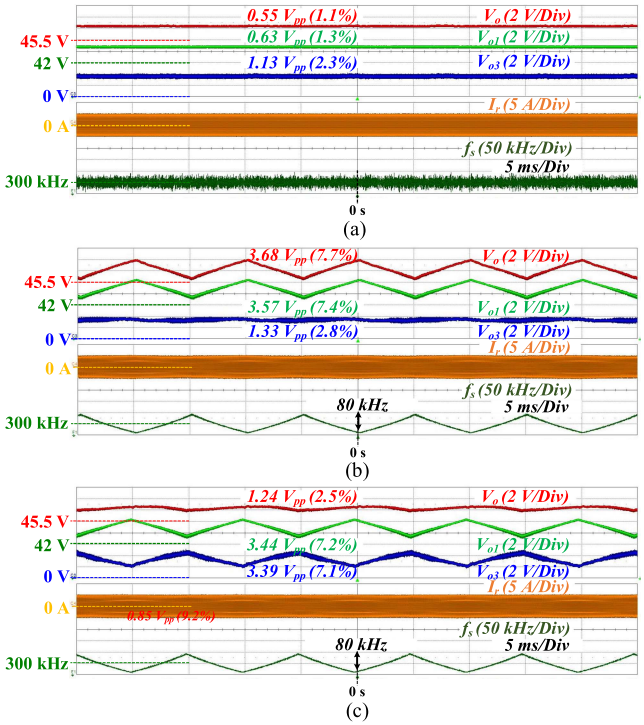


Fig. 13. Experimental waveforms of the PPP *LLC* resonant converter in the steady state at 500 W under the nominal input voltage. (a) No SSM. (b) SSM without compensation. (c) SSM with compensation.

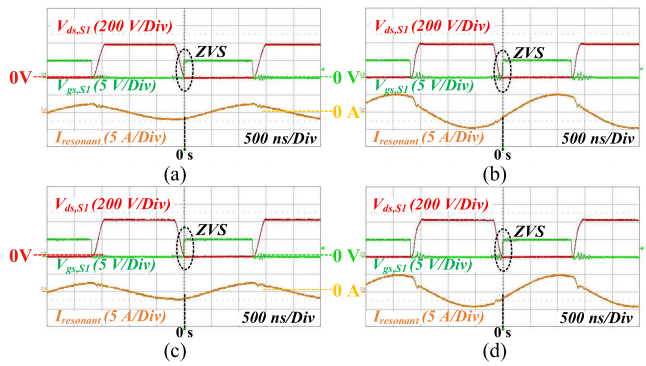


Fig. 14. Experimental voltage and current waveforms of the PPP *LLC* resonant converter at $f_c + \Delta f$. (a) 100 W at $V_{\rm in} = 380$ V. (b) 500 W at $V_{\rm in} = 380$ V. (c) 100 W at $V_{\rm in} = 420$ V. (d) 500 W at $V_{\rm in} = 420$ V.

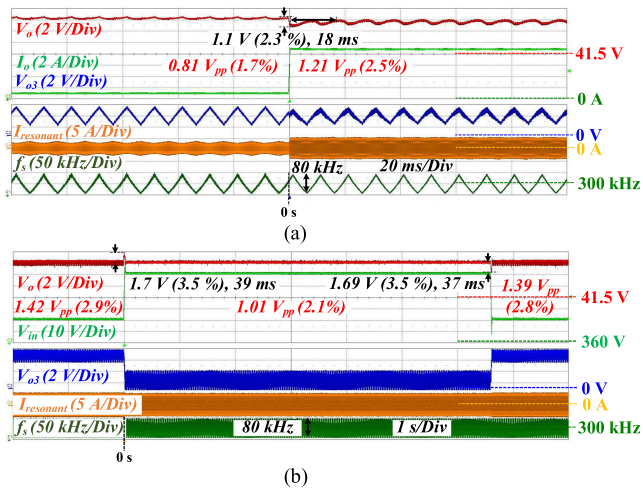


Fig. 15. Experimental waveforms of dynamic responses. (a) 10 to 90% load change at 400 V. (b) Input voltage changes between 380 and 420 V.

of the PPP *LLC* resonant converter is fixed at 340 kHz ($f_c + \Delta f$), which is the worst case described in Section III-B. The power switches achieve the ZVS over the entire load range since the switch turns on after its drain-source voltage is completely discharged.

Fig. 15 shows the dynamic responses of the PPP *LLC* resonant converter. When the load changes from 1.04 (10%) to 9.38 A (90%), undershoot and settling time are observed as 1.1 V (2.3%) and 18 ms, respectively. In addition, the output voltage is stably regulated under the SSM operation within 1.21 $V_{pp}$ (2.5%). In the case of the input voltage transient response, overshoot and undershoot are measured within 1.7 V (3.5%), and settling time is observed within 39 ms. The output voltage is regulated under voltage ripples within 1.42 $V_{pp}$ (2.9%) at each input voltage.

TABLE III
OUTPUT VOLTAGE REGULATION PERFORMANCE

| Steady state | | | |
|---|---|---|---|
| | No SSM | SSM without compensation | SSM with compensation |
| $V_{o1,pp}$ | 0.63 (1.3 %) | 3.57 (7.4 %) | 3.44 (7.2 %) |
| $V_{o3,pp}$ | 1.13 (2.3 %) | 1.33 (2.8 %) | 3.39 (7.1 %) |
| $V_{o,pp}$ | **0.55 (1.1 %)** | **3.68 (7.7 %)** | **1.24 (2.5 %)** |
| **Transient state** | | | |
| | Load transient 10 % to 90 % | | Input transient Between 380 V to 420 V |
| $V_{o,pp}$ | **< 1.21 (2.5 %)** | | **< 1.7 (3.5 %)** |

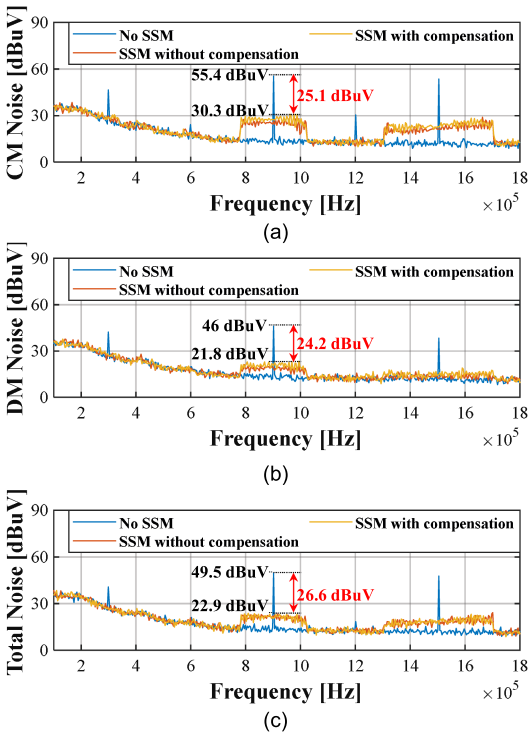


Fig. 16. Measurements of the conducted EM noise reduction performance. (a) Common mode noise. (b) differential mode noise. (c) Total noise.

Although the SSM is conducted, the output voltage is tightly regulated by the proposed method without significant output voltage fluctuations in the transient states. The output voltage regulation performance is summarized in Table III.

Fig. 16 shows the measurements of the conducted EM noise reduction performance. Under the SSM, compared with the fixed switching frequency, CM and DM noises are reduced to 30.3 and 21.8 dB$\mu$V, respectively. In addition, the total conducted EM noise is reduced to 22.9 dB$\mu$V in the peak value manner, which is consistent with the designed reduction performance in Section II-C. The conducted EM noise reduction performances are summarized in Table IV. Noise reduction performance is not affected by the proposed voltage compensation method.

To verify the improvement in power conversion efficiency, the *LLC* DCT, the PPP *LLC* resonant converter, and the two-stage structure are configured. The *LLC* DCT is constructed by opening the tertiary winding of the transformer in the PPP *LLC* resonant converter. At the same time, the conventional

TABLE IV
CONDUCTED EM NOISE REDUCTION PERFORMANCES

| | No SSM | SSM without compensation | SSM with compensation |
|---|---|---|---|
| Peak CM noise | 55.4 dBuV | 29 dBuV | 30.3 dBuV |
| Peak DM noise | 46 dBuV | 21 dBuV | 21.8 dBuV |
| Peak total noise | 49.5 dBuV | 23.3 dBuV | 22.9 dBuV |

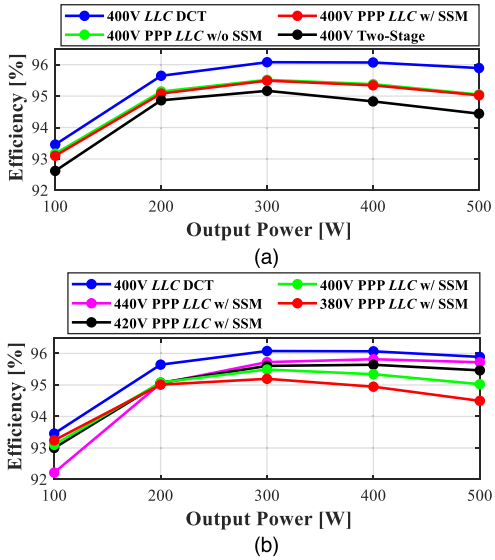


Fig. 17. Measured power conversion efficiency curves. (a) According to different converters. (b) According to input voltage.

two-stage structure is constructed by connecting an *LLC* DCT and a buck converter in series. However, since the output voltage of the *LLC* DCT used in the PPP *LLC* resonant converter is less than 48 V, the output voltage cannot be regulated under the series configuration with the buck converter. Therefore, the turn number of the secondary winding of the *LLC* DCT is increased to five turns, which requires a high voltage rating rectifier, and a series connection of two capacitors. For a fair comparison, the resonant frequency, the power switch, and the transformer core selected in each prototype are the same.

Fig. 17 shows measured power conversion efficiency curves. Due to the single power conversion, the *LLC* DCT shows the best efficiency under the entire load range, especially the maximum of 96.08% at 300 W under the nominal input voltage. However, the output voltage regulation cannot be conducted according to load variations. Although the conventional two-stage structure can regulate the output voltage, it shows the worst efficiency due to the two-stage power conversion. The efficiency is 94.44% at the rated power of 500 W. In contrast, the PPP *LLC* transfers most of the power through the *LLC* DCT, and only 7% of the entire power is delivered by the two-stage power conversion under the nominal input voltage. The maximum efficiency is 95.49% observed at 300 W, 0.59% lower than *LLC* DCT and 0.32% higher than the two-stage structure. The efficiency is 95.03% at 500 W. There is no difference in efficiency according to the operation of the SSM. The higher efficiency can be obtained

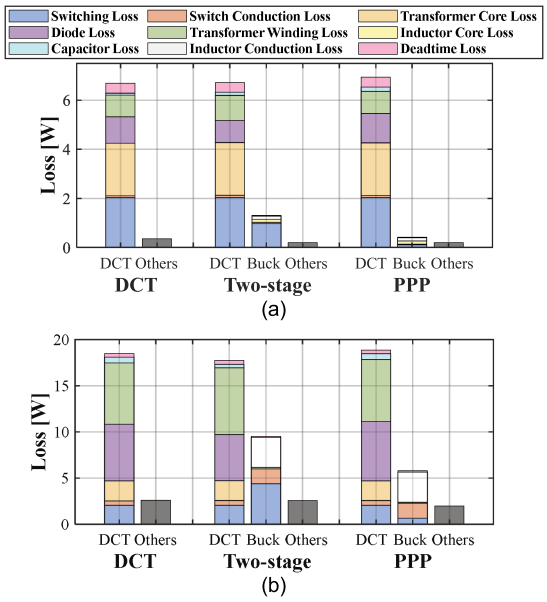


Fig. 18. Loss breakdown and comparison at nominal input voltage among the three alternative converter types. (a) 100 W. (b) 500 W.

under the higher input voltage as shown in Fig. 17(b). Since the output voltage of the DCT increases as the input voltage increases, it reduces the amount of partial power processed by the buck converter. The maximum efficiency of 95.82% is observed at the 440 V 400 W case. However, the PPP *LLC* operates as the DCT since the output voltage exceeds the nominal voltage of 48 V. Compared with the 400 V DCT case, it shows lower efficiency due to higher switching loss and core loss caused by the increment in input voltage. Under the regulation ranges, the PPP *LLC* has a maximum efficiency of 95.64% at 420 V 400 W.

Fig. 18 shows the loss breakdown and comparison at the nominal input voltage among the three alternative converter types. The power losses are calculated based on the loss model of [28], [29]. At 100 W, the total losses at the DCT in the three converters are similar. The transformer core loss and the switching loss account for a large proportion due to the high switching frequency. In the PPP structure, 11 V is input to the buck converter. In contrast, 55 V of the total output voltage of the DCT is input to the buck converter in the two-stage structure, which causes high switching loss. At 500 W, the conduction loss becomes dominant due to the increment of diode and transformer conduction losses. The number of diode rectifiers used in the two-stage structure is less than in the case of the PPP structure. In addition, the relatively high output voltage of the DCT is applied to the rectifier. Therefore, the two-stage structure has relatively low diode conduction loss. However, the switching losses in the buck converter are much bigger than in the 100 W case due to high voltage stress. In contrast, the PPP structure consumes relatively small power in the buck converter. Therefore, the proposed converter can obtain EM noise reduction, tight output regulation, and high power conversion efficiency.

TABLE V
COMPARISON AMONG DIFFERENT METHODS

| | [23] | [24] | Proposed Method |
|---|---|---|---|
| Power switches | 4 | 4 | 4 (2) |
| Diodes | 2 | 4 | 4 (2) |
| Transformers | 1 | 2 | 1 |
| Resonant capacitors | 1 | 2 | 1 |
| Inductors | 1 | 2 | 2 (1) |
| Control strategy and complexity | PFM + PSM (Complex) | PFM (Simple) | PWM (Simple) |
| Applicable structure | Full-bridge only | Multiple converter configuration only | Half & Full bridge |
| **Cost-effectiveness** | **Middle** | **Low** | **High** |

## V. DISCUSSION

Compared with the previous methods shown in [23] and [24] for mitigating the output voltage fluctuation under the SSM in *LLC* resonant converters, the cost-effectiveness and power conversion efficiency have been improved by the proposed method.

### A. Cost-Effectiveness

Table V represents the comparison among different methods. In [23], a hybrid control combining the PSM and PFM is performed to compensate for the output voltage fluctuation due to the SSM. Due to the PSM operation between switching legs under the steady-state operations, the hybrid control algorithm is limited to the full-bridge structure. Therefore, four rated power switches are required. Furthermore, twice the minimum number of turns not to be saturated is required compared with the half-bridge at the same $B_{\max}$ and $A_e$, which increases the volume of the transformer. Although the total number of active devices is larger than [23] due to the additional PPP converter, two tiny-rated diodes are additionally required, and the rated power switches are only two. In addition, the small filter inductor of the buck converter is required since the PPP converter handles a small portion of the output voltage. The work [23] has a complicated control scheme, and the SSM cannot be performed in the transient state due to the increment of the circulating current by the PSM control. In contrast, the work [24] has the simplest control. The output voltage fluctuation is compensated by the phase-shifted SSM operation using two *LLC* resonant converters with a series-connected output stage, which requires two transformers. Due to the multiple converter structure, it has poor cost-effectiveness. In both works [23] and [24], the high quality factor is required to regulate the output voltage by the PFM, which can require an additional inductor in addition to the leakage inductance of the transformer. In contrast, the proposed method only requires one transformer with an additional two turns on the tertiary side, and the resonant inductance is replaced by small leakage inductance. As a result, the proposed method shows high cost-effectiveness.

### B. Power Conversion Efficiency

In [23] and [24], the voltage fluctuation due to the SSM is compensated by full power control. Both converters use the PFM control under each load condition. This means that the switching

frequency moves away from the series-resonant frequency as the load current decreases. Since it increases reactive power and circulating current, power conversion efficiency deteriorates. In contrast to previous methods, the operating frequency under the proposed method is always aligned to the series-resonant frequency during the SSM operation regardless of the load current. In addition, the two-stage power conversion is minimized by allowing the PPP converter to compensate only for the output voltage fluctuation caused by the SSM. Therefore, EM noise reduction performance, tight output voltage regulation, and high power conversion efficiency can be simultaneously obtained by the proposed method.

## VI. Conclusion

This article proposes the output voltage regulation method using the PPP concept, which can obtain EM noise reduction, output voltage regulation, and high power conversion efficiency, simultaneously. The *LLC* DCT performs the SSM with the center frequency aligned to the series resonant frequency to reduce the EM noise. The voltage fluctuations due to the SSM can be compensated by the buck converter composed of PI and feedforward controllers using tiny partial power. Compared with conventional methods using full power regulation for compensation [23], [24], high cost-effectiveness and high power conversion efficiency can be obtained. In addition, unlike [23], the SSM can be performed even in transient operating conditions. In the experiment results, the output voltage is tightly regulated under the steady state operations within 1.24 $V_{pp}$ (2.5%) and even in the transient state within 1.7 $V_{pp}$ (3.5%) under the rated power of 500 W. The CM, DM, and total noise are reduced to 30.3, 21.8, and 22.9 dB$\mu$V, respectively. The above performances are obtained by the 2.8–12% partial power regulation through the PPP buck converter. Finally, the PPP *LLC* resonant converter shows a maximum efficiency of 95.49% under nominal input voltage at the expense of 0.59% efficiency of the *LLC* DCT.

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