Simultaneous Power and Data Modulation Scheme for *LLC* Resonant Converter

Keming Liu, *Graduate Student Member, IEEE*, Yue Hui, *Graduate Student Member, IEEE*,
Jinghui Chen, *Graduate Student Member, IEEE*, Jiande Wu, *Member, IEEE*, and Xiangning He, *Fellow, IEEE*

***Abstract*—Power and signal dual modulation (PSDM) integrates communication functions in power converters, providing an appropriate communication method for power electronics systems. This article discusses the theory and implementation of PSDM in resonant converters. The data are modulated into a resonant converter's gate signal and then transmitted along with power. The fundamental principles of the proposed PSDM modulation are analyzed in detail, and a novel PSDM scheme is proposed. The decoupling between data modulation and power control is realized in the communication process. Furthermore, the design considerations of converter parameters regarding their influence on the output voltage gain are given to evaluate the reliability of the proposed PSDM scheme. Finally, a 500 W prototype with a resonant frequency of 180 kHz is set up, and the experiment achieves a 4.5 kbps bitrate using the proposed modulation scheme, demonstrating the correctness of the scheme.**

***Index Terms*—Power and signal dual modulation (PSDM), power electronics system (PES) communication, resonant dc–dc converter.**

I. INTRODUCTION

POWER electronics systems (PES), which have been used extensively in microgrids, renewable energy generation, and energy storages, are of crucial importance in solving the energy crisis [1], [2], [3]. The performance of PES heavily relies on its communication system [4], which is critical for system condition monitoring, fault diagnosis, energy management, system protection, and flexible control. Therefore, communication in PES has been a main research topic.

Different communication methods, including fieldbus communication, wireless communication, and power line communication, have been applied in PES [5], [6], [7]. However, considering hardware volume, costs, security, and real-time control performance, the mentioned communication methods cannot satisfy the various requirements of PES.

Recently, a novel simultaneous power and information modulation scheme called power and signal dual modulation (PSDM), also dubbed talkative power conversion, has demonstrated the capability to satisfy the PES communication requirements [8], [9], [10], [11]. By embedding information into power using power electronics converters, PSDM can realize simultaneous power conversion and signal generation while multiplexing the power buses as communication wires. As a result, no specialized communication hardware or wires are required for signal transmission, reducing the volume, complexity, and costs of the system. Moreover, power converters are integrated with the communication links, providing good real-time control performance, high reliability, and strong robustness.

PSDM schemes are classified as PSDM by controlled ripple (PSDM-CR) and PSDM by switching carrier (PSDM-SC) [12]. PSDM-CR superimposes signals on the duty cycle in pulse width modulation (PWM), and the converters are controlled to produce low-frequency signals at their input/output ports [13], [14], [15], [16]. A typical power talk strategy is proposed in [13] for direct current microgrids to realize communication, which achieves a bitrate of 0.001–100 bps using baseband data transmission. To broaden the application, [14] discusses the virtual resistance optimization methods to maximize the effective signal-to-noise ratio, but the communication rate is still limited by the baseband data transmission. To achieve a higher communication rate, [15] introduces a phase-control-based carrier into the control loop of the photovoltaic optimizer as the data carrier, and a 2 kbps communication rate is obtained among optimizers. Besides, in [16], orthogonal frequency division multiplexing (OFDM) is applied to enhance the communication rate to 9.6 kbps by increasing frequency band utilization. PSDM-CR is capable of adjusting the signal amplitude to meet the requirements of different applications. However, it is hard to achieve a high communication rate due to the low-frequency control of the duty cycle.

PSDM-SC modulates data into the PWM carrier by controlling its phase or frequency and takes the output ripples of power converters as the data carriers. With the high carrier frequency, a high communication rate can be achieved. In [17], [18], [19], [20], and [21], PSDM-SC schemes using frequency shift keying (FSK) are proposed to integrate data transmission with power conversion. M-ary FSK modulation employs M frequencies as carrier frequencies, thereby enhancing the communication rate [22]. Nevertheless, M-ary FSK requires a larger bandwidth, and the available bandwidth of the converter is limited, which hinders its implementation. To improve the bitrate, modulation schemes including differential phase shift keying (DPSK) and quadrature

---

Manuscript received 7 May 2023; revised 7 August 2023; accepted 26 September 2023. Date of publication 2 October 2023; date of current version 6 December 2023. This work was supported by National Natural Science Foundation of China under Grant 52350003. Recommended for publication by Associate Editor L. Corradini. *(Corresponding author: Jiande Wu.)*

The authors are with the College of Electrical Engineering, Zhejiang University, Hangzhou 310027, China (e-mail: liukeming@zju.edu.cn; yuehui@zju.edu.cn; chenjinghui@zju.edu.cn; eewjd@zju.edu.cn; hxn@zju.edu.cn).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3321120.

Digital Object Identifier 10.1109/TPEL.2023.3321120

TABLE I
LITERATURE COMPARISON

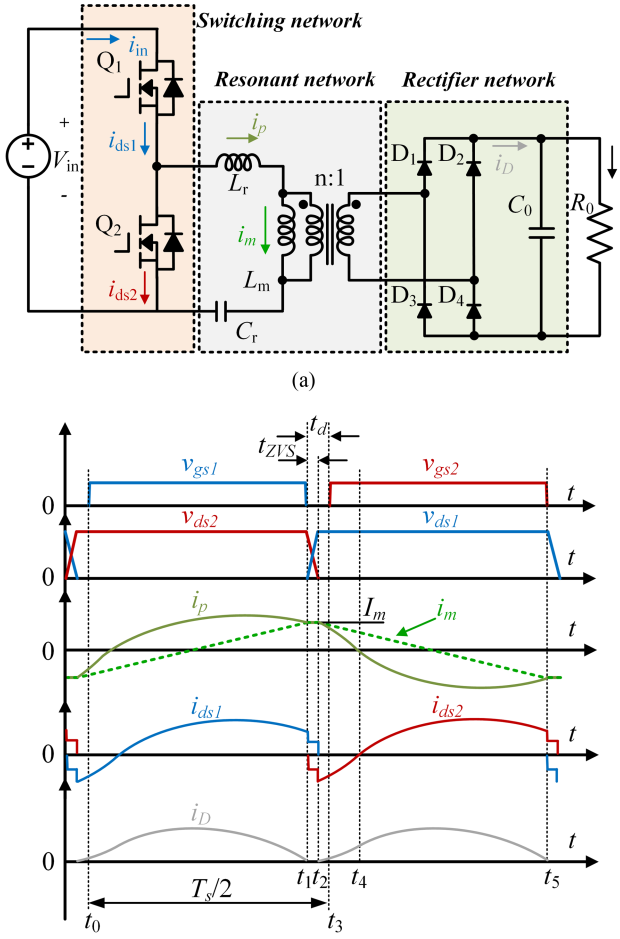
Reference	PSDM type	Topologies	Data modulation
[13]	PSDM-CR	Boost	Time division multiple access (TDMA)
[15]	PSDM-CR	Buck	DPSK
[16]	PSDM-CR	Buck, boost	OFDM
[19]	PSDM-SC	Buck	FSK
[23]	PSDM-SC	Phase shift full bridge (PSFB)	PSK
[24]	PSDM-SC	Two-phase buck	QAM
[26]	PSDM-SC	Buck	Frequency hopping–DPSK (FH–DPSK)

amplitude modulation (QAM) are applied in PSDM-SC [23], [24], [25], [26]. Chen et al. [27] investigate the compatibility of duty cycle, frequency, and phase in PWM and employ a control ripple and switching ripple combined modulation scheme, which further enhances the bitrate performance of PSDM. PSDM-SC is suitable for high-speed communication applications. However, the signal amplitude is determined by the passive components and cannot be adjusted by the software.

According to Table I, the mentioned PSDM schemes focus on communication improvement in nonresonant dc–dc converters. Only a few studies have been carried out on resonant dc–dc converters. In [28] and [29], FSK is achieved based on a *CLLC* converter with a bitrate of 60 bps, and no further improvement on the modulation scheme has been reported. However, resonant converters have higher efficiency and power density than hard-switching converters or soft-switching PWM converters [30], [31] and are widely used in on-board battery chargers, distributed power systems, renewable energy generation systems, etc. Therefore, this arttiicle aims to propose a new PSDM scheme for resonant dc–dc converters to further improve the bitrate. The main contributions of this article are as follows.

1) The control principles of duty cycle, frequency, and phase are discussed in detail, and a novel PSDM scheme is proposed.
2) The design considerations of converter parameters regarding their influence on the output voltage gain are discussed to maintain the power quality and realize reliable communication.
3) An experimental system is built, and reliable communication with a 4.5 kbps bitrate is achieved, which verifies the feasibility of the proposed PSDM scheme.

The rest of this article is organized as follows. Section II discusses the theoretical communication capability of duty cycle, frequency, and phase control and provides a control scheme when frequency and phase are applied for communication. In Section III, the design considerations of converter parameters are given. Section IV conducts the experiments to clarify the correctness of the theory and verify the feasibility of the proposed PSDM scheme. Finally, Section V concludes this article.



(a)

(b)

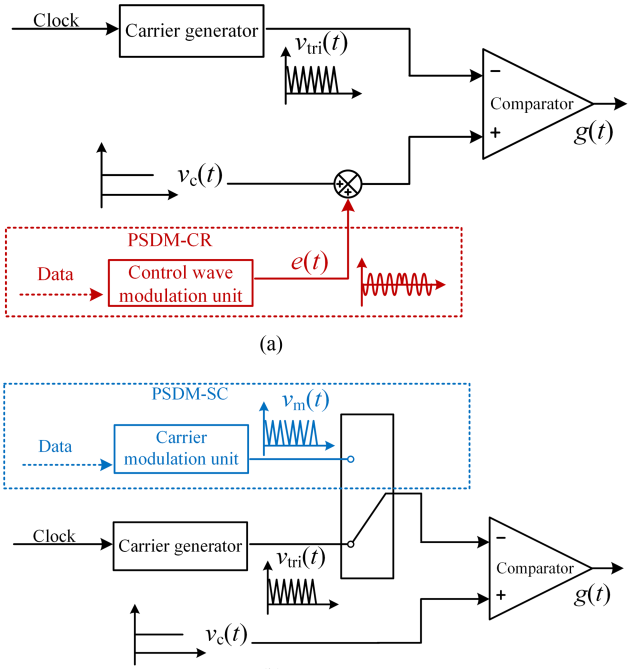
Fig. 1. Topology of half bridge DCX and critical waveforms. (a) Half bridge DCX circuit. (b) Critical waveforms.

II. PRINCIPLE OF PROPOSED MODULATION SCHEME

The fixed-frequency *LLC* converter, also known as a DC transformer (DCX), has good power performance and is convenient in system control and converter design. Thus, it has become a popular resonant dc–dc solution for various industrial applications [32], [33], [34]. Being a typical resonant dc–dc converter, DCX is chosen to be the topology for the theoretical analysis and the PSDM scheme design in this article.

The schematic of a half-bridge DCX with a full-bridge rectifier is depicted in Fig. 1(a). The voltage and current waveforms of the DCX are given in Fig. 1(b). v_{gs1},v_{gs2} and v_{ds1},v_{ds2} are the gate to source voltage and the drain to source voltage of Q_1 and Q_2, respectively. i_{m} is the magnetizing current, and i_{p} is the primary resonant current. i_{ds1} and i_{ds2} are drain to source current of Q_1 and Q_2, respectively. i_{D} is the rectified current. t_{d} is the dead time, and the zero-voltage switching (ZVS) process is realized in t_{ZVS}. The input current i_{in} is the same as the current i_{ds1}. Due to the symmetry of the operation, only half of the switching cycle t_0–t_3 in Fig. 1(b) are described below.

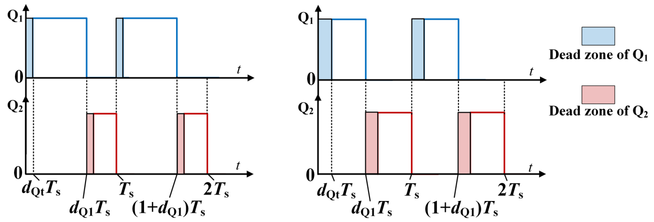
[t_0–t_1]: At t_0, v_{ds1} is already decreased to zero, and Q_1 is turned on with ZVS. L_{r} resonates with C_{r}, and the power is



(a)

(b)

Fig. 2. (a) Modulation diagram of PSDM-CR. (b) Modulation diagram of PSDM-SC.



(a) (b)

Fig. 3. Gate signals of primary mosfets Q_1 and Q_2 in one switching period. (a) Asymmetrical control mode. (b) Symmetrical control mode.

transferred from the primary side to the load. The voltage on L_{m} is clamped by the transformer reflected voltage of output voltage, so i_{m} increases linearly.

[t_1–t_2]: At t_1, Q_1 is turned off. Then, i_{m} charges Q_1 to V_{in} and discharges Q_2 to zero. The voltage on L_{m} is not clamped, so L_{m} starts resonating with L_{r} and C_{r}.

[t_2–t_3]: At t_2, the current through the body diode of Q_2, L_{r} starts resonating with C_{r}, and the power is transferred from the primary side to the load. L_{m} is clamped again. At t_3, v_{ds2} is already decreased to zero, Q_2 is turned on with ZVS, and the current shifts from the body diode to the channel of Q_2.

To realize power conversion, the conventional modulation scheme sets the duty cycle d to $1/2$, the switching frequency f_{s} to f_{r}, and the phase fixed, where f_{r} is the series-resonant frequency determined by

$$f_{\mathrm{r}} = \frac{1}{2\pi\sqrt{L_{\mathrm{r}}C_{\mathrm{r}}}}. \tag{1}$$

The existing PSDM schemes modulate data using the duty cycle, frequency, and phase of the converter's gate signal. Therefore, the three aspects are also used in the proposed PSDM scheme to achieve data modulation, and the detailed discussions are analyzed in this section.

A. Analysis About Data Modulation Capability of Duty Cycle

In PSDM-CR, modulated subcarriers $e(t)$ are superimposed on the reference wave $v_{\mathrm{c}}(t)$, and then compared with switching carrier $v_{\mathrm{tri}}(t)$ to modulate data into gate signal $g(t)$ as shown in Fig. 2(a). When PSDM-CR is applied, there are two methods to control the gate signal of DCX as shown in Fig. 3: asymmetrical and symmetrical control modes. However, both methods have respective drawbacks when applied to DCX.

In Fig. 3(a), asymmetrical gate signals mean that primary switches Q_1 and Q_2 have different duty cycles in a switching period T_{s}, which can be expressed as

$$\begin{cases} d_{\mathrm{Q1}} + d_{\mathrm{Q2}} = 1 \\ d_{\mathrm{Q1}} = d_{\mathrm{Qt}} + d_{\mathrm{Qv1}} \\ d_{\mathrm{Q2}} = d_{\mathrm{Q}t} + d_{\mathrm{Qv2}} \\ d_{\mathrm{Q1}}, d_{\mathrm{Q2}} \neq 0.5 \end{cases} \tag{2}$$

where d_{Q1} and d_{Q2} are duty cycle of Q_1 and Q_2 in T_{s}, respectively, and they consist of dead time part d_{Qt} and valid time part $d_{\mathrm{Qv}x}$ $(x = 1, 2)$. Data can be modulated into gate signals by changing d_{Q1} and d_{Q2}. Once applied in DCX, this type of gate signal brings the dc voltage component to the resonant capacitor C_{r}, and the dc component to the magnetizing inductor L_{m}. It is clear that C_{r} and L_{m} have higher voltage and current stress, making it harder for converter design and increasing costs. Moreover, the ZVS condition of the primary switches will be influenced, which is unacceptable for the converter. Thus, the asymmetrical gate signals cannot be adopted for simultaneous power and signal transmission.

In Fig. 3(b), symmetrical gate signals mean that primary switches Q_1 and Q_2 have the same duty cycle in a switching period, which can be expressed as

$$\begin{cases} d_{\mathrm{Q1}} = d_{\mathrm{Q2}} = 0.5 \\ d_{\mathrm{Q1}},\ d_{\mathrm{Q2}} = d_{\mathrm{Qt}} + d_{\mathrm{Qv}} \end{cases} \tag{3}$$

where d_{Q1} and d_{Q2} are duty cycle of Q_1 and Q_2 in T_{s}, respectively, and they have the same dead time part d_{Qt} and valid time part d_{Qv}. By changing d_{Qt} at different switching periods, data can be modulated into the gate signals. However, due to the ZVS of the primary switches being realized during [t_1, t_2] in Fig. 1(b), different rising edge moments t_3 within [t_2, t_4] of Q_2 bring the same current and voltage waveforms. In this case, the data is modulated only into the gate signals of DCX, but not transmitted along with power. Thus, the symmetrical-mode gate signals cannot be adopted for simultaneous power and signal transmitting as well. Consequently, the duty cycle should not be applied for data modulation.

B. Frequency Modulation Scheme

Data can be modulated into switching carrier using PSDM-SC in Fig. 2(b) by applying FSK. Because the switching frequency

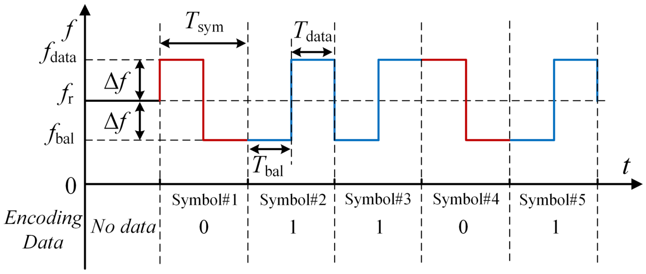


Fig. 4. Waveforms of SFPM.

f_{s} of the DCX is set constant for power control, the average value of f_{s} should remain constant if FSK is used. To achieve this goal, a specialized symmetrical frequency position modulation (SFPM) is developed, which is shown in Fig. 4, where f_{bal} is the balance frequency, f_{data} is the communication frequency, and Δf is the frequency interval between either f_{data} or f_{bal} and f_{r}. f_{data} and f_{bal} can be expressed as

$$\begin{cases} f_{\mathrm{data}} = f_{\mathrm{r}} + \Delta f \\ f_{\mathrm{bal}} = f_{\mathrm{r}} - \Delta f \end{cases} . \tag{4}$$

The amplitude of disturbance brought by the frequency change depends on the difference of f_{data} or f_{bal} to f_{r} and parameters of the resonant network within a symbol duration, the period numbers of f_{data} or f_{bal} are

$$\begin{cases} N_{\mathrm{data}} = f_{\mathrm{data}} \cdot T_{\mathrm{data}} \\ N_{\mathrm{bal}} = f_{\mathrm{bal}} \cdot T_{\mathrm{bal}} \\ T_{\mathrm{data}} = T_{\mathrm{bal}} = T_{\mathrm{sym}}/2 \end{cases} \tag{5}$$

where T_{data} and T_{bal} are duration of f_{data} and f_{bal}, respectively, N_{data} and N_{bal} are positive integers, and T_{sym} is the duration of a symbol. The sequential positions of communication carriers and balance carriers represent two digital numbers.

The rectifier network of DCX doubles the carrier frequency. Suppose the fundamental frequency component of the modulated square gate signal $s_{\mathrm{m}}(t)$ is

$$s_{\mathrm{m}}(t) = \mathrm{A_m} \cos(\omega_{\mathrm{c}} t + \omega_{\mathrm{c}} t_0) \tag{6}$$

where $\mathrm{A_m}$, ω_{c}, and $\omega_{\mathrm{c}} t_0$ are amplitude, angular frequency, and phase, respectively. With full-wave rectification applied, the rectified signal can be expressed as

$$s_{\mathrm{d}}(t) = |s_{\mathrm{m}}(t)| = \mathrm{A_m}\, |\cos(\omega_{\mathrm{c}} t + \omega_{\mathrm{c}} t_0)| \tag{7}$$

where $s_{\mathrm{d}}(t)$ is the rectified signal. As long as the sampling frequency f_{sample} satisfy the Nyquist sampling theorem signified in (8), where $f_{\max} = 2\max(f_{\mathrm{data}})$, demodulation will not be influenced by the rectification

$$f_{\mathrm{sample}} \geq 2 f_{\max}. \tag{8}$$

In conclusion, FSK and SFPM modulation can be combined in the proposed specialized symmetrical frequency encoding method, which increases the bitrate while keeping balanced power control.

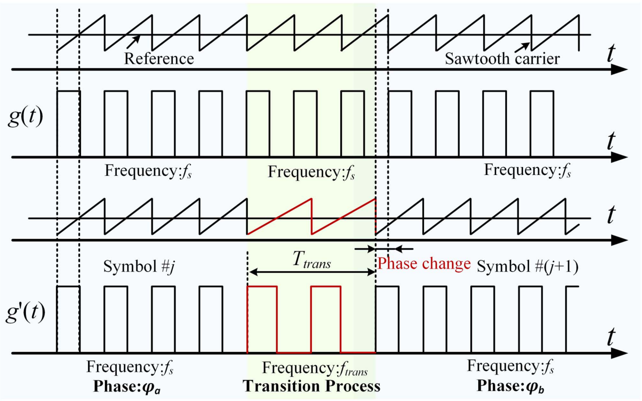


Fig. 5. Critical waveform of transition process.

C. Phase Control and Compatibility With Frequency

A transition process is inserted between two symbols for phase modulation. By controlling the duration of the transition process, the phase of the gate signal can be shifted from one to another, thereby avoiding abrupt phase changes that disturb the working condition of the devices in the converter.

Relevant waveforms are depicted in Fig. 5, where T_{trans} is the duration of transition process, and f_{trans} is the frequency during transition process defined as

$$f_{\mathrm{trans}} = f_{\mathrm{s}} + \Delta f_{\mathrm{trans}}. \tag{9}$$

To balance the power in the transition process, the average frequency difference of transition process should satisfy

$$\sum_{j=1}^{N} \Delta f_{\mathrm{trans}_j} \cdot T_{\mathrm{trans}_j} = 0 \tag{10}$$

where there are N transition process in a data frame, and $\Delta f_{\mathrm{trans}_j}$ and T_{trans_j} are frequency deviation and duration of j_{th} transition process, respectively. Suppose the communication frequency of $(j{+}1)_{\mathrm{th}}$ symbol is $f_{\mathrm{s}} + \Delta f_{\mathrm{data}}$, the total phase shift is decided by

$$\frac{K}{f_{\mathrm{s}} + \Delta f_{\mathrm{trans}_j}} = \frac{\varphi}{2\pi} \cdot \frac{1}{f_{\mathrm{s}} + \Delta f_{\mathrm{data}}} \tag{11}$$

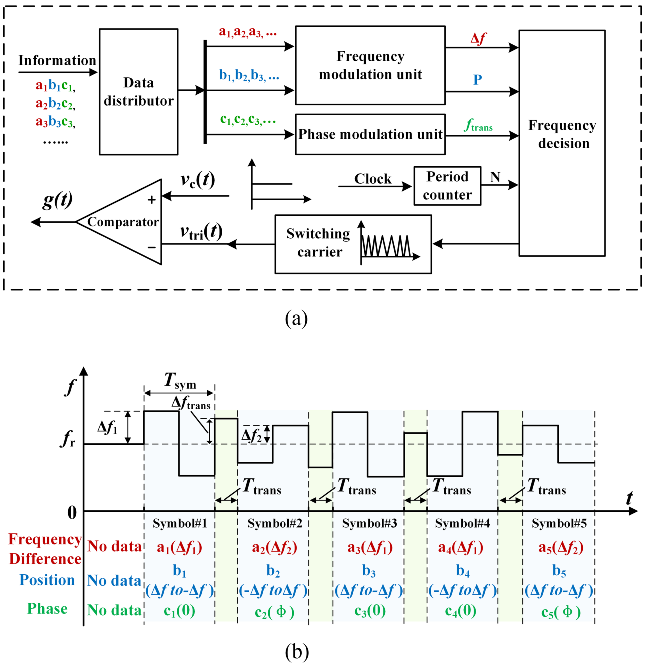
and it can be simplified as

$$\varphi = 2K\pi \cdot \frac{f_{\mathrm{s}} + \Delta f_{\mathrm{data}}}{f_{\mathrm{s}} + \Delta f_{\mathrm{trans}_j}} \tag{12}$$

where there are K periods in the duration of the transition process, φ is the phase shift of the $(j{+}1)_{\mathrm{th}}$ symbol.

D. Modulation and Demodulation Principles

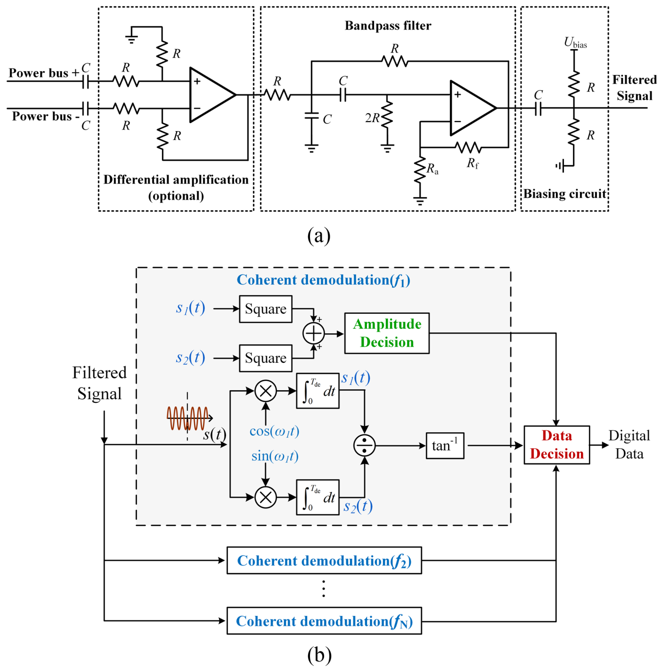
The proposed modulation process of the switching carriers is shown in Fig. 6(a). First, the input bits are split into frequency modulation and phase modulation bit streams. Then, the frequency difference Δf and the sequential position P are obtained according to the frequency data by the frequency modulation



(a)

(b)

Fig. 6. (a) Diagram of Carrier modulation unit. (b) Frequency waveform of proposed PSDM scheme.



(a)

(b)

Fig. 7. Diagram of demodulation process. (a) Voltage sensing circuit. (b) Demodulation process.

unit, and the frequency during the transition process f_{trans} is obtained according to the phase data by the phase modulation unit. The above frequency modulation and phase modulation units are controlled independently. The period counter is responsible for counting the number of periods in the communication process. Finally, the frequency decision unit determines the frequency of the switching carrier based on the three inputs Δf, P, and f_{trans}, the results are modulated switching carrier signals.

Fig. 6(b) indicates the frequency waveform of the proposed PSDM scheme. Different Δf represents different FSK modulation data. The SFPM not only helps keep the average frequency constant but also contains data, and there is one frequency shift from $f_{\text{s}} + \Delta f$ to $f_{\text{s}} - \Delta f$ or vice versa in every symbol. The phase modulation data is modulated only in the frequency component $f_{\text{s}} + \Delta f$ by the transition process. The proposed PSDM communication signal $s(t)$ of the i_{th} symbol can be expressed as

$$s\left(t\right) = \mathrm{A}_{\mathrm{m}} \cos\left[2\pi \left(f_{\mathrm{s}} + \Delta f_i\right) t + \varphi_i\right] \tag{13}$$

$$\varphi_i = \varphi_{i-1} + 2\varphi_{\max} \cdot \frac{d\left(i\right)}{M} \tag{14}$$

where A_{m}, $f_{\text{s}} + \Delta f_i$, φ_i are amplitude, frequency, and phase, respectively, $\varphi_{\max}$ is the maximum phase shift angle and it satisfies $\varphi_{\max} \leq \pi$, $d(i)$ is the i_{th} phase data, and *M* is the total number of the phase.

The proposed demodulation process is shown in Fig. 7. First, a differential amplifier (optional) and a bandpass filter (BPF) are used to extract the signal from the output voltage of the DCX as shown in Fig. 7(a). Then the demodulation is achieved by the DSP as shown in Fig. 7(b). The coherent demodulation is used to extract the frequency and phase of each carrier. The sequential position is acquired according to the results of coherent demodulation. Finally, corresponding data is obtained by the data decision unit.

Different communication frequencies should satisfy the orthogonal condition within a demodulation window

$$\int_0^{T_{\text{de}}} \cos\left(2\pi f_{\text{data}_k} t\right) \cos\left(2\pi f_{\text{data}_i} t\right) dt = 0 \tag{15}$$

where T_{de} is the duration of the demodulation window, f_{data} is the communication frequency, $k \neq i$, k, $i = 1, 2, \ldots, L$. The necessary and sufficient condition of (15) is

$$T_{\text{de}} = \frac{L}{f_{\text{data}}} \tag{16}$$

where $L \in \mathrm{N}^*$. Equation (16) implies that there should be an integral number of communication period in a demodulation window. Suppose the minimum frequency interval in (4) is $\Delta f_{\min}$, the minimum duration of the demodulation window $T_{\text{de\_min}}$ is

$$T_{\text{de\_min}} = \frac{1}{\Delta f_{\min}}. \tag{17}$$

III. Design Considerations

When the data modulation scheme in frequency and phase is applied, the design of the DCX should be optimized to achieve better performance. The optimizations include the design of the switching frequency, the choice of circuit elements, and the implementation of ZVS. Detailed discussions are analyzed and presented in this section.

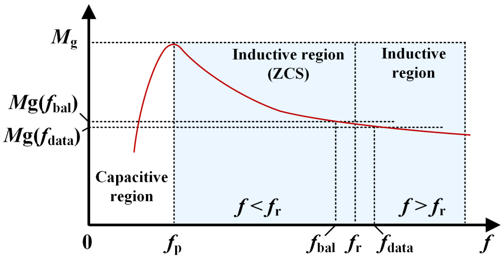


Fig. 8. Division of working frequency area and relationship between communication frequency range and gain perturbation range.

A. Frequency Design

Using fundamental harmonic analysis [35], the normalized input-to-output voltage-transfer function can be expressed as

$$M_\mathrm{g}=\left|\frac{L_\mathrm{n}\times f_\mathrm{n}^2}{[(L_\mathrm{n}+1)\times f_\mathrm{n}^2-1]+\mathrm{j}\,[(f_\mathrm{n}^2-1)\times f_\mathrm{n}\times Q_\mathrm{e}\times L_\mathrm{n}]}\right| \tag{18}$$

where $f_\mathrm{n}=f_\mathrm{s}\,/f_\mathrm{r}$ is the normalized frequency, $L_\mathrm{n}=L_\mathrm{m}\,/L_\mathrm{r}$ is the inductance ratio, $R_\mathrm{e}=\frac{8\times n^2}{\pi^2}\times R_\mathrm{o}$ is the ac equivalent resistance, R_o is the load, and $Q_\mathrm{e}=\frac{\sqrt{L_\mathrm{r}/C_\mathrm{r}}}{R_\mathrm{e}}$ is the quality factor. The gain curve of DCX is shown in Fig. 8, where the peak gain frequency f_p divides the figure into the capacitive region and inductive region. When $f_\mathrm{s}>f_\mathrm{p}$, the converter operates in the inductive region, which can be used for communication. When the converter sends data, the corresponding balance frequency f_bal and communication frequency f_data should satisfy

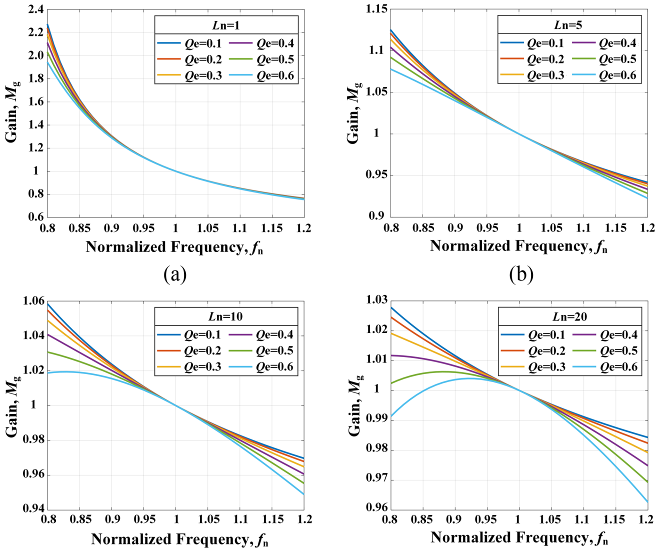
$$\begin{cases} f_\mathrm{p}<f_\mathrm{bal}<f_\mathrm{r}<f_\mathrm{data}\\ M_\mathrm{g}(f_\mathrm{bal})_\mathrm{min}\leq 1\leq M_g(f_\mathrm{data})_\mathrm{max}\\ f_\mathrm{range}=f_\mathrm{data}\,-f_\mathrm{bal}\end{cases} \tag{19}$$

where $M_\mathrm{g}(f_\mathrm{bal})_\mathrm{min}$ and $M_\mathrm{g}(f_\mathrm{data})_\mathrm{max}$ are permitted minimum and maximum gain, respectively. In order to avoid large gain perturbation caused by communication, the communication frequency range f_range should be less than 1/10 of f_r.

From the perspective of communication, the normalized frequency range decreases with increasing f_r, which brings smaller gain perturbation. Under a constant communication frequency range f_range, the higher f_r, the lower the gain perturbation. Meanwhile, as f_r increases, the converter becomes more compact, and the switching losses and ZVS become more significant. Nevertheless, f_r cannot be too high due to component bandwidth, board-layout concerns, magnetic-core losses, parasitic parameters, etc.

B. Influence of L_n and Q_e on Gain Function

L_n and Q_e are fixed once their physical parameters are determined. Fig. 9(a)–(d) illustrate the relationships between f_n and M_g under different L_n and Q_e, where the normalized frequency corresponding to the resonant peak moves with respect to the change in Q_e for a given L_n, and the operating point (f_n, M_g) = (11) is independent of L_n and Q_e.



(a) (b)

(c) (d)

Fig. 9. Gain with respect to L_n and Q_e at given conditions. $Q_e=0.1, 0.2, \ldots, 0.6$. (a) $L_n=1$. (b) $L_n=5$. (c) $L_n=10$. (d) $L_n=20$.

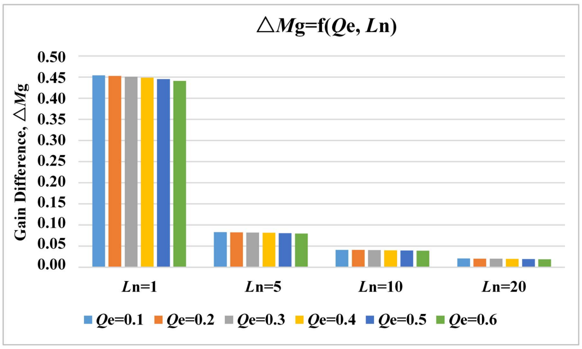


Fig. 10. Maximum gain difference with respect to L_n and Q_e in available communication range at given conditions.

The values of L_n and Q_e should keep the DCX working in the inductive region in the whole communication frequency range. Fig. 10 depicts the maximum relative gain difference ΔMg with respect to L_n and Q_e in the proposed communication frequency range ($f_\mathrm{n}\in[0.9, 1.1]$). When L_n is constant, the increasing Q_e brings a smaller amplitude of the gain perturbation. When Q_e is constant, a large L_n has a significant suppression on gain perturbation.

C. ZVS Realization

The primary-side switches' ZVS is realized by extracting the charge of the switches' parasitic output capacitors using the magnetizing current. The parasitic capacitance C_oss of primary-side switches is nonlinear, so the charge in the capacitor is not proportional to the rated capacitance during the ZVS process. According to [32], the average integral equivalent capacitance C_otr is in proportion to the charge in the capacitor, which helps describe the ZVS process precisely. According to Fig. 1(b), the ZVS condition of primary-side switches is given by

$$I_\mathrm{Lm}\geq\frac{2C_\mathrm{otr}V_\mathrm{in}}{t_\mathrm{ZVS}} \tag{20}$$

TABLE II
EXPERIMENT PARAMETERS

Parameter	Value	Parameter	Value
V_{in}	380 V	T_{b}	666.6 μs
V_{o}	48 V	T_{de}	166.6 μs
L_{m}	120 μH	M-ary (FSK)	2
L_{r}	8.6 μH	M-ary (SFPM)	2
C_{r}	90 nF	M-ary (DPSK)	2
C_{out}	200 μF	DSP	TMS320F28377DZWT
P_{o}	500 W	Primary switches	IPW50R190CE
f_{r}	180 kHz	Rectifying diodes	STPS30SM80C
Δf	3 kHz,6 kHz	Bitrate	4.5 kbps

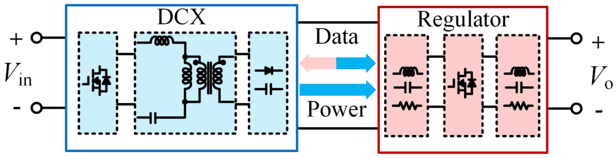


Fig. 11. Block diagram of converters cascade experimental system.

where I_{Lm} is the peak value of magnetizing current, V_{in} is the input voltage. I_{Lm} is related to the on time of primary-side switches as

$$I_{\text{Lm}} \approx \frac{0.5T_{\text{s}} \cdot 0.5V_{\text{in}}}{2L_{\text{m}}} \tag{21}$$

where T_{s} is the switching period. The magnetizing inductance L_{m} should be designed as large as possible to reduce the conduction loss related to current. To guarantee the ZVS realization in the whole communication process, T_s should equal the minimum communication period T_{balmin}. Then substituting (21) into (20), the condition for the magnetizing inductor is derived as

$$L_{\text{m}} \leq \frac{T_{\text{balmin}} \cdot t_{\text{ZVS}}}{16C_{\text{otr}}}. \tag{22}$$

From the perspective of the ZVS realization, the tradeoff between L_{m} and t_{ZVS} should be made once the primary-side switches and T_{balmin} are determined.

IV. EXPERIMENTAL VERIFICATIONS

To validate the feasibility of the proposed PSDM scheme applied in DCX, a prototype system is built, and its parameters are listed in Table II. The duty cycle of the gate signal is set to $1/2$. Frequency control is applied for the transition processes, FSK and SFPM. The switching frequency is 180 kHz when DCX is not sending data. Phase control modulates data on the phase of output voltage/current ripples. When DCX is cascaded to a voltage regulator, the block diagram of the experimental system is shown in Fig. 11.

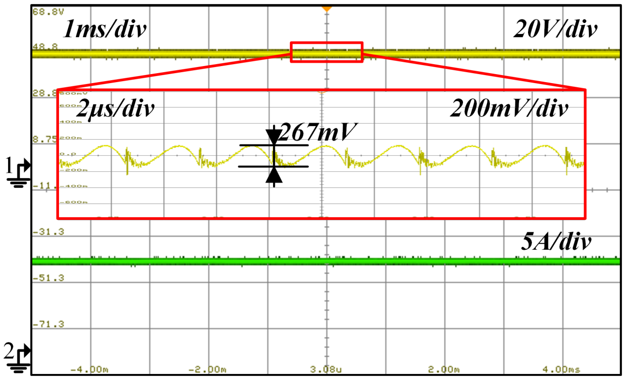


Fig. 12. Waveforms of output voltage and current.

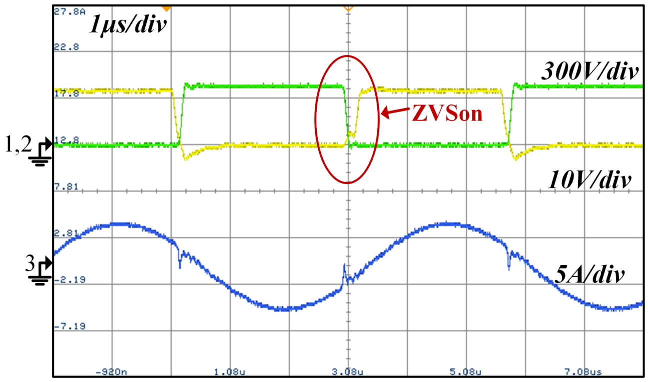


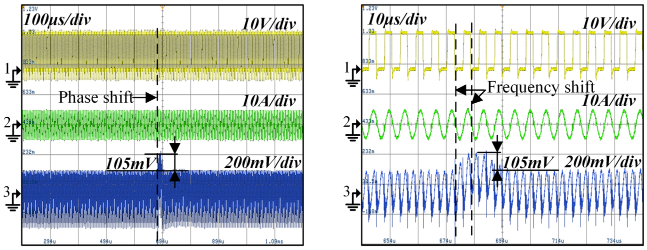
Fig. 13. Soft-switching waveforms of primary switches.

Fig. 12 shows the output voltage (CH1) and output current (CH2) waveforms of the DCX when the switching frequency is set to 180 kHz, and their dc values are 48.5 V and 10.3 A, respectively. From the zoomed-in waveform of CH1, the voltage ripple is 360 kHz due to the rectification of the secondary rectifiers, and the peak-to-peak amplitude of the voltage ripple at the resonant frequency is 267 mV.

The soft-switching waveforms of the primary switches are shown in Fig. 13. These waveforms are tested at the resonant frequency with $V_{\text{in}} = 380$ V. CH1 is the gate signal, CH2 is the voltage waveform between the drain and source of Q_1, and CH3 is the primary resonant current. The secondary parasitic capacitance has an influence on the ZVS [36], leading to a small perturbation of the primary resonant current during the dead time in CH3.

The phase-shift experimental waveforms with the transition process are illustrated in Fig. 14, where CH1-3 is the gate signal of Q_1, the primary resonant current, and the output voltage ripple, respectively. The frequency of the gate signal is 180 kHz. One 174 kHz switching period is introduced as a transition process, leading to an approximately 24.8° phase shift of the 360 kHz output voltage ripple. The amplitude of the output voltage disturbance caused by the transition process is 105 mV. Compared with the output voltage ripple, the disturbance is small enough that it does not affect the power conversion.

The waveforms of phase shift when the converter sends random data are shown in Fig. 15, where CH1 denotes the primary resonant current, CH2 denotes the output voltage ripple, CH3 and CH4 denote sent and received data, respectively, and CH5



(a) (b)

Fig. 14. Experimental waveforms of a single phase shift in (a) large time scale and (b) small time scale.

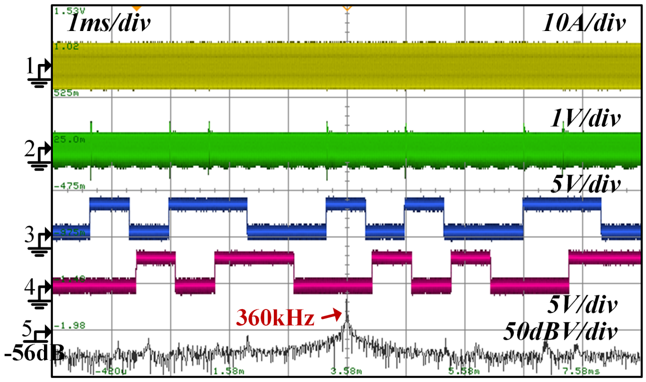


Fig. 15. Experimental waveforms of phase shift with transition process when sending random data.

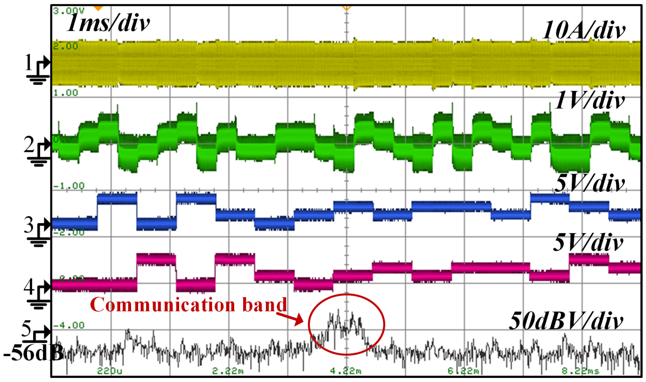


Fig. 16. Experimental waveforms of FSK and SFPM.

denotes the frequency spectrum of CH2. The output voltage is stable in the signal transmission process, and the 360 kHz frequency component can be explicitly seen from CH5. Comparing the data sent and received, all data are received correctly. Therefore, it is applicable to realize information transmission using phase in DCX without affecting the power conversion.

The FSK and SFPM experimental waveforms are shown in Fig. 16, CH1-5 are the primary resonant current, the output voltage ripple, the sent data, the received data, and the frequency spectrum of CH2, respectively. The output voltage varies with the change in frequency while its average value remains constant. The amplitude of the variation is determined by the gain curve of the DCX and the range of frequency variation. In addition, all the data are received correctly, demonstrating the proposed frequency modulation scheme can be applied for communication. Due to the data modulation, 183 and 186 kHz are used for communication frequencies, and the corresponding balanced frequencies are 177 and 174 kHz, respectively. Therefore, there is no peak at 360 kHz in CH5.

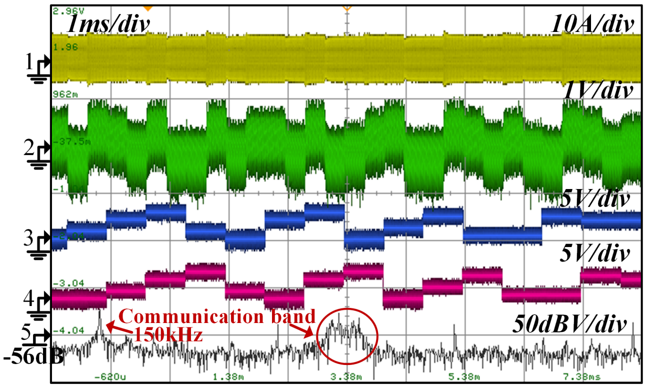


Fig. 17. Experimental waveforms of proposed PSDM scheme under multiple operating converters.

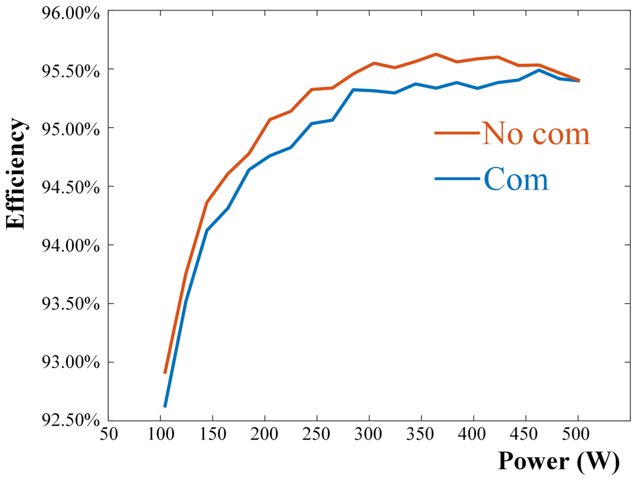


Fig. 18. Efficiency comparison experiment.

When converters are connected as shown in Fig. 11, the performance of the proposed scheme is shown in Fig. 17, where the DCX serves as the data sender and the regulator (buck) serves as the data receiver. The regulator operates at 150 kHz, and it can be clearly observed in CH5. For DCX, 183 and 186 kHz are used for communication frequencies, and the corresponding balanced frequencies are 177 and 174 kHz, respectively. Therefore, there is no peak at 360 kHz in CH5. CH1 is the primary resonant current of DCX, CH2 is the output voltage ripple of DCX, CH3 is the sent data of DCX, and CH4 is the received data of regulator.

The communication from the DCX to the down-stream voltage regulator is established, and all data is correctly transmitted or received. Furthermore, using the existing PSDM methods [18] and [26], the regulator can also serve as the data sender, which has been studied in previous research and is not discussed in detail in this article. The conclusion can be drawn that the communication is applicable in occasions with multiple operating converters. It should be noted that there may be corruption in the data when the converter responds to transients in power. If the frequency of the power transient response is not within the bandwidth of the BPF, it can be suppressed and filtered by the BPF. If the frequency of the power transient response is within the bandwidth of the BPF, the data demodulation will be influenced. The relevant power transient response suppression methods merit further research.

Fig. 18 shows the efficiency curves of applying the proposed PSDM scheme (blue line) and traditional fix-frequency control (red line) for LLC-DCX. The maximum efficiency difference is 0.3%.

V. CONCLUSION

This article proposes a novel PSDM scheme for resonant dc–dc converters. By multiplexing the power buses as communication wires, no extra modulation units or auxiliary power supply are needed, simplifying the system structure and improving communication reliability. The control principles of duty cycle, frequency, and phase are analyzed, showing the feasibility of the proposed scheme using frequency and phase control. A practical modulation method using frequency and phase control is proposed for bitrate improvement. In addition, design considerations of converter parameters are provided to achieve the ZVS and maintain power quality during the communication process. Finally, the bit rate of 4.5 kbps is achieved on a 500 W experimental platform to verify the rationality of the theoretical analysis.

REFERENCES

[1] M. Faisal, M. A. Hannan, P. J. Ker, A. Hussain, M. B. Mansor, and F. Blaabjerg, “Review of energy storage system technologies in microgrid applications: Issues and challenges,” *IEEE Access*, vol. 6, pp. 35143–35164, 2018, doi: 10.1109/ACCESS.2018.2841407.

[2] D. Vinnikov, A. Chub, E. Liivik, R. Kosenko, and O. Korkh, “Solar optiverter—A novel hybrid approach to the photovoltaic module level power electronics,” *IEEE Trans. Ind. Electron.*, vol. 66, no. 5, pp. 3869–3880, May 2019, doi: 10.1109/TIE.2018.2850036.

[3] Y. Li and J. Yan, “Cybersecurity of smart inverters in the smart grid: A survey,” *IEEE Trans. Power Electron.*, vol. 38, no. 2, pp. 2364–2383, Feb. 2023, doi: 10.1109/TPEL.2022.3206239.

[4] S. K. Mazumder et al., “A review of current research trends in power-electronic innovations in cyber–physical systems,” *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 5, pp. 5146–5163, Oct. 2021, doi: 10.1109/JESTPE.2021.3051876.

[5] Y. Zhu, F. Zhuo, and L. Xiong, “Communication platform for energy management system in a master-slave control structure microgrid,” in *Proc. 7th Int. Power Electron. Motion Control Conf.*, 2012, pp. 141–145, doi: 10.1109/IPEMC.2012.6258875.

[6] H. Nosato, Y. Kasai, E. Takahashi, and M. Murakawa, “A very low-cost low-frequency PLC system based on DS-CDMA for DC power lines,” in *Proc. IEEE Int. Symp. Power Line Commun. Appl.*, 2012, pp. 398–403, doi: 10.1109/ISPLC.2012.6201320.

[7] H. Liang, B. J. Choi, W. Zhuang, and X. Shen, “Stability enhancement of decentralized inverter control through wireless communications in microgrids,” *IEEE Trans. Smart Grid*, vol. 4, no. 1, pp. 321–331, Mar. 2013, doi: 10.1109/TSG.2012.2226064.

[8] H. Liu et al., “Power talk: A novel power line communication in DC MicroGrid,” in *Proc. IEEE 8th Int. Power Electron. Motion Control Conf.*, 2016, pp. 2870–2874, doi: 10.1109/IPEMC.2016.7512753.

[9] X. He, R. Wang, J. Wu, and W. Li, “Nature of power electronics and integration of power conversion with communication for talkative power,” *Nature Commun.*, vol. 11, no. 1, Dec. 2020, Art. no. 2479, doi: 10.1038/s41467-020-16262-0.

[10] J. Chen, J. Wu, R. Wang, R. Zhang, and X. He, “Coded PWM based switching ripple communication applied in visible light communication,” *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 9659–9667, Aug. 2021, doi: 10.1109/TPEL.2021.3056754.

[11] M. Liserre, H. Beiranvand, Y. Leng, R. Zhu, and P. A. Hoeher, “Overview of talkative power conversion technologies,” *IEEE Open J. Power Electron.*, vol. 4, pp. 67–80, 2023, doi: 10.1109/OJPEL.2023.3237709.

[12] R. Wang, X. He, J. Wu, R. Zhang, and W. Li, “Power and signal dual modulation with info nature of power converters,” *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 11, no. 1, pp. 588–601, Feb. 2023, doi: 10.1109/JESTPE.2022.3199099.

[13] M. Angjelichinoski, C. Stefanovic, P. Popovski, H. Liu, P. C. Loh, and F. Blaabjerg, “Multiuser communication through power talk in DC MicroGrids,” *IEEE J. Sel. Areas Commun.*, vol. 34, no. 7, pp. 2006–2021, Jul. 2016, doi: 10.1109/JSAC.2016.2566138.

[14] M. Angjelichinoski, C. Stefanovic, and P. Popovski, “Power talk for multibus DC MicroGrids: Creating and optimizing communication channels,” in *Proc. IEEE Glob. Commun. Conf.*, 2016, pp. 1–7, doi: 10.1109/GLOCOM.2016.7842158.

[15] Y. Zhu, J. Wu, R. Wang, Z. Lin, and X. He, “Embedding power line communication in photovoltaic optimizer by modulating data in power control loop,” *IEEE Trans. Ind. Electron.*, vol. 66, no. 5, pp. 3948–3958, May 2019, doi: 10.1109/TIE.2018.2838081.

[16] R. Zhang, Y. Hui, J. Wu, R. Wang, Z. Lin, and X. He, “Embedding OFDM-based carrier communication into power control loop of converter in DC microgrids,” *IEEE Trans. Ind. Electron.*, vol. 69, no. 7, pp. 6914–6924, Jul. 2022, doi: 10.1109/TIE.2021.3095821.

[17] W. Stefanutti, S. Saggini, P. Mattavelli, and M. Ghioni, “Power line communication in digitally controlled DC–DC converters using switching frequency modulation,” *IEEE Trans. Ind. Electron.*, vol. 55, no. 4, pp. 1509–1518, Apr. 2008, doi: 10.1109/TIE.2008.917145.

[18] J. Wu, J. Du, Z. Lin, Y. Hu, C. Zhao, and X. He, “Power conversion and signal transmission integration method based on dual modulation of DC–DC converters,” *IEEE Trans. Ind. Electron.*, vol. 62, no. 2, pp. 1291–1300, Feb. 2015, doi: 10.1109/tie.2014.2336628.

[19] T. Kohama, S. Hasebe, and S. Tsuji, “Simple bidirectional power line communication with switching converters in DC power distribution network,” in *Proc. IEEE Int. Conf. Ind. Technol.*, 2019, pp. 539–543, doi: 10.1109/ICIT.2019.8755053.

[20] D. Yu, Y. Hua, S. Yu, P. Zhang, H. H. C. Iu, and T. Fernando, “A new modulation–demodulation approach to DC power-line data transmission for SRG-integrated microgrid,” *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 12370–12382, Nov. 2020, doi: 10.1109/TPEL.2020.2984911.

[21] D. Yu et al., “A novel power and signal composite modulation approach to powerline data communication for SRM in distributed power grids,” *IEEE Trans. Power Electron.*, vol. 36, no. 9, pp. 10436–10446, Sep. 2021, doi: 10.1109/TPEL.2021.3061469.

[22] H.-J. Choi and J.-H. Jung, “Enhanced power line communication strategy for DC microgrids using switching frequency modulation of power converters,” *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4140–4144, Jun. 2017, doi: 10.1109/tpel.2017.2648848.

[23] J. Du, J. Wu, R. Wang, Z. Lin, and X. He, “DC power-line communication based on power/signal dual modulation in phase shift full-bridge converters,” *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 693–702, Jan. 2017, doi: 10.1109/tpel.2016.2527739.

[24] J. Rodriguez, D. G. Lamar, P. F. Miaja, and J. Sebastian, “Reproducing single-carrier digital modulation schemes for VLC by controlling the first switching harmonic of the DC–DC power converter output voltage ripple,” *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7994–8010, Sep. 2018, doi: 10.1109/TPEL.2017.2774178.

[25] J. Rodriguez Mendez, D. G. Lamar, D. G. Aller, P. F. Miaja, and J. Sebastian, “Reproducing multicarrier modulation schemes for visible light communication with the ripple modulation technique,” *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 1532–1543, Feb. 2020, doi: 10.1109/TIE.2019.2912795.

[26] J. Chen, J. Wu, K. Liu, R. Wang, W. Li, and X. He, “Improved switching ripple modulation strategy for simultaneous power conversion and data communication in DC–DC converters,” *IEEE Trans. Power Electron.*, vol. 37, no. 8, pp. 9275–9284, Aug. 2022, doi: 10.1109/TPEL.2022.3161059.

[27] J. Chen, K. Liu, J. Wu, R. Wang, W. Weng, and X. He, “Simultaneous power and data transmission using combined three degrees of freedom modulation strategy in DC-DC converters,” *IEEE Trans. Power Electron.*, vol. 38, no. 3, pp. 3191–3200, Mar. 2023, doi: 10.1109/TPEL.2022.3226468.

[28] H.-P. Park, M. Kim, J. Baek, M. Kang, and J.-H. Jung, “Spread spectrum based power line communication and EM noise reduction technique for bidirectional HB CLLC resonant converter,” in *Proc. IEEE Energy Convers. Congr. Expo.*, 2020, pp. 5470–5473, doi: 10.1109/ECCE44975.2020.9236232.

[29] H.-P. Park, M. Kim, and J.-H. Jung, “Bidirectional CLLC resonant converter employing PLC capability and EM noise reduction technique for small-sized ESS application,” *IEEE J. Emerg. Sel. Topics Ind. Electron.*, vol. 2, no. 3, pp. 277–286, Jul. 2021, doi: 10.1109/JESTIE.2021.3061902.

[30] X. Wu, H. Chen, and Z. Qian, “1-MHz LLC resonant DC transformer (DCX) with regulating capability,” *IEEE Trans. Ind. Electron.*, vol. 63, no. 5, pp. 2904–2912, May 2016, doi: 10.1109/TIE.2016.2521606.

[31] C. Fei, F. C. Lee, and Q. Li, “High-efficiency high-power-density LLC converter with an integrated planar matrix transformer for high-output current applications,” *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 9072–9082, Nov. 2017, doi: 10.1109/TIE.2017.2674599.

[32] X. Wu and H. Shi, “High efficiency high density 1 MHz 380–12 V DCX with low FoM devices,” *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 1648–1656, Feb. 2020.

[33] Y.-C. Liu, C. Chen, K.-D. Chen, Y.-L. Syu, and N. A. Dung, “High-frequency and high-efficiency isolated two-stage bidirectional DC–DC converter for residential energy storage systems,” *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 3, pp. 1994–2006, Sep. 2020, doi: 10.1109/JESTPE.2019.2953117.

[34] T. Liu, X. Wu, and S. Yang, “1 MHz 48–12 V regulated DCX with single transformer,” *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 1, pp. 38–47, Feb. 2021, doi: 10.1109/jestpe.2019.2955607.

[35] H. Huang, “FHA-based voltage gain function with harmonic compensation for LLC resonant converter,” in *Proc. 25th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2010, pp. 1770–1777, doi: 10.1109/APEC.2010.5433473.

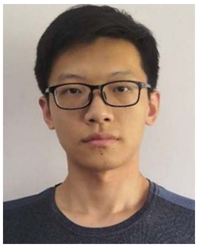
[36] H. Chen and X. Wu, “Analysis on the influence of the secondary parasitic capacitance to ZVS transient in LLC resonant converter,” in *Proc. IEEE Energy Convers. Congr. Expo.*, 2014, pp. 4755–4760, doi: 10.1109/ECCE.2014.6954052.

Keming Liu (Graduate Student Member, IEEE) received the B.S. degree in electrical engineering from the Zhejiang University, Hangzhou, China, in 2021. He is currently working toward the Ph.D. degree in electrical engineering with the College of Electrical Engineering, Zhejiang University, Hangzhou, China.

His current research interests include distributed power electronics system and communication technique applied in power electronics.

Yue Hui (Graduate Student Member, IEEE) received the B.S. degree in electrical engineering, in 2020, from Zhejiang University, Hangzhou, China, where she is currently working toward the Ph.D. degree in electrical engineering with the College of Electrical Engineering, Zhejiang University.

Her current research interests include distributed power electronics system.



Jinghui Chen (Graduate Student Member, IEEE) received the B.S. degree in electrical engineering from the Zhejiang University, Hangzhou, China, in 2018. He is currently working toward the Ph.D. degree in electrical engineering with the College of Electrical Engineering, Zhejiang University, Hangzhou, China.

His current research interests include communication technique in DC microgrid and switching rippled based communication.

Jiande Wu (Member, IEEE) was born in Zhejiang, China, in 1973. He received the B.Sc., M.Sc., and Ph.D. degrees in electrical engineering from Zhejiang University, Hangzhou, China, in 1994, 1997 and 2012, respectively.

Since 1997, he has been a faculty member with Zhejiang University, where he is currently an Associate Professor. From 2013 to 2014, he was an academic visitor at the University of Strathclyde, Glasgow, U.K. His research interests include power electronics control, distributed power electronics system and fieldbus communication.

Xiangning He (Fellow, IEEE) received the B.Sc. and M.Sc. degrees from the Nanjing University of Aeronautical and Astronautical, Nanjing, China, in 1982 and 1985, respectively, and the Ph.D. degree from the Zhejiang University, Hangzhou, China, in 1989, all in electrical engineering.

In 1991, he obtained a Fellowship from the Royal Society of U.K., and conducted research in Heriot-Watt University, Edinburgh, U.K., as a Post-Doctoral Research Fellow for two years. In 1994, he joined Zhejiang University as an Associate Professor. Since 1996, he has been a Full Professor with the College of Electrical Engineering, Zhejiang University. His research interests include power electronics and their industrial applications.