Reliability-Oriented Application Method of Discontinuous PWM for Single-Phase Five-Level T-Type NPC Inverter

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***Abstract*—Discontinuous pulsewidth modulation (DPWM) is generally used for improving the efficiency of inverters, but it reduces the power quality. Therefore, in previous research, the efficiency and power quality are typically considered when DPWM methods are applied. Even though it also affects the power losses of the power devices and dc-link capacitors and thus their reliability, a study on the effect of DPWM on the reliability of inverters is insufficient. In this article, the impact of different DPWM methods on the reliability of a single-phase five-level T-type neutral-point clamped (NPC) inverter is comparatively investigated by considering the lifetime of the power devices and dc-link capacitors. Then, the reliability-oriented application method of DPWM called ED^{2}PWM(PON) is proposed based on the analysis results. Finally, the feasibility and effectiveness of the proposed DPWM strategy are verified through simulations and experiments. The proposed ED^{2}PWM(PON) reduces the negative effect on the lifetime of the dc-link capacitor compared with the existing DPWM methods while keeping the advantages of power loss reduction and lifetime improvement of the power devices. Consequently, the inverter under the proposed method has the longest lifetime.**

***Index Terms*—DC-link capacitor, discontinuous pulsewidth modulation (DPWM), inverter, lifetime, power device, reliability, t-type inverter.**

I. Introduction

PULSEWIDTH modulation (PWM) methods significantly influence the performance of inverters such as efficiency, power quality, and reliability. Therefore, various PWM methods have been introduced to improve certain aspects of the performance of inverters.

The unipolar PWM (UP-PWM) is commonly used for the single-phase five-level T-type neutral-point clamped (NPC) (5LT-NPC) inverter for reducing harmonic components of the output voltage, which requires a smaller filter size [1]. The discontinuous PWM (DPWM) is generally used to improve the efficiency of the inverter [2], [3], [4]. It reduces the number of switching transitions within a switching cycle to decrease the switching loss of the power devices. Hence, the efficiency of the inverter increases. However, the application of the DPWM leads to an increase in the total harmonic distortion (THD) of outputs.

Several DPWM methods have been proposed to improve the efficiency of the single-phase 5LT-NPC inverter. In [5], [6], the DPWM method called one pole clamping PWM (OPC-PWM) has been proposed, where one leg is fixed to a switching state [P] or [N] depending on the polarity of the reference voltage during its fundamental period. Therefore, the power loss of the inverter is reduced because nearly no switching occurs in the clamped leg. This method is called OPC-PWM(PN) in this article. A similar DPWM method denoted by OPC-PWM(PON) has also been introduced, where the clamped leg not only has a switching state [P] or [N] but also has a switching state [O] for a certain period depending on the magnitude of the reference voltage [7], [8], [9]. The last one is equally distributed DPWM (ED^{2}PWM), where two legs have equal clamping periods for switching state [P] and [N] during the fundamental period [10], [11]. This method has been proposed not only for power loss reduction but also for junction temperature (T_j) reduction of the power devices with balanced T_j distribution between two legs.

The previous research typically focuses on the analysis of the efficiency and power quality when DPWM methods are applied whereas the study about the impact of the DPWM on the reliability of the inverter is insufficient even though the different PWM methods lead to the variation of power losses of power devices and dc-link capacitors and thus their thermal loadings. Consequently, it has a significant impact on the lifetime of power devices and dc-link capacitors since thermal stress is one of the main causes of wear-out failure of them [12], [13], [14]. Furthermore, the lifetime of these components plays a key role in the reliability of the inverter since they are considered the reliability-critical components in power converters according to Yang et al. [15]. The effect of OPC-PWM on the reliability of the inverter has been performed in [9], but it only has considered the lifetime of a single power device. In [10], the effect of the DPWM on the reliability of the dc-link capacitor has been investigated. Nevertheless, a comprehensive analysis regarding efficiency, THD, and reliability has not been performed yet, which needs to be considered to ensure the required performance of inverters by analyzing the tradeoff between efficiency, power quality, and reliability.

The initial study was performed in [16], where only the thermal loadings of the power devices and dc-link capacitor of the single-phase 5LT-NPC inverter under UP-PWM and three DPWM methods are comparatively analyzed.

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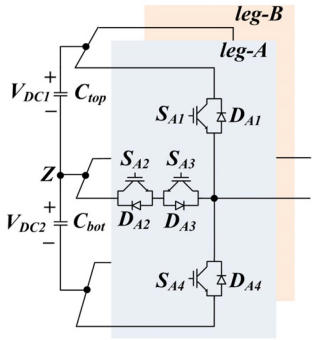

Fig. 1. Topology of the single-phase five-level T-type NPC (5LT-NPC) inverter.

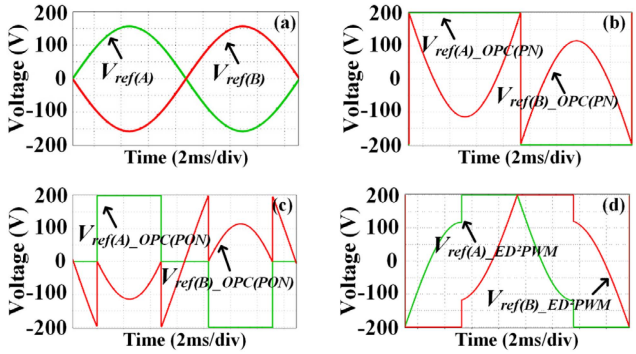

Fig. 2. Reference voltages of two legs with (a) UP-PWM, (b) OPC-PWM (PN), (c) OPC-PWM (PON), and (d) ED^{2}PWM.

TABLE I
SWITCHING STATUS AND POLE VOLTAGE DEPENDING ON SWITCHING STATES

Switching state	Status of switches	Pole voltage
[P]	S_{x1}, S_{x2} : ON, S_{x3}, S_{x4} : OFF	$V_{DC}/2$
[O]	S_{x2}, S_{x3} : ON, S_{x1}, S_{x4} : OFF	0
[N]	S_{x3}, S_{x4} : ON, S_{x1}, S_{x2} : OFF	$-V_{DC}/2$

In this article, the reliability-oriented application method of DPWM has been proposed based on a more detailed reliability evaluation of the single-phase five-level T-type inverter by focusing on the power devices and dc-link capacitors under different DPWM strategies. The rest of this article is organized as follows. The existing UP-PWM and DPWM methods are explained first in Section II. Then, the impact of UP-PWM and different DPWM methods on the reliability of the single-phase five-level T-type inverter is investigated in detail with a focus on the power devices and dc-link capacitors by considering their power losses and thermal loadings in Section III. After that, the proposed reliability-oriented application method of DPWM is explained in Section IV with the comparative analysis of the thermal loadings of power devices and dc-link capacitors with existing DPWM methods. In Section V, the comparative mission-profile-based reliability analysis of the single-phase 5LT-NPC inverter has been performed by focusing on the power devices and dc-link capacitors under seven different PWM strategies to show the effectiveness of the proposed DPWM method in terms of the reliability. Finally, the feasibility and effectiveness of the proposed DPWM method is validated through the experiments.

II. UP-PWM AND DPWM METHODS FOR SINGLE-PHASE FIVE-LEVEL T-TYPE NPC INVERTER

A. UP-PWM

Fig. 1 illustrates the topology of the single-phase 5LT-NPC inverter. Each leg has three types of switching states [P], [O], and [N]. The status of switches and corresponding output pole voltage depending on the switching states are given in Table I.

The reference voltages ($V_{\mathrm{ref}(A)}$ and $V_{\mathrm{ref}(B)}$) for the UP-PWM are shown in Fig. 2(a) and defined as follows:

$$V_{\mathrm{ref}(A)} = V_m \sin(2\pi f_g t), \quad V_{\mathrm{ref}(B)} = -V_{\mathrm{ref}(A)} \tag{1}$$

where V_m is the magnitude of the reference voltage and f_g stands for the fundamental frequency of the grid.

B. DPWM Methods

For applying DPWM, the reference voltages are modified depending on their magnitudes. This explanation is under the assumption that leg-A is clamped.

1) OPC-PWM(PN): For the OPC-PWM(PN), leg-A is fixed to [P] or [N]. If $V_{\mathrm{ref}(A)}$ / ($V_{\mathrm{DC}}/2$) is above 0, the reference voltage of leg-A ($V_{\mathrm{ref}(A)\_\mathrm{OPC(PN)}}$) is modified to $V_{\mathrm{DC}}/2$ so that its switching state is clamped to [P]. Then, the reference voltage of leg-B ($V_{\mathrm{ref}(B)\_\mathrm{OPC(PN)}}$) is modified to $V_{\mathrm{ref}(B)} + (V_{\mathrm{DC}}/2 - V_{\mathrm{ref}(A)})$ to keep the difference between the two reference voltages. In the other case when the $V_{\mathrm{ref}(A)}$ / ($V_{\mathrm{DC}}/2$) is less than 0, $V_{\mathrm{ref}(A)\_\mathrm{OPC(PN)}}$ is changed to $-V_{\mathrm{DC}}/2$ to fix the switching state to [N], and $V_{\mathrm{ref}(B)\_\mathrm{OPC(PN)}}$ becomes $V_{\mathrm{ref}(B)} - (V_{DC}/2 + V_{\mathrm{ref}(A)})$. The modified reference voltages for the OPC-PWM (PN) are given as follows:

$$\begin{aligned}
&(\text{if } V_{\mathrm{ref}(A)}/(V_{\mathrm{DC}}/2) \geq 0)\\
&\quad [\text{for [P] Clamping of Leg} - \mathrm{A}]\\
&\quad V_{\mathrm{ref}(A)_\mathrm{OPC(PN)}} = V_{\mathrm{DC}}/2\\
&\quad V_{\mathrm{ref}(B)_\mathrm{OPC(PN)}} = V_{\mathrm{DC}}/2 - V_{\mathrm{ref}(A)} + V_{\mathrm{ref}(B)}\\
&(\text{if } V_{\mathrm{ref}(A)}/(V_{\mathrm{DC}}/2) < 0)\\
&\quad [\text{for [N] Clamping of Leg} - \mathrm{A}]\\
&\quad V_{\mathrm{ref}(A)_\mathrm{OPC(PN)}} = -V_{\mathrm{DC}}/2\\
&\quad V_{\mathrm{ref}(B)_\mathrm{OPC(PN)}} = -V_{\mathrm{DC}}/2 - V_{\mathrm{ref}(A)} + V_{\mathrm{ref}(B)}.
\end{aligned} \tag{2}$$

2) OPC-PWM(PON): In the OPC-PWM(PON), the clamped leg also has the switching state [O] depending on the magnitude of the reference voltage. When $V_{\mathrm{ref}(A)}$ / ($V_{\mathrm{DC}}/2$) is between 0.5 and –0.5, the reference voltage of leg-A ($V_{\mathrm{ref}(A)\_\mathrm{OPC(PON)}}$) becomes 0 to make the switching state of leg-A [O] for this period and the reference voltage of leg-A ($V_{\mathrm{ref}(B)\_\mathrm{OPC(PON)}}$) is modified to $V_{\mathrm{ref}(B)} - V_{\mathrm{ref}(A)}$. When $V_{\mathrm{ref}(A)}$ / ($V_{\mathrm{DC}}/2$) is above 0.5, the leg-A is fixed to [P] and it is clamped to [N] when $V_{\mathrm{ref}(A)}$ / ($V_{\mathrm{DC}}/2$) is below –0.5 as the OPC-PWM (PN). Consequently, the reference voltages are modified for the OPC-PWM (PON)

as follows:

$$
\begin{aligned}
&(\text{if } V_{\text{ref}(A)}/(V_{\text{DC}}/2) \geq 0.5)\\
&\quad[\text{for [P] Clamping of Leg} - \text{A}]\\
&\quad V_{\text{ref}(A)\_\text{OPC(PON)}} = V_{\text{DC}}/2\\
&\quad V_{\text{ref}(B)\_\text{OPC(PON)}} = V_{\text{DC}}/2 - V_{\text{ref}(A)} + V_{\text{ref}(B)}\\
&(\text{if } -0.5 \leq V_{\text{ref}(A)}/(V_{\text{DC}}/2) < 0.5)\\
&\quad[\text{for [O] Clamping of Leg} - \text{A}]\\
&\quad V_{\text{ref}(A)\_\text{OPC(PON)}} = 0\\
&\quad V_{\text{ref}(B)\_\text{OPC(PON)}} = -V_{\text{ref}(A)} + V_{\text{ref}(B)}\\
&(\text{if } V_{\text{ref}(A)}/(V_{\text{DC}}/2) < -0.5)\\
&\quad[\text{for [N] Clamping of Leg} - \text{A}]\\
&\quad V_{\text{ref}(A)\_\text{OPC(PON)}} = -V_{\text{DC}}/2\\
&\quad V_{\text{ref}(B)\_\text{OPC(PON)}} = -V_{\text{DC}}/2 - V_{\text{ref}(A)} + V_{\text{ref}(B)}. \qquad (3)
\end{aligned}
$$

The reference voltages under OPC-PWM(PN) and OPC-PWM(PON) are shown in Fig. 2(b) and (c), respectively.

3) ED²PWM: In the case of ED²PWM, two legs are alternately fixed to [P] or [N] for 90° depending on the polarity of the reference voltages. For example, during the period where $V_{\text{ref}(A)}$ is positive, $V_{\text{ref}(A)}$ is modified so that leg-A is fixed to [P] or leg-B is clamped to [N], where the clamping periods for each switching state are equally distributed during the fundamental period as shown in Fig. 2(d). Finally, the modified reference voltages for ED²PWM are expressed as follows:

$$
\begin{aligned}
&(\text{if } V_{\text{ref}(A)} \geq 0)\\
&\quad[\text{for [P] Clamping of Leg} - \text{A}]\\
&\quad V_{\text{ref}(A)\_\text{ED²PWM}} = V_{\text{DC}}/2\\
&\quad V_{\text{ref}(B)\_\text{ED²PWM}} = V_{\text{DC}}/2 - V_{\text{ref}(A)} + V_{\text{ref}(B)}\\
&\quad[\text{for [N] Clamping of Leg} - \text{B}]\\
&\quad V_{\text{ref}(A)\_\text{ED²PWM}} = -V_{\text{DC}}/2 + V_{\text{ref}(A)} - V_{\text{ref}(B)}\\
&\quad V_{\text{ref}(B)\_\text{ED²PWM}} = -V_{\text{DC}}/2\\
&(\text{if } V_{\text{ref}(A)} < 0)\\
&\quad[\text{for [N] Clamping of Leg} - \text{A}]\\
&\quad V_{\text{ref}(A)\_\text{ED²PWM}} = -V_{\text{DC}}/2\\
&\quad V_{\text{ref}(B)\_\text{ED²PWM}} = -V_{\text{DC}}/2 - V_{\text{ref}(A)} + V_{\text{ref}(B)}\\
&\quad[\text{for [P] Clamping of Leg} - \text{B}]\\
&\quad V_{\text{ref}(A)\_\text{ED²PWM}} = V_{\text{DC}}/2 + V_{\text{ref}(A)} - V_{\text{ref}(B)}\\
&\quad V_{\text{ref}(B)\_\text{ED²PWM}} = V_{\text{DC}}/2\,. \qquad (4)
\end{aligned}
$$

III. Comparative Analysis of Thermal Loadings of Power Devices and DC-Link Capacitors

In this section, the thermal loadings of the power devices and dc-link capacitors are comparatively analyzed under UP-PMW and three different DPWM methods through the simulations under the following conditions: dc-link voltage (V_{DC}): 325 V (modulation index of 0.96), 400 V (modulation index of 0.78), 500 V (modulation index of 0.62), switching frequency (f_{sw}): 20 kHz, dc-link capacitance (C_{DC}): 2200 μF, grid voltage (V_g): 220 V_{rms}, grid frequency (f_{grid}): 60 Hz, ambient temperature (T_a): 40 °C, rated output power (P_{out}): 7 kW, dc-link capacitor: E93E451VNT222MCA5U, IGBT module: 10-12NMA040SH-M267F. The representative analysis is performed by considering the V_{DC} of 400 V.

A. Thermal Loading Analysis of Power Devices Under Different PWM Methods

The junction temperature (T_j) of the power devices is obtained as follows:

$$
\begin{aligned}
&T_j(t) = P_d(t) \cdot Z_{\text{th}(j-h)}(t) + P_{\text{m}}(t) \cdot Z_{\text{th}(h-a)}(t) + T_a\\
&Z_{\text{th}(j-h)}(t) = \sum_{i=1}^{n} R_i(1 - e^{-t/\tau_i}) \qquad (5)
\end{aligned}
$$

where P_d = power loss of device, P_m = power loss of IGBT module, $Z_{\text{th}\,(h\text{-}a)}$ = heatsink to ambient thermal impedance, T_a = ambient temperature, $Z_{\text{th}\,(j\text{-}h)}$ = junction to heatsink thermal impedance, $\tau_i = R_i\, C_i$, R is the thermal resistance and C is the thermal capacitance at the number (i) of RC combinations for the Foster model [17]. The parameters of the thermal model can be obtained from the datasheet. $R_{\text{th}\,(h\text{-}a)}$ is set to 0.18 K/W in order that T_j is about 70% of the rated junction temperature at the rated power [18].

The UP-PWM leads to the symmetric power loss distributions of the power devices between two legs, and $S_{A1,4}$ and $S_{B1,4}$ have higher power losses than the other devices as shown in Fig. 3(a), and thus have the highest T_j of 104 °C as shown in Fig. 4(a) .

The power loss distribution under the OPC-PWM(PN) is shown in Fig. 3(b), where it is assumed that leg-A is clamped. Since leg-A is clamped to [P] or [N] for the fundamental period, S_{A1} and S_{A4} have only conduction loss, and their total power loss slightly increases. However, the power losses of $S_{A2,3}$ and $D_{A2,3}$ notably decrease since no current flows through them. The T_j of the power devices of leg-A is illustrated in Fig. 4(b). Because of the reduced total power loss of the IGBT module, the T_j of all power devices is fallen compared with those under the UP-PWM. Especially, there are large T_j drops in $S_{A2,3}$ and $D_{A2,3}$. In the case of leg-B, the period for [O] increases since the modulation index of leg-B is reduced. Therefore, the power losses of $S_{B2,3}$ and $D_{B2,3}$ increase but the power losses of $S_{B1,4}$ decrease. Consequently, the T_j of $S_{B2,3}$ and $D_{B2,3}$ increase, but the T_j of $S_{B1,4}$ decreases as shown in Fig. 4(c), where $D_{B2,3}$ has the highest T_j of 111.2 °C.

Applying OPC-PWM(PON) results in similar power loss and similar T_j distributions with the OPC-PWM(PN). However, since leg-A is fixed to not only [P] and [N], but also [O] for a certain period, the power loss of $S_{A1,4}$ a bit decreases, but the power loss of $S_{A2,3}$ and $D_{A2,3}$ increases as shown in Fig 3(c). Therefore, a similar T_j distribution of leg-A is obtained as given in Fig. 4(d). In the case of leg-B, the power loss of $S_{B2,3}$ and $D_{B2,3}$ is reduced, but the power loss of $S_{B1,4}$ increases, which leads to a decrease in the highest T_j of $D_{B2,3}$ from 111.2 °C to 108.8 °C as illustrated in Fig. 4(e).

The power loss and T_j distributions under the ED²PWM are shown in Figs. 3(d) and 4(f), respectively. Since the clamping period is equally applied between two legs, they have balanced power loss distribution and thus balanced T_j distribution between

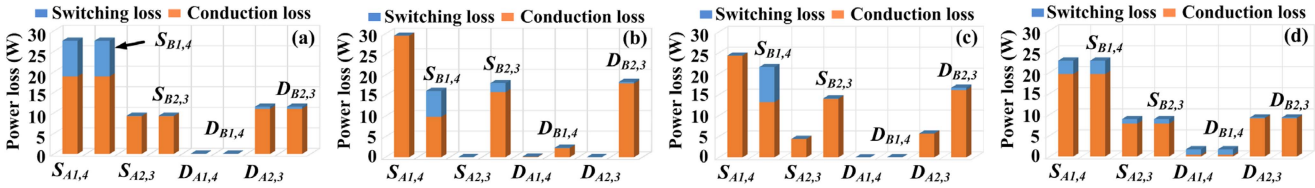

Fig. 3. Power loss distribution of all power devices with modulation index (*MI*) of 0.78 under (a) UP-PWM, (b) OPC-PWM(PN), (c) OPC-PWM(PON), and (d) ED^{2}PWM.

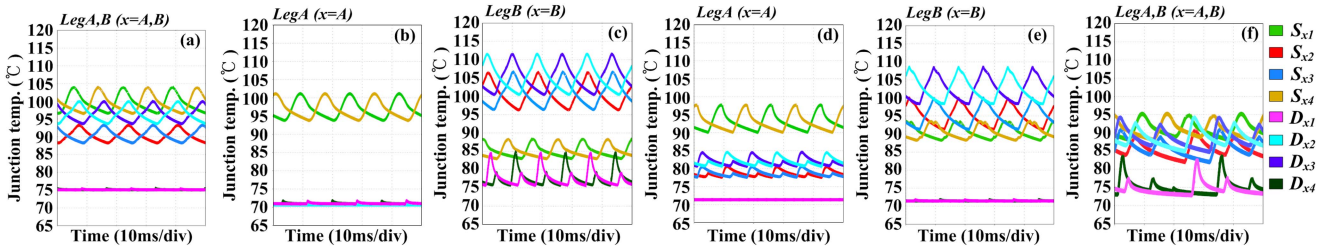

Fig. 4. Junction temperature of power devices of the T-type inverter at 7 kW with *MI* of 0.78 under different PWM methods (a) UP-PWM, (b) Leg-A with OPC-PWM(PN), (c) Leg-B with OPC-PWM(PN), (d) Leg-A with OPC-PWM(PON), (e) Leg-B with OPC-PWM(PON), and (f) ED^{2}PWM.

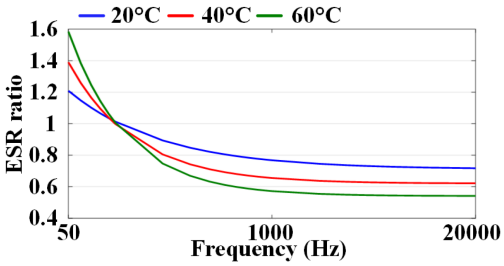

Fig. 5. Ratio of equivalent series resistance (R_{ESR}) depending on frequency [19].

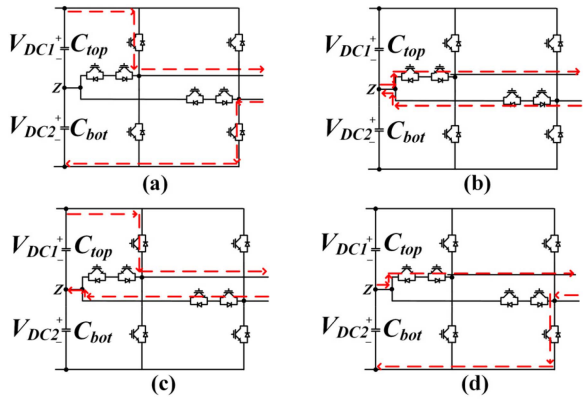

Fig. 6. Influence of voltage vector on the ripple current of DC-link capacitors. (a) Large voltage vector [PN]. (b) Zero voltage vector [OO]. (c) Small voltage vector [PO] (P-type). (d) Small voltage vector [ON] (N-type).

two legs. Furthermore, the highest T_j of $S_{A1,4}$ and $S_{B1,4}$ is reduced from 104 °C to 95.2 °C due to reduced switching loss.

The total power loss due to power devices under the UP-PWM is 193.8 W and it is reduced to 170.1, 173.7, and 170.7 W, when the OPC-PWM(PN), OPC-PWM(PON), and ED^{2}PWM are applied, respectively.

From the above results, it can be concluded that the application of two OPC-PWM methods causes asymmetric thermal loadings of power devices between two legs. It also increases the highest T_j compared with that under the UP-PWM and the highest T_j under the OPC-PWM(PN) is higher than that under the OPC-PWM(PON). Therefore, the OPC-PWM methods give a negative effect on the reliability of the power devices of the inverter. However, the ED^{2}PWM improves the reliability of the power devices since it leads to reduced T_j with symmetric distribution between two legs. It seems that there are no significant differences in the total power loss of the power devices between DPWM methods.

B. Thermal Loading Analysis of DC-Link Capacitors With the PWM Methods

The hot-spot temperature ($T_{\rm hot}$) of capacitors is associated with the power loss of capacitor ($P_{\rm cap}$), ambient temperature (T_a), and thermal impedance as follows:

$$\begin{aligned} T_{\rm hot} &= Z_{\rm th} \cdot P_{\rm cap} + T_a \\ P_{\rm cap} &= \textstyle\sum_{h=1}^{n} \left(I_{C({\rm RMS})}(f_h)\right)^2 \times R_{\rm ESR}(f_h) \end{aligned} \tag{6}$$

where $Z_{\rm th}$ is the thermal impedance from the hotspot to the ambient environment, $I_{c({\rm RMS})}(f_h)$ and $R_{\rm ESR}(f_h)$ are the ripple current and the equivalent series resistance of the capacitor at a certain frequency (f_h), respectively. At the low frequency, the $R_{\rm ESR}(f_h)$ is relatively higher than that at the high frequency.

Therefore, the magnitude and frequency of the ripple current play a major role in $P_{\rm cap}$ and thus $T_{\rm hot}$. The related parameters to analyze the thermal loading of the capacitors are given in [19], [20]. $R_{\rm ESR}$ is 0.045 Ω at 120 Hz, 25 °C, and its frequency dependency is shown in Fig. 5. It is seen that $R_{\rm ESR}$ decreases as frequency increases. The thermal impedance $Z_{\rm th}$ of the capacitor used in this study is 6.655 K/W.

Fig. 6 shows the operations of the T-type NPC inverter with different voltage vectors and their influence on the capacitor ripple current.

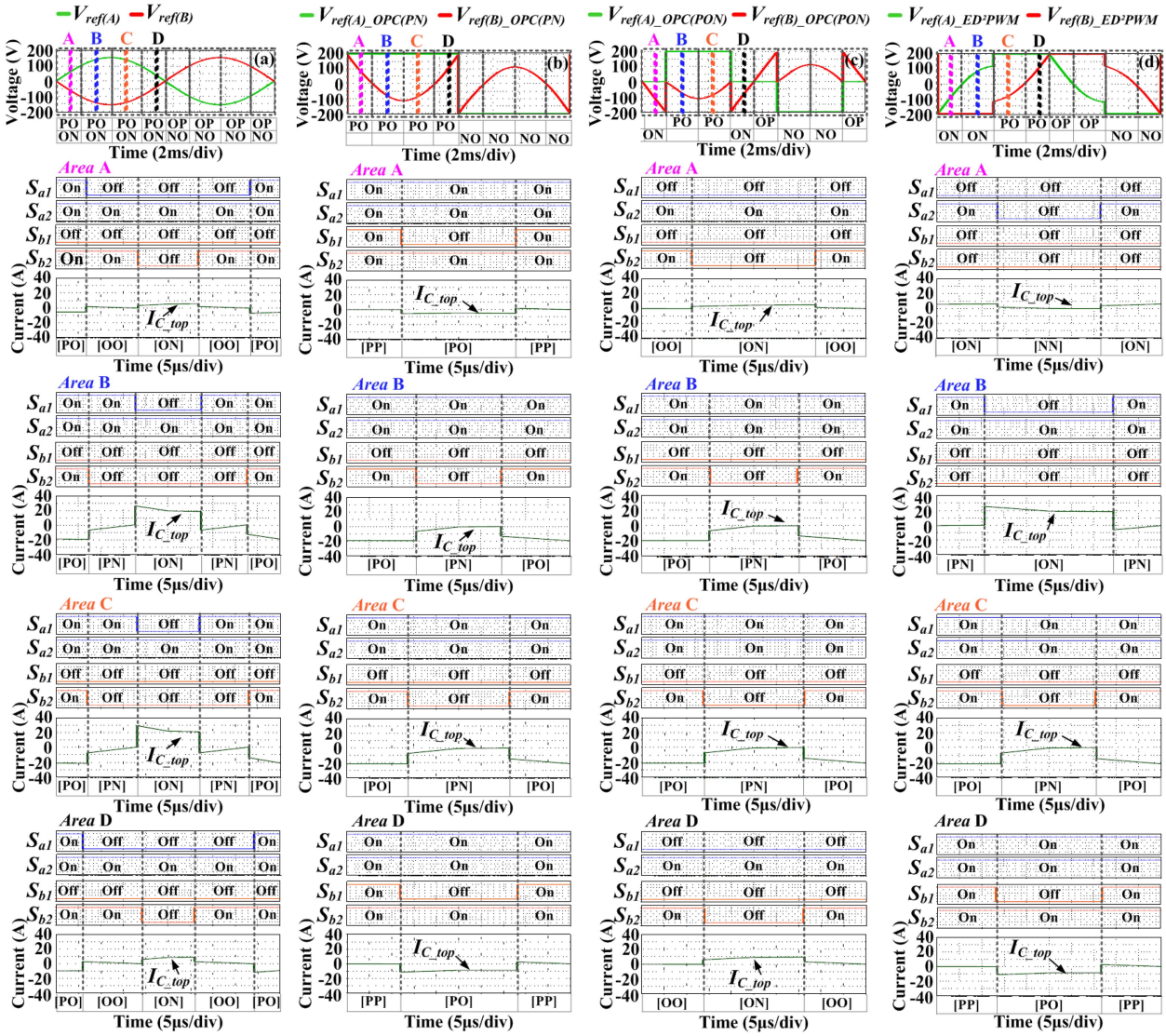

Fig. 7. Reference voltages, corresponding voltage vector, and capacitor current in a switching cycle under different PMW methods. (a) UP-PWM. (b) OPC-PWM(PN). (c) OPC-PWM(PON). (d) ED^{2}PWM.

Under [PN], the outputs are unconnected to neutral-point Z as shown in Fig. 6(a), and thus the current does not flow into Z. In the case of [OO], since two outputs are connected to Z as illustrated in Fig. 6(b), the current does not flow into Z. Under the P-type switching states of small voltage vectors such as [PO] as shown in Fig. 6(c), the current flows into Z. Therefore, the lower capacitor voltage (V_{DC2}) is raised, but the upper capacitor voltage (V_{DC1}) is reduced. The N-type switching states such as [ON] make V_{DC1} increase, but $V_{\mathrm{DC}\,2}$ decreases because the current flows out from Z as shown in Fig. 6(d). Consequently, the small voltage vectors affect the ripple current of the dc-link capacitors but the impact of the large and zero vectors is inconsiderable on the ripple current of the dc-link capacitors.

Fig. 7 shows the reference voltages, corresponding switching states, and capacitor current in a switching cycle under different PMW methods. The upper capacitor current is analyzed by considering the half fundamental period, where the reference voltage of leg-A has a positive value. There are both N-type and P-type switching states of small vectors in a switching cycle in all areas as shown in Fig. 7(a). It means that the polarity of the capacitor current changes in a switching cycle. However, under the DPWM methods, there is only one type of the small voltage vector in a switching cycle, and it is maintained for a certain clamping period as shown in Fig. 7(b)–(d), respectively. The polarity of the capacitor current does not change for that period. As illustrated in Fig. 7(b), under the OPC-PWM(PN), leg-A is kept to [P] during half of the fundamental period.

Therefore, only [PO] exists in all areas *A*, *B*, *C*, and *D*. The polarity of the capacitor current is maintained for half of the fundamental period. Consequently, the polarity of the capacitor current changes once for the fundamental period. In the case of OPC-PWM(PON), there is [ON] in areas *A* and *D*, where the leg-A is clamped to [O] but [PO] in areas *B* and *C*, where the leg-A is fixed to [P]. Hence, the polarity of the capacitor current changes five times during the fundamental period as shown in Fig. 7(c). Lastly, the capacitor current under the ED^{2}PWM

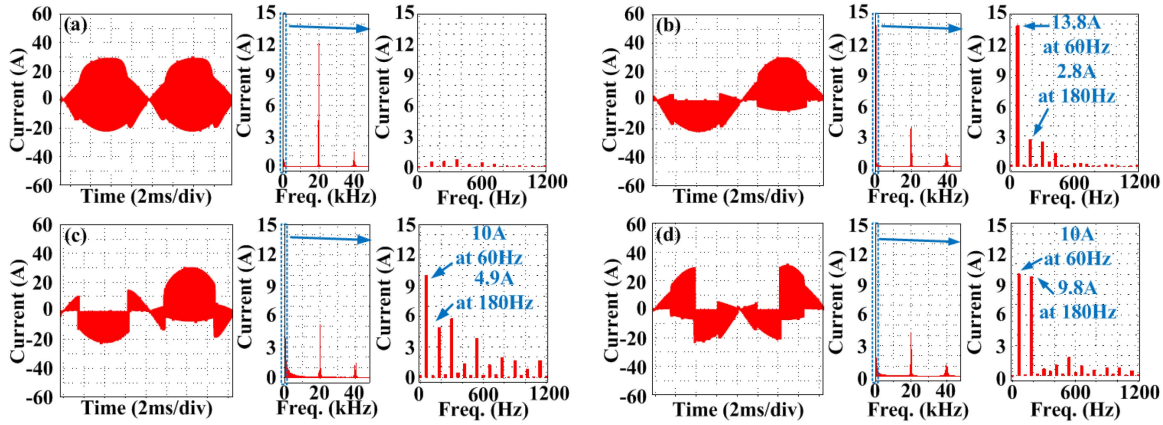

Fig. 8. DC-link capacitor current and FFT analysis at 7 kW with *MI* of 0.78 under different PWM methods. (a) UP-PWM. (b) OPC-PWM(PN). (c) OPC-PWM(PON). (d) ED^{2}PWM.

is shown in Fig. 7(d). It is seen that [ON] exists in areas *A* and *B*, while there is [PO] in areas *C* and *D*. The polarity of the capacitor current is changed twice during the fundamental period. Consequently, compared with that under UP-PWM, the polarity of the capacitor current is changed less frequently when the DPWM methods are applied. Therefore, it can be expected that the capacitor current has more low-frequency components under the DPWM methods. It causes higher power loss and thus higher hot-spot temperature. Furthermore, the DPWM methods also affect capacitor current differently.

Fig. 8 shows the currents of the upper dc-link capacitor (I_{C_top}) and their fast Fourier transform (FFT) analysis results under considered four PWM methods, respectively. As expected, the dc-link capacitor has higher ripple currents at low-frequency regions when the DPWM methods are applied. The dc-link capacitor mainly has a ripple current at 20 kHz when the UP-PWM is applied, where P_{cap} is 3.86 W. Under OPC-PWM(PN) as shown in Fig. 8(b), the capacitor has ripple currents at low-frequency regions. It has the highest ripple current of 13.8 A at 60 Hz, which is the dominant current in P_{cap} since R_{ESR} has a relatively higher value at low-frequency regions and tends to decrease as the frequency increases. Therefore, P_{cap} is increased by 7.16 W. It is seen that under OPC-PWM(PON), the ripple current at 60 Hz is reduced from 13.8 to 10 A. Even though the ripple currents at other frequencies such as 180 and 240 Hz are increased, the effect of the reduction in the ripple current at 60 Hz on P_{cap} is more significant. It has a lower P_{cap} of 6.02 W compared with that under OPC-PWM(PN). In the case of ED^{2}PWM, compared with OPC-PWM(PON), it has the same ripple current at 60 Hz but an increased ripple current at 180 Hz. Therefore, P_{cap} is 6.72 W, which is higher than that under OPC-PWM(PON) but lower than that under OPC-PWM(PN).

The corresponding T_{hot} is given in Fig. 9 under four PWM methods. The capacitor under UP-PWM has the lowest T_{hot} of 65.2 °C. It has the highest T_{hot} of 87.7 °C under OPC-PWM(PN) as analyzed and followed by T_{hot} of 84.7 °C under ED^{2}PWM and T_{hot} of 80.1 °C under OPC-PWM(PON).

It is seen that applying DPWM methods lower the reliability of the dc-link capacitor due to increased T_{hot}.

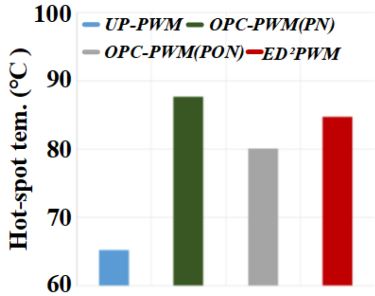

Fig. 9. Hotspot temperature of the DC-link capacitor under different PWM methods.

IV. Reliability-Oriented Application Method of DPWM

A. Proposed DPWM Strategy

As previously analyzed in Section II, the OPC-PWM methods cause the asymmetric T_j distribution between two legs. Furthermore, the highest T_j of the power devices is also increased. ED^{2}PWM leads to the symmetric T_j distribution of power devices between two legs with the reduced highest T_j of the power devices. Therefore, the application method of ED^{2}PWM for equal T_j distribution should be retained. However, this method leads to the highest T_{hot} of the dc-link capacitors. The OPC-PWM(PON) has the best performance among the DPWM methods in terms of T_{hot}. The period where the switching state is fixed to [O] contributes to the polarity change of the dc-link capacitor current, which leads to less increase in T_{hot}. Therefore, this period is required to be kept.

The proposed DPWM method, called ED^{2}PWM(PON) is developed by adopting the advantages of the above two DPWM methods. Under the proposed DPWM, each leg is alternately fixed for the clamping period of 90° as ED^{2}PWM, while during the clamping period, the switching state is fixed to not only [P] or [N] but also [O] as OPC-PWM(PON) depending on the magnitude of the reference voltage. The reference voltages of the proposed ED^{2}PWM(PON) are illustrated in Fig. 10 and obtained

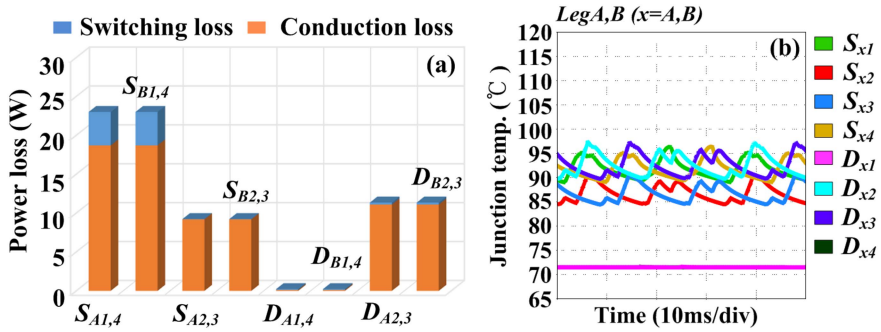

Fig. 11. Power loss and thermal loadings under the proposed ED²PWM(PON) with *MI* of 0.78. (a) Power loss distribution. (b) Junction temperature distribution.

as follows:

$$
\begin{aligned}
&(\text{if } V_{\text{ref}(A)}/(V_{\text{DC}}/2) \geq 0.5)\\
&\quad [\text{for [P] Clamping of Leg} - \text{A}]\\
&\quad V_{\text{ref}(A)\_\text{ED}^2\text{PWM(PON)}} = V_{\text{DC}}/2\,,\\
&\quad V_{\text{ref}(B)\_\text{ED}^2\text{PWM(PON)}} = V_{\text{DC}}/2 - V_{\text{ref}(A)} + V_{\text{ref}(B)}\\
&\quad [\text{for [N] Clamping of Leg} - \text{B}]\\
&\quad V_{\text{ref}(A)\_\text{ED}^2\text{PWM(PON)}} = -V_{\text{DC}}/2 + V_{\text{ref}(A)} - V_{\text{ref}(B)}\\
&\quad V_{\text{ref}(B)\_\text{ED}^2\text{PWM(PON)}} = -V_{\text{DC}}/2\\
&(\text{if } -0.5 \leq V_{\text{ref}(A)}/(V_{\text{DC}}/2) < 0.5)\\
&\quad [\text{for [O] Clamping of Leg} - \text{A}]\\
&\quad V_{\text{ref}(A)\_\text{ED}^2\text{PWM(PON)}} = 0,\\
&\quad V_{\text{ref}(B)\_\text{ED}^2\text{PWM(PON)}} = -V_{\text{ref}(A)} + V_{\text{ref}(B)}\\
&\quad [\text{for [O] Clamping of Leg} - \text{B}]\\
&\quad V_{\text{ref}(A)\_\text{ED}^2\text{PWM(PON)}} = V_{\text{ref}(A)} - V_{\text{ref}(B)}\\
&\quad V_{\text{ref}(B)\_\text{ED}^2\text{PWM(PON)}} = 0\\
&(\text{if } V_{\text{ref}(A)}/(V_{\text{DC}}/2) < -0.5)\\
&\quad [\text{for [N] Clamping of Leg} - \text{A}]\\
&\quad V_{\text{ref}(A)\_\text{ED}^2\text{PWM(PON)}} = -V_{\text{DC}}/2\\
&\quad V_{\text{ref}(B)\_\text{ED}^2\text{PWM(PON)}} = -V_{\text{DC}}/2 - V_{\text{ref}(A)} + V_{\text{ref}(B)}\\
&\quad [\text{for [P] Clamping of Leg} - \text{B}]\\
&\quad V_{\text{ref}(A)\_\text{ED}^2\text{PWM(PON)}} = V_{\text{DC}}/2 + V_{\text{ref}(A)} - V_{\text{ref}(B)}\\
&\quad V_{\text{ref}(B)\_\text{ED}^2\text{PWM(PON)}} = V_{\text{DC}}/2. \qquad (7)
\end{aligned}
$$

B. Thermal Loadings of Power Devices and DC-Link Capacitors Under the Proposed DPWM

Thermal loadings of power devices and dc-link capacitors are analyzed based on (5) and (6) as previously performed. The power loss and T_j distributions are shown in Fig. 11 under the proposed ED²PWM(PON) with MI of 0.78. It is seen that two legs have symmetric power loss and T_j distributions.

The total power losses and the junction temperatures of the

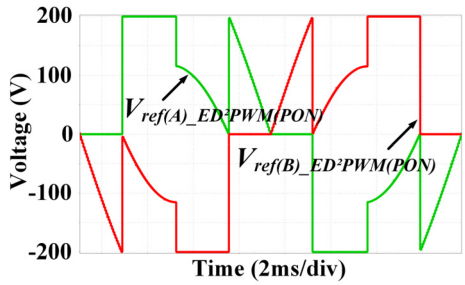

Fig. 10. Reference voltages under the proposed ED²PWM(PON).

are summarized in Table II for comparison. Even though the proposed ED²PWM(PON) leads to a slightly higher power loss of 174.2 W and T_j of 97.5 °C than those under the conventional ED²PWM when MI is 0.78, it is not significant and still keeps the advantages of ED²PWM in terms of the reliability of the power devices and efficiency. Under the other modulation indices of 0.96 and 0.62, the proposed ED²PWM(PON) keeps the advantage in power loss reduction and T_j reduction with symmetric T_j distribution.

The reference voltages, corresponding switching states, and capacitor current in a switching cycle under the proposed ED²PWM(PON) are shown in Fig. 12. It is seen that during each clamping period, there is only one type of switching state of small voltage vectors. There is only [PO] in areas *A* and *C* and [ON] in areas *B* and *D*. However, the polarity change in dc-link capacitor current occurs when the area is changed from one to another. Consequently, the polarity of the capacitor current is switched six times during the fundamental period.

Fig. 13 shows the I_{C_top} and its FFT analysis result under the proposed method when the modulation index is 0.78. It is seen that the ripple current at 60 Hz is remarkably reduced compared with that under the ED²PWM (see Fig. 8). Furthermore, although the ripple current at 180 Hz is still higher compared with those under the OPC-PWM methods, due to the significant decrease in the ripple current at 60 Hz, it has the lowest power loss of 5.33 W and thus lowest T_{hot} of 75.4 °C under the ED²PWM(PON) among the DPWM methods as listed in Table III.

In the case of the different modulation indices of 0.96 and 0.62, a similar tendency also can be seen. The proposed ED²PWM(PON) leads to the lowest T_{hot} of 59.0 °C and T_{hot} of 87.6 °C under *MI* of 0.96 and *MI* of 0.62, respectively.

Fig. 14 shows V_{DC1} and V_{DC2} under different DPWM

TABLE II
JUNCTION TEMPERATURE AND TOTAL POWER LOSS OF THE POWER DEVICE UNDER THE DIFFERENT PWM METHODS AND MODULATION INDICES

MI	PWM Methods	*Junction Temperature* T_j (°C)								Power Loss (W)
		$S_{A1,4}$	$S_{A2,3}$	$D_{A1,4}$	$D_{A2,3}$	$S_{B1,4}$	$S_{B2,3}$	$D_{B1,4}$	$D_{B2,3}$	
0.96	UP-PWM	102.8	81.7	71.1	86.6	102.8	81.7	71.1	86.6	171.9
	OPC-PWM(PN)	98	67.7	68.2	67.7	93.1	88.6	76.1	93.6	153.5
	OPC-PWM(PON)	96.1	73.5	68.1	76.1	96.2	84.9	68.2	91.6	155.7
	ED^{2}PWM	95.9	79.5	75.4	82.6	95.8	79.6	75.4	82.6	153.6
	ED^{2}PWM(PON)	96.2	79.6	68.3	84.4	96.2	79.6	68.3	84.4	155.9
0.78	UP-PWM	104	93.2	75.3	99.9	104	93.2	75.3	99.9	193.8
	OPC-PWM(PN)	101.1	70.8	71.4	70.8	88.2	106.3	82.6	111.2	170.1
	OPC-PWM(PON)	97.7	80.6	71.4	84.5	93.6	100.1	71.6	108.8	173.7
	ED^{2}PWM	95.2	90.8	82.6	94.2	95.2	90.8	82.6	94.2	170.7
	ED^{2}PWM(PON)	96.4	90.8	71.7	97.5	96.4	90.8	71.7	97.5	174.2
0.62	UP-PWM	106.3	103.8	79.5	111.6	106.3	103.8	79.5	111.6	216.3
	OPC-PWM(PN)	104.3	73.7	74.7	73.7	84.3	125.3	94.2	125.4	187.5
	OPC-PWM(PON)	97.5	90.2	74.7	95.9	95.4	110.8	74.9	119.9	191.6
	ED^{2}PWM	95.2	101.8	90.2	102.9	95.2	101.8	90.2	102.9	187.3
	ED^{2}PWM(PON)	97.2	100.6	74.9	108.3	97.2	100.6	74.9	108.3	191.4

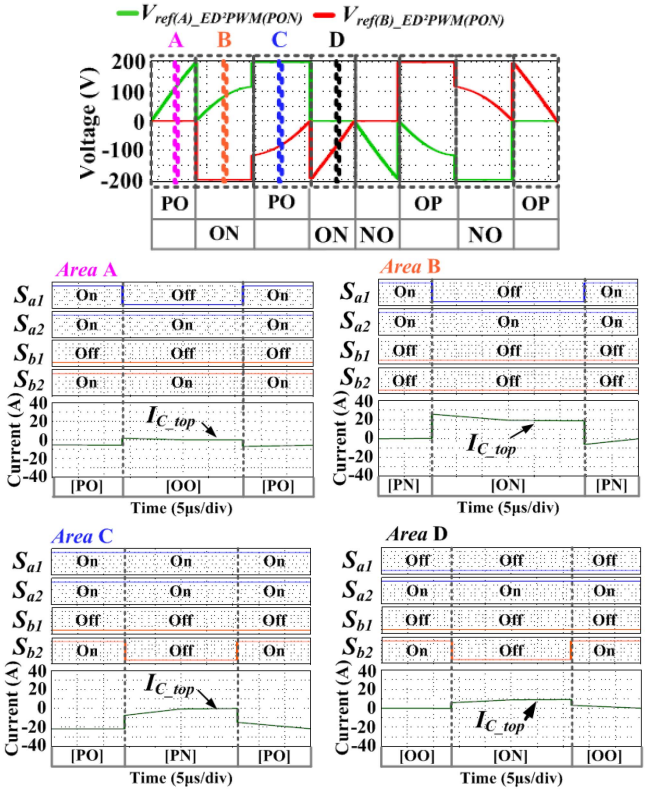

Fig. 12. Reference voltages, corresponding voltage vector and capacitor current in a switching cycle under the proposed ED^{2}PWM(PON).

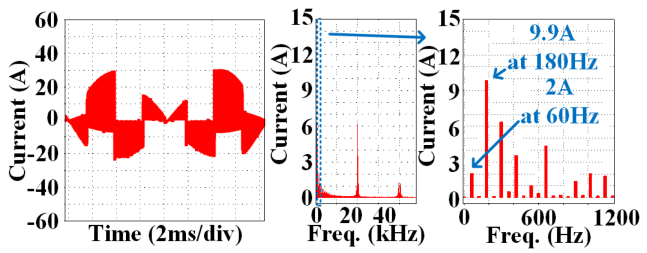

Fig. 13. DC-link capacitor current and FFT analysis at 7 kW under *MI* of 0.78 when the ED^{2}PWM(PON) is applied.

TABLE III
HOTSPOT TEMPERATURE OF THE DC-LINK CAPACITORS UNDER THE DIFFERENT PWM METHODS AND MODULATION INDICES

MI	PWM Methods	UP-PWM	OPC-PWM (PN)	OPC-PWM (PON)	ED^{2}PWM	ED^{2}PWM (PON)
0.96	P_{cap} (W)	2.17	3.62	2.98	3.57	2.85
	T_{hot} (°C)	54.4	64.1	59.9	63.8	59.0
0.78	P_{cap} (W)	3.86	7.16	6.02	6.27	5.33
	T_{hot} (°C)	65.2	87.7	80.1	84.7	75.4
0.62	P_{cap} (W)	4.93	11.15	8.52	9.40	7.16
	T_{hot} (°C)	72.8	114.2	96.7	102.4	87.6

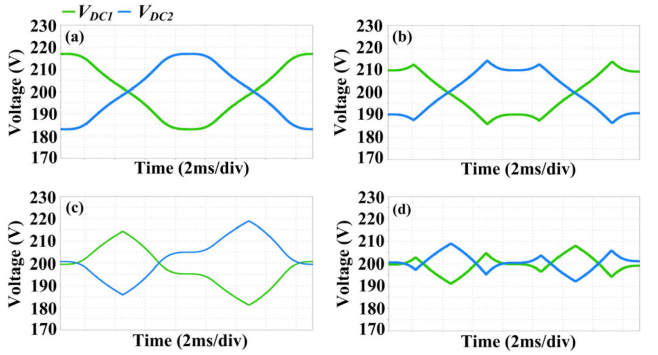

Fig. 14. Two capacitor voltages under different DPWM methods. (a) OPC-PWM(PN). (b) OPC-PWM(PON) (c) ED^{2}PWM (d) ED^{2}PWM(PON).

capacitor voltages is the lowest when the proposed ED^{2}PWM(PON) is applied.

V. MISSION PROFILE-BASED COMPARATIVE RELIABILITY EVALUATION

In this section, the mission profile-based reliability assessment of the single-phase five-level T-type NPC inverter is performed under different PWM methods to validate the effectiveness of the proposed ED^{2}PWM(PON). The mission profile of the PV system composed of solar irradiation and ambient temperature recorded from Arizona in the USA as shown in

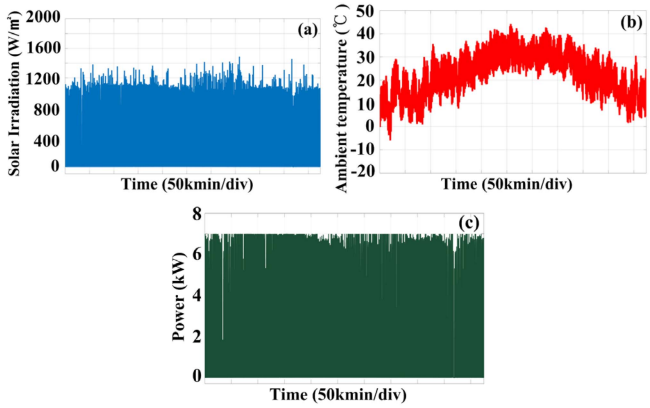

Fig. 15. Annual PV mission profile recorded in Arizona of USA. (a) Solar irradiation. (b) Ambient temperature. (c) Corresponding generated power.

Fig. 15 is used for the case study and the corresponding generated power is shown in Fig. 15(c).

The lifetime evaluation of the power devices and dc-link capacitors is carried out first by assessing their accumulated damages. Then, the system-level reliability of the T-type inverter is evaluated by considering all power devices and dc-link capacitors. A more detailed procedure for the reliability assessment can be found in [21], [22], [23], and [24].

A. Accumulated Damage of Power Devices Under Different PWM Methods

Thermal stress is the dominant cause of wear-out failure of the power device [12]. Typically, the lifetime presented as the number of cycles to failure (N_f) can be determined from the thermal stress factors of T_j-swing (ΔT_j), mean value of T_j (T_{jm}), and heating time ($t_{\rm on}$). By the Rainflow counting method, these factors are extracted from the T_j profile obtained through the look-up table-based approach as explained in [21], [22], [23], and [24]. In this study, the lifetime model given in [25] is used because the lifetime model of the IGBT module considered in this study is not available. Therefore, it is suggested that the results should be considered only for the purpose of the comparison. The lifetime model for the bond-wire failure is given as follows:

$$N_f = A \cdot (\Delta T_j)^{-\beta_1} \cdot \exp\left(\frac{\beta_2}{T_{jm}+273}\right) \cdot (t_{\rm on})^{\beta_3} \cdot I^{\beta_4} \cdot V^{\beta_5} \cdot D^{\beta_6}. \tag{8}$$

The parameter values for the lifetime model are listed in Table IV and also can be obtained from [25]. The accumulated damage (*AD*) of power devices is computed based on Miner's rule as follows:

$$\text{AD} = \sum_{i=1}^{k} \frac{n_i}{(N_f)_i} \tag{9}$$

where n_i is the number of cycles accumulated at a certain combination of thermal stress factors (S_i) and $(N_f)_i$ is the number of cycles to failure at S_i. If *AD* becomes 1, it is regarded that the capacitor reaches the end-of-life [26].

TABLE IV
PARAMETERS FOR LIFETIME MODELS OF POWER DEVICES AND DC-LINK CAPACITORS [20], [25]

Lifetime model			
Power device		*Capacitor*	
Parameter	*Value*	*Parameter*	*Value*
A	2.03e+14	L_0	3000 [h]
β_1	-4.416	T_0	105 [°C]
β_2	1285	V_0	500 [V]
β_3	-0.436	n	1
β_4	-0.716		
β_5	-0.761		
β_6	-0.5		

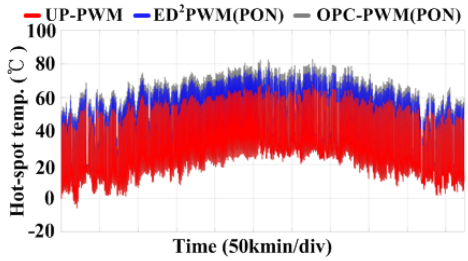

Fig. 16. Hotspot temperature profiles of DC-link capacitors in the mission profile with the UP-PWM, OPC-PWM(PN), and ED^{2}PWM(PON).

The *AD* of each power device under different PWM methods during the mission profile is summarized in Table IV, where the alternating OPC-PWM (Alt. OPC-PWM) means that each leg is alternately clamped per day to balance *AD* between two legs. *AD* under the proposed ED^{2}PWM(PON) has a slightly higher value than that under conventional ED^{2}PWM, but it is not significant and still low compared with those under the other PWM methods. Therefore, it can keep the advantage of the conventional ED^{2}PWM in terms of the reliability of power devices. Furthermore, the results also show that the Alt. OPC-PWM reduces the highest *AD* and also balances *AD* between two legs. Thus, the lifetime of the power device can increase compared with that under the conventional OPC-PWM.

B. Accumulated Damage of DC-Link Capacitors Under Different PWM Methods

The wear-out failure mechanism of aluminum electrolytic capacitors is accelerated as $T_{\rm hot}$ and applied voltage (V) are higher [14]. Therefore, the lifetime of the capacitor at a certain operating condition (L_f) is generally modeled by considering those factors as follows:

$$L_f = L_0 \times 2^{((T_0 - T_{hot})/10)} \times (V/V_0)^{-n} \tag{10}$$

where L_o is the lifetime at the accelerated test condition, V is the applied voltage at the operating condition, V_o is the voltage at the accelerated test condition, $T_{\rm hot}$ is the hotspot temperature, T_o is the temperature at the accelerated test condition, and n is the voltage stress exponent. The related lifetime model parameters are listed in Table IV and also can be obtained in [20].

The $T_{\rm hot}$ profiles of the capacitors are also obtained based on (6) in a similar way to obtain the T_j profile. The selected $T_{\rm hot}$ profiles under the UP-PWM, OPC-PWM(PON), and proposed ED^{2}PWM(PON) are illustrated in Fig. 16. It is seen that dc-link

TABLE V
ACCUMULATED DAMAGES OF CAPACITORS AND POWER DEVICES OF THE T-TYPE NPC INVERTER WITH THE DIFFERENT PWM METHODS

PWM Methods	Accumulation Damage (%)								
	Component								
	$S_{A1,4}$	$S_{A2,3}$	$D_{A1,4}$	$D_{A2,3}$	$S_{B1,4}$	$S_{B2,3}$	$D_{B1,4}$	$D_{B2,3}$	$C_{top,bot}$
UP-PWM	1.270	0.641	0.127	1.065	1.270	0.641	0.127	1.065	1.353
OPC-PWM (PN)	1.113	0.092	0.099	0.099	0.431	1.531	0.279	2.238	3.614
OPC-PWM (PON)	0.897	0.234	0.100	0.336	0.638	1.055	0.103	1.908	2.519
Alt. OPC-PWM (PN)	0.772	0.812	0.189	1.165	0.772	0.812	0.189	1.165	3.614
Alt. OPC-PWM (PON)	0.768	0.645	0.102	1.122	0.768	0.645	0.102	1.122	2.519
ED^{2}PWM	0.738	0.554	0.282	0.749	0.738	0.554	0.282	0.749	3.131
ED^{2}PWM(PON)	0.800	0.546	0.104	0.925	0.800	0.546	0.104	0.925	2.077

capacitors have the lower T_{hot} profile under the ED^{2}PWM(PON) than T_{hot} profile under the OPC-PWM(PON).

The *AD* of the capacitor also can be similarly obtained from (9) based on Miner's rule and it is listed in Table V. The capacitor has the lowest *AD* of 2.077 under the proposed ED^{2}PWM(PON) among the DPWM methods. Therefore, the longest lifetime can be expected.

The reliability of the inverter should be evaluated at the system level by considering all power devices and capacitors since the failure of each component leads to the inverter failure.

C. Comparative Analysis of Reliability of the T-Type Inverter

The lifetime distributions of the component can be obtained by employing the Monte Carlo analysis method, which is carried out with a population of 10 000 samples by considering 5% variations with normal distribution in the thermal stress and lifetime model parameters for the power device and capacitors, respectively. More detailed information about the Monte Carlo method can be found in [21], [22], [23], and [24]. As a result, the lifetime distributions of each power device and capacitor are acquired. By fitting the lifetime data of 10 000 samples of each component into the Weibull distribution, the cumulative distribution function (CDF) considered unreliability function is obtained as follows:

$$F(t) = \int_0^t \left(\frac{\beta}{\eta} \left(\frac{t}{\eta} \right)^{\beta-1} e^{-\left(t/\eta\right)^{\beta}} \right) dt \tag{11}$$

where $F(t)$ = CDF, β = shape parameter, η = scale parameter, and t = operating time. The CDF of the T-type inverter system ($F_{\text{inv}}(t)$) is affected by the CDF including all power devices ($F_d(t)$) and all capacitors ($F_c(t)$). $F_{\text{inv}}(t)$ is given as follows:

$$\begin{aligned} F_d(t) &= 1 - \prod_{m=1}^{i} (1 - F_m(t)), \\ F_c(t) &= 1 - \prod_{n=1}^{j} (1 - F_n(t)), \\ F_{\text{inv}}(t) &= 1 - (1 - F_d(t))(1 - F_c(t)) \end{aligned} \tag{12}$$

where $F_m(t)$ and $F_n(t)$ are the CDF of each power device and capacitor, respectively.

The percentile lifetime called B_x lifetime can be obtained from the unreliability function. In this article, the B_{10} lifetime, which indicates the time by which failure in 10% of the inverters occurs, namely the reliability is 0.9, is considered.

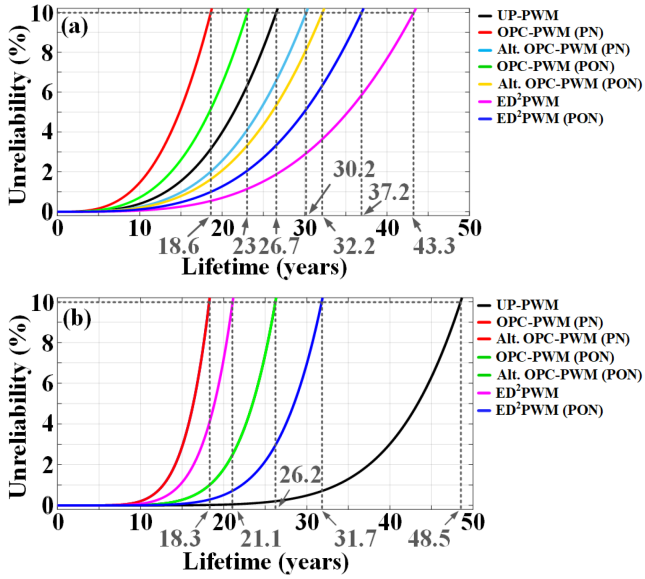

Fig. 17. Unreliability functions under different PWM methods. (a) Power devices. (b) DC-link capacitors.

Fig. 17(a) shows the unreliability function of the power device considering all power devices under different PWM methods. It is seen that the B_{10} lifetime is 26.7 years under the UP-PWM and reduced to 18.6 and 23 years when the OPC-PWM(PN) and OPC-PWM(PON) are applied, respectively. However, the Alt. OPC-PWM methods increase it by more than 30 years. Under the conventional ED^{2}PWM, it has the longest B_{10} lifetime of 43.3 years followed by the B_{10} lifetime of 37.2 years under the proposed ED^{2}PWM(PON). Even though the proposed ED^{2}PWM(PON) leads to a shorter B_{10} lifetime than that under ED^{2}PWM, a significant increase in the B_{10} lifetime still can be seen.

The unreliability functions of the dc-link capacitor under different PWM methods are illustrated in Fig. 17(b). The lifetime is reduced when all considered DPWM methods are applied as expected in Section III. However, the proposed ED^{2}PWM(PON) has the least negative effect on the reliability of the dc-link capacitor. It has the longest B_{10} lifetime of 31.7 years under the proposed ED^{2}PWM(PON). It is increased by more than

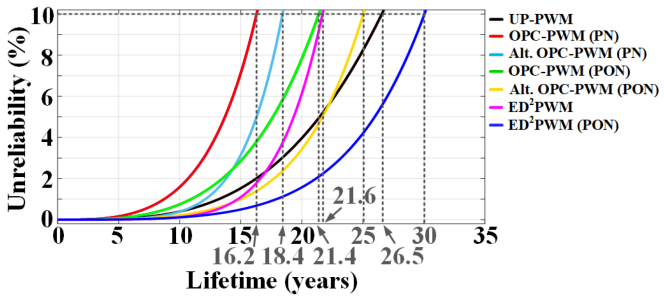

Fig. 18. Unreliability functions of T-type inverter including power devices and DC-link capacitors under different PWM methods.

TABLE VI
B_{10} LIFETIME OF POWER DEVICES, CAPACITORS AND T-TYPE NPC INVERTER UNDER DIFFERENT PWM METHODS

PWM	B_{10} Lifetime (years)		
	Device	Cap	Inverter
UP-PWM	26.7	48.5	26.5
OPC-PWM (PN)	18.6	18.3	16.2
OPC-PWM (PON)	23	26.2	21.4
Alt. OPC-PWM (PN)	30.2	18.3	18.4
Alt. OPC-PWM (PON)	32.2	26.2	25
ED^{2}PWM	43.3	21.1	21.6
ED^{2}PWM(PON)	37.2	31.7	30

10 and 5 years compared with conventional ED^{2}PWM and OPC-PWM(PON), respectively.

$F_{\text{inv}}(t)$ under all considered PWM methods are shown in Fig. 18. Under the UP-PWM, the inverter has the B_{10} lifetime of 26.5 years, where the reliability of the power device plays a key role in the reliability of the single-phase 5LT-NPC inverter. When the OPC-PWM(PN) and OPC-PWM(PON) are applied, it is reduced to 16.2 years and 21.4 years, respectively, because the lifetimes of both the power device and capacitor decrease. Under the Alt. OPC-PWM(PN) and Alt. OPC-PWM(PON), even though the B_{10} lifetime of the power device increases, the B_{10} lifetime of the inverter decreases to 18.4 and 25 years, respectively, due to the reduced B_{10} lifetime of the capacitor. As expected, under the conventional ED^{2}PWM, the lifetime of the power device is increased. However, the lifetime of the inverter is reduced to 21.6 years due to the decrease in the lifetime of the dc-link capacitor. The lifetime of the capacitor predominantly affects the lifetime of the 5LT-NPC inverter under those three PWM methods. Under the proposed ED^{2}PWM(PON), the lifetime of the dc-link capacitor is relatively longer than those under the other PWM methods even though the lifetime of the dc-link capacitor is decreased compared with that under the UP-PWM. Furthermore, the lifetime improvement of the power device also can be kept. Consequently, the longest B_{10} lifetime of 30 years of the 5LT-NPC inverter is achieved.

The B_{10} lifetime of the power device, capacitor, and inverter under PWM methods are summarized in Table VI.

VI. EXPERIMENTS

The feasibility and effectiveness of the proposed DPWM are verified through experiments under the following conditions: dc-link capacitors (C_{DC}): 2200 μF, dc-link voltage (V_{DC}): 400 V (*MI* of 0.78), 325 V (*MI* of 0.96), switching frequency (f_{sw}): 20 kHz, and load (R, L): 40 Ω, 1.5 mH.

Fig. 19(a) shows the pole voltages (V_A and V_B), output voltage (V_{out}), output current (I_{out}) in the time domain, and the output voltage (V_{out}) in the frequency domain under *MI* of 0.78 when UP-PWM is applied. The pole voltage of each leg and output voltage have three levels and five levels, respectively, and the sinusoidal output current is generated. It is seen that the capacitor has a ripple current mainly at 120 Hz as shown in Fig. 20(a).

Under the OPC-PWM(PN), the pole voltage of leg-A is clamped to $V_{\text{DC}}/2$ or $-V_{\text{DC}}/2$ as shown in Fig. 19(b). In the case of OPC-PWM (PON), leg-A has not only $V_{\text{DC}}/2$ or $-V_{\text{DC}}/2$ but also 0 for a certain period as shown in Fig. 19(c). Therefore, reduced switching loss can be obtained under both OPC-PWM methods. The output voltage has five levels, but it is seen that the output currents have more ripple components compared with that under the UP-PWM because the switching frequency of the output voltage is reduced by half due to the clamping leg-A. It is represented by the FFT result of V_{out}, which has a higher harmonic component at 20 kHz, and it results in the increase of the output THD. The dc-link capacitor has additional ripple currents at 60 and 180 Hz as shown in Fig. 20(b). Thus, it verifies that the DPWM methods lead to higher P_{cap} and thus higher T_{hot} due to higher ripple currents at lower frequency regions. Under the OPC-PWM(PON) as shown in Fig. 20(c), the capacitor has a smaller ripple current at 60 Hz than that under the OPC-PWM(PN). Therefore, even though it has a higher ripple current at 180 Hz, the smaller P_{cap}, which leads to the lower T_{hot} can be expected as analyzed in the previous Section III since R_{ESR} has a higher value at 60 Hz than that at 180 Hz.

As illustrated in Fig. 19(d), two legs are alternately clamped to [P] or [N] per 90°, and thus they have the corresponding pole voltage of $V_{\text{DC}}/2$ or $-V_{\text{DC}}/2$ when ED^{2}PWM is applied. Therefore, improved efficiency is expected due to reduced switching loss. Furthermore, because the clamping period is equally distributed, the symmetric T_j distribution between the two legs can be expected. The output voltage also has five levels and the output current similar to those under OPC-PWM methods is obtained. In this case, the dc-link capacitor also has ripple currents at 60 and 180 Hz as shown in Fig. 20(d). The magnitude of the ripple current at 60 Hz is almost the same, but the magnitude of the ripple current at 180 Hz is higher than that under the OPC-PWM(PON). However, compared with the OPC-PWM(PN), the ripple current at 60 Hz is smaller, but the ripple current at 180 Hz is higher. Consequently, it results in higher than that under the OPC-PWM(PON) but lower T_{hot} than that under the OPC-PWM (PN) as analyzed in the previous Section III.

The V_A, V_B, V_{out}, I_{out}, and V_{out} in the frequency domain under the proposed ED^{2}PWM(PON) are shown in Fig. 19(e). Similar to the ED^{2}PWM, two legs are alternately clamped per 90° but it is clamped to [O] as well as [P] or [N]. The reduced switching loss can be expected since one of the two legs is clamped during the fundamental period. Furthermore, an equal T_j distribution between the two legs also can be expected. There are no additional distortions in the output voltage and current compared with conventional DPWM methods. The FFT analysis result of the dc-link current under the proposed ED^{2}PWM (PON) is

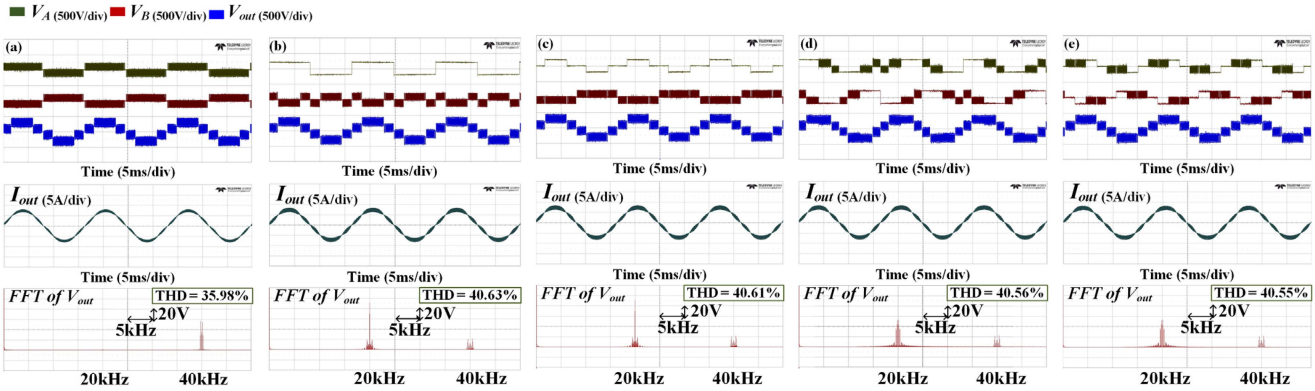

Fig. 19. Pole voltages (V_A and V_B), output voltage ($V_{\rm out}$), and output current ($I_{\rm out}$) and FFT results of $V_{\rm out}$ operated at *MI* of 0.78 under different PWM methods. (a) UP-PWM. (b) OPC-PWM(PN). (c) OPC-PWM(PON). (d) ED^{2}PWM. (e) Proposed ED^{2}PWM(PON).

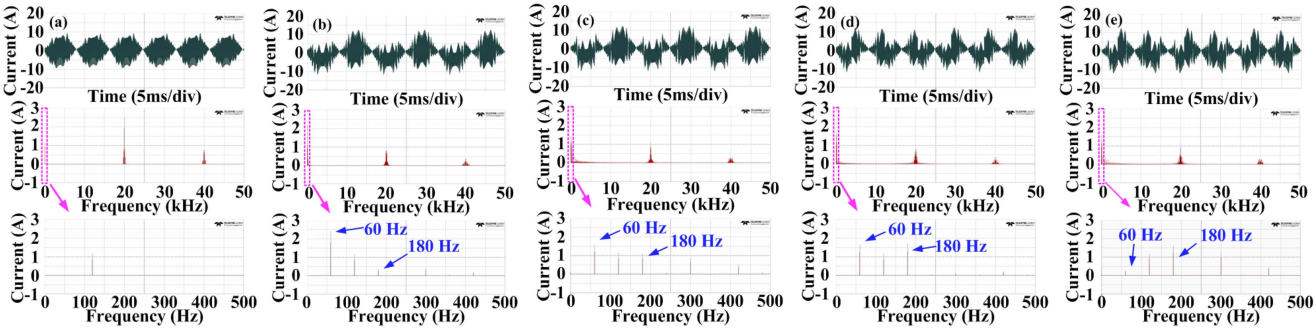

Fig. 20. Upper DC-link capacitor current ($I_{C\_\rm top}$) and FFT result operated at *MI* of 0.78 under different PWM methods. (a) UP-PWM. (b) OPC-PWM(PN). (c) OPC-PWM(PON). (d) ED^{2}PWM. (e) Proposed ED^{2}PWM(PON).

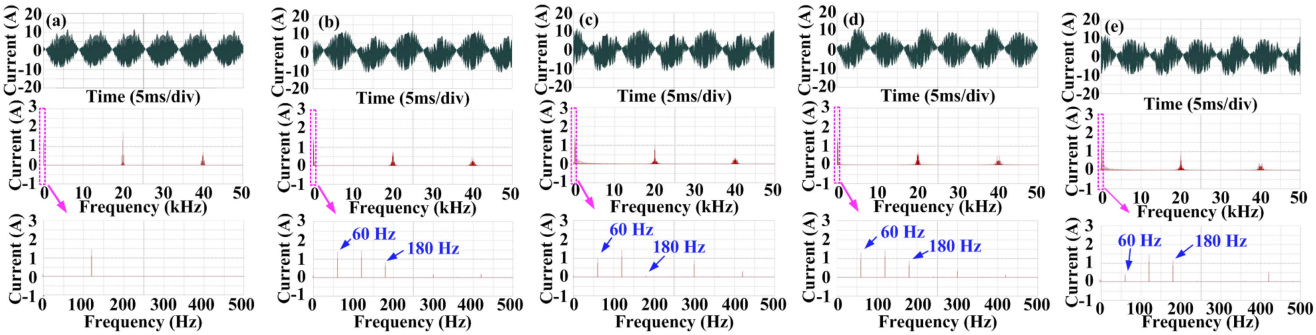

Fig. 21. Upper DC-link capacitor current ($I_{C\_\rm top}$) and FFT result operated at *MI* of 0.96 under different PWM methods. (a) UP-PWM. (b) OPC-PWM(PN). (c) OPC-PWM(PON). (d) ED^{2}PWM. (e) Proposed ED^{2}PWM(PON).

shown in Fig. 20(e). The ripple current at 60 Hz is remarkably reduced compared with those under the other DPWM methods, and the ripple current at 180 Hz is similar to that under ED^{2}PWM. Consequently, the lowest $T_{\rm hot}$ is achieved due to the significant reduction of the ripple component at 60 Hz.

The upper capacitor currents and its FFT analysis results under different PWM methods operated at a higher modulation index of 0.96 are illustrated in Fig. 21. It appears that when applying DPWM methods, there is a noticeable increase in ripple currents at both 60 and 180 Hz. This can lead to higher power loss and an elevated $T_{\rm hot}$. Similar to the previous result, the DPWM methods that contain switching state [O] tend to have a smaller ripple current compared to the other DPWM methods. When using the OPC-PWM(PON), there is a notable decrease in ripple current at 180 Hz. On the other hand, the proposed ED^{2}PWM(PON) method results in a significant reduction in ripple current at 60 Hz. As a result, it is expected that the dc-link capacitors under the proposed ED^{2}PWM(PON) have the lowest power loss and, therefore, the lowest $T_{\rm hot}$ due to the significant reduction in the ripple current at 60 Hz.

VII. Conclusion

This article has proposed a reliability-oriented DPWM strategy called ED^{2}PWM(PON) for the single-phase 5LT-NPC inverter. The proposed method can improve the lifetime of power devices by reducing the switching loss and achieving reduced T_j with symmetric distribution between the two legs. In addition, the dc-link capacitor has a lower $T_{\rm hot}$ compared with those under other DPWM methods, which reduces the negative effect of DPWM on the lifetime of the dc-link capacitor. The effectiveness of the proposed ED^{2}PWM(PON) is verified through the mission profile-based reliability assessment of the 5LT-NPC inverter as a case study, where it achieves the longest B_{10} lifetime of 30 years among the considered seven PWM strategies. Furthermore, the feasibility and effectiveness of the proposed DPWM method are also verified through experiments.

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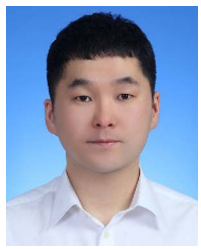

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