Phase-Shift Modulated Hybrid LLC and Half-Bridge Converter With Fixed Frequency for Wide Voltage Gain Range Application

Haiming Yu, Xiaogao Xie, *Senior Member, IEEE*, and Hanjing Dong, *Member, IEEE*

***Abstract*—In this article, a novel hybrid *LLC* and half-bridge (HB) converter is proposed for wide voltage gain applications. The proposed converter is composed of a conventional *LLC* resonant converter and a HB converter. The *LLC* resonant converter and the HB converter are connected in parallel on the primary side with an auxiliary winding of the *LLC* transformer inserted in the primary power loop of the HB converter, while the secondary windings of two converters transformers are inversely connected and share a voltage-doubler rectifier. The *LLC* and HB operate with the same fixed frequency, and the phase-shift modulation control between two converters is utilized to regulate the output voltage. Zero-voltage switching of all the primary switches and zero-current switching of all second side diodes can be achieved over a wide range of output voltage and load conditions. Detailed principle and voltage gain analysis based on time-domain method has been presented. After that, a simple approximate analysis method is proposed so that the voltage gain can be obtained more easily and main parameters of the converter can be fast optimally designed. Finally, a 1 KW laboratory prototype with 400 V input/50 V–450 V output has been built up to verify the theoretical analysis of the proposed converter. The peak efficiency achieves 97.9%, and features good voltage regulation capability. Thus, the proposed converter is suitable for wide voltage gain range applications.**

***Index Terms*—*LLC* resonant converter, phase-shift modulation, wide voltage gain.**

I. Introduction

THE wide voltage range dc–dc converters are becoming the core of numerous industrial applications, such as renewable power systems, electric vehicle, and charging systems [1]. The electric vehicle batteries or renewable energy storage batteries cover a wide output voltage range so it is necessary to design wide voltage gain range converters to be compatible with different voltage levels [2]. The *LLC* resonant converters have attracted much attention in wide voltage gain range applications due to their simple structure, Zero-voltage switching (ZVS) zero-current switching (ZCS) over the full load range, and high efficiency [3]. However, in wide voltage gain applications, since *LLC* is a frequency modulated method, switching frequency (f_s) must swing in a wide large range to meet the wide voltage gain range. This wide f_s rang makes the switching frequency deviate from the resonant frequency (f_r), which causes *LLC* efficiency to drop fast [4]. And the low band of switching frequency is a critical parameter for designing magnetic components. In order to meet wide voltage gain requirements, the minimum switching frequency is much lower than the resonant frequency. The lower switching frequency means larger magnetic cores size are required, which results in low power density. When the switching frequency is beyond the resonant frequency, it suffers from poor voltage regulation due to the gain curve tends to be smooth. Therefore, *LLC* with traditional frequency modulation is not suitable for wide voltage gain applications.

In order to solve the problems mentioned above, many schemes have been proposed [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30].

One of the solutions is to reduce the variation range of the switching frequency [5], [6], [7], [8]. In [5], the phase-shift modulation (PSM) combined with pulse frequency modulation (PFM) are adopted to the primary legs of a full-bridge (FB) *LLC* resonant converter for achieving wide voltage gain. However, the large phase-shift angle between primary legs under low input voltage increases the rms current on the primary side greatly and deteriorates the efficiency. In [6] and [7], an auxiliary *LC* resonant circuit is added to the third winding of the transformer, and the auxiliary circuit can change the equivalent magnetizing inductance according to the switching frequency. When the switching frequency decreases, the equivalent magnetizing inductance will decrease, so as to get a steeper gain curve making the gain further increased. Thus, within the same frequency variation range, the gain range is larger than that of a conventional *LLC*. However, it increases the magnetic core loss and resonant tank input current. This incurs high conduction and switching loss on the primary side switches. Besides, there is a risk of short circuit due to the zero impedance at the series resonance of the auxiliary inductor and the auxiliary capacitor at their resonance frequency. In [8], an improved scheme of adding *LC* branches is proposed. This solution requires two transformers, both primary and secondary of transformers are

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connected in series, and an auxiliary capacitor is connected in parallel with the primary side of one transformer. The auxiliary capacitor and the magnetizing inductance are in parallel resonance, which avoids the risk of short circuit due to the series resonance of the *LC* branch in [6] and [7]. However, the minimum switching frequency is 130 kHz, which is still too low compared to the resonant frequency of 200 kHz.

Another kind of solution is to modify the *LLC* structure through different state combinations of switch so that the wide voltage gain application requirement can be met [9], [10], [11], [12], [13], [14], [15], [16], [17], [18].

In [9], a secondary-side pulse width modulation (PWM) controlled *LLC* converter is proposed. The output voltage is regulated by changing the structure of the secondary side rectifier through the duty cycle of the secondary side auxiliary MOSFET. However, it has a large turn-OFF current and asymmetric inductor current. Besides, secondary-side auxiliary MOSFET needs to be floating driven.

In [10], a variable *LLC* structure with multiple operating modes is proposed, the converter has three operation modes, namely, dual full-bridge operation mode, full-bridge operation mode, and half-bridge operation mode, which can cover the high voltage gain range, medium voltage gain range, and low voltage gain range operations, respectively. However, the two diodes on the secondary side are idle in the dual full-bridge operation mode, the two MOSFETs on the primary side are idle in the full-bridge mode, and only part of devices of both the primary side and the secondary side are used and only one transformer is in operation in the half-bridge mode. This phenomenon makes the rate of component utilization too low, which results in lower power density. Besides, in full-bridge mode, there are electro magnetic interference (EMI) issues and reliability degradation due to current spikes flowing through unused MOSFETs.

In [11], a topology with a FB *LLC* and HB *LLC* connected in parallel on the primary side with a shared HB leg is introduced. The primary side can operate in two modes: double HB in parallel or HB and FB in parallel to expand voltage gain range. However, on the switching point between two modes, due to the inflection of the gain curve, the problem of frequency jump is serious. In [12], an H5-bridge is proposed. By morphing the H5 bridge, the input of each resonant tank can be configured as either full-bridge, half-bridge, or idle, which can form six topologies structures. In [13] and [14], a five switches inverter bridge structure is proposed to extend the output voltage range of the *LLC* converter. By reconfiguring the inverter bridge, a wider output range can be achieved. In [15], a structure-reconfigurable without extra switches is proposed. By different combinations of primary four switches, four operation modes are available: 1) original gain mode, 2) double gain mode, 3) quadruple gain mode, and 4) sixfold gain mode, which expand the gain range of *LLC* converters greatly. In [16], a hybrid *LLC* converter is proposed. By changing the modulation strategies, the proposed converter can operate in three modes, namely, 1) low-gain, 2) medium-gain, and 3) high-gain operation modes to achieve a wide output range. Another topology-morphing method is introduced in [17] and [18]. As the up-switch of one bridge leg is permanently OFF and the down-switch of the same leg is permanently ON, the FB *LLC* converter is morphed to an HB *LLC*.

This category of reconfiguring topology methods above can extend the operation range of converter effectively. However, the power density has been reduced due to the low component utilization. Moreover, the system life and reliability are sacrificed due to the uneven operating time of the components.

The anther type of method adopts PSM control scheme between two parallel *LLC* resonant converters for achieving wide voltage range [19], [20], [21], [22], [23].

In [19], a two-phase FB interleaved *LLC* resonant converter with a hybrid rectifier is proposed for wide output voltage range applications. However, too many MOSFETs and diodes are used, which leads to a complex structure. Moreover, complex PFM combined with PSM are required for this converter. In [20] and [21], a two-phase interleaved *LLC* resonant converter is proposed. The primary side of the transformers is two interleaved paralleled HB *LLC* and the secondary side of the transformers is in inverse series with sharing full bridge rectifier. The parameters of the two half-bridges *LLC* are identical, and both operate at the resonant frequency. The output voltage is regulated by changing the phase angle between the two HB converters. However, when low voltage output is required, the resonant current and secondary diodes current are triangular waves instead of sine waves, which results in a large drop in efficiency at the low output voltage. Moreover, the triangular current waveform produces complex EMI interference. Besides, at low-voltage output, one phase converter will transfer power from output to input, which causes a very large circulating current and results in a sharp drop in efficiency. Moreover, the total size of magnetic components is much larger than that in conventional *LLC* resonant converter. In [22], a hybrid combination of a FB and HB *LLC* circuits is proposed, and the two bridges share the same leg. The HB is uncontrolled so it always operates at resonant frequency point. The output voltage is regulated through phase-shift angle of the two legs of the full bridge. But, when the phase-shift angle increases, the circulating current of the primary side increases. In order to realize the ZVS of the MOSFETs, the magnetizing inductance should be reduced, which results in worse efficiency. In [23], a dual-phase *LLC* resonant converter with a variable frequency-based zero circulating current phase-shift modulation scheme for wide input voltage applications is proposed. However, twelve MOSFETs used in the converter lead to complex circuit structure. Besides, variable frequency and phase-shift multiple control methods lead to complicated control. In [24], *LLC* hybrid buck converter topology is proposed. A buck converter is series connection with *LLC* converter on the secondary side. The *LLC* converter output voltage range is expended by changing the duty cycle of the buck.

The last major category is to change the gain curve of traditional *LLC* by changing the resonant tank structure [25], [26], [27], [28], [29], [30], such as adding inductors and capacitors in parallel resonant called notch filter on the primary side [25], [26], [27] or secondary side [28] of *LLC* converters, or parallel capacitance across resonant inductors [29], [30]. The notch filter reduces the gain curve of *LLC* to zero at twice the resonant frequency point, which greatly remedies the defect of traditional *LLC*, i.e., the gain curve becomes flat when the operating frequency is higher than the resonant frequency.

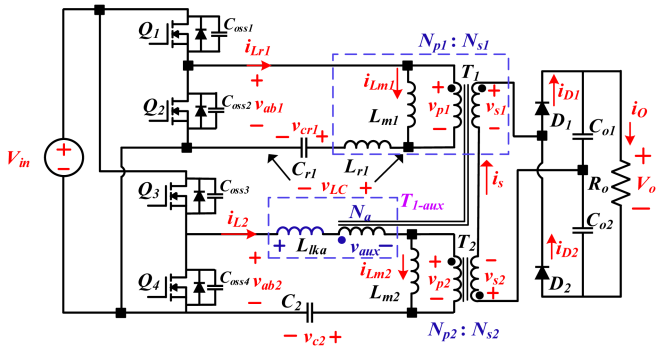

Fig. 1. Circuit diagram of the proposed *LLC*+HB converter.

In this article, a novel hybrid *LLC* and a HB parallel converter is proposed. On the primary side, the *LLC* converter and HB converter are connected in parallel with an auxiliary winding of the *LLC* transformer inserted in the primary power loop of the HB converter, while the secondary windings of two converters transformers are inversely connected and share a voltage-doubler rectifier. The converters in the proposed topology always operates at a fixed frequency, which facilitates magnetic components design and is helpful for reducing EMI. The output voltage is regulated by the phase-shift angle between *LLC* resonant converter and HB converter. Compared to the topologies shown in [20] and [21], one resonant inductor is saved, which is benefit for the cost save and power density improvement.

The rest of this article is organized as follows. Operation process of the proposed topology is presented in Section II. Detailed theoretical analysis, gain calculation and design guidance are discussed in Section III. The experimental results are given in Section IV. Finally, Section V concludes this article.

II. Operation Principle

The circuit diagram of the proposed hybrid *LLC*+HB parallel converter is shown in Fig. 1. Where, L_{r1} and C_{r1} are the resonant inductor and the resonant capacitor of the *LLC* converter, respectively. And L_{m1} and L_{m2} are the magnetizing inductors of transformers T_1 and T_2, respectively. $T_{1\text{-aux}}$ is the auxiliary winding of the transformer T_1, and C_2 is the dc blocking capacitor of the HB converter for preventing the magnetic flux asymmetry of the transformer T_2. The *LLC* resonant converter and the HB converter are connected in parallel on the primary side. The auxiliary winding $T_{1\text{-aux}}$ of the *LLC* transformer T_1 is connected in series with the primary winding of the HB transformer T_2. The secondary side is a voltage-doubler rectifier, which is shared by inversely connected secondary windings of transformer T_1 and T_2. Both *LLC* converter and HB converter operate at the same fixed frequency f_s, which equals to the resonant frequency f_r determined by L_{r1} and C_{r1}. The output voltage is regulated by changing the phase-shift angle between *LLC* and HB. The range of phase-shift angle is [0, π].

The key steady-state waveforms with a certain phase-shift angle φ is shown in Fig. 2. The steady-state operation process can be divided into ten operation modes. Fig. 3 shows the equivalent

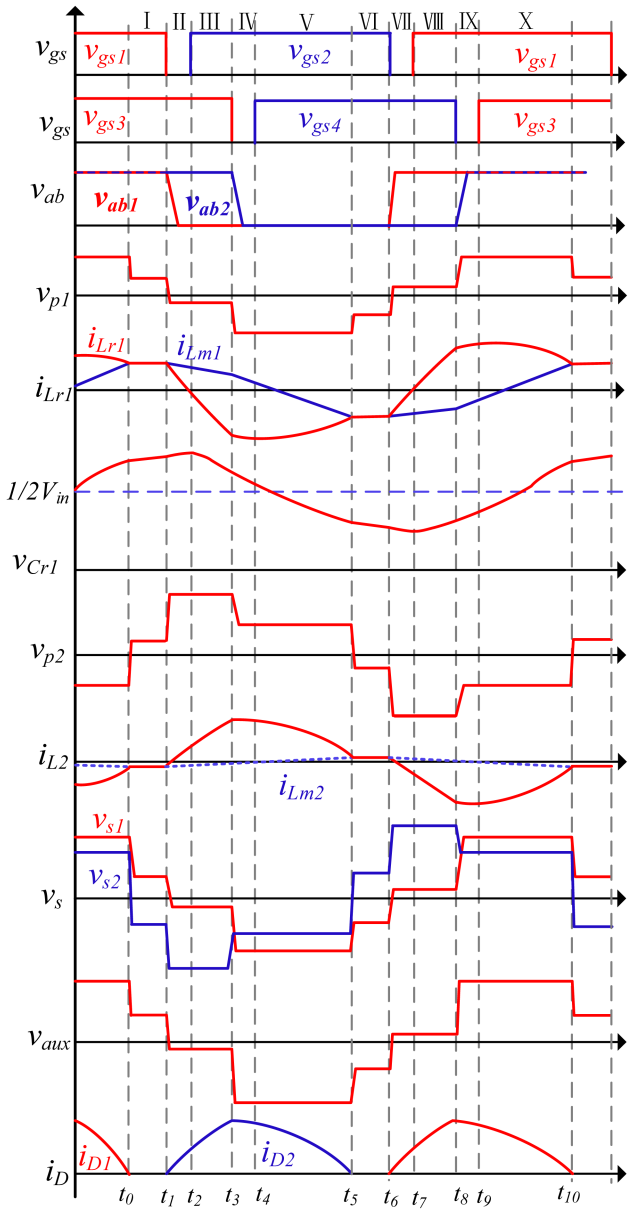

Fig. 2. Key steady-state waveforms of the proposed topology.

circuits of the first five modes over a half cycle and the next five modes in next half cycle are not analyzed due to the symmetry. It should be noted that the voltage and current directions shown in the equivalent circuits in Fig. 3 is the actual directions. And it is specified that the dotted terminal of the transformer T_1 is the positive direction.

To simplify the analysis, some assumptions are made.

1) The output capacitances of the primary MOSFETs are identical and the parasitical parameters of other components are ignored.
2) The magnetizing inductance $L_{m2}>>L_{m1}$.
3) Capacitor C_2 is large enough and $v_{c2}\approx 1/2V_{in}$.
4) The driving signals of each pair of switches (Q_1 and Q_2, Q_3 and Q_4) are complementary with approximate 50% duty cycles.

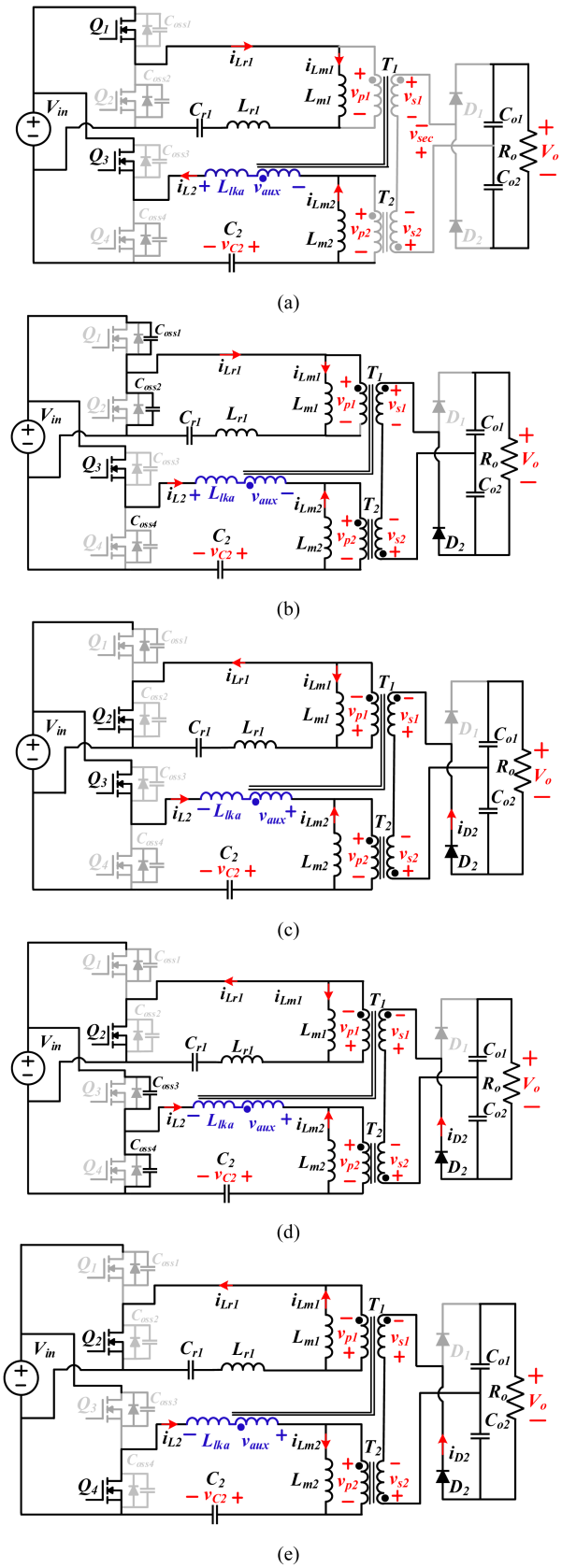

Fig. 3. Equivalent circuits of different operation modes. (a) Mode I [t_0-t_1]. (b) Mode II [t_1-t_2]. (c) Mode III [t_2-t_3]. (d) Mode IV [t_3-t_4]. (e) Mode V [t_4-t_5].

5) The leakage inductance L_{lka} is small enough which does not affect the operation of the HB converter.

Mode I [t_0-t_1]: Before t_0, Q_1 and Q_3 are ON, while Q_2 and Q_4 are OFF. At the same time, the secondary side diode D_1 is conducted to supply power to the load and the current i_{L2} in HB converter is negative. At t_0, the resonant current i_{Lr1} of *LLC* is equal to the magnetizing current i_{Lm1}, thus, the current i_{D1} of the secondary side diode D_1 reaches zero and D_1 realizes ZCS turn-OFF. At this moment, transformers T_1 and T_2 break the connection from the secondary side, and the output capacitors C_{o1} and C_{o2} provide energy to the load. Meanwhile, the i_{L2} is equal to the magnetizing current i_{Lm2} during this interval. Because of the magnetizing inductance $L_{m2}>>L_{m1}$, the i_{Lm2} is much smaller than i_{Lm1}. The equivalent circuit of Mode I is shown in Fig. 3(a).

Mode II [t_1-t_2]: At t_1, Q_1 is turned OFF and the other switches maintain the states as Mode I. The positive resonant current i_{Lr1} charges the C_{oss} of Q_1 and discharges the C_{oss} of Q_2 so as to create ZVS condition for Q_2. The diode D_2 starts conducting to provide energy to the load. Meanwhile, i_{L2} increases and crosses zero in a positive direction. The equivalent circuit of Mode II is shown in Fig. 3(b).

Mode III [t_2-t_3]: At t_2, Q_2 is turned ON with ZVS. During this interval, i_{Lr1} reaches zero and reverses. And i_{L2} keeps positive increasing, diode D_2 keeps conduction. The equivalent circuit of Mode II is shown in Fig. 3(c).

Mode IV [t_3-t_4]: At t_3, Q_3 is turned OFF. During this interval, i_{L2} keeps positive, which charges the C_{oss} of Q_3 and discharges the C_{oss} of Q_4. At the same time, D_2 keeps conduction. The equivalent circuit of Mode II is shown in Fig. 3(d).

Mode V [t_4-t_5]: At t_4, Q_4 is turned ON with ZVS. During this interval, i_{Lr1} drops to negative, i_{L2}keeps positive, and diode D_2 is still on. The equivalent circuit of Mode II is shown in Fig. 3(e).

At t_5, i_{Lr1} equal to i_{Lm1} and Mode V is finished. So far, half of the operating cycle is over. The operation modes in the next half cycle are similar, which are not discussed for simplicity.

III. Theoretical Analysis and Design Considerations

A. Voltage Gain Based on Time-Domain Analysis

In order to facilitate the voltage gain analysis, the following assumptions are made.

1) The coefficient k ($k = L_{m1}/L_{r1}$) of *LLC* is large, which make the voltage gain curve very smooth. Although the actual values of the resonant inductance L_{r1} and the resonant capacitance C_{r1} will cause deviation between the preset fixed operation frequency f_s and the actual resonant frequency f_r, the deviation is small enough to be ignored.
2) The dead time is very short enough to be ignored.

Based on the assumptions abovementioned, the simplified waveforms of the converter are shown in Fig. 4.

The output voltage is regulated by the phase-shift angle φ between *LLC* and HB. The current through the resonant components is not sinusoidal, as shown in Fig. 4. Thus, the first harmonic approximation is not suitable here. In the following

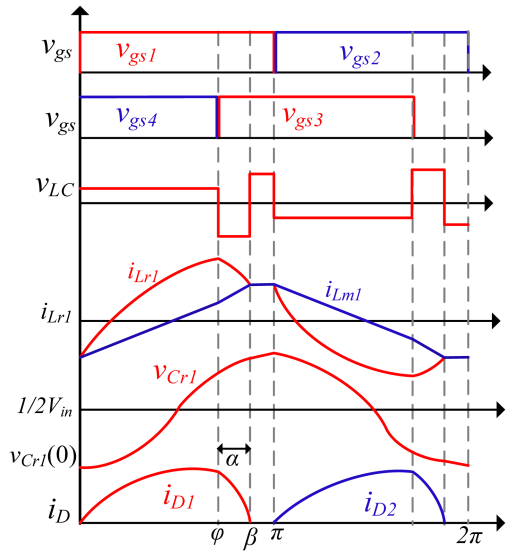

Fig. 4. Simplified waveforms of the converter for voltage gain calculation by neglecting the deadtime between bridge switches.

gain calculation, the time-domain method is used to calculate the voltage gain.

As shown in Fig. 1, N_{p1}, N_{s1}, and N_{p2}, N_{s2} are the primary and secondary winding turns of the transformers T_1 and T_2, respectively, N_a is the turns of the auxiliary winding of the transformer T_1. The turns ratios of transformers T_1 and T_2 are defined as $n_1 = N_{p1}/N_{s1}$ and $n_2 = N_{p2}/N_{s2}$, respectively, and the turns ratio of the auxiliary winding is defined as $n_{aux} = N_a/N_{p1}$. As shown in Fig. 4, $v_{cr1}(0)$ is the initial voltage across the resonant capacitor C_{r1} at $\theta = 0$.

The voltage gain G is defined as

$$G = \frac{V_o}{V_{\text{in}}}. \tag{1}$$

The normalized angle variable θ is defined as

$$\theta = \omega_0 t \tag{2}$$

where ω_0 is the angular resonant frequency.

$$\omega_0 = \frac{1}{\sqrt{L_{r1}C_{r1}}}. \tag{3}$$

During the interval [0, φ], Q_1 and Q_4 are conducted, and the primary voltage v_{p2} and the secondary voltage v_{s2} of transformer T_2 are shown in

$$v_{p2} = -\left(n_{aux}v_{p1} + \frac{1}{2}V_{\text{in}}\right) \tag{4}$$

$$v_{s2} = \frac{1}{n_2}\left(n_{aux}v_{p1} + \frac{1}{2}V_{\text{in}}\right) \tag{5}$$

where φ is the phase-shift angle. The primary and secondary voltages v_{p1} and v_{s1} of transformer T_1 are derived as shown in

$$v_{s1} = \frac{1}{2}V_o - \frac{1}{n_2}\left(n_{aux}v_{p1} + \frac{1}{2}V_{\text{in}}\right) \tag{6}$$

$$v_{p1} = \frac{1}{2(n_2 + n_{aux}n_1)}(n_1n_2V_o - n_1V_{\text{in}}). \tag{7}$$

Similarly, during the interval [φ, β], Q_4 is OFF and Q_3 is ON. The primary and secondary voltages v_{p1} and v_{s1} of transformer T_1 are shown as

$$v_{s1} = \frac{1}{2}V_o - \frac{1}{n_2}\left(n_{aux}v_{p1} - \frac{1}{2}V_{\text{in}}\right) \tag{8}$$

$$v_{p1} = \frac{1}{2(n_2 + n_{aux}n_1)}(n_1n_2V_o + n_1V_{\text{in}}). \tag{9}$$

Then, during the intervals [0, φ] and [φ, β], the voltage v_{LC} across the resonant capacitor C_{r1} and the resonant inductor L_{r1} can be obtained as, respectively, as follows:

$$v_{LC} = V_{\text{in}} - \frac{1}{2(n_2 + n_{aux}n_1)}(n_1n_2V_o - n_1V_{\text{in}}) = A \tag{10}$$

$$v_{LC} = -\frac{1}{2(n_2 + n_{aux}n_1)}(n_1n_2V_o + n_1V_{\text{in}}) = B. \tag{11}$$

The oscillation equations of the resonant inductor L_{r1} and the resonant capacitor C_{r1} during the intervals [0, φ] and [φ, β] are shown in, respectively, as follows:

$$v_{Cr1}(t) + L_{r1}C_{r1}\frac{dv_{Cr1}^2(t)}{dt^2} = A\,(0 < \theta < \varphi) \tag{12}$$

$$v_{Cr1}(t) + L_{r1}C_{r1}\frac{dv_{Cr1}^2(t)}{dt^2} = B\,(\varphi < \theta < \beta)\,. \tag{13}$$

According to Ampere's law and ignoring the magnetizing current i_{Lm2} of T_2, the relationship function among the resonant current i_{Lr1}, the HB current i_{L2} and the diode current i_{D1} is obtained, as shown in

$$\begin{aligned} N_{p1}(i_{Lr1} - i_{Lm1}) &= N_{s1}i_{D1} - N_a i_{L2} \\ N_{p2}i_{L2} &= -N_{s2}i_{D1}. \end{aligned} \tag{14}$$

Then, i_{D1} is derived as shown in

$$i_{D1} = \frac{n_1n_2}{n_2 + n_{aux}n_1}(i_{Lr1} - i_{Lm1}). \tag{15}$$

When $\theta = \beta$, i_{Lr1} is equal to i_{Lm1}, and the average value of i_{D1} is the load current I_o. The following equations are established:

$$v_{Cr1}(\pi) + v_{Cr1}(0) = V_{\text{in}} \tag{16}$$

$$i_{Lr1}(\beta) = i_{Lm1}\,(\beta) \tag{17}$$

$$I_o = \frac{V_o}{R_o} = \frac{1}{2\pi}\int_0^{\pi} i_{D1}(\theta)d\theta. \tag{18}$$

Combining (10)–(18), the voltage gain can be solved by numerical method. According to the laboratory prototype parameters $n_1 = 15$, $n_2 \approx 1.88$ and $n_{aux} = 1$, the gain curves under different loads are calculated out as the solid line in Fig. 5 shows. The selection of parameters n_1, n_2, and n_{aux} will be discussed in detail in part C and G of this section. The gain curve of simulation under different loads is shown as the dotted line in Fig. 5. It can be seen that the gain curves of time-domain analysis is almost in coincidence with the simulation results, which proves the high accuracy of the time-domain analysis method.

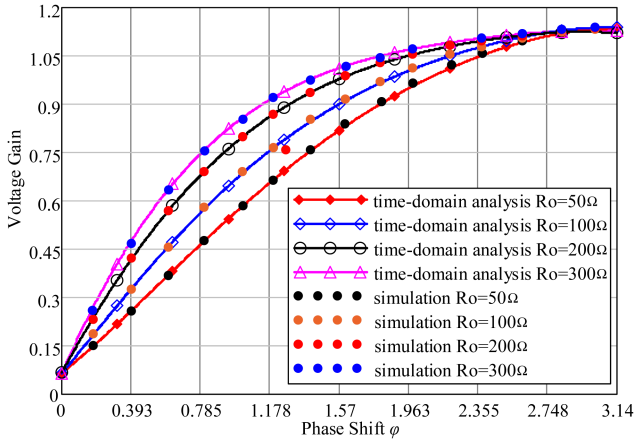

Fig. 5. Voltage gain curves based on time-domain analysis and simulation result versus φ with different R_o.

B. Voltage Gain Based on a Simple Approximate Analysis Method

Although the time-domain analysis for voltage gain is accurate, the calculation process is very complicated. It needs to solve the differential equations and finally, only numerical results can be obtained. Therefore, the time-domain analysis method is difficult to fast determine the system parameters in engineering applications. In this part, a simple approximate analysis method for voltage gain is proposed, which can avoid complex time-domain analysis and does not need to solve the differential equations.

Key waveforms of the converter based on the simply approximate analysis method are shown in Fig. 6. Because the proposed topology operates at the resonance frequency point with a fixed frequency, the *LLC* gain is a constant value and approximately equals to 1. As shown in Fig. 2, although the secondary side voltage v_{s1} of the *LLC* transformer T_1 is an irregular square wave, due to the *LLC* gain is a fixed value of 1, an equivalent square wave with amplitude $v_{s1\text{-}av}$ can be used to represent the original waveform, as shown in Fig. 6.

According to the characteristics of *LLC*, $v_{s1\text{-}av}$ is obtained as follows:

$$v_{s1-av} = \frac{V_{\text{in}}}{2n_1}. \tag{19}$$

Similarly, the auxiliary winding voltage v_{aux} can also be replaced by a square wave with amplitude $v_{aux\text{-}av}$

$$v_{aux-av} = n_{aux}\frac{V_{\text{in}}}{2}. \tag{20}$$

The equivalent waveform $v_{p2\text{-}eq}$ of the primary voltage v_{p2} of the HB transformer T_2 is shown in Fig. 6. The expression of $v_{p2\text{-}eq}$ is as follows:

$$v_{p2-eq}(0<\theta<\varphi) = -\left(n_{aux}\frac{V_{\text{in}}}{2}+\frac{V_{\text{in}}}{2}\right) \tag{21}$$

$$v_{p2-eq}(\varphi<\theta<\pi) = -\left(n_{aux}\frac{V_{\text{in}}}{2}-\frac{V_{\text{in}}}{2}\right). \tag{22}$$

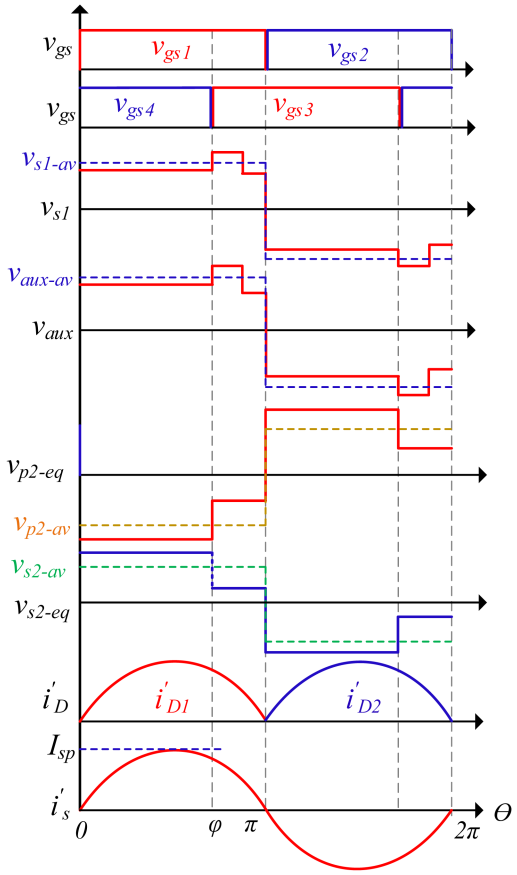

Fig. 6. Key waveforms of the simple approximate analysis.

Similarly, the equivalent waveform $v_{s2\text{-}eq}$ of the secondary voltage v_{s2} of the HB transformer T_2 can be obtained, as shown in

$$v_{s2-eq}(0<\theta<\varphi) = \frac{1}{n_2}\left(n_{aux}\frac{V_{\text{in}}}{2}+\frac{V_{\text{in}}}{2}\right) \tag{23}$$

$$v_{s2-eq}(\varphi<\theta<\pi) = \frac{1}{n_2}\left(n_{aux}\frac{V_{\text{in}}}{2}-\frac{V_{\text{in}}}{2}\right). \tag{24}$$

Furthermore, an equivalent square wave with amplitude $v_{s2\text{-}av}$ is used to represent $v_{s2\text{-}eq}$, as shown in Fig. 6. Then, $v_{s2\text{-}av}$ can be derived, as shown in

$$\begin{aligned} v_{s2-av} &= \frac{\varphi}{\pi}v_{s2-eq}(0<\theta<\varphi)+\frac{\pi-\varphi}{\pi}v_{s2-eq}(\varphi<\theta<\pi) \\ &= \frac{V_{\text{in}}}{\pi n_2}(\varphi+\frac{\pi}{2}n_{aux}-\frac{\pi}{2}). \end{aligned} \tag{25}$$

After using the equivalent square waveforms, the equivalent secondary current i'_s becomes a standard sinusoidal wave, as shown in Fig. 6.

The output voltage V_o can be calculated, as shown in

$$V_o = 2(V_{s1-av}+V_{s2-av}). \tag{26}$$

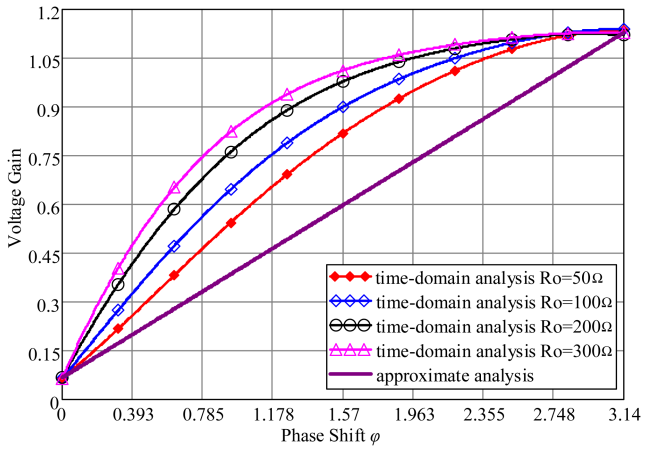

Fig. 7. Calculated voltage gain curves based on the proposed simple approximate analysis and time-domain analysis.

Combining (1), (19), (25), and (26), the approximate voltage gain G can be derived

$$G = \frac{V_o}{V_{\text{in}}} \approx \frac{1}{n_1} + \frac{1}{n_2}\left(\frac{2\varphi}{\pi} + n_{aux} - 1\right). \tag{27}$$

According to the parameters of the laboratory prototype, the approximate gain curve has been calculated out, as shown in Fig. 7. For comparison, the gain curves obtained by time-domain analysis are also shown in Fig. 7.

It can be seen that the voltage gain achieved by the approximate analysis is linear to the phase-shift angle φ. Although there is some deviation between curves achieved by the approximate analysis and the time-domain analysis, the deviation is almost zero at both 0 and π. That is to say, these two methods can achieve almost identical maximum and minimum gains. The biggest advantage of the approximate analysis method lies in that it does not need to solve complex differential equations. Moreover, the linear relationship between the phase-shift angle and voltage gain can be used to quickly determine the main parameters, such as the transformer ratios n_1 and n_2, and auxiliary winding turns ratio n_{aux}, which is convenient for engineering applications. The proposed simply approximate analysis method can also be used in the similar type of topologies with phase-shift control such as those presented in [5] and [20].

C. Design Considerations

According to (27), the voltage gain of the proposed converter is related to the transformer parameters n_1, n_2, and n_{aux}. Fig. 7 shows that the voltage gain increases with phase-shift angle φ. According to Fig. 7, if the converter is designed to achieve maximum voltage gain $G_{\max}$ at $\varphi = \pi$, the reactive power circulating between the primary sides of transformers T_1 and T_2 can be totally eliminated and optimal efficiency can be achieved. While, another boundary condition that the minimal gain $G_{\min}$ occurring at $\varphi = 0$ *is* helpful for reducing the power transferred by T_2 so that the size of it can be reduced. Therefore, an optimal design is to set the variation range of φ to be $0\sim\pi$ over the whole gain range.

Then, substitute the minimal and maximal angle values into (27), it can be derived that

$$G_{\min} \approx \frac{1}{n_1} + \frac{1}{n_2}(n_{aux} - 1). \tag{28}$$

And

$$G_{\max} \approx \frac{1}{n_1} + \frac{1}{n_2}(n_{aux} + 1). \tag{29}$$

Thus, n_2 can be derived according to (29) and (28)

$$n_2 \approx \frac{2}{G_{\max} - G_{\min}}. \tag{30}$$

Because the output voltage range of the prototype is 50 V–450 V, $G_{\min}$ and $G_{\max}$ can be achieved to be 0.125 and 1.125, respectively. According to (30), the initial value of n_2 is obtained to be 2.

The output power P_o of the converter can be further derived according to (27), as shown in

$$P_o \approx V_{\text{in}}\left[\frac{1}{n_1} + \frac{1}{n_2}\left(\frac{2\varphi}{\pi} + n_{aux} - 1\right)\right] I_o \tag{31}$$

where I_o is the load current. According to the principle of the voltage-doubler rectifier, I_o can be obtained according to

$$\frac{1}{2\pi}\int_0^{\pi} I_{sp}\sin(\omega t)d(\omega t) = I_o \tag{32}$$

where I_{SP} is the peak value of the secondary current i_s, which can be obtained according to (32)

$$I_{SP} = \pi I_o. \tag{33}$$

Then, the rms value of i_s is obtained

$$I_{s-\text{rms}} = \frac{\pi}{\sqrt{2}} I_o. \tag{34}$$

The rms value of the fundamental wave of the equivalent secondary voltage of transformer T_2 can be achieved with Fourier decomposition, as shown in

$$U_{s2-\text{rms}} = \frac{2\sqrt{2}}{\pi} v_{s2-av}. \tag{35}$$

Combining (25), (34), and (35), the output power P_{T2} of transformer T_2 is derived

$$P_{T2} \approx \frac{V_{\text{in}}}{\pi n_2}(2\varphi + \pi n_{aux} - \pi) I_o. \tag{36}$$

In the same way, the output power P_{T1} of transformer T_1, which consists of the output power to the secondary side and the power delivered by the auxiliary winding, can be obtained, as shown in

$$P_{T1} \approx I_o\left(\frac{V_{o\max} + V_{o\min}}{2}\right). \tag{37}$$

Equation (37) shows that P_{T1} is unrelated to the transformer parameters n_1, n_2, and n_{aux}, which means the following design does not need to consider transformer T_1.

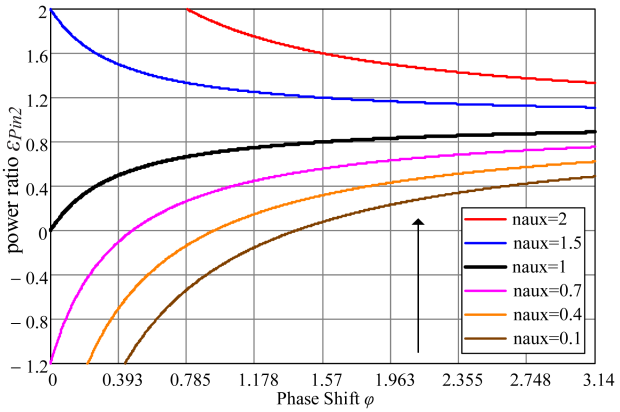

Fig. 8. Power ratio ε_{T2} under different auxiliary winding turns ratio n_{aux}.

Combining (27), (30), (31), and (36), the power ratio ε_{T2} of P_{T2} to P_o is derived, as shown in

$$\varepsilon_{T2} = \frac{4\varphi + 2\pi(n_{aux}-1)}{\pi n_2 \left[G_{\max} + G_{\min} - n_{aux}(G_{\max} - G_{\min})\right] + 4\varphi + 2\pi(n_{aux}-1)}. \quad (38)$$

Substitute $G_{\max} = 1.125$, $G_{\min} = 0.125$, and $n_2 = 2$ into (38), ε_{T2} can be calculated out, as shown in Fig. 8.

Fig. 8 shows that power ratio ε_{T2} increases as n_{aux} increases, which means increased magnetic core size of transformer T_2. Therefore, considering volume and cost, smaller n_{aux} is preferred.

However, if the auxiliary winding turns ratio n_{aux} is lower than 1, according to (24), the secondary voltage $v_{s2\text{-}eq}$ of transformer T_2 is negative and the secondary current i_s of transformer T_2 is positive during the region $\varphi < \theta < \pi$. Meanwhile, T_2 transfers energy from the secondary side to the primary side, which will increase the length of reactive power transmission path and deteriorate the efficiency of the converter. Therefore, $n_{aux} = 1$ is the most optimal parameter after comprehensively considering the volume of transformer and the losses.

Substitute $n_{aux} = 1$, $\varphi = 0$ and $\varphi = \pi$ into (27), $G_{\min}$ and $G_{\max}$ can be rewritten, respectively, as follows:

$$G_{\min} = \frac{V_{o\min}}{V_{\text{in}}} \approx \frac{1}{n_1} \quad (39)$$

$$G_{\max} = \frac{V_{o\max}}{V_{\text{in}}} \approx \frac{1}{n_1} + \frac{2}{n_2}. \quad (40)$$

According to (39) and (40), the $G_{\min}$ and $G_{\max}$ versus transformer ratio n_1 and n_2 are shown in Fig. 9. It can be seen in Fig. 9(b) that $G_{\min}$ is determined by n_1 and independent of n_2. As the increases turn ratio n_1, the minimum gain $G_{\min}$ decreases, but when the n_1 is greater than a certain value, the curve becomes flat. This indicates that increasing n_1 does not help much in obtaining smaller gain $G_{\min}$.

However, $G_{\max}$ is determined by n_1 and n_2 but the influence of n_2 is dominant. Fig. 9(a) shows that as the decreases turn ratio n_2, the maximum gain $G_{\max}$ curve becomes steeper, and the reduction of a small degree of n_2 will bring a significant increase

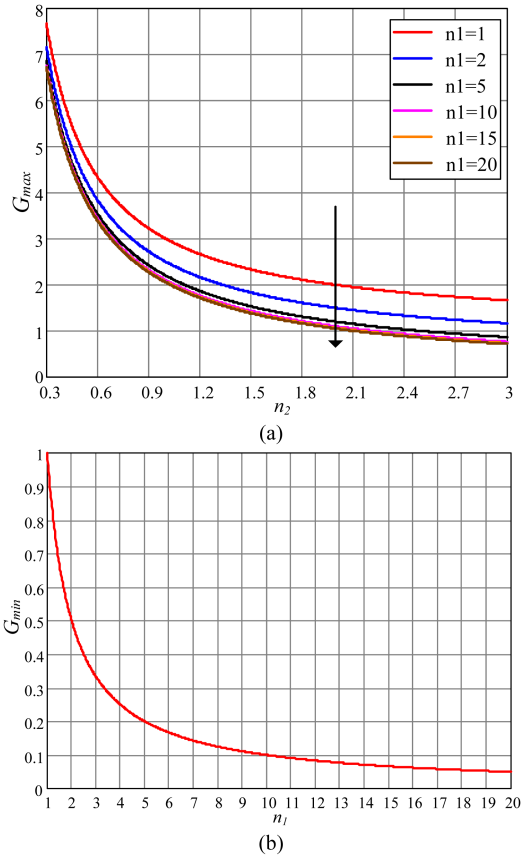

Fig. 9 (a) Maximum voltage gain $G_{\max}$ under different turn ratios n_1 and n_2. (b) Minimum voltage gain $G_{\min}$ under different turn ratios n_1 and n_2.

in $G_{\max}$, which is more conducive to get a large maximum gain $G_{\max}$.

With the optimally selected parameter $n_{aux} = 1$ and according to (31), (37), and (38), the power ratios of transformers T_1 and T_2 can be obtained, as shown

$$\varepsilon_{T1} = \frac{G_{\max} + G_{\min}}{2\left(\frac{1}{n_1} + \frac{2\varphi}{n_2\pi}\right)} \quad (41)$$

$$\varepsilon_{T2} = \frac{2\varphi}{\pi n_2 G_{\min} + 2\varphi}. \quad (42)$$

The curves of ε_{T1} and ε_{T2} versus the phase shift angle φ are shown solid line in Fig. 10. For comparison, the transformer power ratio of [20] is also plotted in Fig. 10, as shown dotted line. It can be seen that the power carried by transformers T_2 of phase-II converter in [20] will be negative as the phase-shift angle φ is smaller than 1.57 rad ($\approx\pi/2$) when the converter enters low output voltage condition, which means transformers T_2 absorbs power from output instead of transferring power to output under this condition. This reactive power brings high conduction losses and deteriorates the efficiency under low output voltages, as shown in Fig. 21 in [20]. On the contrary, in the proposed topology, transformer T_2 will never absorb power from the output.

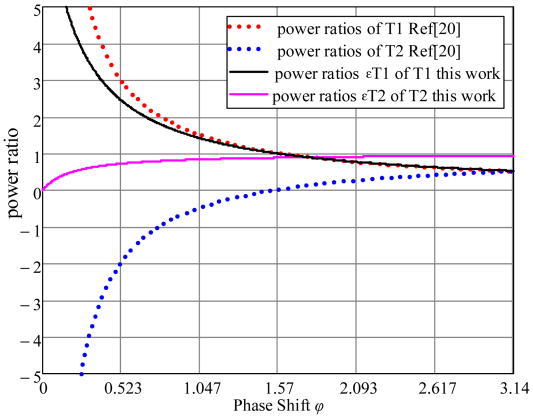

Fig. 10 Transformer power ratios of the proposed topology and the topology presented in [20].

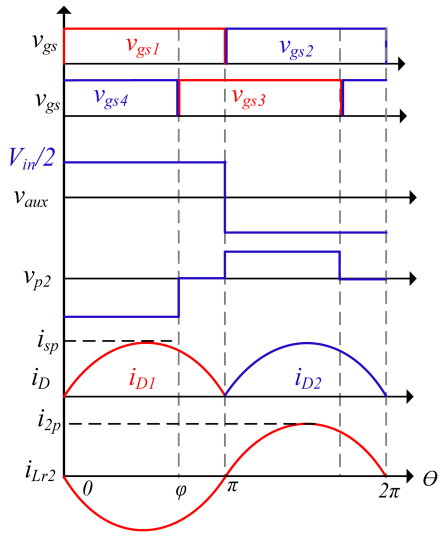

Fig. 11 Key waveform for reactive power analysis.

Meanwhile, it can be seen that when the phase shift angle φ is smaller than 0.942 rad ($\approx\pi/3$), i.e., under lower voltage output, the power ratios ε_{T1} and ε_{T1} of transformer T_1 and T_2 in the proposed topology are significantly smaller than those in [20]. It indicates that the proposed topology can use smaller magnetic cores compared to the topology in [20].

D. Analysis on Reactive Power

According to the simple approximate analysis in Section III-B, it can be known that the voltage v_{aux} of the auxiliary winding N_a of transformer T_1 can be equivalent to a square wave with an amplitude of $V_{\text{in}}/2$ with the optimal $n_{aux} = 1$. Meanwhile, the secondary side current of the transformer $i_s = i_{D1} + i_{D2}$ and the HB current i_{Lr2} can be equivalent to a sine wave, as shown in Fig. 11. Where, i_{sp} and i_{2p} are the peak values of transformer secondary side current i_s and HB current i_{Lr2}, respectively, and φ is phase shifting angle. According to (27), The approximate gain G is shown

$$G = \frac{V_o}{V_{\text{in}}} \approx \frac{1}{n_1} + \frac{2\varphi}{n_2\pi}. \tag{43}$$

When Q_1 and Q_4 are both on during the interval [0, φ], the energy output by the auxiliary winding N_a of transformer T_1 is transmitted to the load through transformer T_2. In this interval, transformers T_1 and T_2 simultaneously transmit energy to the load without reactive power. However, When Q_1 and Q_3 are on during the interval [φ, π], the primary voltage v_{p2} of transformer T_2 is zero, and transformer T_2 does not transmit energy to the load. Therefore, the output energy of the auxiliary winding N_a of transformer T_1 returns to the power source, which is the reactive power. The reactive power P_s is derived, as shown

$$P_s = \frac{1}{\pi}\int_{\varphi}^{\pi} v_{aux} i_{2p} \left|\sin(\theta)\right| d\theta. \tag{44}$$

The relationship between load current I_o and secondary side current i_s is shown

$$I_o = \frac{V_o}{R_o} = \frac{1}{2\pi}\int_{0}^{\pi} i_{sp}\sin(\theta) d\theta. \tag{45}$$

Combining (43)–(45), the relationship between reactive power P_s and output voltage V_o under different loads R_o is derived as

$$P_s = \frac{V_{\text{in}} V_o}{2R_o n_2}\left[1 + \cos\left[\left(\frac{V_o}{V_{\text{in}}} - \frac{1}{n_1}\right)\frac{n_2\pi}{2}\right]\right]. \tag{46}$$

The relationship curve between reactive power P_s and output voltage V_o is shown with solid line in Fig. 12(a). Because reactive power is related to output voltage, for fair comparison, the highest output voltage of laboratory prototype in [20] is redesigned to be 450 V, which is as same as that in this article. The relationship between reactive power and output voltage in [20] is shown with the dotted line in Fig. 12(a). It can be seen that within the whole output voltage range, the reactive power in the proposed converter is almost as same as that in the converter in [20]. The ratio of reactive power to output power shown in Fig. 12(b) is also identical.

However, the reactive power transmission paths in those two converters are different, as shown in Fig. 13(a) and Fig. 13(b), respectively. It can be seen from Fig. 13 that the reactive power of proposed topology feedback to power supply only passes through the primary loop of *LLC* converter, auxiliary winding, and the primary loop of half-bridge converter, but the reactive power in [20] feedback to the power supply passes through the primary and secondary loops of *LLC1*, the output rectifier bridge and the primary and secondary loops of *LLC2*. So, the longer transmission path of reactive power of the topology in [20] will cause higher conduction losses and deteriorates the efficiency of the converter, which is more obvious as the output voltage decreases while the ratio of reactive power increases. This conclusion will be verified in experimental part.

E. ZVS Performance

For the *LLC* topology, the design process of ZVS is the same as that of traditional *LLC*. Because the switching frequency of

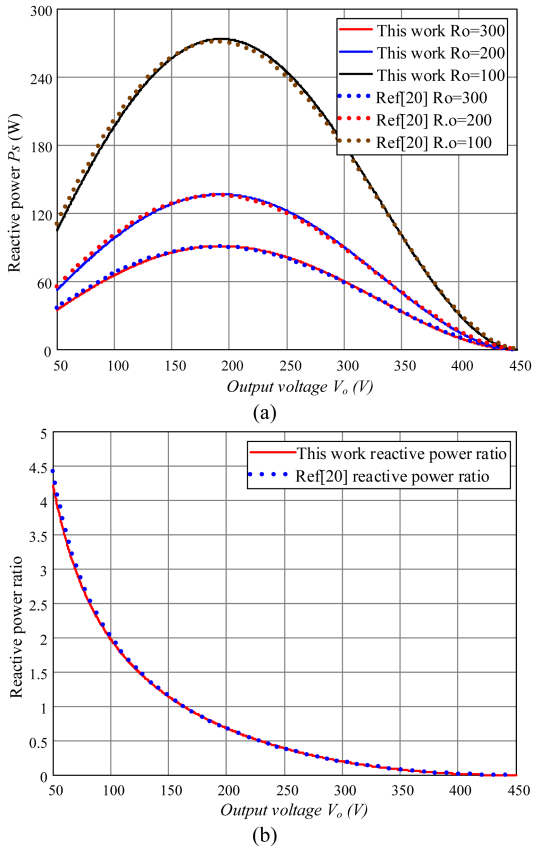

Fig. 12 Comparison on reactive power between the proposed converter and the converter in [20] (with the same 450 V output voltage). (a) Reactive power P_s versus output voltage V_o with different load R_o. (b) Reactive power ratio versus output voltage V_o.

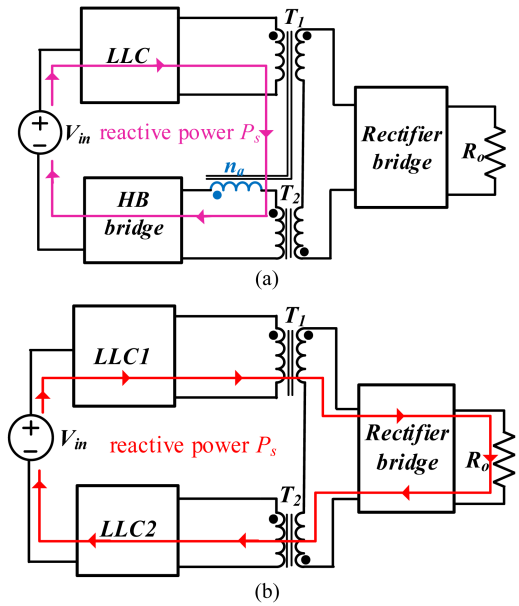

Fig. 13 Reactive power transmission path. (a) Proposed topology. (b) Converter in [20].

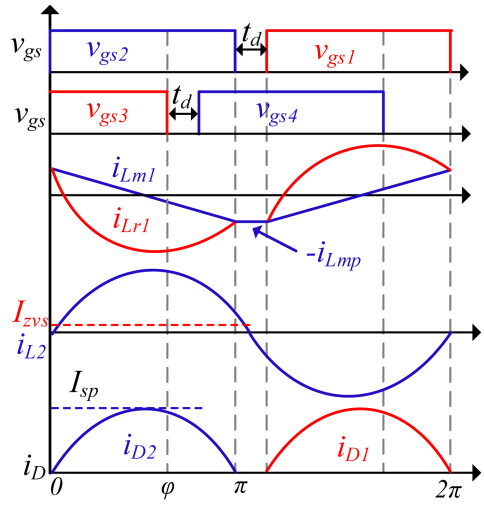

Fig. 14 HB and *LLC* current i_{Lr1} and i_{L2}.

Q_1 and Q_2 is equal to the *LLC* resonant frequency which is decided by L_{r1} and C_{r1} and according to Fig. 6, the primary voltage v_{p1} of transformer T_1 is equivalent to a square wave of $V_{\text{in}}/2$. The magnetizing current i_{Lm1} of transformer T_1 changes linearly, as shown in Fig. 14. Where, i_{Lm1} and i_{Lmp} are the magnetizing current and magnetizing current peak, respectively, and t_d is the dead time. During Q_2 conduction, the magnetizing inductance is clamped by the $-v_{p1}$, and the magnetizing current i_{Lm1} declines linearly. When Q_2 is turned off, the magnetizing current i_{Lm} reaches maximum $-i_{Lmp}$, as shown

$$|i_{Lmp}| = \left| \frac{V_{\text{in}}}{8 L_{m1} f_r} \right|. \tag{47}$$

Due to the short dead time t_d and the large magnetizing inductance L_{m1}, it can be considered that the magnetizing current i_{Lm1} is a constant current source with a current of i_{Lmp}, which simultaneously charges and discharges the output capacitors C_{oss1} and C_{oss2} of Q_1 and Q_2. The charging and discharging time t_{dis} is shown in

$$t_{dis} = \frac{2 V_{\text{in}} C_{oss}}{i_{Lmp}}. \tag{48}$$

As long as t_{dis} is shorter than the dead time t_d, Q_1 and Q_2 can achieve ZVS.

However, the HB bridge current $i_{L2} = (i_{D1} + \mathrm{i}_{D2})/n_2 + i_{Lm2}$, because i_{Lm2} is small enough to be ignored, the realization of ZVS depends on the phase shift angle φ and load current I_o.

As shown in Fig. 2, when the phase shift angle φ is close to 0 or π, the HB bridge current i_{L2} is the minimum, so the MOSFETS of HB are the most difficult to achieve ZVS. According to the waveform analysis, when the phase shift angle φ is close to 0 or π, the *LLC* resonant current i_{Lr1} and HB current i_{L2} are very close to the sine wave. Therefore, HB current i_{L2} is taken as the sine wave for the following approximate analysis and calculation. The HB current i_{L2} and driving signal v_{gs} are shown in Fig. 14. Where, I_{sp} is the peak current of secondary rectifier diode, I_{zvs} is the minimum current for HB bridge MOSFET to

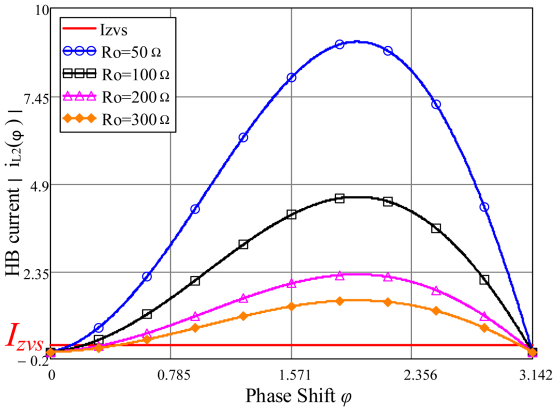

Fig. 15 Profiles of $i_{L2}(\varphi)$ versus phase shift φ under different load conditions.

realize ZVS, and φ is phase shift angle. According to the time starting point of Fig. 14, the current i_{D2} of diode D_2 is expressed as follows:

$$i_{D2}(\theta) = I_{sp}\sin(\theta). \tag{49}$$

At the phase shift angle φ, the MOSFET Q_3 is turned OFF. During the dead time t_d of Q_3 and Q_4, the i_{L2} charges the output capacitor C_{oss} of Q_3 and discharges the C_{oss} of Q_4, respectively, to ensure that Q_4 achieves ZVS. Combining (18), (27), and (49), the expression of HB current i_{L2} at the switch Q_3 turning OFF is as follows:

$$i_{L2}(\varphi) \approx -\frac{1}{n_1 R_o}\left(\frac{1}{n_1}+\frac{2\varphi}{n_2}\right)V_{\text{in}}\sin(\varphi). \tag{50}$$

Because the dead time t_d is very short, it can be considered that i_{L2} is a constant current source during this period. According to the charge conservation, the minimum current I_{zvs} required to achieve ZVS is derived that

$$I_{\text{ZVS}} = \frac{2C_{oss}V_{\text{in}}}{t_d}. \tag{51}$$

As long as $\mathrm{I}i_{L2}(\varphi)\mathrm{I} > I_{\text{zvs}}$, Q_4 can achieve ZVS. And according to laboratory prototype parameters the $i_{L2}(\varphi)$ versus phase shift φ with different R_o is plotted in Fig. 15. Simultaneously, I_{zvs} is also plotted, as shown in Fig. 15, for reference.

As shown in Fig. 15, HB MOSFETS can achieve ZVS in a wide range of phase shifting angles φ when the load R_o varies widely. According to the symmetry of the waveform, the amplitude of HB current i_{L2} when Q_4 turns OFF is equal to that when Q_3 turns OFF, but the direction is opposite. Then, the ZVS condition of Q_4 is met, the ZVS condition of Q_3 will also be met.

F. Control Strategy

Fig. 16 shows the block diagram of the control strategy, which can be easily implemented by the digital control unit. The sampled output voltage v_o is compared with the reference voltage v_{ref} and generates the error signal e_v. The error signal e_v is amplified by the PI compensation network and generates a signal which represents the phase-shift angle φ. Finally, the

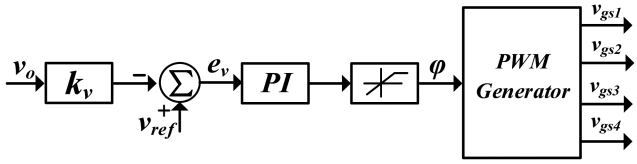

Fig. 16. Block diagram control strategy.

TABLE I
ELECTRICAL SPECIFICATIONS AND COMPONENTS PARAMETERS OF THE EXPERIMENTAL PROTOTYPE

Parameters	Value
Input Voltage	400 V
Output Voltage/Power	50 V–450 V/1 KW
Resonant Capacitor C_{r1}	66 nF
Resonant Inductance L_{r1}	26.5 uH (Leakage inductance of T_1)
Transformer T_1	*PQ4040*, N_{p1}:N_{s1}:N_a=15:1:15, L_{m1}=300 uH
switching frequency	120 KHz
Transformer T_2	*PQ4040*, N_{p2}:N_{s2}=32:17, L_{m2}=3mH
Dc blocking capacitor C_2	1.5 uF
Q_1–Q_4	SCT3210AL
D_1–D_2	BYV30W-600PT2
C_{o1}, C_{o2}	220 uF/250 V

PWM generator generates four drive signals according to the output signal of the compensation network.

G. Design Steps

For a practical engineering design, the step-by-step design procedure for the proposed converter has been summarized as the following.

First, the turn ratio n_1 of transformer T_1 is calculated out based on the minimum gain expression (39) according to the required minimum gain $G_{\min}$.

Second, the turn ratio n_2 of transformer T_2 is calculated out based on the maximum gain expression (40) according to the required maximum gain $G_{\max}$ for the converter.

After that, the parameters of resonant elements and transformers can be designed based on the conventional optimal design method for *LLC* resonant converter.

Finally, the turns of auxiliary winding N_a of T_1 is selected to be as same as the turns of the primary winding N_{p1} of T_1 according to the conclusion drawn in Section III-C.

IV. EXPERIMENTAL RESULT

A 1 kW laboratory experimental prototype with 400 V input and 50 V–450 V output has been built up to verify the feasibility of the proposed topology. The main component parameters and electrical specifications of the laboratory prototype are listed in Table I. The photograph of the laboratory prototype is shown in Fig. 17.

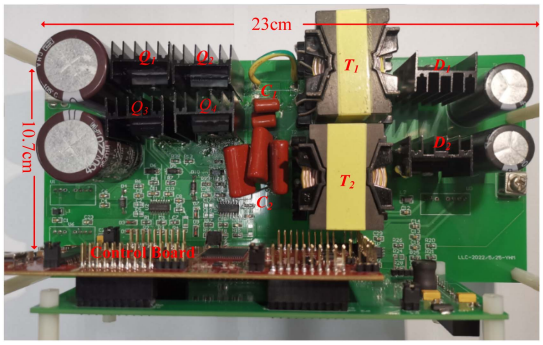

Fig. 17. Photograph of the laboratory prototype.

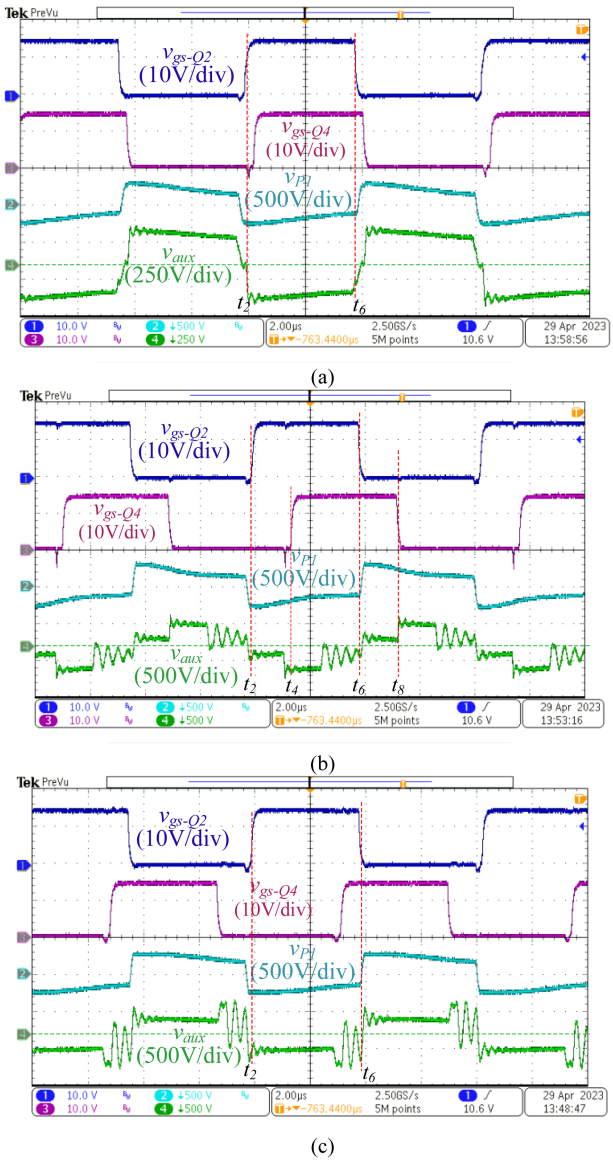

Fig. 18. Steady-state waveforms of v_{aux} and v_{p1}. (a) V_o= 50 V, P_o= 100 W. (b) V_o= 250 V, P_o= 500 W. (c) V_o= 450 V, P_o= 500 W.

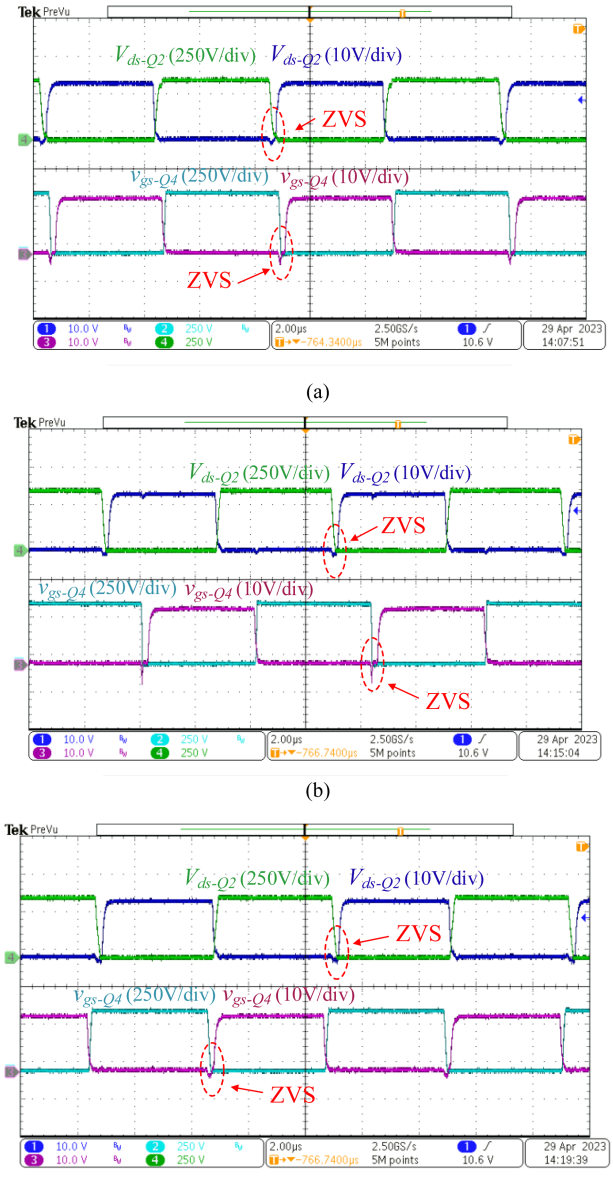

Fig. 19. Measured waveforms of primary switches of *LLC* and HB. (a) V_o = 50 V, P_o= 100 W. (b) V_o= 250 V, P_o= 500 W. (c) V_o= 450 V, P_o= 1000 W.

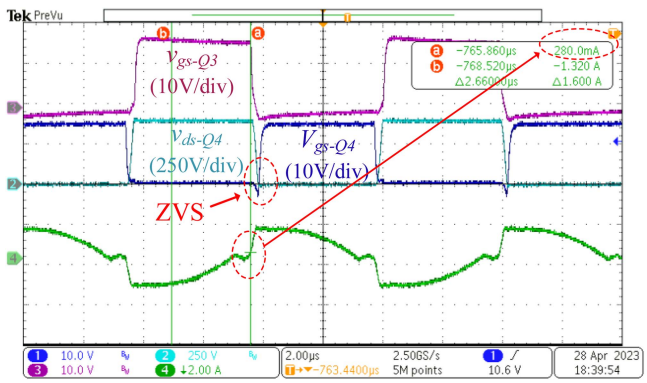

Fig. 20. Measured voltage waveforms of Q_4 and current waveform of i_{L2} under 50 V/40 W.

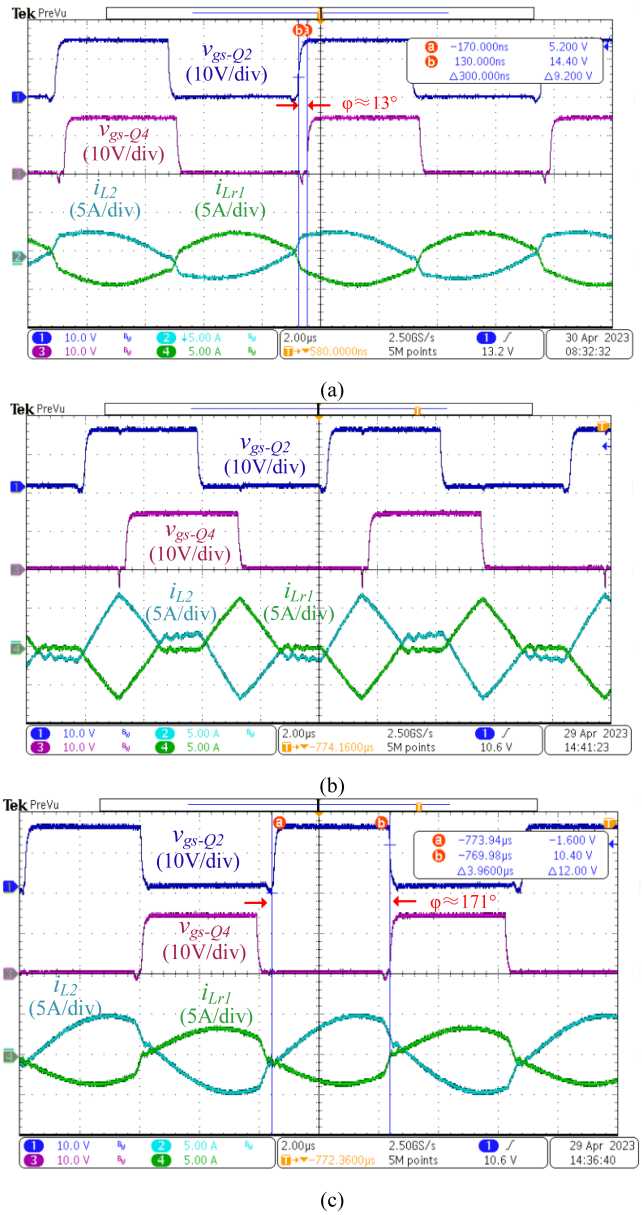

Fig. 21. Measured waveforms of i_{Lr1} and i_{L2} under different output voltages and power values. (a) V_o= 50 V, P_o= 100 W. (b) V_o= 250 V, P_o= 500 W. (c) V_o= 450 V, P_o= 1000 W.

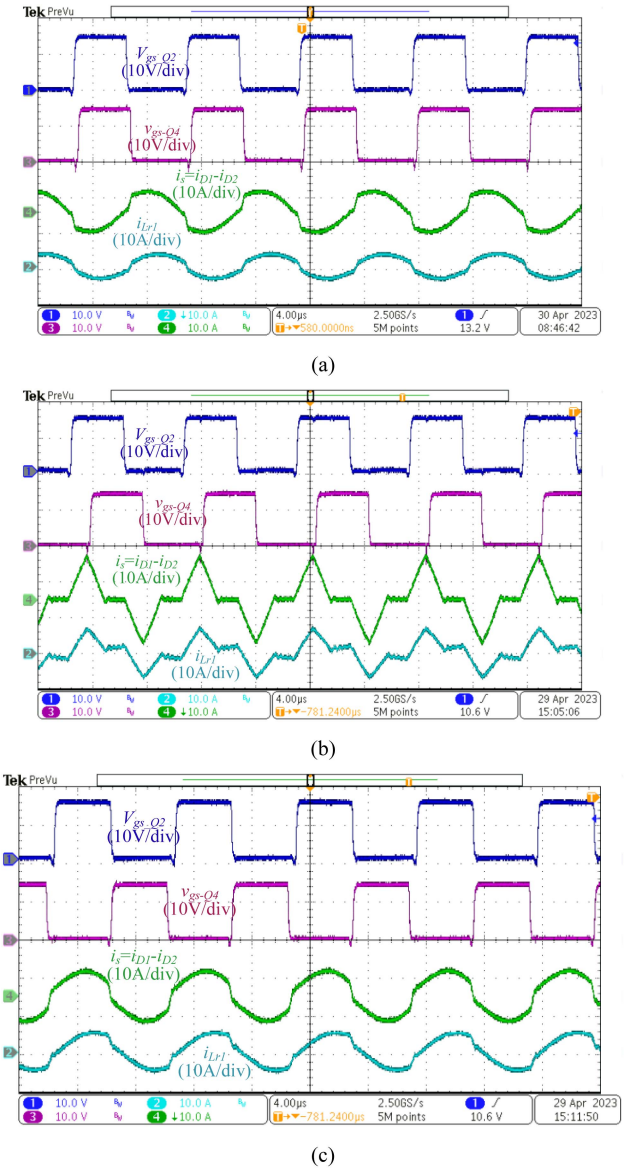

Fig. 22. Measured waveform of i_s under different output voltages. (a) V_o= 50 V, P_o= 100 W. (b) V_o= 250 V, P_o= 500 W. (b) V_o= 450 V, P_o= 1000 W.

The waveforms of auxiliary winding voltage v_{aux} and primary side voltage v_{p1} of transformer T_1 under different output voltages are shown in Fig. 18. The oscillation on auxiliary winding voltage v_{aux} is caused by the resonance inductor L_{r1} and equivalent capacitor across the primary winding of the T_1, which is brough by the parasitic capacitators of rectifier diodes D_1 /D_2 and the parasitic capacitor of transformer T_1. In addition, because the resonant inductor L_{r1} is integrated into transformer T_1, resulting in large leakage inductance of transformer T_1, the waveform of primary side voltage v_{p1} is not exactly the same as that of the auxiliary winding voltage v_{aux}. The four important

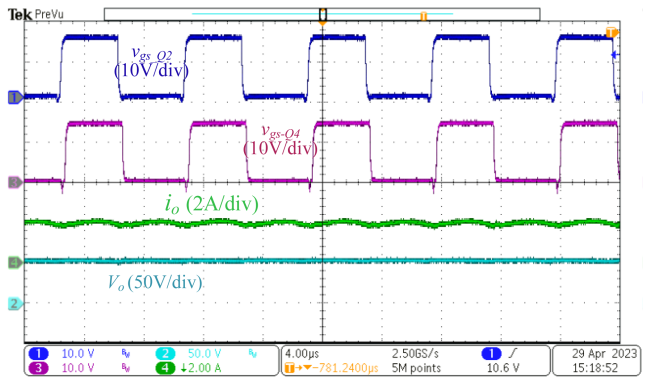

Fig. 23. Waveforms of V_o = 50 V and I_o = 2 A.

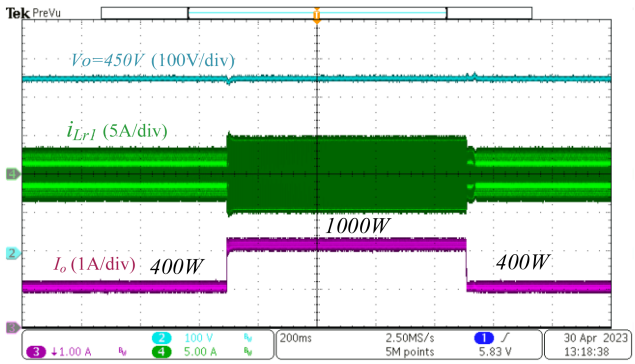

Fig. 24. Experimental waveforms with load step-up/down at output voltage V_o= 450 V.

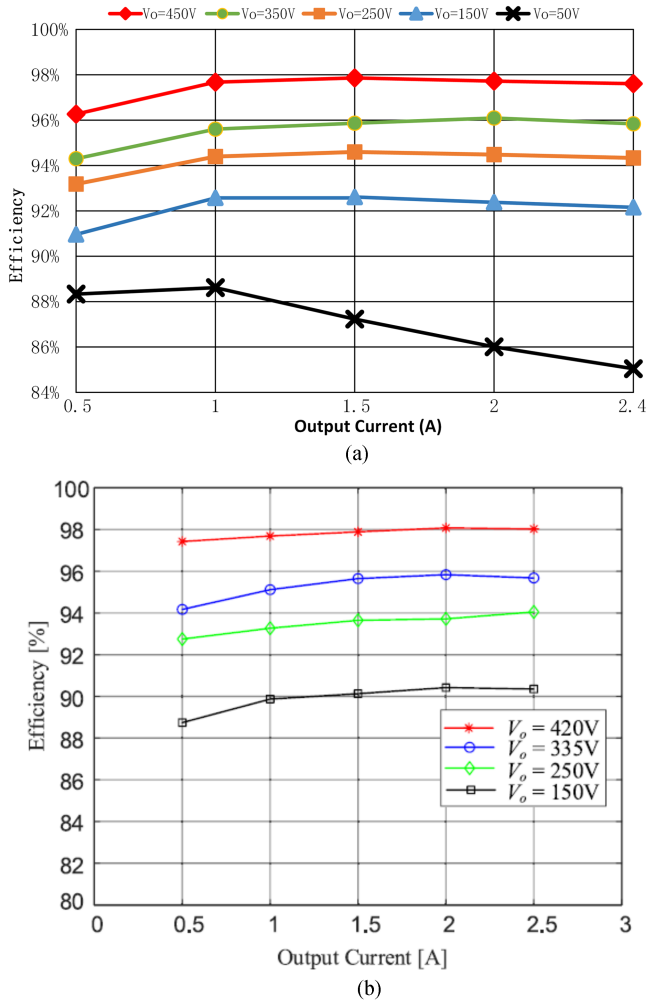

Fig. 25. Efficiency curves versus different V_o. (a) Proposed topology. (b) Ref. [20].

time points t_2, t_4, t_6, and t_8 marked in Fig. 18(b) are corresponding to the time points of the steady-state waveforms in Fig. 2, respectively. It can be seen that the experimental waveforms in Fig. 18 are very consistent with steady-state waveforms in Fig. 2.

The soft switching waveforms of the proposed topology under different output voltages are shown in Fig. 19. Fig. 19(a)–(c) shows waveforms of Q_2 and Q_4 under 50 V/100 W, 250 V/500 W, and 450 V/1000 W outputs, respectively. It is seen that the ZVS can be achieved for the primary switches of *LLC* and HB.

Fig. 20 shows voltage waveforms of Q_4 and current waveform of i_{L2} under 50 V/40 W. According to MOSFETS parameters of laboratory prototype, I_{zvs} is about 200 mA and the phase-shift angle φ is about 0.173 rad at 50 V/40 W output. The calculated current i_{L2} is about 240 mA according to (50), which is larger than I_{zvs}, so Q_4 can realize ZVS theoretically.

As shown in Fig. 20, i_{L2} is about 280 mA at the moment Q_3 turns OFF, which is close to the calculated value. It can be seen that ZVS for Q_4 has been achieved.

Fig. 21 shows the *LLC* current i_{Lr1} and HB current i_{L2} waveforms under different conditions. Since the auxiliary winding of the *LLC* transformer T_1 is inversely inserted into the primary power loop of HB, there is a 180° phase-shift between the HB current i_{L2} and the *LLC* current i_{Lr1}. According to (14) and (15), i_{L2} can be derived, as shown in

$$i_{L2} = -\frac{n_1}{n_2 + n_{aux} n_1} \left(i_{Lr1} - i_{Lm1} \right). \tag{52}$$

Moreover, it can be seen in Fig. 21 that the range of phase-shift angle is about 13°–171°, which is very close to the calculated result.

The waveforms of secondary current i_s, which is the sum of i_{D1} and $-i_{D2}$, is shown in Fig. 22. From Fig. 22, it can be seen that i_s crosses zero naturally, which means ZCS can be achieved for the secondary diodes.

The waveforms of output voltage and current at 50 V/100 W output is shown in Fig. 23.

The dynamic waveforms with load step-up and step-down at output voltage V_o = 450 V is shown in Fig. 24. It can be seen that the output voltage is stable during load steps-up/down, which indicates a good output voltage regulation performance of the proposed topology.

The efficiency curves under different output voltages are plotted in Fig. 25(a). The peak efficiency is about 97.9% at 450 V/700 W output. Fig. 25(b) shows the efficiency curves in [20]. It can be seen that the laboratory prototype features better efficiency performance under low output voltage range.

Table II shows a comparison among the proposed topology and some recently reported topologies for wide output range applications.

It can be seen that the proposed topology can achieve wider output voltage range except the converter presented in [20]. However, the topology in [20] needs one more resonant inductor and larger size of transformers (see Section III-C). Furthermore, the transmission path of reactive power in [20] is longer than the proposed topology (see Section III-D), which results in rapid efficiency drop under low voltage output, while the high output voltage efficiencies of both converters are close.

In summary, the proposed topology features the least components count, simple control, wide output voltage range, and good efficiency.

TABLE II
COMPARISON AMONG THE TOPOLOGIES FOR WIDE OUTPUT VOLTAGE RANGE

Schemes	*LLC*+LC [7]	*LLC* [9]	H5-*LLC* [13]	Interleaved *LLC* [19]	Interleaved *LLC* [20]	This work
Modulation scheme	PFM	PWM	PFM	PFM+PSM	PSM	PSM
Number of switches	4	5	5	8	4	4
Number of diodes	4	3	4	6	4	2
Control complexity	Low	Low	High	High	Low	Low
Maximum voltage gain*	$1/n$	$2/n$	$2+2n_1/n_2$	$2/n$	$1/n$	$1/n_1+2/n_2$
Output voltage of experimental prototype	50–430 V	250–420 V	80–450 V	150–500 V	10–420 V	50–450 V
Power level	3 KW	1 KW	1 KW	3.5 KW	1 KW	1 KW
Peak efficiency	96.8%	96.7%	97.05%	98%	98.1%	97.9%
Resonant frequency	200 KHz	100 KHz	100 KHz	100 KHz	100 KHz	120 KHz

* n_1, n_2, and n are the turns ratio of the transformers.

V. CONCLUSION

In this article, an interleaved *LLC*+HB resonant converter was proposed for wide output voltage range applications. The proposed topology adopts a fixed-frequency phase-shift control to regulate the output voltage. The fixed-frequency operation facilitates optimization of the magnetic component design of the *LLC* converter. The operation principle and detailed theoretical analysis are presented. The numerical calculation of gain in the time-domain method is discussed in detail. Meanwhile, a simple approximate analysis method for voltage gain analysis is proposed, which is helpful for quickly determining the main parameters of the converter in engineering applications. Finally, a 1 KW laboratory prototype with 400 V input/50 V–450 V output has been built-up to verify the feasibility of topology. The laboratory prototype performances ZVS for the primary switches and ZCS for the secondary diodes over a wide output voltage range and load range, and the peak efficiency is 97.9%.

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