Letters

Five-Level ANPC Inverter With Full DC-Bus Utilization

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***Abstract*—This letter presents an improved hybrid active neutral point clamped (IHANPC) five-level (5L) inverter as an upgrade/replacement for a conventional 5L ANPC inverter. Unlike the conventional ANPC inverters, the proposed inverter doubles the utilization of the dc-link voltage, eliminating the need for an additional boosting stage. By charging the switched capacitor (SC) to half the input voltage, it doubles the rms output voltage for a given dc voltage. Also, a tiny inductor is incorporated to limit the prevailing SC impulse charging current without affecting the inverter operation. Moreover, the proposed IHANPC inverter can also self-start and self-balance the voltages of the SC and the dc-link capacitor voltages without any external circuits or balancing techniques. Due to the lower required dc-link voltage and limited SC charging current, devices with lower voltage and current ratings can be selected. Design considerations and a comparative analysis with other current topologies are discussed in detail. The comparison shows that the proposed IHANPC requires the least number of parts to achieve the same performance and output quality. To validate the effectiveness and practicality of the proposed IHANPC inverter, the experimental results for a 1.2-kW system are presented.**

***Index Terms*—Active neutral-point clamped (ANPC) inverter, capacitor charging current, self-balance, switched capacitor (SC).**

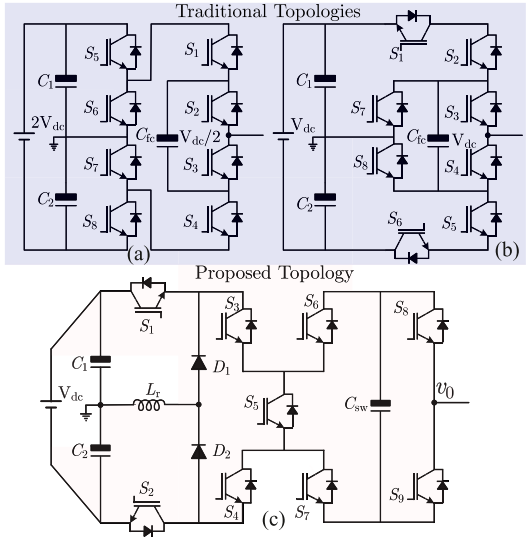

Fig. 1. 5L ANPC inverters with high charging current. (a) Traditional [5]. (b) With unity voltage gain [15]. (c) Proposed 5L IHANPC with limited charging current.

I. Introduction

ONE of the key technologies enabling the seamless integration of renewable energy systems, such as photovoltaic (PV) is the concept of multilevel inverters (MLI) [1], [2], [3]. Cascaded H-bridge inverters, neutral point clamped (NPC) inverters, and flying capacitor inverters are referred to as the traditional MLI topologies [4]. To overcome the problems in the abovementioned topologies, such as the higher number of semiconductors, uneven distribution of losses, and the need for an external circuit/complex balancing approach to balance the dc-link capacitor voltages, the active NPC (ANPC) was invented.

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Although the ANPC outperforms the NPC, the peak output voltage of the ANPC inverter shown in Fig. 1(a) is limited to only half the input dc voltage [5]. In other words, the dc-bus utilization is only 50%, and this shortcoming is not only specific to the ANPC inverter but also applies to all other midpoint clamped inverter structures. In order to enhance the dc-link utilization and generate a higher number of voltage levels, switched capacitors (SCs) are used in conjunction with the traditional ANPC. The dc-link capacitors and SC in [6], [7], and [8] are self-balanced with a voltage gain of only 0.5. Several attempts have been made to develop ANPC structures with minimum semiconductors and self-balancing capability. On this line, the topologies in [9], [10], [11], [12], and[13] have an improved voltage gain of one. However, the SC-based ANPC inverters suffer from the repetitive impulse charging currents that limit their application to medium power [14]. The inverters shown in Fig. 1(b) [15] are one such topology that falls into this category. In the literature, the use of a small inductor is a modest tradeoff between limiting the impulse current and other aspects, such as size, weight, and cost [12], [13]. In [16], a quasi-resonant technique was used to minimize the impulse charging current. In [17], only six switches were used to produce a five-level (5L) staircase output voltage

TABLE I
SWITCHING STATES AND THEIR EFFECT ON SC VOLTAGE

Level	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	D_1	D_2	C_{sw}
V_{dc}	1	0	1	0	1	0	1	1	0	0	0	⇓
$0.5V_{dc}$	1	0	1	1	0	1	1	1	0	0	1	⇑
+ 0	1	0	1	1	0	1	0	0	1	0	0	⇑
- 0	0	1	1	1	0	0	1	1	0	0	0	⇑
$-0.5V_{dc}$	0	1	1	1	0	1	1	0	1	1	0	⇑
$-V_{dc}$	0	1	0	1	1	1	0	0	1	0	0	⇓

1: switch ON, 0: switch OFF, +0 and -0: zero levels during respective positive and negative half cycle, ⇓: discharging, ⇑: charging

with two times the voltage gain. However, the common-mode voltage variation increases due to the unavailability of the dc-link midpoint. Numerous attempts are made in the literature to reduce the number of switches of the 5-L inverters in grid-connected applications, which requires charging SC to V_{dc}.

This letter presents another 5L ANPC-based inverter topology with reduced components for renewable energy applications. For 5L operation, only nine switches, two diodes, and one SC are required, which reduces size, weight, and cost. In addition, a small inductor is attached to limit the SC impulse charging current. The device's voltage stress is limited to half the input voltage, while four of the nine switches operate at line frequency, resulting in lower switching losses. The presence of a common dc-link allows an easy expansion to three-phase operation and better suitability for solar PV applications due to lower common-mode voltage variations. A detailed comparative study and experimental results are presented to highlight the feasibility of the proposed topology.

II. PROPOSED TOPOLOGY AND OPERATING PRINCIPLES

A. Description of the Proposed Topology

Unlike the topologies available in the literature, where SC charges to the DC input voltage (V_{dc}), the proposed improved hybrid active neutral point clamped (IHANPC) charges to only $0.5V_{dc}$ with identical peak output voltage. The circuit topology of the proposed IHANPC inverter is shown in Fig. 1. It consists of nine switches (S_1–S_9), one SC (C_{sw}), two diodes (D_1 and D_2), and an impulse charging current limiting inductor (L_r). Upon inspection, it is clear that the proposed topology is an extension of the widely used ANPC inverter. A suitable switching pattern results in the generation of the following voltage levels: ($-V_{dc}$, $-V_{dc}/2$, 0, $+V_{dc}/2$, and $+V_{dc}$).

B. Modes of Operation

To generate a 5L output voltage, the proposed IHANPC has six switching states with different effects on the SC voltage. The conduction path during each mode is shown in Fig. 2. During the whole operation, the dc-link capacitors and the voltages on SC are naturally balanced. According to the conduction states of the semiconductor switches listed in Table I, the SC is either charged or discharged depending on the direction of the load current.

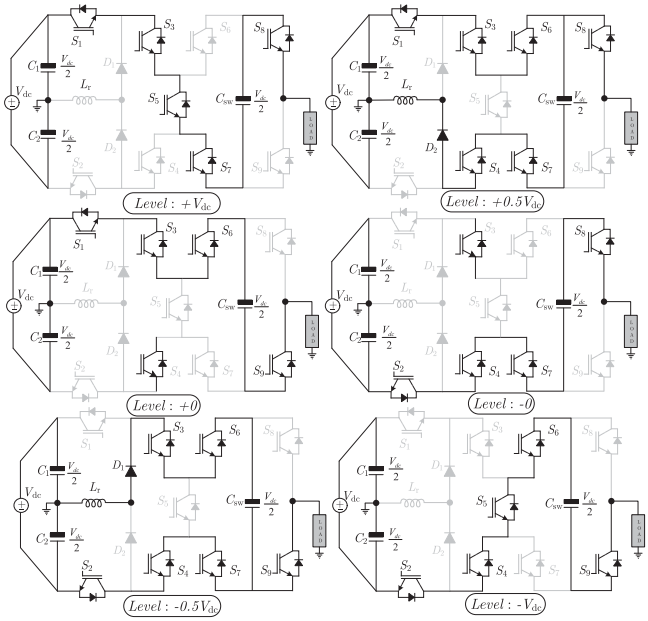

Fig. 2. Active switches and current path for each of the output voltage levels.

C. Modulation Technique

As in Fig. 2 and Table I, a level-shifted phase disposition-based multicarrier pulsewidth modulation technique is used to drive the semiconductors. The principle of this method is to compare a modulating (sinusoidal) signal at line frequency with two level-shifted carrier signals (triangular signals) of identical amplitude, phase, and frequency. At $\pm$ $0.5V_{dc}$ levels, the SC voltage naturally equalizes to $0.5V_{dc}$. Also, a simple lookup table is used to generate gating pulses, and the modulation index M $(= \hat{v}_{ref}/2 \times \hat{v}_{cr1})$.

D. Selection of SC and L_r

The selection of SC is critical as it determines the voltage ripple and the output waveform quality. Since there are two redundant states for zero voltage generation and because of the symmetry operation, a positive half-cycle was considered for sizing SC. The longest discharge period of the SC (i.e., θ_1–θ_2) is considered for its appropriate sizing [12]. The derived equations for SC sizing and the inductor are as follows:

$$\Delta V_X = \int_{\theta_1}^{\theta_2} \frac{I_m \sin\theta\,(T_{ch} - T_{disch})}{C_{sw}} d\theta \tag{1}$$

$$i_{L_r}(t) = \frac{V_{C_1} - V_{C_{sw}}}{\omega L_r} e^{-\frac{R_{eq}}{2L_r}t} \sin\omega t \tag{2}$$

From (2), the maximum value of SC current ($i_{Lr\max}$) is inversely proportional to the value of L_r. This means that using a larger value of the inductor leads to a lower peak charging current at the cost of increased size or reduced power density.

Moreover, owing to the higher voltage rated capacitor requirement of the ANPC topology, its stored energy and thus, the volume is higher than the proposed, which adversely affects

the ANPC's size and power density. On the other hand, the proposed IHANPC inverter uses half of the dc-link voltage than the traditional ANPC, reducing the energy requirements and exhibits higher power density. Further, the proposed topology's volume including the additional passive components (diodes and inductor) is about 50% lesser than that of the ANPC topology, thus, reducing the space requirements and saves initial cost.

E. Self-Balanced Capacitor Voltages

In conventional SC-based converters, an additional precharging circuit is required to charge the SC to the required value and then stabilize it using a corresponding modulation strategy. As a result, this increases the complexity and cost of the overall system. However, in the proposed inverter design the precharging process is integrated within the topology itself.

During the precharging of the dc-link capacitor, the SC alternately trades energy with two dc-link capacitors. For instance, as it is shown in Table I and Fig. 2 consider one complete cycle of V_{ref}. In the positive half-cycle, during the level $+0.5V_{\text{dc}}$ the capacitor C_{sw} is connected in parallel with C_1 through D_2 and the current limiting inductor L_{r}. Therefore, the voltage across C_{sw} gradually increases to reach C_1 value. During level +0, the capacitor C_{sw} is connected in parallel with C_1 through the load. Hence, during this mode, C_{sw} will continue its charging process. This process will continue until the voltages across C_1 and C_{sw} are equal. During the level $+V_{\text{dc}}$, the capacitor C_{sw} will discharge its energy to the load. Similar is the case for C_2 during the negative half-cycle. It means that the charging and discharging process of the capacitor C_{sw} changes alternately over a complete cycle of the output voltage. Its voltages can, therefore, be balanced to half of the dc input voltage automatically but with some ripples.

The energy exchange between C_{sw}, C_1, and C_2 in a power frequency period effectively creates an indirect energy exchange between C_1 and C_2 as well, resulting in the self-balance of the dc-link capacitors' voltages.

III. Comparative Study

Several SC-based 5L inverters in the literature have proven to be better alternatives in their chosen applications. However, most of these structures suffer from the fact that they must be designed for higher currents and voltages, and their three-phase implementation is also not straightforward. Therefore, for a fair and meaningful comparison, the proposed IHANPC is compared with other 5L topologies that share similar characteristics. The topologies in [5], [6], [9], and[10] require a lesser number of switches, while their current carrying capacity is much higher due to the impulse charging current. The topologies in [8] and [11] also have the same limitation with higher number of switches than IHANPC. Although the inverter in [7] has the limited inrush current, the gain is only 0.5. In many cases, the devices must be connected in parallel to meet higher current requirements, driving up the overall cost. The need of only one SC rated for $0.5V_{\text{dc}}$ has positively affects the lifetime of the proposed inverter.

From Table II, [12] and [13] are preferred in terms of gain, inrush current limitation, and cost factor (CF). However, the maximum number of conducting devices in the proposed topology is only six (during $\pm$ $0.5V_{\text{dc}}$ level) as in [12] and less than eight as in [13]. Moreover, the total number of switching transitions in a fundamental cycle is 18, which is 16 in [12], while in [13] it is 32. In addition, the maximum voltage stress on the semiconductors in [13] is thrice than that in the proposed topology, which increases the cost of the inverter and in [13], the impulse charging current is limited at the expense of bulky inductors.

In general, the number of components alone cannot justify the value of a particular inverter, since the power device ratings greatly affect the overall performance and cost. Therefore, the factor total standing voltage (TSV), which translates the switching requirements into the corresponding cost requirements, is calculated for all the selected topologies. As given in the Table II, the proposed IHANPC has the lowest TSV in the class of reduced charging current and unity gain-based 5L inverters. To account for the unique figure of merit, a CF [7] and the corresponding value listed in Table II are used

$$\text{CF} = \frac{N_{\text{sw}} + N_{\text{D}} + N_{\text{C}} + (\alpha \times \text{TSV}) + (\beta \times \text{TCV})}{N_{\text{L}}} \tag{3}$$

where α and β are the coefficients and N_{L} is the number of levels. The factors α and β provide the flexibility in weighing the effect of capacitor voltages and switch stress on the inverter cost. It is evident that the value of CF is lowest for the proposed

TABLE II
Comparison With Other 5L Midpoint Clamped MLIs

MLI–>	[5]	[6]	[7]	[8]	[9]	[10]	[11]	[12]	[13]	[P]
Switches	8	7	6	12	8	8	10	10	12	9
Diodes	0	2	2	0	2	0	0	2	0	2
SCs	1	1	2	1	2	1	1	1	2	1
Inductors	0	0	1	0	0	0	0	1	2	1
Inrush current	H	H	L	H	H	H	H	L	L	L
Self-balance	N	Y	Y	Y	Y	Y	Y	Y	Y	Y
Vgain ($\times V_{\text{dc}}$)	0.5	0.5	0.5	0.5	1	1	1	1	1	1
BA	N	N	N	N	Y	Y	Y	Y	Y	Y
TSV ($\times V_{\text{dc}}$)	3	3.75	3.5	3	9	5	7	6	11	5.5
TCV ($\times V_{\text{dc}}$)	0.25	0.25	0.5	1.5	1	1	0.5	0.5	1	0.5
CF α=0.5	2.15	2.8	2.5	3.2	3.5	2.5	3	3.3	4.1	3.1
at α=1	2.45	3.5	2.8	3.5	4.4	3	3.7	3.9	5.2	3.6
β=1 α=1.5	2.75	4.2	3.2	3.8	5.3	3.5	4.4	4.5	6.3	4.2
Blocking voltage ($\times V_{\text{dc}}$)	4*1/2 4*1/4	2*3/4 2*1/2 3*1/4 2*1/4	4*1/2 2*1/4 2*1/2	12* 1/4	2*3/2 2*1 4*1/2 2*1	2*1 6*1/2	4*1 6*1/2	10*1/2 2*1/2	2*3/2 6*1 4*1/2	9*1/2 2*1/2
MBV ($\times V_{\text{dc}}$)	0.5	0.75	0.5	0.25	1.5	1	1	0.5	1.5	0.5

Vgain: Voltage gain, BA: Boosting ability, TSV: Total Standing Voltage, TCV: Total Capacitor Voltage, CF: Cost Factor, MBV: Maximum Blocking Voltage, H: High, L: Low, Y: Yes, N: No

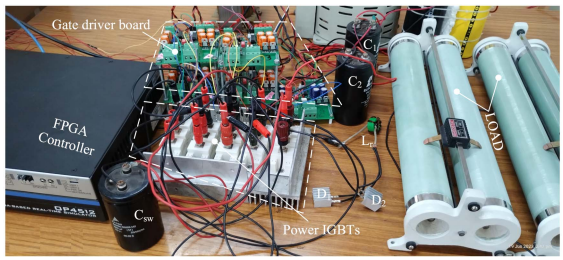

Fig. 3. Experimental setup of the proposed topology.

TABLE III
COST COMPARISON OF 5L INVERTER TOPOLOGIES

Item	Rating	Part Number	Price/unit ($)	[5]	[6]	[7]	[8]	[9]	[10]	[11]	[12]	[13]	[P]
Switches	750V,120A	IKQB120N75CP2	15.88	6	4	–	6	4	4	8	–	2	–
	650V, 75A	IKW75N60T	10.55	–	–	2	–	–	–	–	6	2	6
	650V, 15A	IKP15N65H5	3.27	–	–	4	–	–	–	–	–	4	–
	250V,15A	IPA600N25NM3S	1.92	2	3	–	6	4	4	2	4	4	3
Diodes	650V, 75A	IDW75E60	3.23	–	2	2	–	2	–	–	2	–	2
SCs	470uF, 450V	MAL219357471E3	18.71	–	1	–	–	–	1	–	–	–	–
	2200uF, 300V	B43544E2228M002	16.58	1	–	2	1	2	–	1	1	2	1
DC-link Caps	2200uF, 300V	B43544E2228M002	16.58	2	2	2	2	2	2	2	2	2	2
Gate driver	10-35V, ±1.5A (max)	TLP250	1.78	8	7	5	12	7	8	10	10	12	9
			Total Price ($)	163.1	140.1	116	178	156.4	137.3	198.4	145	161.3	141.3

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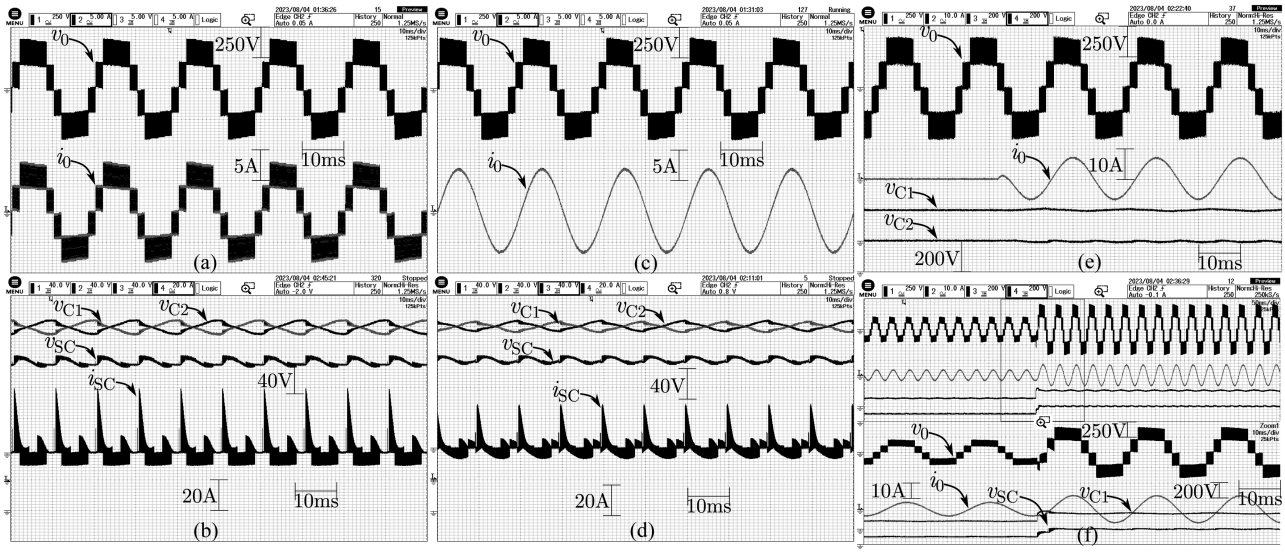

Fig. 4. Key waveforms under steady-state condition with IHANPC inverter feeding (a), (b) *R*-load and (c), (d) *RL*-load. Key waveforms under dynamic condition for (e) change in load from zero to 100% and (f) step increase in input voltage from 200 to 400 V.

TABLE IV
DESIGN SPECIFICATIONS

P_{rated}	V_{dc}	Capacitors	L_{r} (T150-45A)	f_{sw}	Load
1.2 kW	400 V	2200 μF	3.5 μH	10 kHz	50 Ω+80 mH

IHANPC and the one in [12] and [13]. Moreover, the MBV of the proposed inverter is limited to half of the input voltage, which requires the use of lower rated power switches. Therefore, the proposed inverter combines several merits to achieve higher reliability in generating an identical output voltage with similar functionality as its counterparts.

A case study illustrating the lucrative benefits of the proposed IHANPC inverter is presented for a 1.2 kW, $V_{\text{dc}} = 400$ V system. The voltage and current ratings of the devices are appropriately chosen as per the inverter structure and considering the use of hard- or soft-charged capacitors, respectively. Capacitances are calculated based on the given formulas. The resulting costs for each of the considered inverters are tabulated in Table III. From Table III, it can be seen that the proposed IHANPC inverter has the lowest price compared with other similar topologies.

IV. RESULTS AND DISCUSSION

To evaluate the performance of the proposed inverter, the PLECS platform was chosen for simulation analysis. For both simulation and experimental verification, the design specifications and component values are given in Table IV. Owing to the laboratory off-shelf availability of the core type, a toroidal core (iron powder core)-based design was adopted and employed for the proposed topology. The prototype design is as shown in Fig. 3, which is tested under various load conditions.

First, the inverter is operated to feed the resistive (R) load, and the corresponding key waveforms are shown in Fig. 4(a) and (b). Second, the inverter feeds the resistive–inductive (RL) load, and the obtained results are shown in Fig. 4(c) and (d). From the waveforms, it can be seen that the inverter generates a 5L voltage and the capacitor voltages are well balanced at each power factor of the load. It is worth noting that the current of SC is only about four times the load current, unlike the hard-charged SCMLIs. Moreover, the dynamic performance of the proposed inverter is evaluated by increasing the load from zero to 100%. The waveforms in Fig. 4(e) corresponding to the stepwise increase confirm that the inverter is insensitive to such disturbances. If

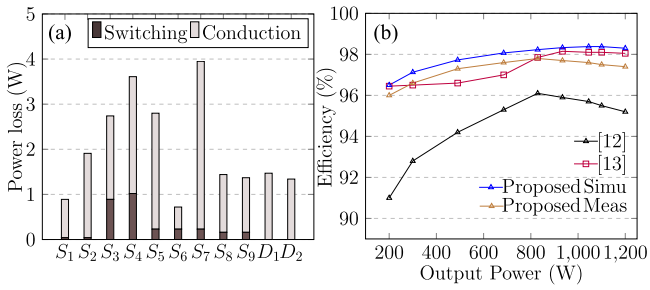

Fig. 5. (a) Device switching and conduction losses. (b) Efficiency versus load.

the input voltage is increased stepwise from 200 to 400 V, as shown in Fig. 4(f), the proposed inverter self-equalizes without significant variation in the capacitor voltages.

Moreover, the switching and conduction losses of the inverter shown in Fig. 5(a) are extracted to determine the efficiency of the inverter. Finally, Fig. 5(b) shows the simulated and measured efficiency of the proposed topology compared with other competent topologies, confirming its suitability for industrial applications. Overall, the experimental results demonstrate the operability and feasibility of the proposed IHANPC with a measured efficiency of over 97% for a wide load range.

V. Conclusion

This letter presents a 5L IHANPC inverter with reduced number of components, reduced dc-link voltage, and 100% dc-link utilization. The lower dc-link voltage requirements significantly reduce the device voltage rating, resulting in lower power losses. The SC voltage is well balanced without the need for voltage sensors. Moreover, the SC impulse current is limited with the help of a small auxiliary inductance embedded in the charging path. The operation of the proposed IHANPC inverter is verified, and the results confirming the improved performance are presented. Due to the midpoint, the proposed IHANPC can be easily extended to three-phase operation. Considering the above advantages, the presented topology emerges as a potential alternative for the grid-connected applications.

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