# Automated Extraction of Low-Order Thermal Model With Controllable Error Bounds for SiC MOSFET Power Modules

Cameron Entzminger, *Member, IEEE*, Wei Qiao, *Fellow, IEEE*, Liyan Qu, *Senior Member, IEEE*, and Jerry L. Hudgins, *Fellow, IEEE*

***Abstract*—This article explores modeling the thermal process of a Silicon carbide (SiC) metal-oxide-semiconductor field-effect transistor (MOSFET) power module through a finite element analysis (FEA) based full-order thermal model (FOM) and then reducing the order of the FEA thermal model using a hybrid model order reduction (MOR) method. This hybrid MOR method takes advantage of Krylov subspace projection method's ability to be applied to higher order systems and the controllable error bound of the Hankel singular value based MOR method using a pure mathematical approximation process without any heuristic assumption. The resulting reduced-order thermal model has a significantly reduced computation cost compared to the FEA model while preserving the accuracy of the FEA model with controllable error bounds. The proposed method is applied to a SiC MOSFET power module to generate reduced-order thermal models, which are validated by computer simulation with respect to the FEA thermal model and are compared with a state-of-the-art three-dimensional thermal equivalent circuit model and the reduced-order thermal models generated by using a Krylov subspace projection method. Experimental validation of the thermal models with respect to the measured SiC MOSFET junction temperature is provided. The results demonstrate higher accuracy and controllable error bound of the proposed method.**

***Index Terms*—Hankel singular value (HSV), Krylov subspace projection, metal-oxide-semiconductor field-effect transistor (MOSFET), model order reduction (MOR), power module, silicon carbide (SiC), thermal modeling.**

## I. Introduction

POWER (electronic) modules are widely used for power conversion equipment, such as industrial motor drives, ac–dc power supplies, renewable energy systems, electric vehicles, and uninterruptible power supplies. Particularly, in the past decade, silicon carbide (SiC) metal-oxide-semiconductor field-effect transistor (MOSFET) power modules have emerged as a promising alternative to traditional silicon-based power modules in these applications for their superior switching speeds, more efficient thermal conductivity characteristics, higher maximum operating temperatures, and higher blocking voltage capabilities [1]. The dependence on power modules for critical applications has led to a concern over the reliability of the devices. One tool used for predicting the reliability of a power module is a thermal model [2]. A thermal model is a mathematical representation of the heat transfer behavior of a power module during its operation. There are many different applications that use thermal models, such as condition monitoring [3] and fault diagnosis [4] of power modules, lifetime prediction of power modules [5], thermal management of power devices and modules to prevent overheating events [6] because cyclical thermal stress can cause chip and baseplate solder layer degradation resulting in over heating events inside power modules [7], [8].

Thermal models provide a way to understand the heat transfer characteristics at different points in a power module. An ideal thermal model has high accuracy and low computational complexity in terms of ease of implementation and computation time. One commonly used thermal model for power modules is the thermal equivalent circuit (TEC) [9], [10], [11]. TECs describe the thermal behavior by representing the physical layers of a power module as an electrical circuit. There are two main types of TEC, Cauer-type and Foster-type. Foster-type TECs are found by fitting the sum of the first-order transfer functions of each resistor-capacitor (*RC*) pair to the transient thermal impedance function from the chip to the baseplate for the power module. Foster-type TECs are limited in estimating fast transient temperature changes within the module [12]. Cauer-type TECs are based on the analogy between the heat diffusion equation and the differential equation for a transmission line with distributed line resistance and shunt capacitance. Moreover, Cauer-type TECs neglect the temperature differences within the individual layers of power modules and oversimplifies the lumped thermal capacitance for thicker layers such as the baseplate [13].

TEC models are capable of real-time applications due to their low complexity. However, these models sacrifice geometric considerations like thermal cross-coupling effects between chips and are generally defined under specific boundary conditions

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The authors are with the Power and Energy Systems Laboratory, Department of Electrical and Computer Engineering, University of Nebraska-Lincoln, Lincoln, NE 68588-0511 USA (e-mail: centzminger@huskers.unl.edu; wqiao3@unl.edu; lqu2@unl.edu; jhudgins2@unl.edu).

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like constant ambient temperature [14], [15]. Therefore, these models may not work for power modules with more complex topologies that deviate from the standard power module layered structure [16], [17]. Press pack topology is an example of a nonstandard topology with significant heat flow in three dimensions compared to the standard power module topology, which is sometimes assumed to be two-dimensional (2-D) during the modeling process [18]. The 3-D-TEC models calculate junction temperature by summing the outputs of multiple Foster-type TECs each used to model the thermal cross-coupling effects from multiple semiconductor chips in a device [19], [20], [21], [22], [23]. These models can create computationally efficient 3-D heat transfer models, but require multiple TEC models manually fit to step response data. The model order of the resulting 3-D-TEC also increases with the number of inputs and outputs. Press-pack topologies rely on 3-D-TECs, and 3-D-TECs rely on Foster and Cauer-type TEC models, which inherit the aforementioned disadvantage of limited estimation of fast transient temperatures [24].

A digital filter model was proposed in [25] to characterize the thermal behavior of a power module using low-order infinite impulse response digital filters, which, however, do not preserve the properties of the thermal behavior across the entire input frequency range. In addition, time-consuming finite element analysis is required for determining the thermal impedance coefficients used in the digital filter model. Analytical models based on Fourier series approximation techniques solving heat conduction equations have been reported [26], [27]. These models while accurate are usually mathematically complex to generate and subject to series truncation choices [28]. More importantly, although TECs, digital filter models, and Fourier series approximation techniques can be implemented online, they rely on certain heuristics, such as series truncation choices for analytical models, neglecting thermal cross-coupling effects between chips, neglecting geometric heat spreading effects due to topological distinctiveness, and determining a sufficient number of *RC* pairs for approximation in 3-D and, therefore, are subject to uncertain and uncontrollable errors. Multichip power module models based on TECs have been reported to consider the thermal coupling between multiple chips, but they neglect the weak coupling effects between distant chips and calculation of the impedance matrix is a time-consuming effort for a module with many thermally coupled chips [29].

High-order state-space thermal models created using a numerical method, such as finite element analysis (FEA), can accurately represent the effects on heat transfer due to complex geometry and the thermal coupling effects that other models oversimplify, but they are computationally complex and impractical for online or real-time implementation [30]. For a finely meshed model, there are typically tens to hundreds of thousands of degrees of freedom (DoFs) to solve for. The order of the model is equal to the total number of DoFs times the number of discretized nodes. Numerical model order reduction (MOR) techniques have been applied to reduce the orders of high-order state-space models for power modules while preserving the dominant input-output dynamics of the thermal behavior of the power modules [31].

There are two main methodologies for large-scale MOR, truncation and projection [32]. One common truncation method is truncating low contributing states by measuring the energies of the Hankel singular values (HSVs) of the system. HSVs measure the contribution of each state to the total input–output behavior of a system, analogous to the eigenvalues of a matrix. By discarding low contributing states of a system, a transformation matrix can be created to transform the system to a lower dimension while preserving the input–output behavior and reducing the computational complexity. For a method called balanced truncation, the approximation error measured with the infinity norm of the difference between the original and reduced models in the frequency domain is bounded by twice the sum of the discarded HSVs. Balanced truncation has been used for MOR of power module thermal models containing silicon insulated-gate bipolar transistor and SiC MOSFET devices [3], [33]. However, the computational complexity of this MOR method grows cubically as the original system order increases [34], [35]. Therefore, while this method has a controllable error bound, it becomes computationally inefficient for larger systems with orders of over 2000.

Another methodology of MOR is using Krylov subspace projection-based techniques. These techniques work by generating a projection matrix that is an orthonormal basis of a Krylov subspace, which is used to project a higher order system to a lower order system of a chosen reduction order while preserving the accuracy of the original model [34]. This method is more computationally efficient for larger systems compared to HSV-based methods because the costly decomposition of the model does not have to be performed [35]. Krylov subspace projection-based methods have been used in [36] to generate lower order models for SiC MOSFET power modules from higher order models. A commonly used Krylov subspace projection-based method is the block Arnoldi Iteration, which has been used for MOR of large-scale building heating models [37] and thermal models of SiC MOSFET power modules [38]. However, these methods have no controllable error bound when producing the lower order systems for a desired minimum approximation error unlike HSV-based methods.

This article proposes a novel hybrid MOR thermal modeling method for extracting a reduced-order state-space thermal model (ROM) with a controllable error bound from a full-order FEA thermal model (FOM) for SiC MOSFET power modules. The proposed thermal modeling method first utilizes the block Krylov subspace projection-based MOR technique to extract a medium-order state-space thermal model (MOM) from an FOM for SiC MOSFET power module. The order of the MOM ensures its error to the FOM is bounded within a certain range, e.g., $<0.1\%$ and is computationally efficient for the HSV-based MOR implementation. Then, the proposed method utilizes the square-root technique for balanced truncation to further reduce the MOM to a final ROM with a controllable error bound. The proposed MOR thermal modeling method uses a mathematical approximation process without any heuristic assumption. The extracted ROM is computationally efficient and can be implemented in real-time in the control hardware of power electronic systems with negligible latency and has a controllable error

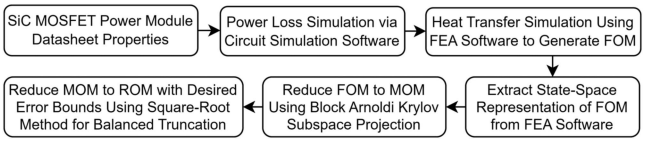


Fig. 1. Proposed hybrid MOR thermal modeling method.

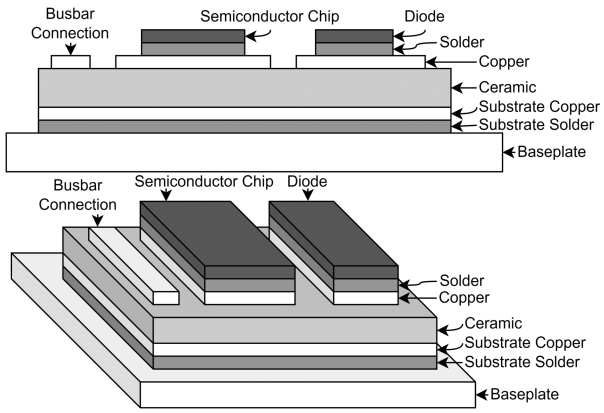


Fig. 2. Standard power module topology.

bound with respect to the FOM. The proposed method is validated by thermal modeling results for a commercial SiC MOSFET power module in comparison with a state-of-the-art 3-D-TEC modeling method [21] and the block Arnoldi Iteration-based MOR method [40].

## II. Proposed MOR Thermal Modeling Method

The proposed MOR thermal modeling method is summarized by Fig. 1. First, the semiconductor power module materials and geometries are obtained. Next, an FEA simulation is performed to create and extract an FOM of the power module. Then, a block Krylov subspace projection-based MOR is performed on the FOM to generate a MOM. Finally, the MOM is reduced further using the square-root technique for balanced truncation to generate the ROM with a controllable error bound with respect to the FOM.

### A. FOM Extraction via FEA

To describe the method, a standard power module topology is used, as seen in Fig. 2, showing seven layers of materials. A substrate consisting of a copper layer, a ceramic layer, and another copper layer is used to electrically isolate the semiconductor chip from the baseplate. This substrate is soldered to the baseplate and the semiconductor chips are soldered to the substrate. During operation, the semiconductor chip experiences a wide temperature swing due to the power loss from conduction and switching losses manifesting as heat in the semiconductor chip. To prevent overheating failures, power modules are often mounted on cold plates to direct heat flow away from the chip, through the material stack, and out of the baseplate. Power modules are often filled with protective gel that thermally insulates the semiconductor chips and prevents dust from damaging the chips.

The dominating heat transfer mode in a power module is conduction. To consider the heat transfer behavior in a power module, the following governing equation can be formulated to model the heat conduction process throughout the model:

$$-\left(\frac{\partial q_x}{\partial x}+\frac{\partial q_y}{\partial y}+\frac{\partial q_z}{\partial z}\right)+Q = \rho c\frac{\partial T}{\partial t} \tag{1}$$

where $q_x$, $q_y$, and $q_z$ are the heat fluxes in each direction [W.m$^{-1}$.K$^{-1}$], $Q$ is the heat generation [W.m$^{-3}$], $\rho$ is the density of the material used in a layer [kg.m$^3$], $c$ is the specific heat capacity [J.kg$^{-1}$.K$^{-1}$], $T$ is the temperature [K], and the term $(\partial T)/(\partial t)$ is the temperature gradient [K.m$^{-1}$]. Using (1), the temperature at any point in the power module can be found as a function of time, the material parameters, the geometries, the boundary conditions, and input heat generation.

Equation (1) is usually solved by using a numerical method such as FEA. An FEA simulation is set up by first importing a geometric computer aided design (CAD) model. Next, boundary conditions are applied to initialize the system. Thermal insulation constraints are applied to power module layers in contact with the dielectric gels used to insulate the semiconductor chips. A convection cooling heat flow constraint is applied to the bottom of the baseplate to simulate a cold plate. Ambient temperature constraints are applied to the outer surfaces of the model. Time-varying heat generation constraints are applied to the transistor and diode chip volumes. After applying initial conditions and boundary constraints, the CAD model is discretized into smaller elements. Each vertex used to create an element is called a node. Using (1) as the governing equation, the Galerkin method can be used to create the system of linear equations that must be solved to approximate the heat conduction behavior for a single element. The system of equations generated for each element can, then, be combined into a larger globally assembled system of equations, which relates the material properties, the number of discretized nodes, the boundary conditions, and initial constraints for each element as seen in

$$C\dot{T}+GT = F \tag{2}$$

where the $n \times n$ matrices $C$ and $G$ are the assembled specific heat capacity and thermal conductivity matrices, respectively; $n$ is the number of DoFs in the model; the vector $T$ represents all the nodal temperatures; the vector $F$ is the summation of each heat generation and convective heat flux boundary conditions applied to the model. The value of each element in $C$ signifies the heat capacity that exists between the nodes corresponding to the indices of that element. Similarly, each element of the matrix $G$ signifies the thermal conductivity that exists between the nodes corresponding to the indices of that element. For each node, there is only one DoF, which is temperature. The time changing temperature vector can be solved for in the following way:

$$\dot{T} = -[C]^{-1}GT+[C]^{-1}F. \tag{3}$$

Data comprised in (3) can be rewritten into a generalized state-space representation of a linear system relating the inputs,

TABLE I
STATE-SPACE SYSTEM DIMENSIONS FOR FOM AND MOM

| FOM Matrix or Vector | FOM System Dimensions | MOM Matrix or Vector ($m << n$) | MOM System Dimensions |
|---|---|---|---|
| $A$ | $n \times n$ | $A_m$ | $m \times m$ |
| $B$ | $n \times Inputs$ | $B_m$ | $m \times Inputs$ |
| $C$ | $Outputs \times n$ | $C_m$ | $Outputs \times m$ |
| $D$ | $Outputs \times Inputs$ | $D_m$ | $Outputs \times Inputs$ |
| $E$ | $n \times n$ | $E_m$ | $m \times m$ |
| $T$ | $n \times 1$ | $z$ | $m \times 1$ |
| $y$ | $Outputs \times 1$ | $y_m$ | $Outputs \times 1$ |
| $u$ | $Inputs \times 1$ | $u$ | $Inputs \times 1$ |

outputs, and state variables, as follows [39]:

$$\begin{cases} E\dot{T}(t) = AT(t) + Bu(t) \\ y(t) = CT(t) + Du(t) \end{cases} \tag{4}$$

where the vector $u$ represents the time varying model inputs such as heat flux or heat generation; the vector $y$ represents the time varying output temperatures as a result of the input and state characteristics; the matrices $A$, $B$, $C$, $D$, and $E$ control the effects of the state variables to other state variables, the input's effect on the state variables, the state variables influence on the selected outputs, the input's effect on the selected outputs, and the rate of change of the state variables effects on other states, respectively. The dimensions of each vector and matrix are shown in Table I, where the system's order, $n$, is the number of DoFs in the extracted system. This extracted system is the FOM which has the highest computational complexity and highest accuracy.

### B. FOM to MOM Reduction via Krylov Subspace Projection

The goal of the MOR is to find a suitable projection matrix to project the FOM down to a MOM of a chosen order while preserving the input–output relationships of the FOM. If the FOM (4) is transformed to the Laplace domain, the input–output relationships of the FOM can be defined by the transfer function defined as follows:

$$H(s) = C(sE - A)^{-1}B + D. \tag{5}$$

where $s$ represents complex frequency. The Taylor series expansion of (5) around a selected expansion point $s_0$ is defined as follows:

$$H(s) = \mu_0(s_0) + \mu_1(s_0)\frac{(s_0 - s)}{1!} + \ldots + \mu_{l-1}(s_0)\frac{(s_0 - s)^{l-1}}{(l-1)!} + \ldots \tag{6}$$

where the system is expanded to $l$ number of terms and the coefficients $\mu$ are called moments of the function. Each moment of the expanded Taylor series can be written in terms of the extracted FOM matrices as follows:

$$A_{s_0} = (A - s_0 E) \tag{7}$$

$$\mu_0 = D - C(A_{s_0})^{-1}B \tag{8}$$

$$\mu_\tau = -C\left[A_{s_0}^{-1}E\right]^{\tau-1}A_{s_0}^{-1}B,\ \tau = 1, 2, \ldots, (l-1). \tag{9}$$

Given an expansion point $s_0$, a suitable projection matrix can be chosen to generate a MOM that matches the first $l$ moments of the FOM by creating a projection matrix based on a Krylov subspace [40].

A Krylov subspace is a span of vectors iteratively computed using successive matrix-vector multiplications. An arbitrary starting vector $b$ is saved as the first column of the span $K_l$. Then, the matrix $A$ of the FOM can be left multiplied against the previous column to generate each new column of $K_l$ as seen in the following equation:

$$K_l(A, b) = span\left\{b, Ab, A^2b, \ldots, A^{l-1}b\right\},\ l \le n \tag{10}$$

where the order of the subspace is the same as the number of moments matched $l$. The vector $b$ can be replaced by the matrix $B$ of the FOM in which the resulting number of columns of $K_l$ is $l$ times the number of inputs. The resulting $K_l$ is then called a block Krylov subspace usually used for systems with multiple inputs. For a selected expansion point $s_0$ a block Krylov subspace using the extracted FOM matrices can be used to generate a projection matrix that will result in a MOM that matches the first $l$ moments of the Taylor series expansion of the FOM if constructed as follows:

$$K_l\left(A_{s_0}^{-1}E, A_{s_0}^{-1}B\right) = span\{A_{s_0}^{-1}B, A_{s_0}^{-1}EA_{s_0}^{-1}B, \ldots \ldots, \left(A_{s_0}^{-1}E\right)^{l-1}A_{s_0}^{-1}B\},\ l \le n. \tag{11}$$

Given a sufficiently large value of $l$, the column vectors of $K_l$ will converge towards the eigenvector that corresponds to the greatest eigenvalue of $A$.

An orthonormal basis can be constructed from (11) using the Gram–Schmidt method by which each column vector $k$ in $K_l$ of (11) is orthogonalized by first subtracting the projections of $k$ onto each previous column vector $o$ as follows:

$$o_i = k_i - \sum_{j=1}^{i-1}\frac{\langle o_j, k_i\rangle}{\langle o_j, o_j\rangle}o_j,\ i = 1, 2, \ldots, m \tag{12}$$

where $m$ is the $l$ times the number of inputs. Next, the resulting orthogonal vector $o$ of the Krylov projection matrix is normalized by dividing by its magnitude as follows:

$$v_i = \frac{o_i}{\|o_i\|},\ i = 1, 2, \ldots, m. \tag{13}$$

Using (12), (13), and (14), the Krylov projection matrix $V$ of dimension $n \times m$ can be created as follows, where $n$ is the order of the FOM usually satisfying $m << n$:

$$V = [v_1\ v_2\ v_3\ \ldots\ v_m]. \tag{14}$$

The original $n$-dimensional state vector $T$ can be projected as a $m$-dimensional state vector $z$ in the Krylov subspace, and their relationship can be expressed as follows:

$$T = Vz. \tag{15}$$

The relationship (15) can be substituted into (4) with a right multiplication of $V^T$ to extract a MOM state space system

$$\begin{cases} E_m \dot{z}\,(t) &= A_m\, z\,(t) + B_m u\,(t) \\ y\,(t) &= C_m\, z\,(t) + D_m u\,(t) \end{cases} \tag{16}$$

where $A_m = V^T AV$, $B_m = V^T B$, $C_m = CV$, $D_m = D$, and $E_m = V^T EV$ are the resulting matrices of the MOM system of an order $m$ after projecting (4) onto the lower dimensional Krylov subspace using the projection matrix $V$ in (14). The resulting MOM system dimensions are listed in Table I.

### C. Reduction of MOM to ROM With a Controllable Error Bound via Balanced Truncation

The second step of the MOR is to perform a balanced truncation to compute a lower order approximation of the MOM based on discarding the lower energy HSVs of the MOM system. In a balanced truncation, a coordinate transform is performed that makes the controllability and observability Gramians of the MOM system equal [32]. The HSVs of the original system provide a measurement of the contribution of each state to the overall input output behavior of the dynamic system. The HSVs with a lower magnitude contribute less to the overall input output behavior and can be discarded to reduce the system to a lower order. The transformation matrix used for the coordinate transformation is created by keeping the HSVs up to a specified reduction order and setting the others to zero, effectively truncating these states from the system after transformation. However, calculation of the balancing transformation matrix may be numerically ill-conditioned [41]. To avoid this problem, a reduced order system can be produced with the square-root method, which uses well-conditioned transformation matrices [41]. The upper bound of approximation error introduced into the system can be calculated by analyzing the energies of the truncated states using HSVs and comparing the reduced and original systems.

First, the controllability Gramian $P$ and observability Gramian $Q$ are obtained by solving the generalized Lyapunov equations for the MOM in (17) and (18) as follows:

$$A_m P E_m + E_m P A_m^T + B_m\, B_m^T = 0 \tag{17}$$

$$A_m^T Q E_m + E_m Q A_m + C_m^T\, C_m = 0. \tag{18}$$

The HSVs of the MOM are defined in the following way:

$$\sigma_i = \lambda_i (PQ)^{1/2} \tag{19}$$

where $\sigma_i$ is the $i$th HSV of the MOM and $\lambda_i(PQ)$ denotes the $i$th eigenvalue of the product of $P$ and $Q$.

A balanced realization of an ROM associated with the largest $r$ eigenvalues of the MOM is found when the controllability Gramian $P_r$ and observability Gramian $Q_r$ of the ROM equal the following:

$$P_r = Q_r \;=\; \Sigma_{BAL} \;:\; diag\,(\sigma_1,\, \ldots,\, \sigma_r) \tag{20}$$

where $\Sigma_{BAL}$ is an $r \times r$ diagonal matrix with the largest $r$ HSVs of the MOM along its diagonal. $P_r$ and $Q_r$ can be calculated using the $m \times r$ transformation matrices $S_{L,BIG}$ and $S_{R,BIG}$ as

$$P_r = S_{L,BIG}^T\, P S_{L,BIG} \tag{21}$$

$$Q_r = S_{R,BIG}^T\, Q S_{R,BIG.} \tag{22}$$

The Cholesky decompositions of $P$ and $Q$ defined in (23) and (24), respectively, provide a numerically robust means of finding the transformation matrices $S_{L,BIG}$ and $S_{R,BIG}$

$$P \;= S_c\, S_c^T \tag{23}$$

$$Q \;= R_c\, R_c^T \tag{24}$$

where $S_c$ and $R_c$ are $m \times m$ lower triangular matrices.

The singular value decomposition of ${R_c}^T S_c$ is defined as follows:

$$R_c^T\, S_c = U_c\, \Sigma_c V_c^T \tag{25}$$

where $U_c$, $V_c$, and $\Sigma_c$ are of dimension $m \times m$ and $\Sigma_c$ has the HSVs of the MOM $\sigma_1,\ \ldots,\ \sigma_m$ sorted largest to smallest on its main diagonal. Then, the $V_{L,BIG}$ and $V_{R,BIG}$ matrices can be constructed using the Cholesky decompositions in (23) and (24) and the information of the singular value decomposition of ${R_c}^T S_c$ in (25) as follows:

$$V_{L,BIG} = R_c\, U_c [I_r\ 0]^T \tag{26}$$

$$V_{R,BIG} = S_c\, V_c [I_r\ 0]^T \tag{27}$$

where $V_{L,BIG}$ and $V_{R,BIG}$ are $m \times r$ matrices whose columns form bases for the left and right eigenspaces of $PQ$ associated with the largest $r$ eigenvalues ${\sigma_1}^2,\ \ldots,\ {\sigma_r}^2$, and $[I_r\ 0]$ is an $r \times m$ matrix consisting of an identity matrix $I_r$ of dimension $r \times r$ used to preserve the largest $r$ HSVs in the ROM and a zero matrix of dimension $r \times (m - r)$ used to truncate the smallest $(m - r)$ HSVs.

According to (25)–(27), the product of $V_{L,BIG}$ and $V_{R,BIG}$ simplifies to the following form:

$$V_{L,BIG}^T\, V_{R,BIG} = \; [I_r\ 0]\, \Sigma_c\, [I_r\ 0]^T = \Sigma_{BAL}\,. \tag{28}$$

Thus, $S_{L,BIG}$ and $S_{R,BIG}$ can be formulated as follows:

$$S_{L,BIG} = R_c\, U_c \left[\Sigma_{BAL}^{-1/2}\ 0\right]^T \tag{29}$$

$$S_{R,BIG} = S_c\, V_c \left[\Sigma_{BAL}^{-1/2}\ 0\right]^T \tag{30}$$

where $[\Sigma_{BAL}^{-1/2}\ 0]$ is an $r \times m$ matrix consisting of the dominant HSVs along the matrix diagonal and a zero matrix of dimension $r \times (m - r)$ used to truncate smaller HSVs.

The transformation matrices $S_{L,BIG}$ and $S_{R,BIG}$ can create a balanced realization of the MOM while truncating the lower energy HSVs to create the following final ROM:

$$\begin{cases} E_r \dot{z}_r\,(t) &= A_r\, z_r\,(t) + B_r u\,(t) \\ y\,(t) &= C_r\, z_r\,(t) + D_r u\,(t) \end{cases} \tag{31}$$

where $A_r = S_{L,BIG}^T A_m S_{R,BIG}$, $B_r = S_{L,BIG}^T B_m$, $C_r = C_m S_{R,BIG}$, $D_r = D_m$, and $E_r = S_{L,BIG}^T E_m S_{R,BIG}$ are the transformed and truncated system matrices and $z_r$ is the resulting truncated $r$-dimensional state vector of the ROM of order $r$. This

TABLE II
SiC MOSFET Power Module Layer Geometries and Material Properties

| Power Module Material Layer | Length (mm) | Width (mm) | Thickness (mm) | Thermal Conductivity (W/(m*K)) | Density (kg/m^3) | Specific Heat Capacity (J/(kg*K)) | Thermal Resistance (W/(m*K)) | Thermal Capacitance (J/K) |
|---|---|---|---|---|---|---|---|---|
| SiC (MOSFET Chip) | 4.14 | 6.38 | 0.38 | 490 | 3100 | 670 | 0.0294 | 0.0208 |
| Silver (MOSFET) | 4.14 | 6.38 | 0.05 | 200 | 8580 | 233 | 0.0094 | 0.0026 |
| SiC (Diode Chip) | 5 | 5 | 0.18 | 490 | 3100 | 670 | 0.0147 | 0.0093 |
| Silver (Diode) | 5 | 5 | 0.05 | 200 | 8580 | 233 | 0.0100 | 0.0025 |
| Copper (Top) | 19.24 | 10.3 | 0.28 | 400 | 8960 | 385 | 0.0226 | 0.0299 |
| Aluminium Nitride | 31.24 | 23.6 | 0.68 | 321 | 3260 | 800 | 0.0442 | 0.0849 |
| Copper (Bottom) | 31.24 | 23.6 | 0.28 | 400 | 8960 | 385 | 0.0125 | 0.0540 |
| Solder (Baseplate) | 31.24 | 23.6 | 0.05 | 50 | 8600 | 173 | 0.0174 | 0.0043 |
| Copper (Baseplate) | 45 | 107.5 | 3 | 400 | 8960 | 385 | 0.0407 | 1.9085 |
| Silicone Grease (TIM) | 45 | 107.5 | 0.05 | 0.7 | 2100 | 1460 | 0.3873 | 0.7416 |

method guarantees an upper error bound on the infinity norm of the error, i.e., the maximum singular value of the difference between the MOM and ROM for all frequencies, which is expressed as follows:

$$\|H_m(s) - H_r(s)\|_\infty \leq 2\sum_{i=r+1}^{m} \sigma_i \tag{32}$$

where $s$ is the complex frequency input to the frequency responses of the MOM and ROM, $H_m$ and $H_r$. The upper error bound is twice the sum of the truncated HSV values of the MOM. Thus, the percentage error of the ROM with respect to the MOM, $e$, can be calculated using the following equation:

$$e = \frac{\|H_m(s) - H_r(s)\|_\infty}{2\sum_{i=1}^{m}\sigma_i} \times 100\% \leq \frac{\sum_{i=r+1}^{m}\sigma_i}{\sum_{i=1}^{m}\sigma_i} \times 100\% \tag{33}$$

where $r$ is the desired number of HSVs to keep in the ROM, thus becoming the needed reduction order. According to (33), given a desired approximation error percentage $e$, the reduction order $r$ of the ROM can be determined a priori by truncating the $m$ – $r$ smallest HSVs of the MOM until the remaining total is at a desired percentage of the original total.

## III. Simulation Validation

### A. FEA Simulation

A single phase of a CREE CCS050M12CM2 All-SiC Six-Pack MOSFET power module was simulated to validate the proposed thermal modeling method. The module has three material stacks each for a single phase of a three-phase inverter. The module's layer geometries and material properties are based off the datasheet parameters of the CCS050M12CM2 [42], [43] and are compiled in Table II. Each semiconductor chip is mounted on the baseplate through a stack of different material layers as seen in Fig. 2. The process to create an ROM for the single phase of the module from an FEA simulation is described in Fig. 1.

During module operation, the heat generated at the semiconductor chips is conducted through the material layers to the baseplate. The heat flux curves of each SiC MOSFET and SiC diode were developed from the device characteristics and operational parameters of a switch used in a three-phase inverter with an induction motor load, which was designed in MATLAB/Simulink

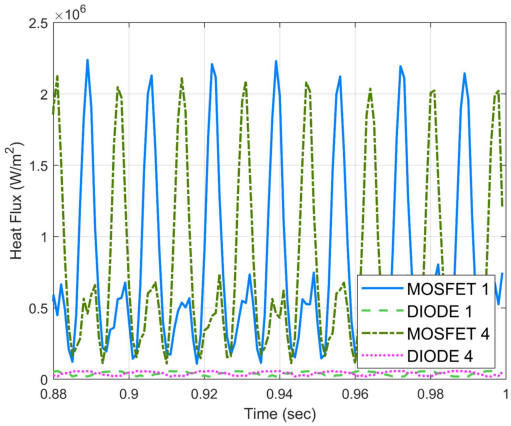


Fig. 3. Heat flux curves for the two MOSFETs and two diodes of a single phase of the inverter obtained from MATLAB/Simulink Simscape.

with the add-on Simscape. Device properties, such as turn-ON and turn-OFF energies and on-state resistance, were obtained from the CREE CCS050M12CM2 datasheet. A sine-triangle pulse-width modulation switching scheme was used with the inverter to drive the induction motor load. The inverter used a 400 V dc-link voltage, 60 A peak sinusoidal output current, 5 kHz switching frequency, and 60 Hz line frequency. Simscape MOSFET and diode models were used for the simulation because the heat flux during operation can be directly extracted from these models. The resulting four heat fluxes for the two MOSFETs and two diodes used for a single phase of the inverter are shown in Fig. 3. The simulation generated heat flux curves for 1 s while Fig. 3 displays a subsection from 0.88 to 1 s.

COMSOL Multiphysics was used for FEA thermal modeling of the power module. A cooling convective heat flux constraint was applied to the bottom of the thermal interface material (TIM) layer with a chosen heat transfer coefficient value of 5000 W/m$^2$ K, which is a standard value for a liquid cooling heat sink system [44], [45]. The ambient operational temperature of 60 °C was chosen to simulate hot operating conditions. Since material properties were assumed to be temperature independent for modeling, other ambient temperatures would lead to similar results.

The four heat flux curves in Fig. 3 were applied as heat flux constraints to the tops of the corresponding MOSFETs and diodes


Fig. 4. Three-dimensional temperature plot of SiC MOSFET power module in COMSOL.

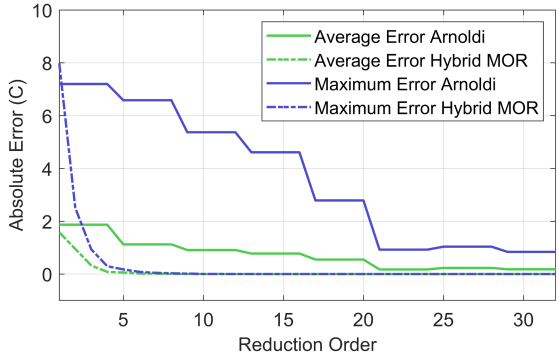


Fig. 5. Average and maximum absolute error between FOM and ROMs of orders 1 to 32 generated using Arnoldi Iteration and proposed hybrid MOR method.

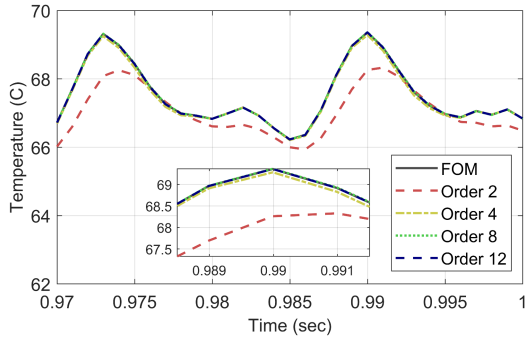


Fig. 6. Transient temperature response of MOSFET 1 chip obtained from FOM and ROMs of orders 2, 4, 8, and 12 using hybrid MOR method.

in the FEA thermal model to result in the transient responses of each chip. This resulted in the 3-D temperature plot of the power module shown in Fig. 4. The power loss coming from the MOSFETs seen in Fig. 4 is a larger contribution overall to the power loss than the diodes. The thermal coupling between the four semiconductor chips for a single phase can be seen clearly in Fig. 4 during operation. The software COMSOL LiveLink for MATLAB is an interfacing software used to run the COMSOL API within MATLAB. The command mphstate was used to extract the FOM (4) with a system order of 51 585 from COMSOL into MATLAB, which was solved using the backwards Euler method.

### *B. Comparison of Proposed Hybrid MOR Method and Block Arnoldi Iteration*

The proposed hybrid MOR method was compared to a popular Krylov subspace projection-based MOR method, the block Arnoldi Iteration [37], [46], to generate an ROM. In the hybrid MOR method, the FOM was reduced to a MOM with a system order of 1000. The reduction order for the ROM can be swept from 1 to 1000 for the hybrid MOR method but is constrained to multiples of 4 for the block Arnoldi Iteration due to the formulation of the projection matrix for a multi-input system. The MOSFET 1 chip temperature transient response was simulated using the ROMs of orders 1 to 32 generated from the two MOR methods and the resulting average and maximum absolute error between the FOM and the ROMs is displayed in Fig. 5. The hybrid MOR method is shown to have improved average and maximum absolute error at all reduction orders compared to the block Arnoldi Iteration. Fig. 6 shows that the MOSFET 1 chip temperature transient response obtained from the ROM generated by the hybrid MOR method is closer to that obtained from the FOM as the reduction order increases from 2 to 4, 8, and 12. Table III provides a quantitative comparison of the average and maximum absolute error for reduction orders 4, 8, and 12 for the block Arnoldi Iteration and the hybrid MOR method. The average absolute error for the hybrid MOR method stayed below 0.1 °C, 0.01 °C, and 0.001 °C for orders above 4, 8, and 12, respectively. The maximum and average absolute error of the hybrid MOR method is only 4.11%–0.07% and 4.34%–0.09% of that of the block Arnoldi Iteration for reduction order from 4 to 12, respectively, indicating that the proposed method can generate much more accurate ROM than the block Arnoldi Iteration for real-time applications.

TABLE III
MAXIMUM AND AVERAGE ABSOLUTE ERROR OF MOSFET 1 CHIP TEMPERATURE TRANSIENT RESPONSE BETWEEN FOM AND ROMS GENERATED BY PROPOSED HYBRID MOR METHOD AND BLOCK ARNOLDI ITERATION

| Reduction Order | Maximum Absolute Error (°C) | | Average Absolute Error (°C) | |
|---|---|---|---|---|
| | Block Arnoldi | Hybrid MOR | Block Arnoldi | Hybrid MOR |
| 2 | N/A | 2.505 | N/A | 0.951 |
| 4 | 7.196 | 0.296 | 1.868 | 0.081 |
| 8 | 6.582 | 0.029 | 1.124 | 0.0078 |
| 12 | 5.369 | 0.0036 | 0.910 | 0.0008 |

### *C. Comparison of Step Response Results of Proposed Hybrid MOR Method and 3-D-TEC*

An ROM of order 4 was created for a chosen error bound of 5% using (33) and compared to a 3-D-TEC model of order 128 illustrated in Fig. 7 [21]. In Fig. 7, a voltage-controlled voltage source represents the temperature contribution from each cross-coupled heat flux input for each material layer of

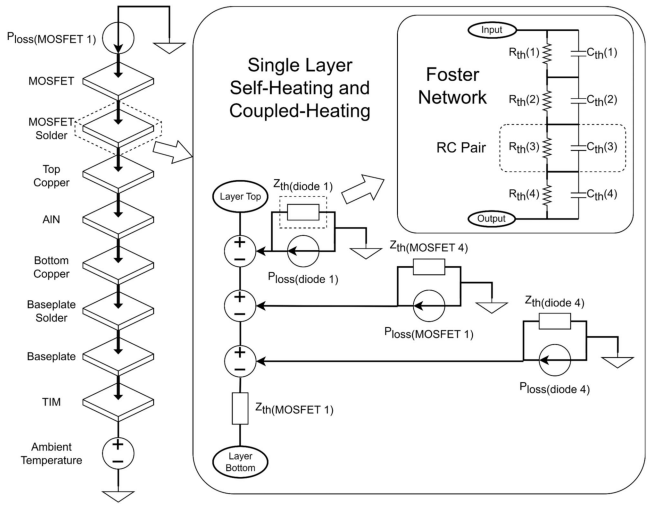


Fig. 7. Three-dimensional-TEC model per layer heating contributions with Foster-type TECs.

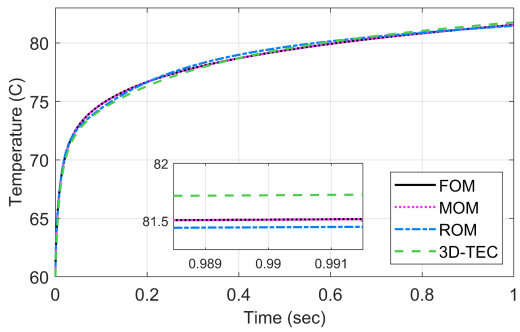


Fig. 8. MOSFET 1 chip temperature step response obtained from FOM, MOM, and ROM of order 4 generated from the hybrid MOR method, and 3-D-TEC when a constant heat flux was applied on MOSFET 1 only.

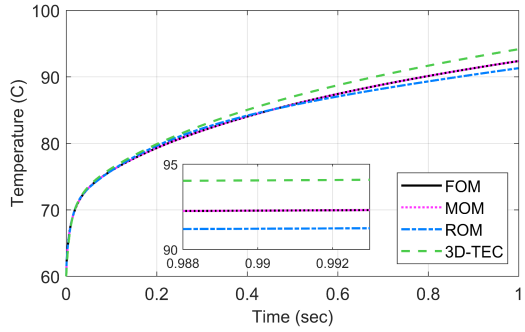


Fig. 9. MOSFET 1 chip temperature response obtained from FOM, MOM, and ROM of order 4 generated by the hybrid MOR method, and 3-D-TEC when a constant heat flux was applied on all four chips.

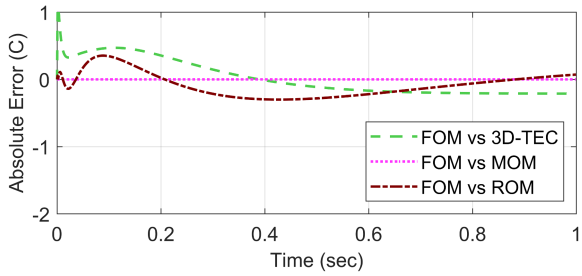


Fig. 10. Absolute error of MOSFET 1 chip temperature step response between FOM and 3-D-TEC, FOM, and MOM, and FOM to ROM of order 4 when a constant heat flux was applied on MOSFET 1 only.

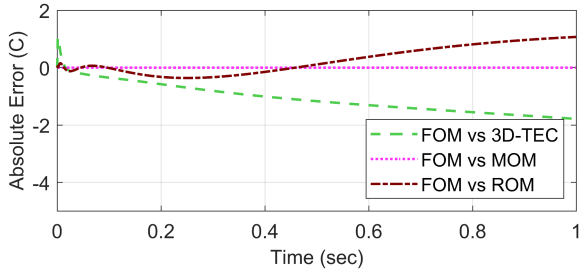


Fig. 11. Absolute error of MOSFET 1 chip stepped temperature response between FOM and 3-D-TEC, FOM, and MOM, and FOM to ROM of order 4 when a constant heat flux was applied on all four chips.

the MOSFET 1 chip material stack. The thermal impedance between a material layer and cross-coupled heat flux input was modeled using a Foster-type TEC with four *RC* pairs fitted to the corresponding FEA temperature step response. The thermal impedances between consecutive material layers in the MOSFET 1 chip material stack were modeled as Foster-type TECs with four *RC* pairs fitted to the differences between FEA temperature step responses between each consecutive pair of layers. Increasing the number of *RC* pairs used to create a Foster-type TEC resulted in higher fitting accuracy, until four, where additional *RC* pairs resulted in a negligible increase in fitting accuracy. Four *RC* pairs for each cross-coupled heat flux per material layer, four *RC* pairs for each material layer interface, and eight material layers resulted in 128 *RC* pairs inside the 3-D-TEC model for MOSFET 1.

Shown in Fig. 8 are the temperature step response profiles of MOSFET 1 for the FOM, MOM, ROM, and 3-D-TEC when a constant heat flux of 2 271 000 W/m$^2$K, equal to the maximum instantaneous heat flux value from MOSFET 1 in Fig. 3, was applied to the top of the MOSFET 1 chip. Shown in Fig. 9 are the results when all four chips had the same constant heat flux of 2 271 000 W/m$^2$K applied to demonstrate the temperature contributions of cross-coupled heat flux inputs. The chip temperature step response fluctuates with a temperature change of 21.5 °C in Fig. 8 when the constant heat flux is applied to MOSFET 1 only and with a temperature change of 32.3 °C in Fig. 9 when the constant heat flux is applied to all chips.

The solved temperature absolute error between the FOM and the 3-D-TEC, the FOM and the MOM, and the FOM and the ROM when the constant heat flux is applied to MOSFET 1 only and when the constant heat flux is applied to all chips can be seen in Figs. 10 and 11, respectively. The maximum absolute error for each step response case and comparison to the FOM can be seen in Table IV. Compared with the 3-D-TEC, the proposed hybrid MOR method shows a smaller maximum absolute error

TABLE IV
MAXIMUM ABSOLUTE ERROR OF TEMPERATURE STEP RESPONSE BETWEEN FOM AND 3-D-TEC, MOM, AND ROM

| Step Response | FOM vs 3-D-TEC (°C) | FOM vs MOM (°C) | FOM vs ROM (°C) |
|---|---|---|---|
| MOSFET 1 Only | 1.102 | 4.198e-11 | 0.353 |
| All Chips | 1.783 | 0.005 | 1.071 |

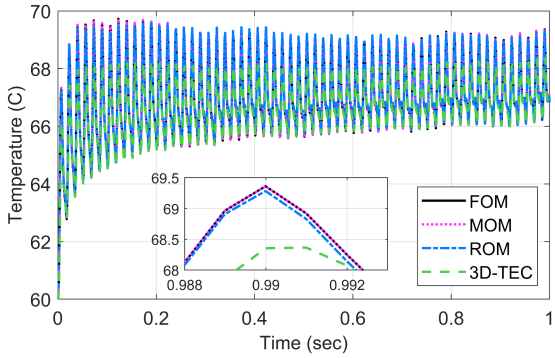


Fig. 12. MOSFET 1 chip temperature transient response obtained from FOM, MOM, and ROM of order 4 generated by the hybrid MOR method, and 3-D-TEC when the heat flux curve was applied for MOSFET 1 only.

of 0.353 °C, which is only 32.03% of that of 1.102 °C of the 3-D-TEC when the constant heat flux is applied to MOSFET 1 only. The proposed hybrid MOR method shows a smaller maximum absolute error of 1.071 °C, which is only 60.07% of that 1.783 °C of the 3-D-TEC when the constant heat flux is applied to all chips. This comparison shows that the proposed method is better than the 3-D-TEC to characterize the thermal coupling effect between chips in a power module during its operation. Note, the maximum absolute error between the FOM and MOM is only 4.198e-11 °C when the constant heat flux is applied to MOSFET 1 only and 0.005 °C when the constant heat flux is applied to all chips, indicating the error between the FOM and the MOM is negligible.

### *D. Comparison of Transient Response Results of Proposed Hybrid MOR Method and 3-D-TEC*

Shown in Fig. 12 are the temperature transient response profiles of MOSFET 1 for the FOM, MOM, ROM, and 3-D-TEC when the heat flux curve for MOSFET 1 in Fig. 3 was applied as the only input. Shown in Fig. 13 are the results when the heat flux curves for all four chips in Fig. 3 were applied as inputs to demonstrate the temperature contributions from cross-coupled heat flux inputs. The chip temperature transient response fluctuates between 66 °C and 69 °C. The temperature absolute error between the FOM and the 3-D-TEC, the FOM and the MOM, and the FOM and the ROM for the results in Figs. 12 and 13 are presented in Figs. 14 and 15, respectively. The maximum absolute error for each transient response case and comparison to the FOM can be seen in Table V. The proposed hybrid MOR method showed consistently less maximum absolute error than the 3-D-TEC for the chip temperature transient response of MOSFET 1. When the heat flux was only applied for MOSFET 1, the proposed method

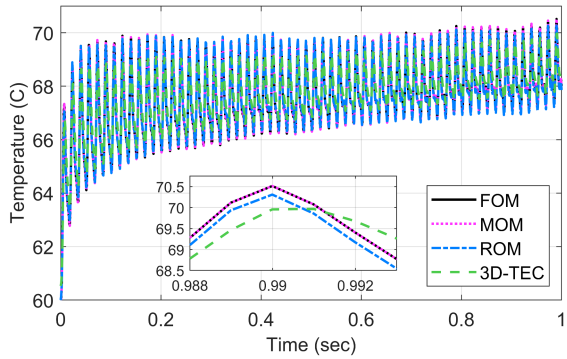


Fig. 13. MOSFET 1 chip transient temperature response obtained from FOM, MOM, and ROM of order 4 generated by the hybrid MOR method, and 3-D-TEC when the heat flux curves for all four chips were applied.

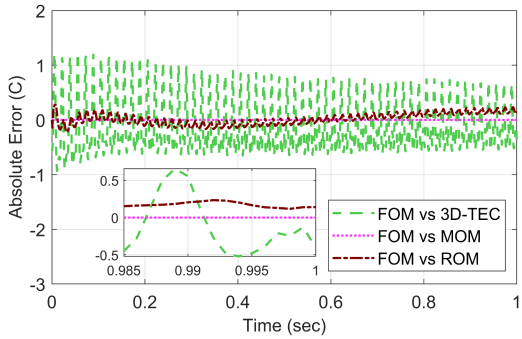


Fig. 14. Absolute error of MOSFET 1 chip temperature transient response between FOM and 3-D-TEC, FOM and MOM, and FOM and ROM of order 4 when the heat flux curve was applied for MOSFET 1 only.

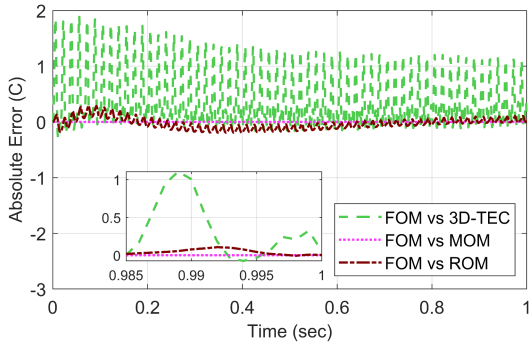


Fig. 15. Absolute error of MOSFET 1 chip transient temperature response between FOM and 3-D-TEC, FOM and MOM, and FOM and ROM of order 4 when the heat flux curves for all four chips were applied.

TABLE V
MAXIMUM ABSOLUTE ERROR OF TEMPERATURE TRANSIENT RESPONSE BETWEEN FOM AND 3-D-TEC, MOM, AND ROM

| Transient Response | FOM versus 3-D-TEC (°C) | FOM versus MOM (°C) | FOM versus ROM (°C) |
|---|---|---|---|
| MOSFET 1 Only | 1.907 | 3.272e-11 | 0.296 |
| All Chips | 1.227 | 0.004 | 0.280 |

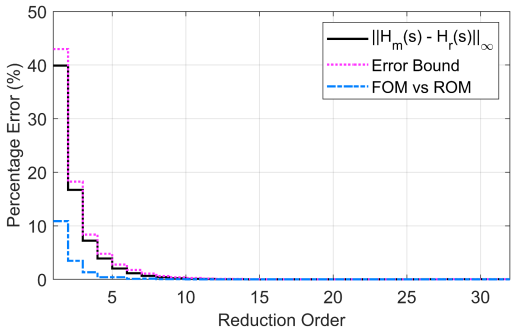


Fig. 16. Percentage error and error bound between MOM and ROM and between FOM and ROM of all four chips transient temperature response for reduction orders 1 through 32 using proposed hybrid MOR method.

showed a maximum absolute error of 0.296 °C, which is only 15.52% of that of 1.907 °C of the 3-D-TEC method. For the transient response with all heat flux curves applied this showed in a maximum absolute error of 0.280 °C for the proposed method, which is only 22.82% of that of 1.227 °C of the 3-D-TEC method. Note, the maximum absolute error between the FOM and MOM is only 3.272e-11 °C when only the heat flux curve for MOSFET 1 was applied and 0.004 °C when the heat flux curves for all four chips were applied, demonstrating that the error between the FOM and the MOM is negligible for transient heat flux inputs.

### *E. Error Bound Validation of Proposed Hybrid MOR Method*

A comparison between the percentage error of the ROM with respect to the MOM and the error bound calculated by (33) is given in Fig. 16 for reduction orders 1 through 32. The percentage error of the ROM is always less than or equal to the error bound, i.e., the sum of the truncated HSVs divided by the sum of all HSVs of the MOM when creating the ROM. The percentage error between the FOM and the ROM was obtained from the temperature transient response profiles of MOSFET 1 when the heat flux curves for all four chips in Fig. 3 were applied as inputs. The percentage error decreases as the reduction order increases and always stays below the error bound for reduction orders 1 through 32. Negligible error between the FOM and the MOM resulted in a maximum percentage error between the FOM and the ROM less than or equal to the error bound for reduction orders 1 through 32.

## IV. Experimental Validation

Experimental tests were conducted to further validate the proposed thermal modeling method. Fig. 17 shows the experimental setup schematic and Fig. 18 shows the equipment used in the experiment. A programmable dc power supply was used to provide test currents for heating the power module. An oscilloscope was used to measure the steady-state and transient electrical signals $I_{DS}$ and $V_{DS}$ of the power module. A function generator was used to provide a logic level square wave gate drive signal for MOSFET gate driver. Two dc power supplies were used to provide 20 V during turn-ON and –5 V during

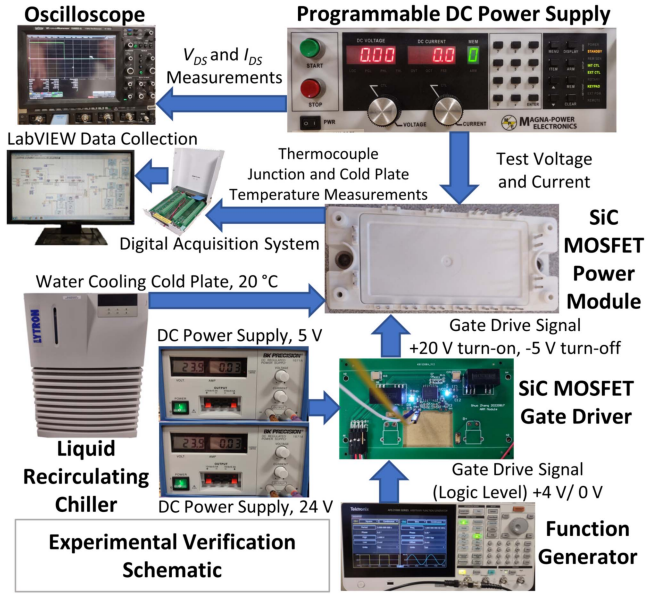


Fig. 17. Experimental setup schematic for validation of the proposed thermal modeling method.

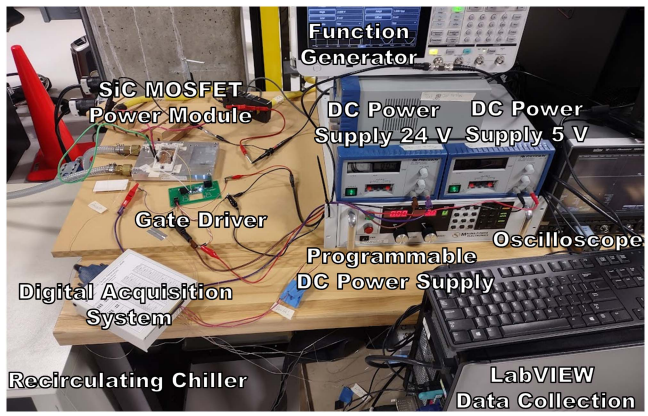


Fig. 18. Photograph of experimental setup.

turn-OFF to the gate driver for converting the logic level gate drive signal from the function generator to appropriate voltage levels for driving the gate of the MOSFET. Additionally, the gate driver provided electrical isolation for the function generator and power supplies. The power module was mounted to a cold plate with a thin layer of thermal paste applied between the bottom of the power module baseplate and the cold plate. The cold plate was connected to a liquid recirculating chiller set to maintain the inlet coolant temperature at 20 °C. Distilled water was used as the coolant. Tweezers were used to remove insulating silicone above the SiC MOSFET chip, and a type K 0.13 mm diameter thermocouple was attached to the center point of the top of the SiC MOSFET chip using a small amount of conductive silver paint for measuring the junction temperature, $T_j$. A second thermocouple was mounted on top of the cold plate coolant inlet and insulated with aluminium tape for measuring the cold plate temperature. A National Instruments data acquisition system was used for

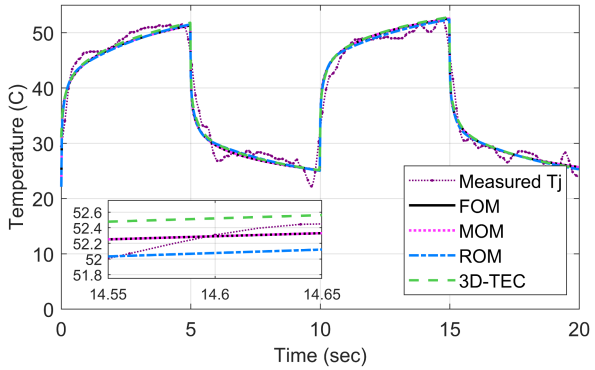


Fig. 19. Comparison between measured $T_j$ and $T_j$ obtained from FOM, MOM, ROM of order 4 generated by the hybrid MOR method, and 3-D-TEC of order 128 for on-state $I_{DS}$ of 40.1 A.

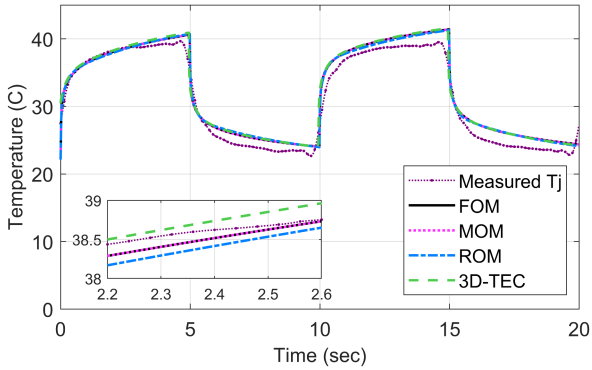


Fig. 20. Comparison between measured $T_j$ and $T_j$ obtained from FOM, MOM, ROM of order 4 generated by the hybrid MOR method, and 3-D-TEC of order 128 for on-state $I_{DS}$ of 31.9 A.

acquiring the temperatures measured using thermocouples in addition to a LabVIEW program for data collection.

Two power cycling tests to gradually heat and cool the SiC MOSFET module while monitoring the junction temperature were performed. A switching period of 10 s was used to generate a gate driver signal with a 50% duty cycle. Constant test currents of 40.1 A and 31.9 A from the programmable dc power supply were applied for the first and second tests, respectively, to the first SiC MOSFET transistor out of six total inside the power module. The on-state resistance, $R_{DS(\mathrm{on})}$, of the SiC MOSFET was calculated to be 0.039 Ω by measuring continuous drain current $I_{DS}$ and drain-to-source voltage $V_{DS}$ for multiple values of $V_{DS}$ with a set gate voltage $V_{GS}$ of 20 V. The value for $R_{DS(\mathrm{on})}$ was validated with the on-resistance figure provided by the power module datasheet using the measured peak junction temperature data during MOSFET conduction. This resulted in 62.96 W of power loss occurring at the SiC MOSFET for the first test and 39.69 W for the second test. The calculated on-state power loss, gate driver signal switching period, and average measured cold plate temperature of 22.1 °C were used as simulation inputs for the FOM, MOM, ROM, and 3-D-TEC for a 20 s simulation time length for both power cycling tests. The measured $T_j$ data had an adaptive degree Savitzky–Golay filter applied to it with a maximum polynomial degree of 9 to preserve the trends in the measured data while filtering out noise from the thermocouple sensors [47]. For each simulation model, $T_j$ was calculated and displayed alongside the measured $T_j$ in Fig. 19 for the first test and Fig. 20 for the second test.

Comparison results between the measured $T_j$ and calculated $T_j$ for the first test is displayed in Table VI. The mean absolute error between the measured $T_j$ and the calculated $T_j$ for the 3-D-TEC, MOM, and ROM was 1.21 °C, 1.27 °C, and 1.22 °C, respectively. The maximum $T_j$ during the second turn-ON state was 52.45 °C, and the difference between the maximum measured $T_j$ and the maximum calculated $T_j$ for the 3-D-TEC, MOM, and ROM was 0.37 °C, 0.13 °C, and −0.06 °C, respectively. The minimum measured $T_j$ during the second turn-OFF state was 23.89 °C and the difference between the minimum measured $T_j$ and the minimum calculated $T_j$ for the 3-D-TEC, MOM, and ROM during the second turn-OFF state was 1.62 °C, 1.81 °C, and 1.43 °C, respectively. These results demonstrate that the thermal models can predict the maximum and minimum temperatures of the power cycles while the mean absolute error is no more than 1.27 °C, which is within the temperature measurement error of ±2.20 °C provided by the type K thermocouple. These observations were further verified with the second test where the mean absolute error for each model was no more than 1.32 °C, and the largest absolute difference when predicting the maximum $T_j$ for the second turn-ON state or minimum $T_j$ for the second turn-OFF state for all models was below 1.89 °C, as shown in Table VII.

TABLE VI
METRIC COMPARISONS FOR MEASURED $T_j$ AND CALCULATED $T_j$ FROM 3-D-TEC, MOM, AND ROM FOR ON-STATE $I_{DS}$ OF 40.1 A

| Metric | Measured $T_j$ | 3-D-TEC | MOM | ROM |
|---|---|---|---|---|
| Mean Absolute Error (°C) | - | 1.21 | 1.27 | 1.22 |
| Maximum Temperature (°C) | 52.45 | 52.82 | 52.58 | 52.39 |
| Difference in Maximum Temperature (°C) | - | 0.37 | 0.13 | -0.06 |
| Minimum Temperature (°C) | 23.89 | 25.50 | 25.70 | 25.31 |
| Difference in Minimum Temperature (°C) | - | 1.62 | 1.81 | 1.43 |

TABLE VII
METRIC COMPARISONS FOR MEASURED $T_j$ AND CALCULATED $T_j$ FROM 3-D-TEC, MOM, AND ROM FOR ON-STATE $I_{DS}$ OF 31.9 A

| Metric | Measured $T_j$ | 3-D-TEC | MOM | ROM |
|---|---|---|---|---|
| Mean Absolute Error (°C) | - | 1.32 | 1.24 | 1.22 |
| Maximum Temperature (°C) | 39.66 | 41.55 | 41.40 | 41.28 |
| Difference in Maximum Temperature (°C) | - | 1.89 | 1.74 | 1.62 |
| Minimum Temperature (°C) | 22.81 | 24.26 | 24.39 | 24.14 |
| Difference in Minimum Temperature (°C) | - | 1.45 | 1.58 | 1.33 |

The comparison results of the computational complexity of the 3-D-TEC, MOM, and ROM are displayed in Table VIII. The 3-D-TEC was converted from a Simulink model to a generalized state-space representation in the form of (4) for comparison.

TABLE VIII
COMPUTATIONAL COMPLEXITY FOR 3-D-TEC, MOM, AND ROM

| Model | Order | Required Computational Memory (kB) | Mean Computation Time (sec) |
|---|---|---|---|
| MOM | 1000 | 16040 | 1.9696 |
| 3-D-TEC | 128 | 268.33 | 0.0333 |
| ROM | 4 | 0.352 | 0.0034 |

Each element in a system matrix of a state space system of equations was represented using a double data type according to IEEE Standard 754 for double precision, where each double uses 8 bytes to store a number in memory. The 3-D-TEC model had an order of 128 which required 268.33 kB to store in computational memory whereas the ROM had an order of 4, which required 0.352 kB to store in memory. This shows that the ROM only required 0.13% of the memory needed for the 3-D-TEC. To test the computational time required to solve each model, the transient simulation of 1000 time steps shown in Fig. 12 was solved 100 times. The computation time required to solve each simulation was recorded then all recorded times were averaged. The 3-D-TEC model required 0.0333 s on average to solve the simulation whereas the ROM required 0.0034 s on average. This shows that the ROM requires only 10.21% of the time needed to solve a simulation compared to the 3-D-TEC. Both models show similar mean absolute error when comparing their predicted junction temperature with the measured data, but the results show that the ROM is a more memory efficient model with a significantly reduced computation time compared to the 3-D-TEC.

## V. CONCLUSION

This study proposed a hybrid MOR method for modeling the thermal behavior of a SiC MOSFET power module with an ROM extracted automatically without any heuristic assumptions from an FOM generated by the FEA method. The proposed MOR thermal modeling method first used a block Krylov subspace projection approach for reducing the FOM to a MOM, then used the square-root method for balanced truncation to generate a final ROM with a much lower order number that is suitable for real-time applications. The ROM extracted by the proposed hybrid MOR method has a controllable approximation error bound with respect to the FOM where the order number of the ROM was determined by a chosen error bound using a mathematical relationship elaborated in the article. The proposed hybrid MOR method was applied for thermal modeling of a CREE CCS050M12CM2 all-SiC MOSFET power module in comparison with the block Arnoldi Iteration-based MOR method and a state-of-the-art 3-D-TEC thermal modeling method. The results showed that the time response average absolute error of using the proposed hybrid MOR was no more than 6.28% of that using the block Arnoldi Iteration to create an ROM of the same order. The lowest order ROM for a desired error bound was determined directly without trial and error and was verified through simulation. Compared to the 3-D-TEC method, the proposed method generated an ROM not only with a much lower order but also a much lower maximum absolute error. For example, the maximum absolute error of the chip temperature transient response of the SiC MOSFET power module obtained from an ROM of order 4 generated by the proposed method was less than 14% of that obtained from a 3-D-TEC model of order 128. Furthermore, experimental tests demonstrated an ROM of order 4 and a 3-D-TEC model of order 128 can predict SiC MOSFET junction temperature with a mean absolute error of no more than 1.32 °C, which is within the $\pm 2.20$ °C temperature measurement error provided by the thermocouple used in the tests, but the ROM only required 0.13% of the memory and 10.21% of the time needed for implementing the 3-D-TEC. In addition to SiC MOSFETs, the proposed method can be applied to generate high-fidelity, low-order thermal models with controllable error bounds for other types of semiconductor power modules.

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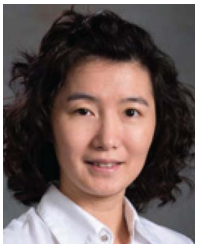
**Cameron Entzminger** (Member, IEEE) received the B.S. degree in computer engineering in 2016 from the University of Nebraska–Lincoln, Lincoln, NE, USA, where he is currently working toward the Ph.D. degree in electrical engineering.

He was a Software Engineering Intern with Garmin Ltd., Olathe, KS, USA, in 2016. He was a Data Analyst Intern with Bluestem Energy Solutions, Omaha, NE, USA, in 2017. He was an Algorithm Research Intern with Silicon Austria Labs, Villach, Austria, in 2021. His research interests include thermal modeling of power devices, condition monitoring, and model reduction techniques.

**Wei Qiao** (Fellow, IEEE) received the B.Eng. and M.Eng. degrees in electrical engineering from Zhejiang University, Hangzhou, China, in 1997 and 2002, respectively, the M.S. degree in high-performance computation for engineered systems from Singapore-MIT Alliance, Singapore, in 2003, and the Ph.D. degree in electrical engineering from Georgia Institute of Technology, Atlanta, GA, USA, in 2008.

Since 2008, he has been with the University of Nebraska–Lincoln, Lincoln, NE, USA, where he is currently the Clyde Hyde Professor of Electrical and Computer Engineering. He has authored or coauthored more than 280 papers in refereed journals and conference proceedings and holds 13 U.S. patents issued. His research interests include modeling, control, condition monitoring, and optimization of renewable energy systems, power electronic systems, electric motor drives, energy storage systems, electric vehicles, and electric power grids; decision making and risk management in the electricity markets with high penetrations of renewable energy; and electrical energy conversion devices.

Dr. Qiao was a recipient of the 2010 U.S. National Science Foundation CAREER Award and the recipient of the 2021 IEEE Power Electronics Society Sustainable Energy Systems Technical Achievement Award and the 2010 IEEE Industry Applications Society Andrew W. Smith Outstanding Young Member Award.



**Liyan Qu** (Senior Member, IEEE) received the B.Eng. (with the highest distinction) and M.Eng. degrees from Zhejiang University, Hangzhou, China, in 1999 and 2002, respectively, and the Ph.D. degree from the University of Illinois at Urbana–Champaign, Champaign, IL, USA, in 2007, all in electrical engineering.

From 2007 to 2009, she was an Application Engineer with Ansoft Corporation, Irvine, CA, USA. Since January 2010, she has been with the University of Nebraska−Lincoln, Lincoln, NE, USA, where she is currently an Associate Professor with the Department of Electrical and Computer Engineering. Her research interests include energy efficiency, renewable energy, numerical analysis and computer aided design of electric machinery and power electronic devices, dynamics and control of electric machinery, and magnetic devices.

Dr. Qu was a recipient of the 2016 U.S. National Science Foundation CAREER Award.

**Jerry L. Hudgins** (Fellow, IEEE) received the Ph.D. degree in electrical engineering from Texas Tech University, Lubbock, TX, USA, in 1985.

He was a member of faculty with the University of South Carolina, Columbia, SC, USA, until 2004. He has been the Chair wih the Electrical and Computer Engineering Department, University of Nebraska–Lincoln, Lincoln, NE, USA, since 2004. He was Interim Director of the Nebraska Center for Energy Sciences Research for 2019–2023, having also was an Associate Director for many years. He has authored ad coauthored more than 160 technical papers, books, and book chapters concerning power semiconductors, electronic packaging, power electronics, renewable energy systems, and engineering education. His research interests include power electronic device characterization and modeling, power electronics design, electronics packaging, and renewable energy systems.

Dr. Hudgins was named as an IEEE Third Millennium Medal recipient for "Outstanding Contributions in the area of Power Electronics," in 2000. He is a past member of the IEEE Board of Directors (Division II Director and IEEE Treasurer) and a current member of the IEEE Foundation Board of Directors. He was the President of the IEEE Power Electronics Society for the years of 1997 and 1998, and as President of the IEEE Industry Applications Society in 2003