An Improved Indirect Pulsewidth Modulation Technique for Modular Multilevel Converters

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***Abstract*—For a modular multilevel converter (MMC) operating in the medium-voltage range, carrier-based pulsewidth modulation (PWM) methods are good options for modulating the converter, as harmonic contents of the phase voltage/current can be centered around the carrier frequency and/or its multiples. However, in the relevant literature, arm voltage references are mostly normalized by the submodule (SM) capacitor voltage reference, leading to the so-called direct modulation, while the indirect modulation considering the capacitor voltage ripples receives much less attention. This article investigates the indirect modulation of MMCs, focusing on a specific PWM method where only two SMs per phase operate in PWM mode in each control period. It is found that the direct PWM (DiPWM) generates phase voltages/currents that contain high-amplitude low-order harmonics, while the indirect PWM (IndiPWM) presents well-suppressed low-order harmonics but significant distortions around the carrier frequency. The cause of the above problem of the IndiPWM is revealed theoretically through Fourier analysis, and a solution with simple implementation is developed by rearranging the switching pulses of the PWM-mode SMs. Both simulations and experiments are carried out. The results show that the proposed method combines the advantages of both DiPWM and IndiPWM, achieving low harmonic distortions simultaneously in the low frequency and around the carrier frequency.**

***Index Terms*—Harmonic analysis, modular multilevel converters (MMCs), pulsewidth modulation (PWM).**

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I. Introduction

THE modular multilevel converter (MMC) is an excellent option for medium- and high-voltage power conversion systems considering its modularity and scalability [1]. Fig. 1 shows the generic circuit of one converter phase of an MMC, consisting of the upper and lower arms. Each arm is composed of a number of (given by N) submodules (SMs) in series connection and an inductor for current buffering. As the fundamental building block of an MMC, each half-bridge SM is controlled by a pair of complementary gate signals to either insert the capacitor into or bypass it from the arm current path, forming a multilevel arm voltage and, therefore, phase voltage. Other SM topologies are also available, featuring enhanced functionality but increased number of power devices as well [2]. As N increases, the voltage and power rating of an MMC can be easily scaled up, bringing much convenience to its interconnections with medium/high-voltage systems while significantly improving the quality of the phase voltage/current.

The MMC was first proposed in 2001 [3]. During the last two decades, various aspects of the MMC have been extensively investigated, including the circuit topologies, control and modulation strategies, applications, etc. [1], [4], [5]. Regarding the modulation, the nearest level control (NLC) [6] is a widely adopted method for applications where a large number of SMs are required to reach high voltage rating. The implementation of the NLC is simple as the SM capacitor voltages in each arm can be well balanced through the conventional sorting-and-selecting procedures, and the phase voltage/current also presents high quality [7]. However, as N decreases, the performance of the NLC degrades due to the use of the rounding function when normalizing the arm voltage references [8].

Pulsewidth modulation (PWM) schemes serve as a proper choice for medium-voltage (MV) MMCs where N is not high [9]. With properly determined switching instants, the arm

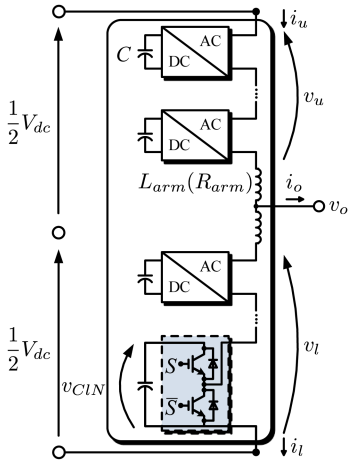

Fig. 1. Generic circuit of one phase of an MMC.

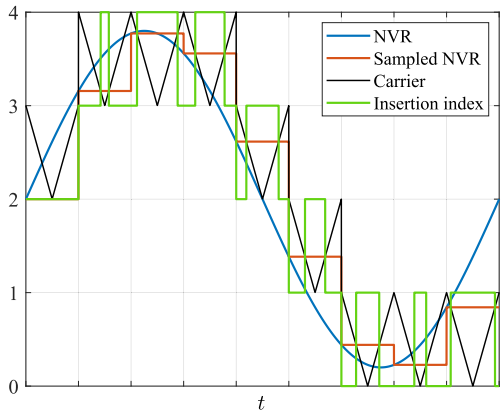

Fig. 2. Insertion-index determination for an arbitrary arm using the PWM method in [16] (NVR: normalized voltage reference).

voltages can be generated more accurately, and harmonic contents can be concentrated around the carrier frequency (denoted by f_c) and/or its multiples, being the main advantage of the PWM. Commonly used PWM techniques for MMCs are phase-shifted PWM (PS-PWM) [10], [11] and level-shifted PWM (LS-PWM) [12], [13], where each SM is equipped with a carrier, and the carriers of each arm are arranged with uniform interleaving in a horizontal and vertical manner, respectively. Comparative studies of both PWM schemes are presented in [14] and [15].

In addition, an efficient PWM technique is proposed in [16], where only one SM in each arm operates in PWM mode in each control period (thus, only one carrier per arm is required), while the switched-ON/OFF SMs and PWM-mode SM are determined through the sorting-and-selecting scheme. Compared with the conventional PS-PWM/LS-PWM alternatives, it features simpler implementation and is, thus, quite suitable for MV applications such as MV dc distribution grid, MV motor drives, etc. This PWM technique is further improved in terms of phase voltage quality through phase shift of one arm carrier [17]. Its harmonic characteristics are analyzed in [18] and [19], while Zhou et al. [19] study the influence of the phase shift between both arm carriers in the same phase on the phase voltage and circulating current harmonics. Performance evaluation for a wide range of N and f_c with comparison to the conventional NLC method is presented in [20]. The issue of switching frequency reduction (SFR) is also investigated in [21]. However, in all the above works, the arm voltage references are normalized by the reference value of SM capacitor voltages. Such an implementation is called direct modulation [22]. Due to the neglecting of capacitor voltage ripples, the resulted insertion indices of the direct PWM (DiPWM) are inaccurate and may cause performance degradation [23], [24]. In comparison, the indirect PWM (IndiPWM) considering the actual capacitor voltage values generates more accurate insertion indices but is adopted and studied in much fewer works [22].

This article investigates the IndiPWM for MV MMCs. It is revealed through harmonic analysis that the IndiPWM presents much higher phase voltage distortions around the carrier frequency (referred to as CF distortions) than the DiPWM, though the low-frequency (LF) harmonics are well suppressed. Such high CF harmonic distortions would cause undesirable consequences in MV applications, e.g., increased losses in MV distribution grids, high-frequency resonance in MMC-MVDC systems, performance degradation in MV motor systems, etc. To address this issue, an improved IndiPWM (I-IndiPWM) is proposed, which rearranges the switching pulses (SPs) of both PWM-mode SMs in the same phase to mitigate the CF harmonic distortions in the phase voltage, while maintaining low LF distortions.

The rest of this article is organized as follows. Section II reviews the conventional PWM technique with direct and indirect modulations. Section III describes the proposed IndiPWM scheme, followed by Section IV introducing an improved version of the proposed method with reduced switching frequency. Sections V and VI provide the simulation and experimental validations, respectively. Finally, Section VII concludes this article.

II. Conventional PWM Method With Direct and Indirect Modulations

A. Conventional PWM Method

To explain the idea of the PWM method investigated in this article [16], Fig. 2 provides an example of the modulating waveforms for an arbitrary arm. Here, the ac fundamental frequency is configured only a bit lower than f_c for a better comprehension of the concept. With the arm voltage references v_y^* (subscript $y = u, l$ denotes upper and lower arm, respectively) given by dedicated controllers (e.g., phase current controller and circulating current controller [25]), the arm insertion index can be obtained through normalization

$$N_y = \frac{v_y^*}{V_C} \tag{1}$$

where V_C denotes the reference value of SM capacitor voltage, and it equals $V_{\rm dc}/N$. floor(N_y) gives the number of SMs to be switched ON in the entire carrier period, while the fractional part

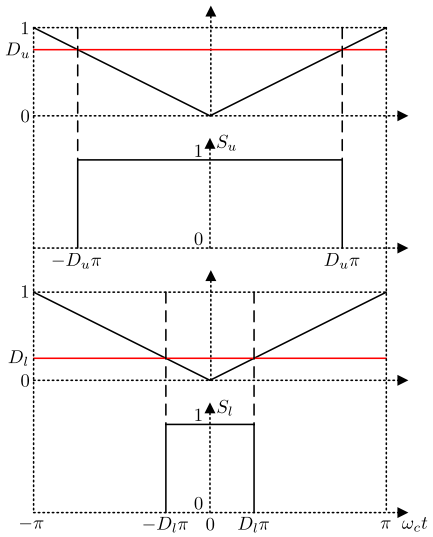

Fig. 3. Modulation of both PWM-mode SMs in one phase.

gives the duty ratio of the PWM-mode SM as

$$D_y = N_y - \text{floor}(N_y). \tag{2}$$

The switched-ON SMs are selected through the sorting-and-selecting scheme as the NLC modulation, while the PWM-mode SM is selected as the SM next to the switched-ON SMs on the sorting list. It should be noted that the resulted insertion index in Fig. 2 is the same as the LS-PWM technique [12]. The only difference is on the SM-and-gate-signal assignations. Throughout this article, the PWM schemes under investigation adopt a carrier period equal to the sampling and control period, and the single-edge regular sampling is employed with the samplings conducted at the beginning of each period.

Regarding carrier selection, as revealed in [17], using identical carriers in both arms of the same phase (as shown in Fig. 3) results in the best harmonic performance in terms of phase voltage. Thus, actually, only one carrier is required for each phase.

B. DiPWM and IndiPWM

The DiPWM and IndiPWM are differentiated by how the arm voltage reference v_y^* is normalized [22]. The DiPWM normalizes v_y^* by V_C as (1), while the IndiPWM uses the actual SM capacitor voltage for normalization as

$$N_y = \frac{v_y^*}{v_{Cy}} \tag{3}$$

where v_{Cy} is the mean value of the SM capacitor voltages of the corresponding arm, assuming that they are well balanced. As the capacitor voltage ripples are considered, the resulted insertion indices of the IndiPWM are more accurate, especially when v_{Cy} presents high ripples. It is worth noting that using v_{Cy}, the SM capacitor voltages may not be well stabilized. This issue can be overcome through extra control loops [24] or open-loop estimation of v_{Cy} [26].

C. Limitation of IndiPWM

Though the IndiPWM features high accuracy, the phase voltage (and therefore phase current) of the MMC will present increased CF harmonic distortions than using the DiPWM. To elaborate this point, Fourier analysis is conducted to the generated SPs (S_y) shown in Fig. 3, as the technique used in [27]. Specifying the carrier frequency ($f_c = \frac{\omega_c}{2\pi}$) as the fundamental frequency, S_y can be expanded into Fourier series as

$$\widetilde{S}_y = D_y + \sum_{h=1}^{\infty} \underbrace{\frac{2}{h\pi}\sin(h\pi D_y)}_{\widetilde{D}_{yh}} \cos(h\omega_c t). \tag{4}$$

Applying the PWM scheme as illustrated in Fig. 2, considering (2)–(4) and the MMC phase circuit in Fig. 1, the phase voltage can be expressed as

$$v_o = \frac{v_l - v_u}{2} = \frac{v_{Cl}}{2}\left(N_l + \sum_{h=1}^{\infty}\widetilde{D}_{lh}\right) - \frac{v_{Cu}}{2}\left(N_u + \sum_{h=1}^{\infty}\widetilde{D}_{uh}\right) \tag{5}$$

where the voltage drops on arm inductors are neglected for simplicity. Apparently, the phase voltage harmonics stem from the terms

$$\widetilde{v}_o = \frac{1}{2}\sum_{h=1}^{\infty}(v_{Cl}\widetilde{D}_{lh} - v_{Cu}\widetilde{D}_{uh}). \tag{6}$$

Here, an emphasis is put on the most significant term when $h = 1$, which can be derived considering (4) as

$$\begin{aligned}\widetilde{v}_{o1} &= \frac{v_{Cl}}{2}\widetilde{D}_{l1} - \frac{v_{Cu}}{2}\widetilde{D}_{u1} \\ &= \frac{1}{\pi}[v_{Cl}\sin(\pi D_l) - v_{Cu}\sin(\pi D_u)]\cos(\omega_c t)\end{aligned} \tag{7}$$

and this harmonic term is located at f_c.

In the DiPWM using (1), it can be inferred that

$$D_u + D_l = 1 \tag{8}$$

as v_u^* and v_l^* (and thus N_u and N_l) are always complementary neglecting the voltage adjustments from circulating current controller, which are relatively trivial [16], [17]. Considering that the capacitor voltage ripples are normally negligible compared to the rated value such that

$$v_{Cu} \approx v_{Cl} \approx V_C \tag{9}$$

it can be concluded according to (7) that $\widetilde{v}_{o1}$ under the DiPWM equals zero.

However, if the IndiPWM using (3) is applied, the relationship in (8) does not hold anymore. As a result, $\widetilde{v}_{o1}$ cannot be neglected. Furthermore, coupling with the LF components in the MMC system, significant phase voltage (and therefore phase current) harmonic distortions may appear around f_c, as will be verified in Sections V and VI.

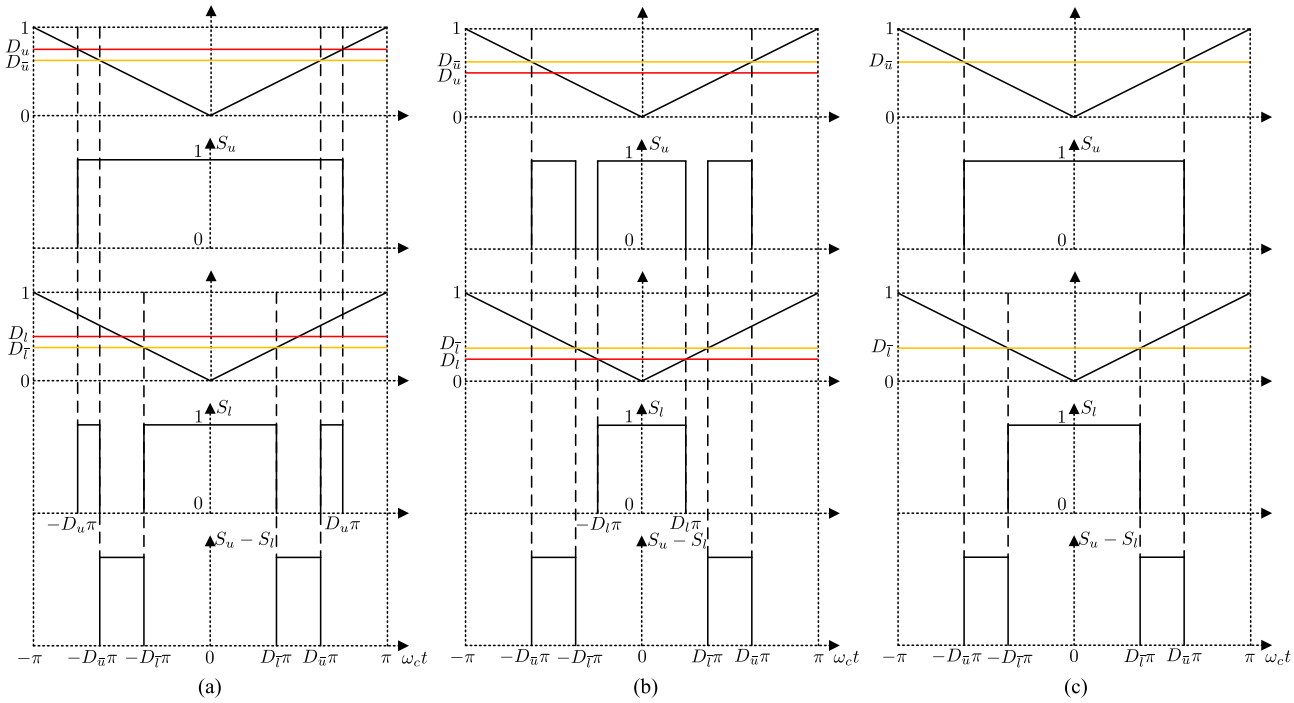

Fig. 4. Principles of the proposed I-IndiPWM. (a) I-IndiPWM when $D_u + D_l > 1$. (b) I-IndiPWM when $D_u + D_l < 1$. (c) Equivalent DiPWM.

III. Proposed I-IndiPWM

A. Switching Pulse Rearrangement

To resolve the abovementioned issue of the IndiPWM, an I-IndiPWM is proposed in this section. Basically, the idea is to rearrange the SPs in Fig. 3 such that the resulted SPs of $S_u - S_l$ are equivalent to the DiPWM, as illustrated in Fig. 4. Here, two cases of the IndiPWM need to be discussed, i.e., $D_u + D_l > 1$ and $D_u + D_l < 1$, as shown in Fig. 4(a) and (b), respectively.

1) When $D_u + D_l > 1$: As illustrated in Fig. 4(a), the proposed technique alters the SPs of both PWM-mode SMs of the original IndiPWM with duty cycles D_y (represented by the red curves): the SP corresponding to the larger duty cycle (between D_y) remains unchanged, while the other SP is decomposed into three portions, considering

$$D_{\bar{y}} = D_y - D_\delta \tag{10}$$

where

$$D_\delta = \frac{1}{2}(D_u + D_l - 1). \tag{11}$$

The two narrow pulses with equal width on both ends are the common-mode components of S_y, which are canceled out when both arm voltages form the phase voltage as (5). Here, $S_u - S_l$ is investigated as plotted in Fig. 4 to reflect the profile of phase voltage CF distortions. As a result, the generated phase voltage is equivalent to the DiPWM with duty cycles $D_{\bar{y}}$ (represented by the yellow curves). The equivalent DiPWM is illustrated in Fig. 4(c), which shows identical SPs of $S_u - S_l$ to the proposed technique in Fig. 4(a).

2) When $D_u + D_l < 1$: As illustrated in Fig. 4(b), the proposed technique alters the SPs of the original IndiPWM in a different way from the previous case: the SP corresponding to the smaller duty cycle (between D_y) remains unchanged, while the other SP is decomposed into three portions. The common-mode components of S_y in this case are the two intervals with equal width between the three pulses of S_u, which are canceled out when both arm voltages form the phase voltage. Therefore, similar to the previous case, the generated phase voltage is also equivalent to the DiPWM illustrated in Fig. 4(c) with duty cycles $D_{\bar{y}}$.

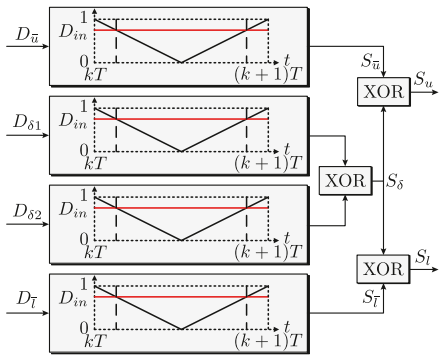

Fig. 5. Implementation diagram of the proposed I-IndiPWM.

B. Implementation and Features

The implementation diagram of the proposed method is provided in Fig. 5. All of the four PWM blocks are identical except for the duty ratio inputs. The same triangular carrier is used, and thus, only one carrier per phase is required. $[kT, (k+1)T]$ (k is an integer) denotes an arbitrary sampling/control/carrier interval

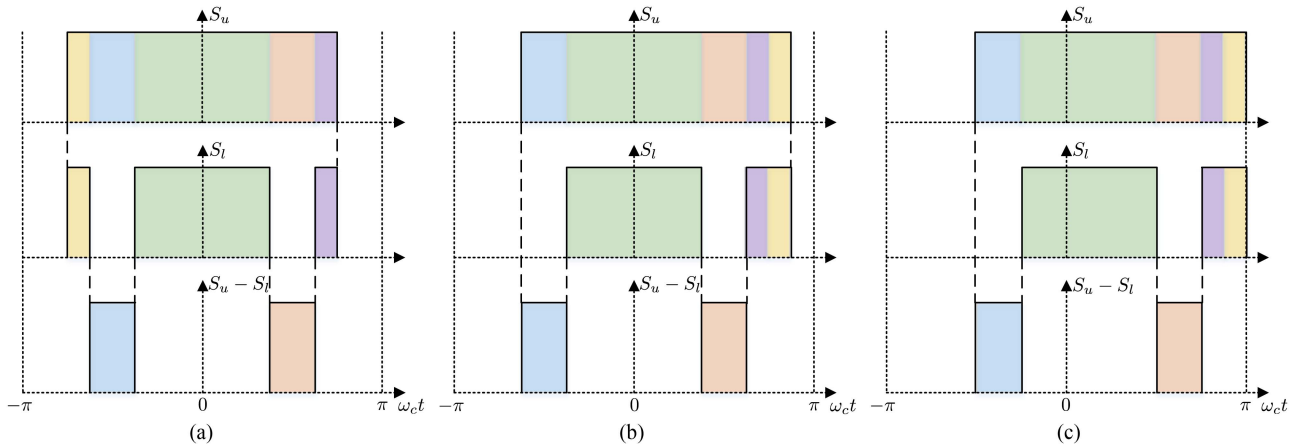

Fig. 6. Principle of the I-IndiPWM-SFR when $D_u + D_l > 1$. (a) I-IndiPWM. (b) Intermediate step. (c) I-IndiPWM-SFR.

TABLE I
VALUES OF f_{swb} FOR DIFFERENT PWM SCHEMES

Method	DiPWM	IndiPWM	I-IndiPWM	I-IndiPWM-SFR
f_{swb}	$2f_c/N$	$2f_c/N$	$4f_c/N$	$2.25f_c/N$

with a period of T. D_{in1} and D_{in2} are given as

$$D_{\delta 1} = \begin{cases} \text{Max}(D_u, D_l), & D_u + D_l > 1 \\ \text{Min}(D_u, D_l), & D_u + D_l < 1 \end{cases} \tag{12}$$

$$D_{\delta 2} = D_{\delta 1} - D_\delta \tag{13}$$

where Max and Min are the functions that output the maximum and minimum of the input arguments, respectively.

In every carrier interval, S_δ (corresponding to the common-mode components discussed previously) is determined first by logical operation XOR using the outputs of the two PWM blocks in the middle. Then, S_δ performs the XOR operation with both SPs of the original IndiPWM, leading to the new SPs of the proposed method. Since only logical operations and value comparisons are involved in Fig. 5, the proposed method can be well implemented on a field-programmable gate array (FPGA), and the desired SPs can be obtained instantaneously.

It can be inferred from (10) and (11) that

$$D_{\bar{u}} + D_{\bar{l}} = 1 \tag{14}$$

similar to (8). Thus, the proposed I-IndiPWM should present low CF harmonic distortions, similar to the DiPWM. It is worth noting that the average voltage output by each PWM-mode SM during the carrier period remains unchanged by the proposed technique. Thus, the merits of the original IndiPWM, i.e., higher accuracy of insertion-index determination and lower LF harmonic distortion, should be kept.

IV. I-INDIPWM WITH SFR

A. Reducing the Switching Frequency of I-IndiPWM

Though the proposed I-IndiPWM features salient harmonic characteristics, the switching frequency could be higher than the conventional IndiPWM and DiPWM too. To gain an insight into the switching frequency f_{sw} (averaged value of all the switching devices in one phase), the switchings are divided into two parts, i.e., the switchings at and between sampling instants, the corresponding switching frequencies of which are denoted as f_{swa} and f_{swb}, respectively. Apparently, f_{swb} is proportional to the carrier frequency f_c, and its values for different PWM methods are summarized in Table I. The proposed I-IndiPWM presents an f_{swb} twice that of the conventional DiPWM and IndiPWM, resulting in higher switching losses especially when N is low.

To resolve the above issue, an improved version of the proposed technique is developed with SFR. To explain the proposed I-IndiPWM-SFR scheme, Fig. 6 illustrates how the I-IndiPWM case shown in Fig. 4(a) ($D_u + D_l > 1$) is equipped with SFR. For differentiation, different pulse areas are filled with shade of different colors. As the first step, the two common-mode SPs (with yellow and purple shade) corresponding to S_δ are arranged in the same side adjacent to each other, as shown in Fig. 6(b). Through such an operation, two switchings between sampling instants are avoided, while $S_u - S_l$ remains unchanged; thus, the phase voltage is unaffected. Then, all of the SPs are phase-shifted to the far right of the carrier period, as shown in Fig. 6(c). In this way, two more switchings between sampling instants can be avoided, while whether extra switchings at sampling instants are generated depends on the switching states of the corresponding SMs during the next carrier period. For example, if both SMs in Fig. 6(c) are completely switched ON during the next period, no extra switchings are produced. It should be noted that through the above phase-shift operation, $S_u - S_l$ is phase-shifted too. However, it does not influence the amplitude of $\widetilde{v}_{o1}$ derived in (7). Thus, the harmonic performance of the I-IndiPWM-SFR should be comparable to the I-IndiPWM. Similarly, Fig. 7 illustrates the I-IndiPWM-SFR technique for the case when $D_u + D_l < 1$.

The value of f_{swb} for the I-IndiPWM-SFR scheme shown in Figs. 6(c) and 7(c) are $2f_c/N$ and $2.5f_c/N$, respectively. Thus, f_{swb} of the proposed I-IndiPWM-SFR method is given as $2.25f_c/N$, which is much lower than the I-IndiPWM and only slightly higher than the original IndiPWM. Since f_{swb} is only related to one SM per arm, the corresponding increase

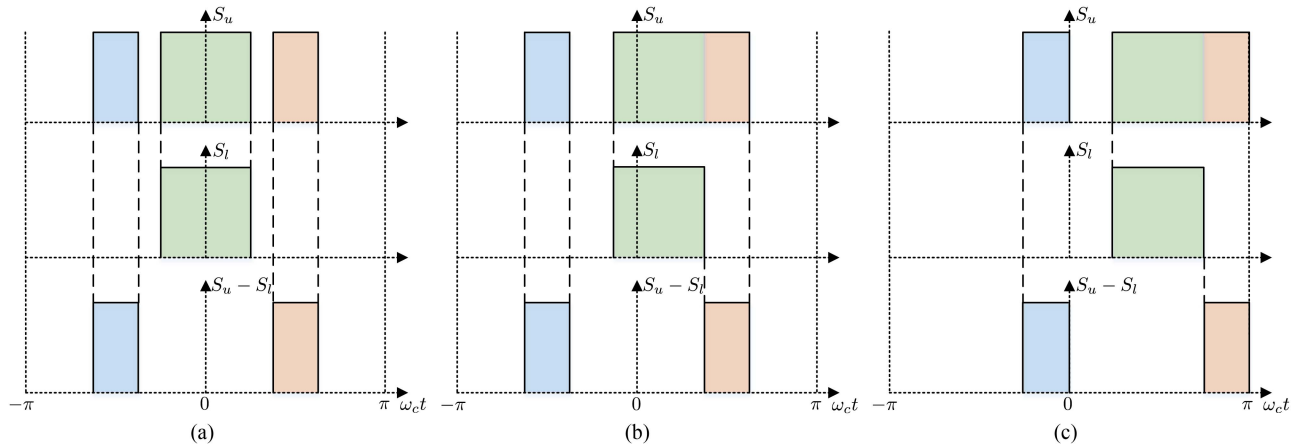

Fig. 7. Principle of the I-IndiPWM-SFR when $D_u + D_l < 1$. (a) I-IndiPWM. (b) Intermediate step. (c) I-IndiPWM-SFR.

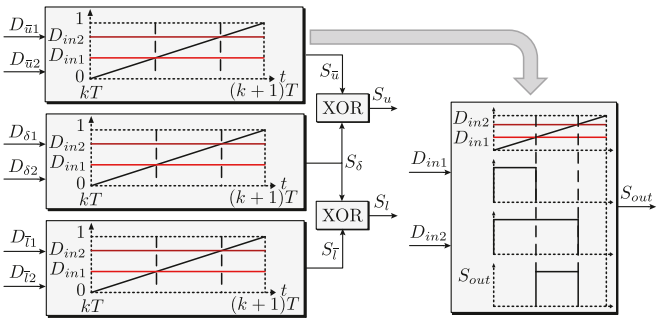

Fig. 8. Implementation diagram of the proposed I-IndiPWM-SFR.

of the overall average switching frequency of the proposed technique is further limited (divided by N). In terms of the switchings at sampling instants, it is difficult to conclude which PWM alternative achieves lower f_{swa} than the others. Thus, the proposed I-IndiPWM-SFR scheme should present comparable or only slightly higher overall switching frequency than the original IndiPWM. It should be noted that there exist many SFR methods in the literature [20], [21], [25] that can reduce f_{swa} while maintaining the system performance, which can be applied independently of the proposed techniques. Thus, the overall switching frequency can be easily regulated to meet certain requirements in real applications, and the slight increase of f_{swb} of the proposed I-IndiPWM-SFR is not a critical issue considering the significant performance enhancement it brings.

B. Implementation of I-IndiPWM-SFR

To implement SPs with asymmetry and phase shift, one possible option is to employ triangular carriers with time-varying phase shifts [27]. However, multiple carriers would be required for such an implementation of the proposed method, increasing the complexity. Fig. 8 provides the implementation diagram of the proposed I-IndiPWM-SFR method. Only one sawtooth carrier is required for each phase. For each PWM block, the two input duty ratios D_{in1} and D_{in2} (corresponding to the start and end of an SP) are, respectively, compared with the carrier, and the XOR operation is performed to the results. In this way, an SP with an arbitrary phase shift is implemented.

To determine the input duty ratios of different PWM blocks, the first step is to calculate the duty ratio corresponding to the symmetry axis between both SPs of $S_u - S_l$ as

$$D_{\text{mid}} = \begin{cases} 1 - \frac{1}{2}\text{Max}(D_{\bar{u}}, D_{\bar{l}}) - D_\delta, & D_u + D_l > 1 \\ 1 - \frac{1}{2}\text{Max}(D_{\bar{u}}, D_{\bar{l}}), & D_u + D_l < 1 \end{cases}. \tag{15}$$

Then, the following input duty ratios can be obtained:

$$\begin{cases} D_{\bar{y}1} = D_{\text{mid}} - \frac{1}{2}D_{\bar{y}} \\ D_{\bar{y}2} = D_{\text{mid}} + \frac{1}{2}D_{\bar{y}} \end{cases} \tag{16}$$

$$D_{\delta 1}, D_{\delta 2} = \begin{cases} 1 - D_\delta, 1, & D_u + D_l > 1 \\ \frac{1}{2} - D_\delta, \frac{1}{2}, & D_u + D_l < 1 \end{cases}. \tag{17}$$

It should be noted that the scheme in Fig. 8 can also be implemented efficiently using the FPGA, similar to the scheme in Fig. 5.

V. Simulation Validations

To validate the effectiveness of the proposed I-IndiPWM and I-IndiPWM-SFR methods, several simulations are conducted in MATLAB/Simulink. A single-phase MMC with the ac output terminal feeding an RL load is investigated, the detailed parameters of which are provided in Table II.

Fig. 9 shows the steady-state performance of different PWM schemes in terms of phase voltage and its harmonic spectrum. The system operates in open loop for simplicity. For comparison, the conventional DiPWM and IndiPWM are also evaluated. Coinciding with the previous analysis, the DiPWM presents high amplitude of LF harmonics. Theoretically, CF harmonics should be canceled out between both arms when forming the phase voltage [15]. Here, the CF distortions in Fig. 9(b) are induced by the capacitor voltage ripples [17] that violate condition (9). The conventional IndiPWM shows much better suppressed LF harmonics but higher CF distortions. In comparison, the proposed I-IndiPWM exhibits good harmonic performance in the entire investigated frequency range (up to the 50th harmonic). In

TABLE II
PARAMETERS OF THE MMC-BASED SYSTEMS UNDER STUDY

Parameter	Value in	
	Simulation	Experiment
Number of SMs per arm, N	10	4
SM capacitance, C	2 mF	0.41 mF
Arm inductance, L_{arm}	3.4 mH	4 mH
Arm resistance, R_{arm}	0.5 Ω	0.5 Ω
DC-link voltage, V_{dc}	10 kV	200 V
Load inductance, L	10 mH	10 mH
Load resistance, R	50 Ω	30 Ω
Modulation index, M	0.9	0.9
AC frequency, f	50 Hz	50 Hz
Carrier frequency, f_c	2 kHz	4 kHz

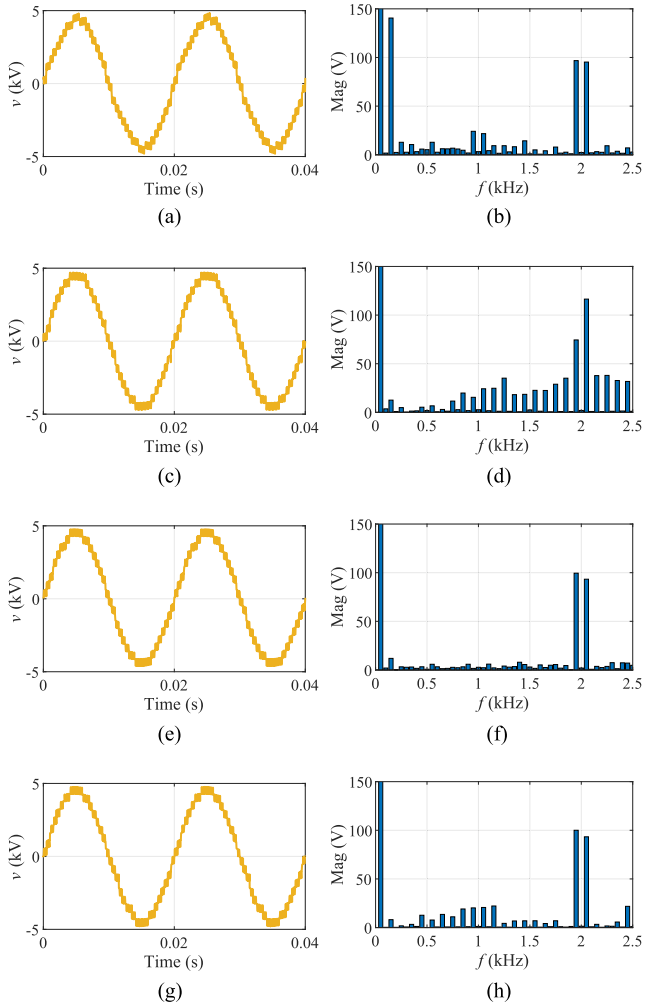

Fig. 9. Simulation results: phase voltage and its harmonic spectrum. (a) and (b) DiPWM. (c) and (d) IndiPWM. (e) and (f) I-IndiPWM. (g) and (h) I-IndiPWM-SFR.

Fig. 9(h), the overall harmonic distortions are slightly increased compared with the I-IndiPWM, due to the SP irregularity introduced by the phase-shift operation. However, generally, the I-IndiPWM-SFR maintains the good harmonic performance of

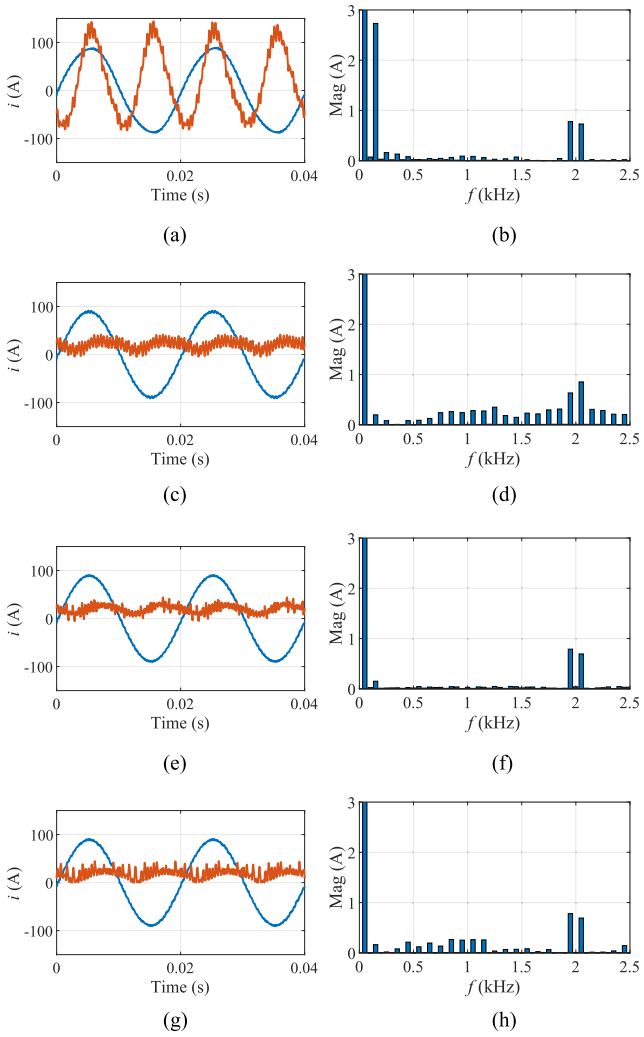

Fig. 10. Simulation results: phase current (blue), its harmonic spectrum and circulating current (red). (a) and (b) DiPWM. (c) and (d) IndiPWM. (e) and (f) I-IndiPWM. (g) and (h) I-IndiPWM-SFR.

the I-IndiPWM, and it outperforms the conventional DiPWM and IndiPWM.

Fig. 10 shows the phase current, its harmonic spectrum, and the circulating current. In general, the phase current presents similar harmonic profile to the phase voltage except for the enlarged low-order distortions due to the low-pass effect of the load inductance. The DiPWM presents much higher circulating current than the three IndiPWM schemes, thus highlighting the advantage of the more accurate IndiPWM alternative. The three IndiPWM schemes show distinct waveforms of circulating current, but comparable peak-to-peak ripples.

For a quantitative analysis, various total harmonic distortion (THD) indices of phase voltage in the above simulations are calculated, as summarized in Table III. The weighted THD (WTHD) is also calculated, which scales down the amplitude of each considered harmonic by its corresponding order, thus assigning heavier weights to the more important lower order harmonics. The subscripts denote the maximum or minimum/maximum harmonic order considered by the index. WTHD_{20} and $\text{THD}_{30,50}$ evaluate the LF and CF harmonic

TABLE III
THD AND WTHD (%) VALUES OF PHASE VOLTAGE OF DIFFERENT PWM SCHEMES IN SIMULATIONS

Method	THD_{50}	$WTHD_{50}$	$WTHD_{20}$	$THD_{30,50}$
DiPWM	4.57	1.067	1.064	3.10
IndiPWM	3.95	0.154	0.113	3.68
I-IndiPWM	3.11	0.124	0.096	3.08
I-IndiPWM-SFR	3.30	0.119	0.084	3.11
I-IndiPWM-SFR-1	3.33	0.118	0.081	3.11

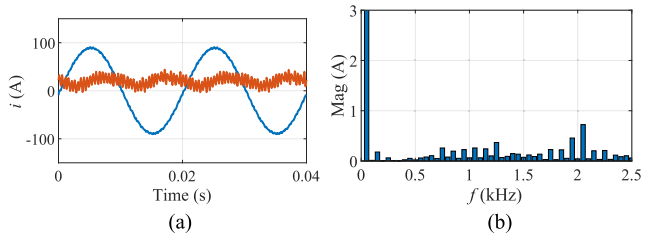

Fig. 11. Simulation results of IndiPWM with ac-side inductance increased by 30%. (a) Phase current (blue) and circulating current (red). (b) Phase current spectrum.

distortions, respectively. As shown in Table III, both proposed schemes present much better overall harmonic performance with lower THD/WTHD values than the conventional alternatives, and generally, the performance of the I-IndiPWM and I-IndiPWM-SFR are comparable.

As can be observed from the above results, the proposed technique leads to lower distortion in phase voltage and consequently in phase current, therefore improving the power quality. To achieve this effect with the conventional PWM alternatives, higher hardware costs would be required. As an example, to achieve comparable THD_{50} of phase current to the I-IndiPWM-SFR (which is 1.39%), the ac-side inductance of the IndiPWM in the above test has to increase by 30%, the results of which are shown in Fig. 11, with the THD_{50} value decreased from 1.68% to 1.40%. Nevertheless, higher inductance also means larger volume and higher expenditure of the hardware.

The average device switching frequency of the four methods are 775, 779, 1151, and 865 Hz, respectively. Compared with the I-IndiPWM, the proposed SFR technique reduces the switching frequency significantly by 25%. Compared with the conventional DiPWM and IndiPWM, the proposed I-IndiPWM-SFR presents around 11% higher switching frequency. As commented in Section IV, this is not a significant issue since the overall switching frequency can be easily lowered through modified capacitor voltage balancing methods that reduce f_{swa} as [20], [21], [25]. To exemplify this point, the proposed I-IndiPWM-SFR with further reduced f_{swa} (referred to as I-IndiPWM-SFR-1) is implemented, where the already switched-ON SMs are more likely to maintain their switching states during the sorting-and-selecting process [20]. The consequent switching frequency is 770 Hz, which is comparable to the conventional DiPWM and IndiPWM. The results are illustrated in Fig. 12, with various THD/WTHD values of the phase voltage given in Table III, which are very similar to the original I-IndiPWM-SFR technique.

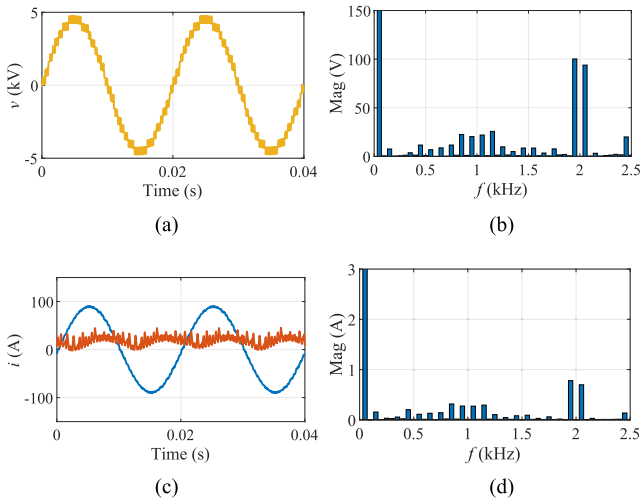

Fig. 12. Simulation results of I-IndiPWM-SFR-1 with further reduced f_{swa}. (a) Phase voltage. (b) Phase voltage spectrum. (c) Phase current (blue) and circulating current (red). (d) Phase current spectrum.

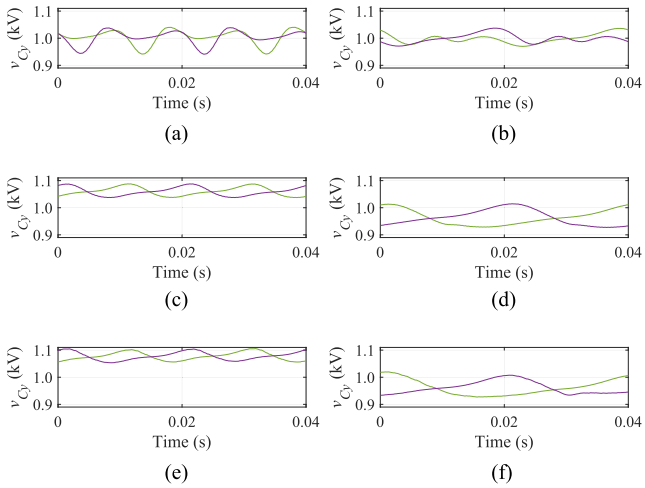

Fig. 13. Simulation results: average SM capacitor voltages of the upper/lower arms (green/purple). (a) DiPWM, 50 Hz. (b) DiPWM, 25 Hz. (c) IndiPWM, 50 Hz. (d) IndiPWM, 25 Hz. (e) I-IndiPWM-SFR, 50 Hz. (f) I-IndiPWM-SFR, 25 Hz.

It is well known that when the MMC operates at low ac frequency, SM capacitor voltages present large fluctuations, which bring in more harmonic distortions to the system [1]. To validate the effectiveness of the proposed technique in such a scenario, the above tests are conducted with the ac frequency of the MMC halved to 25 Hz. The average SM capacitor voltages of the upper/lower arms of different cases are illustrated in Fig. 13. It can be observed that the IndiPWM and I-IndiPWM-SFR show similar profile in both the scenarios, including the slight deviations of dc components of capacitor voltages to the reference value as the system operates in open loop with no extra regulation for arm capacitor voltages. Generally, the capacitor voltage ripples increase significantly as the ac frequency halves, except for the DiPWM showing apparent influences from the LF harmonics in the system, with much higher capacitor voltage ripples at 50 Hz but attenuated fluctuations at 25 Hz as a fourth harmonic is induced (which is a coincidence for the specific

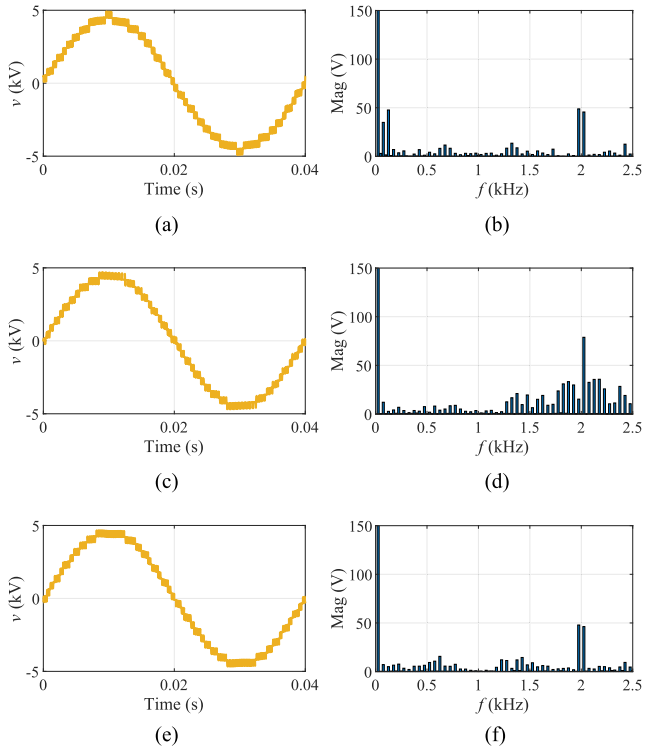

Fig. 14. Simulation results when the fundamental frequency is halved to 25 Hz: phase voltage and its harmonic spectrum. (a) and (b) DiPWM. (c) and (d) IndiPWM. (e) and (f) I-IndiPWM-SFR.

Fig. 15. Experimental MMC setup with an RTU-BOX204 controller (the top enclosure).

system configuration). The performances of different PWM alternatives at 25 Hz are illustrated in Fig. 14. Similar to the previous case of 50 Hz, the proposed I-IndiPWM-SFR is still able to combine the low-CF-distortion feature of the DiPWM and low-LF-distortion feature of the IndiPWM.

VI. Experimental Validations

For experimental validations, a single-phase MMC setup is employed, as shown in Fig. 15, with the above-studied PWM

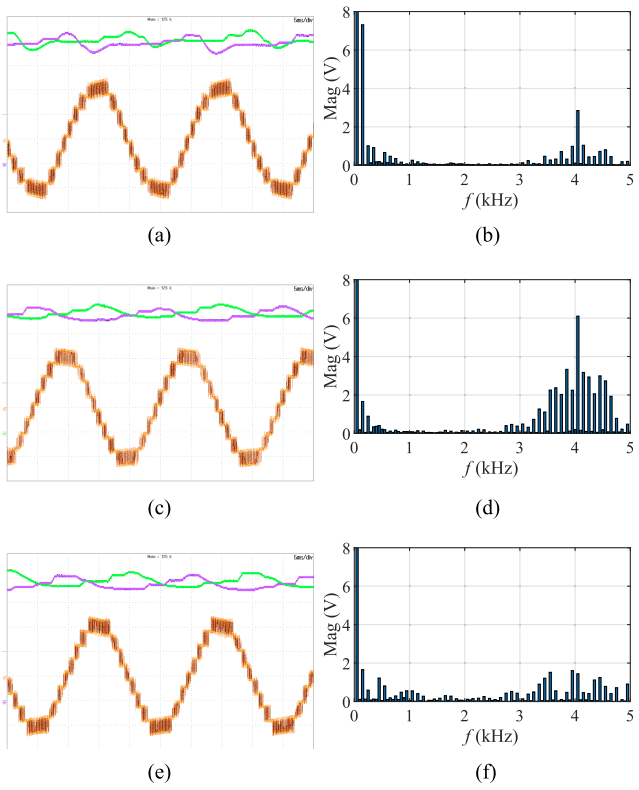

Fig. 16. Experimental results (5 ms/div): phase voltage (yellow, 30 V/div), its harmonic spectrum, and SM capacitor voltages (green/purple, 10 V/div). (a) and (b) DiPWM. (c) and (d) IndiPWM. (e) and (f) I-IndiPWM-SFR.

TABLE IV
THD and WTHD (%) Values of Phase Voltage of Different PWM Schemes in Experiments

Method	THD_{100}	$WTHD_{100}$	$WTHD_{20}$	$THD_{70,90}$
DiPWM	4.93	1.448	1.448	2.04
IndiPWM	6.43	0.357	0.348	5.85
I-IndiPWM-SFR	2.84	0.349	0.347	1.92

schemes implemented on an RTU-BOX204 real-time digital controller. Related parameters are detailed in Table II.

Figs. 16 and 17 illustrate the results in terms of phase voltage/SM capacitor voltages (one per arm) and phase/circulating current, respectively. The I-IndiPWM scheme is not evaluated here for its much higher switching frequency, as shown in the previous section. It can be clearly observed that the DiPWM presents higher circulating current, larger capacitor voltage ripple, and significant LF distortions in the phase voltage/current, while the conventional IndiPWM shows significant CF harmonics. In comparison, the proposed I-IndiPWM-SFR technique exhibits much better performance in the entire frequency range (up to the 100th harmonic). In terms of the SM capacitor voltage, IndiPWM and I-IndiPWM-SFR present similar profile.

Table IV summarizes the values of various THD/WTHD indices of phase voltage in the above experiments. $THD_{70,90}$ evaluates the CF harmonic distortions. Results coincide with the previous analysis and are very similar to the simulations in Section V.

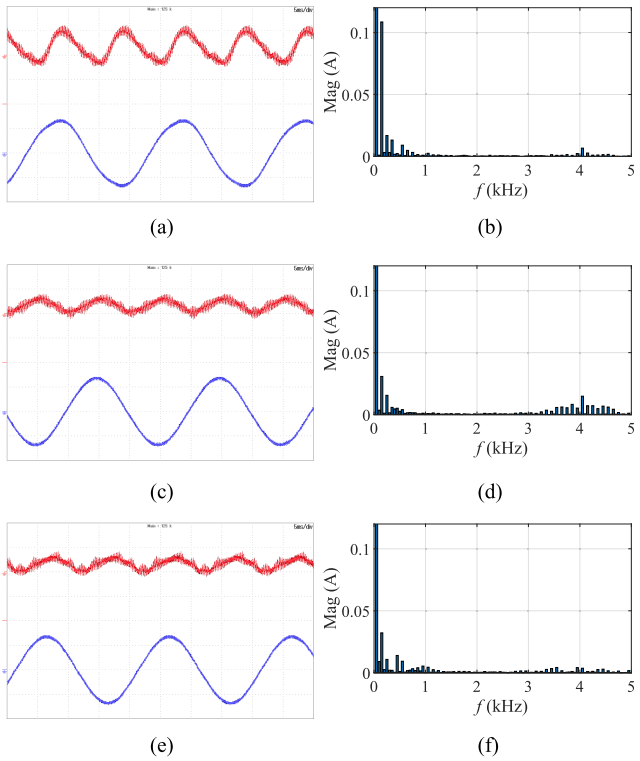

Fig. 17. Experimental results (5 ms/div): phase current (blue, 2 A/div), its harmonic spectrum, and circulating current (red, 2 A/div). (a) and (b) DiPWM. (c) and (d) IndiPWM. (e) and (f) I-IndiPWM-SFR.

VII. Conclusion

This article investigated the application of the IndiPWM to an MV MMC instead of the commonly adopted DiPWM. Through Fourier harmonic analysis on the phase voltage when employing a specific PWM technique, it was revealed that the IndiPWM inherently results in high CF distortions, though it is more accurate and can suppress the LF harmonics better than the DiPWM. To address the above issue, the original IndiPWM technique was improved through rearrangement of SPs, lowering the CF distortions while maintaining the merit of LF harmonic suppression. Implementation of the proposed method, with considerations on SFR, was also described, which can be efficiently carried out on an FPGA platform. Several simulations and experiments were conducted for validation. The results verified the advantages of the proposed method with significantly reduced distortions in both the LF and CF harmonics.

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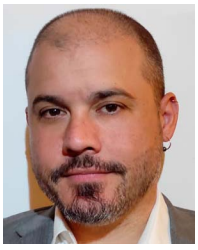

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