An Expandable Interline DC Power Flow Controller

Hao Guo, Wu Chen, *Senior Member, IEEE*, Yiqing Zhu, and Miao Zhu, *Senior Member, IEEE*

***Abstract*—The power flow control capability of high-voltage dc power grid can be improved by integrating a dc power flow controller into the grid. In this article, an expandable interline dc power flow controller (IDCPFC) is proposed. Compared with the existing dc power flow controller, the proposed IDCPFC has the advantages of high expandability, less active switching devices, simpler control, and wider adjustment range. A three-port IDCPFC is selected as the case study and the performance of IDCPFC is verified through simulation and experiment. Experimental results show that the proposed IDCPFC can achieve multiline power flow control under various conditions.**

***Index Terms*—Expandable interline dc power flow controller (IDCPFC), multiterminal HVdc grid, power flow control.**

I. Introduction

HIGH-VOLTAGE dc (HVdc) system and multiterminal HVdc system based on voltage source converter (VSC) can effectively solve the problems of grid integration and absorption of renewable energy, and have attracted extensive attention in recent years [1], [2], [3]. As the number of nodes in dc power grid increases, the structure of dc power grid is becoming increasingly complex. Hence, precise dc power flow control can hardly be achieved by only adjusting the output power of VSCs. Therefore, it is necessary to use dc power flow controller to control dc power flow.

In a dc grid, the power flow of each dc line is only determined by the voltage of converter stations and the line resistance [4], [5]. Hence, there are two types of dc power flow controllers: the resistance type and voltage source type DCPFC.

Jovcic et al. [6] proposed a typical resistance type scheme by inserting variable resistors in series in the transmission lines, which has the advantages of simple structure and control. However, it increases the loss on the line, and can only adjust the power flow in one direction.

Generally, there are three main types of voltage source DCPFC: dc transformer, series adjustable voltage source (SAVS), and interline dc power flow controller (IDCPFC). DC transformer can be used to connect dc power grids with different voltage levels, and to regulate power flow in power grids with the same voltage level [7], [8], [9], [10]. However, dc transformer must withstand the system-level voltage and handle all the power. It may handle up to dozens or even hundreds of megawatts, leading to high cost and loss. The SAVS with external power supply can insert positive and negative adjustable and variable size dc voltage source into the line [11], [12], [13], [14], [15], [16]. Therefore, its voltage and power levels are lower. Compared with the dc transformer, SAVS does not need to withstand the system voltage, but it requires additional external power supply to provide power, and an insulation transformer to provide the isolation between ac and dc grids, which increases the design cost of the power flow controller.

IDCPFC does not require transformer structure or external ac or dc power sources, consequently leading to lower power requirements and lower costs. Therefore, it has good application prospects. IDCPFC can be divided into three types according to the power transfer principle: circulation-coupled, capacitance-coupled, and inductance-coupled. The circulation-coupled IDCPFC achieves power flow control by controlling the dc component of the modular multilevel converter (MMC) module and energy balance by controlling the ac component [17]. This type of IDCPFC has a large control range and relatively small ripple, but its construction cost is high and the control strategy is relatively complex. The capacitance-coupled IDCPFC has a simple structure and achieves power transmission from one line to another by continuously inserting capacitors between lines [18], [19], [20]. However, frequent insertion of capacitors can introduce large ripples in the power grid, interfering with the normal operation of the transmission lines. In our previous work [21], [22], an inductance-coupled IDCPFC was proposed, using inductance as the transmission medium for capacitive energy. This type of IDCPFC outperforms the abovementioned two types of IDCPFC with the advantages of small ripple and simple control.

However, as the dc transmission system becomes more complex, abovementioned IDCPFC cannot cope with the complex power flow conditions because of the insufficient degree of control freedom. It can only actively control the current on one line and passively control the current on the other. Therefore, it is necessary to investigate the multiport IDCPFC.

The multiport IDCPFC proposed in [23], [24], [25], and [26] cannot simultaneously meet the requirements of reverse power flow, small voltage and current ripple, and fewer active switching devices. In terms of inductance-coupled IDCPFC, Zhong et al. [26] proposed a multiport IDCPFC with bidirectional regulation

Manuscript received 13 March 2023; revised 2 July 2023 and 28 August 2023; accepted 9 October 2023. Date of publication 17 October 2023; date of current version 6 December 2023. This work was supported by the National Natural Science Foundation of China under Grant U2166216. Recommended for publication by Associate Editor F. Dijkhuizen. *(Corresponding author: Wu Chen.)*

Hao Guo, Wu Chen, and Yiqing Zhu are with the School of Electrical Engineering, Southeast University, Nanjing 210096, China (e-mail: 220213130@seu.edu.cn; chenwu@seu.edu.cn; 220222691@seu.edu.cn).

Miao Zhu is with the School of Electronic Information and Electrical Engineering, Shanghai Jiao Tong University, Shanghai 200240, China, and also with the Key Laboratory of Control of Power Transmission and Conversion (SJTU), Ministry of Education, Shanghai 200240, China (e-mail: miaozhu@sjtu.edu.cn).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3325225.

Digital Object Identifier 10.1109/TPEL.2023.3325225

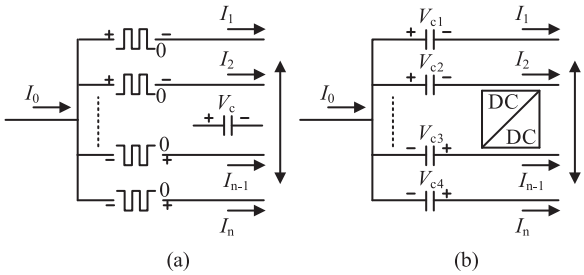

Fig. 1. Two different types of IDCPFCs. (a) Proposed in [24] and [25]. (b) Proposed in [26].

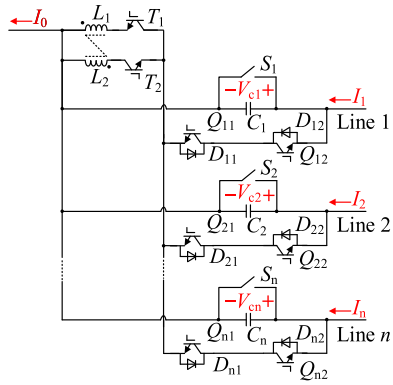

Fig. 2. Proposed IDCPFC topology.

capability based on [22]. However, for an n-port power flow controller, it requires a total number of $4n$ active switching devices, which will increase the cost. Therefore, there is still a considerable room for improvement in the research of the multiport IDCPFC in future complex dc systems.

In this article, a multiport IDCPFC with coupled inductor that has the ability of bidirectional power flow control is proposed. This topology requires fewer switching devices for an n-port power control, that is, it only needs $(2+2n)$ active switching devices. Moreover, it is able to cope with the power flow reversal condition and almost no voltage and current ripple is injected into the dc power grid. The rest of this article is organized as follows. In Section II, the general topology structure is given, and the operation principle of three-port IDCPFC is illustrated as an example. Protection considerations for the three-port IDCPFC topology are given in Section III to cope with dc faults. Simulation results of three-port IDCPFC are given in Section IV, and the proposed circuit is experimentally verified by a four-terminal grid in Section V. Finally, Section VI concludes this article.

II. Expandable IDCPFC

A. Comparisons Between Two Types of IDCPFCs

In order to illustrate the improved performance of the inductance-coupled IDCPFC, the schematic diagrams of capacitance-coupled and inductance-coupled are depicted in Fig. 1 and their operation principles are compared in detail.

Specifically, Fig. 1(a) shows the schematic diagram of the capacitance-coupled IDCPFC mentioned in [24] and [25]. Since the voltage drop of a capacitor is stable when the capacitor is fully charged, the capacitor can be considered as a voltage source in the stable state. By turning ON or OFF the corresponding switches, either a positive or a negative voltage sources V_c is periodically inserted into the correspondent transmission lines. Consequently, this method will introduce large voltage ripple and current ripple in the lines, which may be large enough to cause resonance or the malfunction of other devices. Redesigning the original filters in the dc power grid or adding additional filters may be an effective way to eliminate the impact of injected ripple, but this will undoubtedly increase the cost.

In contrast, the operation principle of the inductance-coupled IDCPFC mentioned in [26] is depicted in Fig. 1(b). N capacitors that can be considered as n stable dc voltage sources in the steady state are directly inserted into n transmission lines that require power flow control. To ensure the constant voltage drops of the capacitors, it is necessary to introduce a dc/dc converter to transfer the power between n capacitors. Although more energy storage components are required in Fig. 1(b) compared with Fig. 1(a), the advantage of inductance-coupled IDCPFC lies in that almost no injection of voltage ripple will be introduced into the transmission lines due to large capacitance.

B. Structure of the Expandable IDCPFC

This article proposes a new IDCPFC, and the topology is shown in Fig. 2. For the n-port IDCPFC, n capacitors C_i ($i = 1, 2, \ldots, n$) are inserted into n lines respectively, S_i is the bypass switch for each capacitor, L_1 and L_2 are coupled inductors, T_1 and T_2 are their respective switches, $Q_{11}\sim Q_{n2}$ are $2n$ IGBTs, and $D_{11}\sim D_{n2}$ are their antiparallel diodes.

When the bypass switches are all turned ON, all capacitors are shorted and the IDCPFC stops functioning as a power flow regulator. In order to achieve power flow regulation, the switches T_1, T_2, Q_{i1}, and Q_{i2} should be properly controlled while the bypass switches are turned OFF to maintain the constant voltage of each capacitor.

In the next section, three typical operation modes of IDCPFC will be analyzed according to different control objectives, and the reference directions of voltage and current are shown in Fig. 2.

C. Operation Principle

To illustrate the operation principle of the proposed IDCPFC, three typical modes of three-port IDCPFC are taken as examples. Detailed analyses are as follows.

Mode 1. I_1, I_2, and I_3 are in Positive Direction: In this mode, I_1 and I_2 are controlled to decrease actively, while I_3 is controlled to increase passively. According to the regulation requirement, positive resistances should be injected into Line 1 and Line 2, and a negative resistance should be injected into Line 3. Hence, the energy should be transferred from C_1, C_2 to C_3 and the voltage polarities of V_{c1}, V_{c2}, and V_{c3} are shown in Fig. 3.

According to the energy transfer path and voltage polarities, Q_{11} and T_1 are turned ON as shown in Fig. 3(a). C_1, D_{12}, Q_{11}, T_1, and L_1 form a current loop, and the inductor current I_{L1}

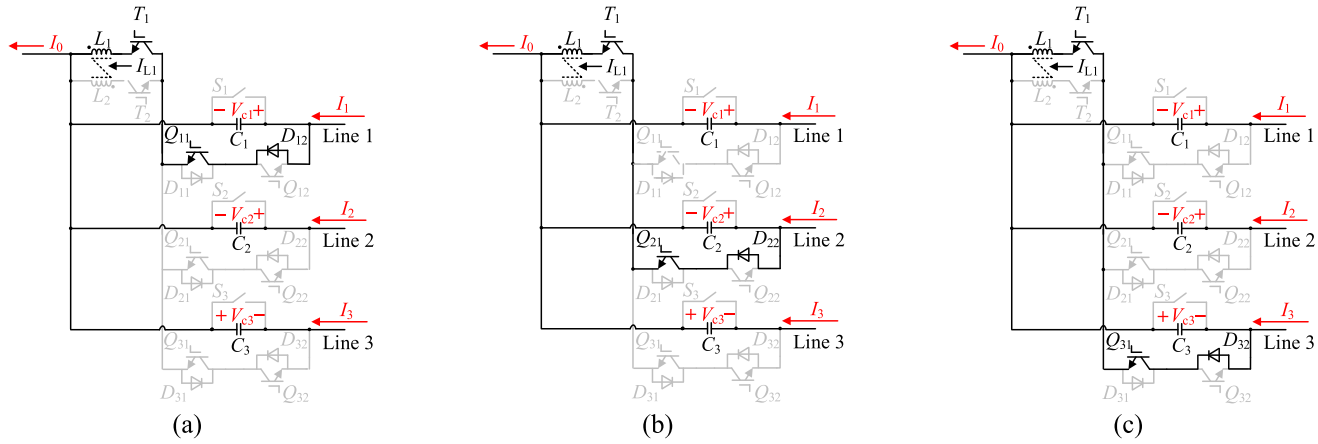

Fig. 3. Operation states in mode 1. (a) T_1 and Q_{11} are ON. (b) T_1 and Q_{21} are ON. (c) T_1 and Q_{31} are ON.

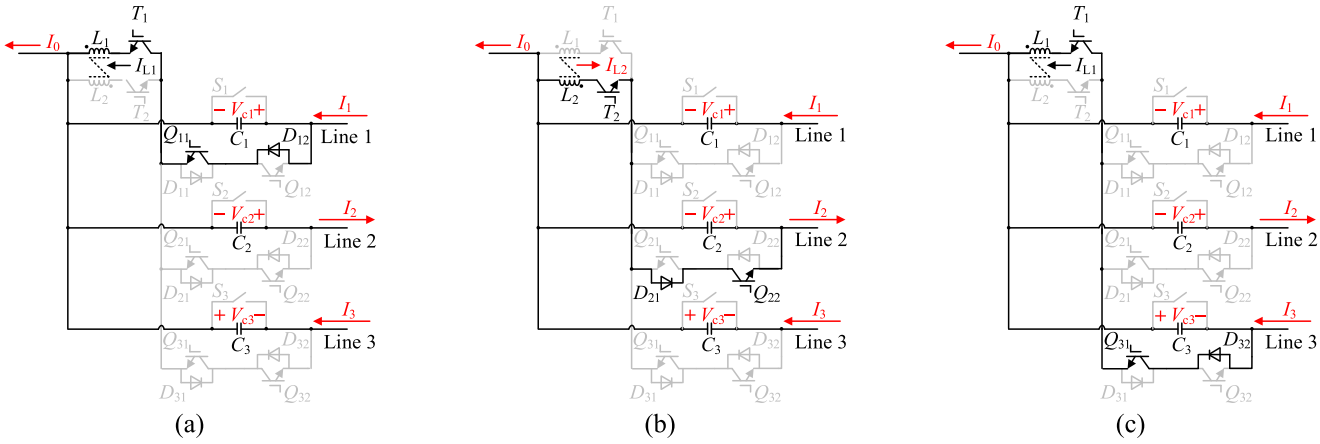

Fig. 4. Operation states in mode 2. (a) T_1 and Q_{11} are ON. (b) T_2 and Q_{22} are ON. (c) T_1 and Q_{31} are ON.

increases linearly, assuming that V_{c1} remains constant during the switching cycle. When Q_{11} is turned OFF, Q_{21} is turned ON, as shown in Fig. 3(b). Then, C_2, D_{22}, Q_{21}, T_1, and L_1 form a current loop, the inductor current I_{L1} continues to increase. When Q_{21} is turned OFF, Q_{31} is turned ON, as shown in Fig. 3(c). Then, C_3, D_{32}, Q_{31}, T_1, and L_1 form a current loop, inductor current I_{L1} starts to decrease. When Q_{31} is turned OFF and Q_{11} is turned ON, another switching cycle begins. In this way, the energy stored in C_1 and C_2 is released to C_3 through the inductor L_1, so that the line currents are maintained at the given current reference values.

Mode 2. I_1 and I_3 are in Positive Direction, while I_2 is in Negative Direction: In this mode, I_2 and I_3 increase actively by control, while I_1 decreases passively. According to the regulation requirement, a positive resistance should be injected into Line 1, and negative resistances should be injected into Line 2 and Line 3. Hence, the energy should be transferred from C_1 to C_2, C_3 and the voltage polarities of V_{c1}, V_{c2}, and V_{c3} are shown in Fig. 4.

According to the energy transfer path and voltage polarities, Q_{11} and T_1 are turned ON as shown in Fig. 4(a). C_1, D_{12}, Q_{11}, T_1, and L_1 form a current loop, and the inductor current I_{L1} starts to increase. When Q_{11}, T_1 are turned OFF, Q_{22}, T_2 are turned ON, as shown in Fig. 4(b). Then, C_2, L_2, T_2, D_{21}, and Q_{22} form a current loop, the energy in coupling inductor L_1 is transferred to coupling inductor L_2 first, and then transferred to capacitor C_2 through L_2. When Q_{22}, T_2 are turned OFF, Q_{31}, T_1 are turned ON, as shown in Fig. 4(c). Then, C_3, D_{32}, Q_{31}, T_1, and L_1 form a current loop, the energy in coupling inductor L_2 is transferred to coupling inductor L_1 first, and then transferred to capacitor C_3 through L_1. When Q_{31} is turned OFF and Q_{11} is turned ON, another switching cycle begins. In this way, the energy stored in C_1 is released to C_2 and C_3 through the coupled inductors L_1 and L_2, so that the line currents are maintained at the given current reference values.

Mode 3. I_1, I_2, and I_3 are in Opposite Direction: In this mode, I_1 and I_2 are controlled to increase actively, while I_3 is controlled to decrease passively. According to the regulation requirement, negative resistances should be injected into Line 1 and Line 2, and a positive resistance should be injected into Line 3. Hence, the energy should be transferred from C_3 to C_1, C_2 and the voltage polarities of V_{c1}, V_{c2}, and V_{c3} are shown in Fig. 5.

According to the energy transfer path and voltage polarities, Q_{12} and T_2 are turned ON, as shown in Fig. 5(a). C_1, L_2, T_2, D_{11}, and Q_{12} form a current loop, and the inductor current I_{L2} decreases linearly. When Q_{12} is turned OFF, Q_{22} is turned ON, as

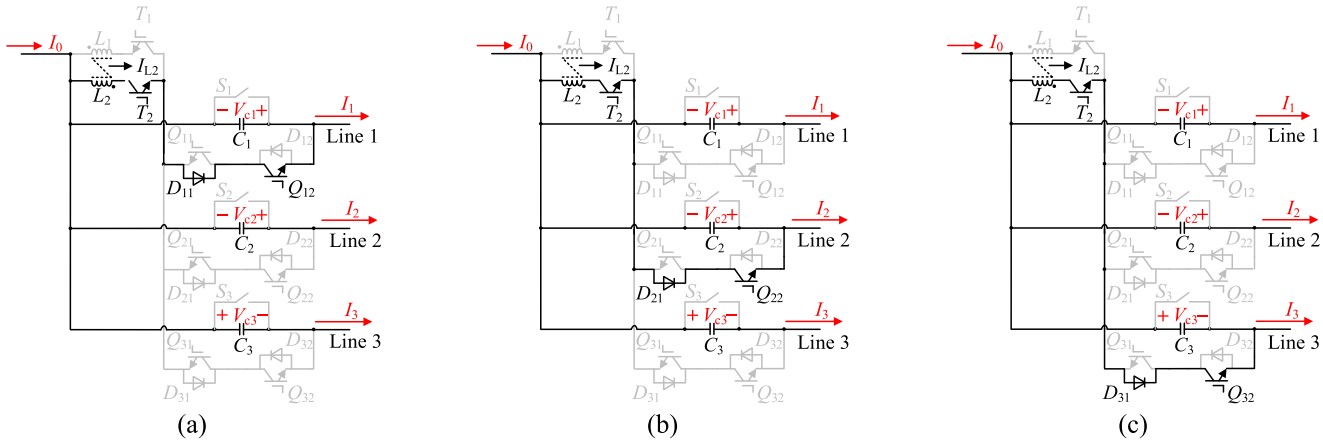

Fig. 5. Operation states in mode 3. (a) T_2 and Q_{12} are ON. (b) T_2 and Q_{22} are ON. (c) T_2 and Q_{32} are ON.

TABLE I
SUMMARY OF MODES 1, 2 AND 3

Mode	Direction of $I_1/I_2/I_3$	Regulation requirement of $I_1/I_2/I_3$	Controlled switch	$V_{c1}/V_{c2}/V_{c3}$ polarity
1	P/P/P	↓/↓/↑	Q_{11}, Q_{21}, Q_{31}, T_1	+/+/−
2	P/N/P	↓/↑/↑	Q_{11}, Q_{22}, Q_{31}, T_1, T_2	+/+/−
3	N/N/N	↑/↑/↓	Q_{12}, Q_{22}, Q_{32}, T_2	+/+/−

shown in Fig. 5(b). Then, C_2, L_2, T_2, D_{21}, and Q_{22} form a current loop, the inductor current I_{L2} continues to decrease. When Q_{22} is turned OFF, Q_{32} is turned ON, as shown in Fig. 5(c). Then, C_3, L_2, T_2, D_{31}, and Q_{32} form a current loop, inductor current I_{L2} starts to increase. When Q_{32} is turned OFF and Q_{12} is turned ON, another switching cycle begins. In this way, the energy stored in C_3 is released to C_1 and C_2 through the inductor L_2, so that the line current is maintained at the given current reference values.

The abovementioned three modes are summarized in Table I, including the regulation requirements of power flow, controlled switch devices, and polarities of inserted capacitors.

D. Characteristics Analysis

Due to the similarity of operation principle in different modes, mode 1 (referring to Fig. 3) is taken as an example to analyze the characteristics of IDCPFC.

The duty cycles for Q_{11}, Q_{21}, and Q_{31} are set as D_1, D_2, and D_3 ($D_1+D_2+D_3=1$), respectively. When the inductor current is continuous, according to the voltage–second balance principle, the following is obtained as:

$$V_{c1}D_1T_s + V_{c2}D_2T_s - V_{c3}D_3T_s = 0 \tag{1}$$

where T_s is switching period.

When the voltage of C_1, C_2, and C_3 are continuous, the following (2)–(4) based on charge conversation can be obtained as:

$$(I_1 - I_{L1})\,D_1T_S + I_1\,(1-D_1)\,T_S = 0 \tag{2}$$

$$(I_2 - I_{L1})\,D_2T_S + I_2\,(1-D_2)\,T_S = 0 \tag{3}$$

$$(I_3 - I_{L1})\,D_3T_S + I_3\,(1-D_3)\,T_S = 0 \tag{4}$$

where I_{L1} is the current of inductor 1.

By simplifying the above equations, the following (5)–(7) can be obtained as:

$$I_1 = D_1I_{L1} \tag{5}$$

$$I_2 = D_2I_{L1} \tag{6}$$

$$I_3 = D_3I_{L1} \tag{7}$$

It can be seen that the duty cycle D_1, D_2, and D_3 have a linear relationship with the corresponding line current, which indicates that the current of line i can be controlled by controlling D_i. Assuming that the conversion efficiency of IDCPFC is 100%, following can be obtained as:

$$V_{c1}I_1 + V_{c2}I_2 - V_{c3}I_3 = 0 \tag{8}$$

The ripple formulas of V_{c1}, V_{c2}, and V_{c3} are

$$\begin{cases} \Delta V_{c1} = \frac{I_1(I_2+I_3)}{fC_1(I_1+I_2+I_3)} \\ \Delta V_{c2} = \frac{I_2(I_1+I_3)}{fC_2(I_1+I_2+I_3)} \\ \Delta V_{c3} = \frac{I_3(I_1+I_2)}{fC_3(I_1+I_2+I_3)} \end{cases} \tag{9}$$

where f is the switching frequency.

Similar analysis can be done for other modes, and the control strategy will be given in the next section.

E. Control Strategy

For the n-port dc power flow controller, the current of n lines is independently controlled, and the duty cycles of each line switch devices are defined as D_1, D_2, …, D_n, respectively. Taking the positive operation of n lines as an example, the general control strategy of the n-port power flow controller is shown in Fig. 6. In the block diagram, the initial duty cycle signals are generated according to the difference between the reference values and the actual values of each line current. Then, the duty cycle signals are logically processed and finally applied to the switches of each

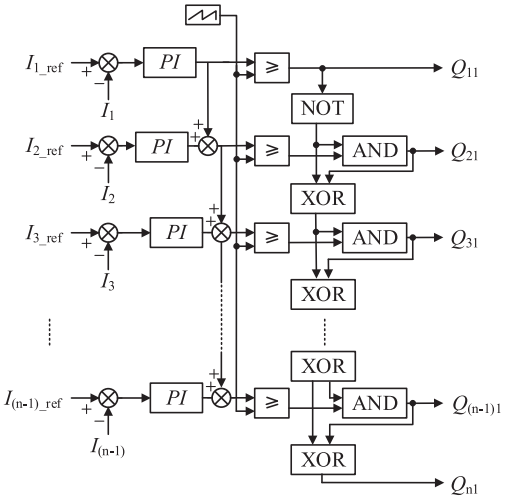

Fig. 6. Block diagram of strategy.

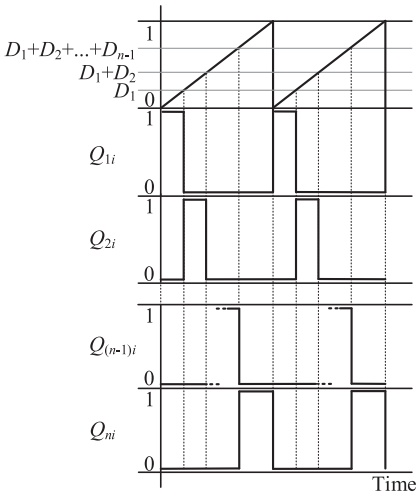

Fig. 7. Switch signals (i = 1, 2).

line. Noted that the ON states of produced switch signals have a complementary relationship, and the specific switch signals are given in Fig. 7.

III. Bypass Protection During Faults

To safely disconnect the IDCPFC in the dc transmission lines in the event of a short-circuit fault or switch open-circuit fault, it is necessary to improve the original IDCPFC topology. According to the protection method of the dc power flow controller in the event of the fault in the dc power grid mentioned in [24], [27], and [28], an additional protection scheme for three-port IDCPFC is proposed, as is shown in Fig. 8. Although this implies the need for additional switches and thus a more complex structure, it is necessary to apply such protection device to IDCPFCs.

Since a normally operating switch may be unable to stand the fault current level, another path is required to transfer the current. By connecting a bidirectional switch in parallel between each transmission line and the busbar, the current can be transferred

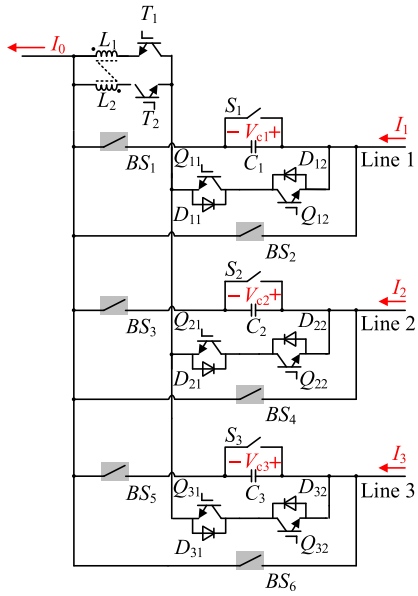

Fig. 8. Additional protection equipment for the three-port IDCPFC topology.

to the branch where the parallel bidirectional switch is located when a fault occurs. In addition, a normally closed switch is connected in series with the capacitor. It should be opened before closing the parallel switch to avoid the short circuit of the capacitor.

A. Transmission Line Fault

Suppose a short-circuit fault occurs in Line 1, the steps to bypass the IDCPFC are as follows. After detecting the fault, close switches T_1, T_2, and Q_{11}~Q_{32} to interrupt the power flow control function and disconnect the normally closed switches BS_1, BS_3, and BS_5 to prevent the capacitors from short circuit at t_1. Then, close the parallel bidirectional switches BS_2, BS_4, and BS_6 to provide a path for the fault current. At t_3, Q_{11} and Q_{12} are turned OFF, allowing all fault currents to pass through the fault transfer branch, and the faulty line is removed from the system by opening the dc circuit breaker (DCCB) of the faulty line at t_4. Finally, open BS_2, BS_4, and BS_6 and the other lines return to normal operation. The line fault isolation process is shown in Fig. 9.

In addition, combining the power flow controller with a dc breaker so that one topology has both capabilities is also a feasible way [29], [30], [31], [32]. In [32], a hybrid DCCB with power flow control device was proposed to study its ability to control current and to cope with dc faults.

B. Switch Q_{i1} or Q_{i2} Fault

Assuming that an open-circuit fault occurs at switches Q_{11} or Q_{12} on Line 1, the procedure for bypassing the IDCPFC is as follows. First, the switches of Lines 2 and 3 operate in the alternate operation mode of equal duty cycle and enter the protection state. Next, switch BS_1 is opened and switch BS_2 is closed so that the current in Line 1 is followed by BS_2. For Line

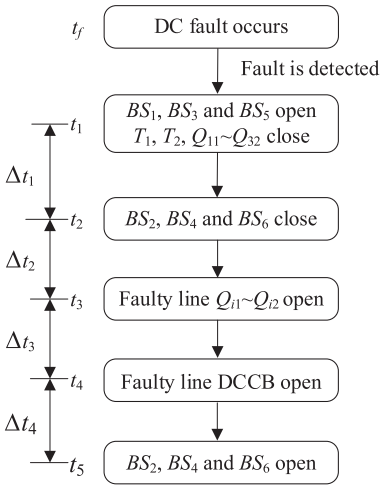

Fig. 9. Line fault isolation process.

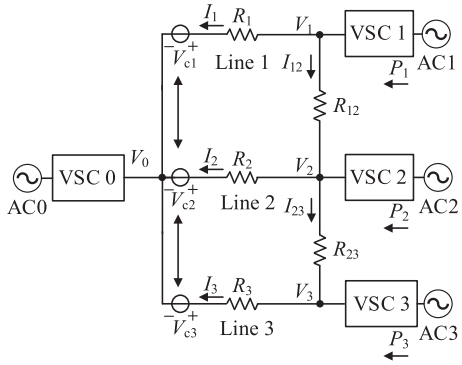

Fig. 10. Four-terminal VSC-HVdc system with IDCPFC.

TABLE II
PARAMETERS OF TRANSMISSION LINES

Parameter	Line 1	Line 2	Line 3	Line 12	Line 23
Length/km	200	150	200	100	100
Resistance/Ω	2	1.5	2	1	1
Inductance/mH	80	60	80	40	40

1, this treatment is equivalent to bypassing the IDCPFC. Finally, control current I_2 or current I_3 to the reference value, and restart power flow control mode.

IV. SIMULATION VERIFICATION

To verify the effectiveness of the proposed topology, an equivalent four-terminal HVdc system including the three-port IDCPFC is built, as shown in Fig. 10. Line parameters are given in Table II. With VSC 0 operating in a constant voltage mode, the voltage of terminal 0 is maintained at $V_0 = 400$ kV. The other three terminals operate in a constant power mode, delivering 540, 360, and 180 MW to the HVdc system, respectively. The IDCPFC is installed at terminal 0 and the capacitors C_1, C_2, and C_3 are inserted into Line 1, Line 2, and Line 3, respectively. The switching frequency of IDCPFC is 2 kHz, and $C_1 = 3.5$ mF, $C_2 = 3.6$ mF, $C_3 = 2.9$ mF, and $L_1 = L_2 = 1.2$ mH.

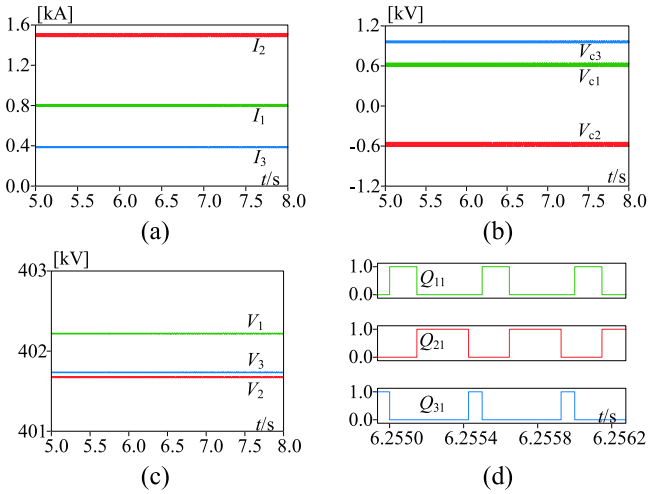

Fig. 11. Simulation results of steady-state operation. (a) I_1, I_2, and I_3. (b) V_{c1}, V_{c2}, and V_{c3}. (c) V_1, V_2, and V_3. (d) Q_{11}, Q_{21}, and Q_{31}.

According to Fig. 10, (10) and (11) can be obtained. When the IDCPFC is bypassed, the line currents and terminal voltages can be calculated as $I_1 = 0.97$ kA, $I_2 = 1.05$ kA, $I_3 = 0.67$ kA, $V_1 = 401.94$ kV, $V_2 = 401.57$ kV, and $V_3 = 401.34$ kV

$$\begin{cases} I_{12} = \frac{V_1 - V_2}{R_{12}} \\ I_{23} = \frac{V_2 - V_3}{R_{23}} \\ I_1 = \frac{V_1 - V_0 - V_{c1}}{R_1} \\ I_2 = \frac{V_2 - V_0 - V_{c2}}{R_2} \\ I_3 = \frac{V_3 - V_0 - V_{c3}}{R_3} \end{cases} \tag{10}$$

$$\begin{cases} P_1 = (I_1 + I_{12})\, V_1 \\ P_2 = (I_2 + I_{23} - I_{12})\, V_2 \\ P_3 = (I_3 - I_{23})\, V_3. \end{cases} \tag{11}$$

A. Steady-State Operation

Before 3 s, the IDCPFC is bypassed and at $t = 3$ s, the IDCPFC is enabled to control the currents I_1 and I_2, whose reference values are set to 0.8 and 1.5 kA, respectively.

The simulation waveforms are shown in Fig. 11. As shown in Fig. 11(a), after the IDCPFC is put into operation, the line currents quickly stabilize to the reference values. The capacitor voltages of C_1, C_2, and C_3 are shown in Fig. 11(b), reaching 0.62, −0.57, and 0.96 kV, respectively. Fig. 11(c) shows the terminal voltages of the VSCs. The waveforms of the complementary switching signals are shown in Fig. 11(d), which validates the control strategy.

B. Step Change in P_2 With Unchanged Line Current

Before 6 s, the operation of the power flow controller is the same as that of case A, and when $t = 6$ s, the output power of VSC 2 drops from 360 to 250 MW, while the output power of other converter stations remains unchanged. At this time, the power flow controller controls the current of Line 1 and Line 2 to keep the same.

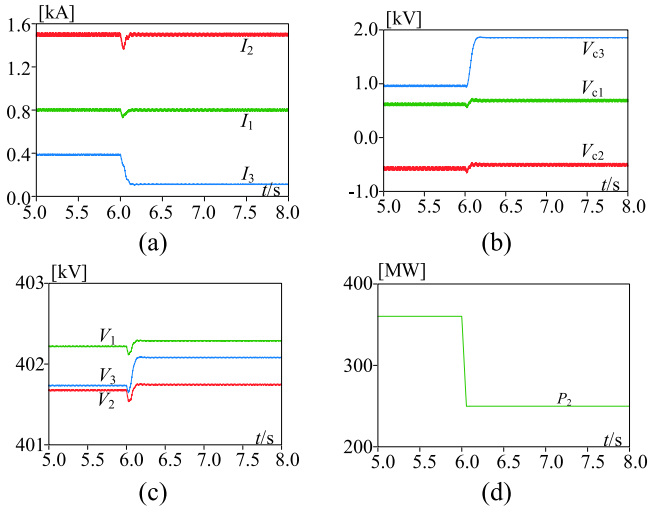

Fig. 12. Simulation results of step change in P_2 with unchanged line current. (a) I_1, I_2, and I_3. (b) V_{c1}, V_{c2}, and V_{c3}. (c) V_1, V_2, and V_3. (d) P_2.

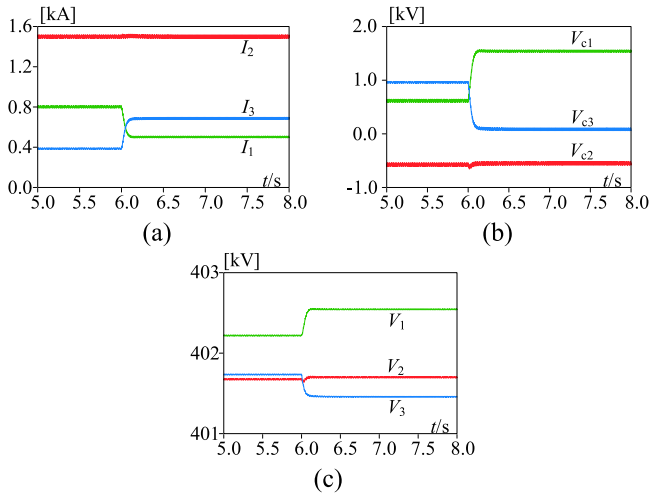

Fig. 13. Simulation results of active control of one line's power flow. (a) I_1, I_2, and I_3. (b) V_{c1}, V_{c2}, and V_{c3}. (c) V_1, V_2, and V_3.

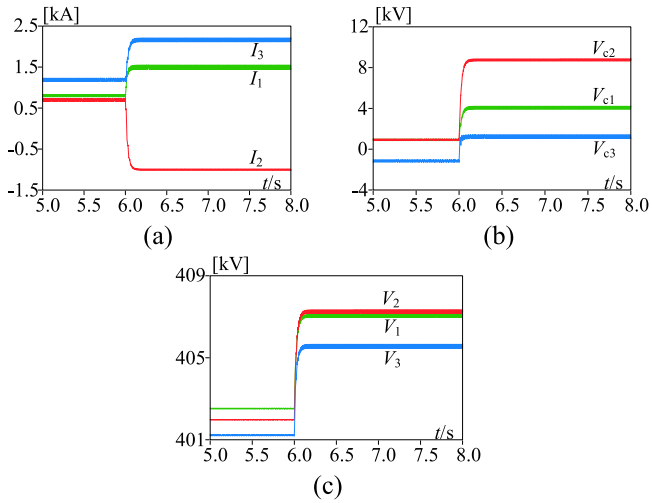

Fig. 14. Simulation results of power flow reversal. (a) I_1, I_2, and I_3. (b) V_{c1}, V_{c2}, and V_{c3}. (c) V_1, V_2, and V_3.

The simulation waveforms are shown in Fig. 12. Fig. 12(a) shows the current waveforms of the three controlled lines. It can be seen that currents I_1 and I_2 return to their respective given values of 0.8 and 1.5 kA after 0.1 s, while current I_3 decreases due to the decrease in VSC 2 output power. As shown in Fig. 12(b) and (c), the voltages of inserted capacitors and terminal voltages of VSCs quickly reach a new steady state. After the output power of VSC 2 drops for 0.1 s, the voltages of adjustable voltage sources C_1, C_2, and C_3 change to 0.69, −0.50, and 1.86 kV, respectively.

C. Active Control of One Line's Power Flow

In this case, the IDCPFC is enabled at 3 s (I_1 and I_2 are controlled to be 0.8 and 1.5 kA, respectively), and at instant $t =$ 6 s, the reference value of I_1 is set to 0.5 kA, while I_2 remains unchanged.

Fig. 13 shows the simulation waveforms. The simulation waveforms of the three controlled lines are shown in Fig. 13(a). When $t = 6$ s, the current I_1 of Line 1 decreases from 0.8 kA to 0.5 kA after 0.1 s, while the current I_2 of Line 2 remains unchanged. Fig. 13(b) shows the voltages of adjustable voltage sources C_1, C_2, and C_3, which change from 0.62, −0.57, and 0.96 kV to 1.54, −0.55, and −0.09 kV, respectively, as the reference value of I_1 changes. The terminal voltages of the VSCs are shown in Fig. 13(c).

D. Power Flow Reversal

Under this condition, the capability of the proposed IDCPFC to cope with power flow reversal is verified. Before 6 s, IDCPFC is put into operation, and I_1 and I_2 are set to 0.8 and 0.7 kA, respectively. When $t = 6$ s, the reference values of I_1 and I_2 are changed to 1.5 and −1 kA, respectively, so that the current flow of I_2 is reversed.

As shown in Fig. 14(a), the power flow controller acts at 6 s and the direction of I_2 changes from positive to negative after 0.1 s, verifying that the proposed IDCPFC is capable of coping with the reversal of the power flow. In Fig. 14(b) and (c), the voltages of inserted capacitors and terminal voltages of VSCs reach a new steady state after a short transient process. The voltages of adjustable voltage sources C_1, C_2, and C_3 reach to 4.08, 8.75, and 1.23 kV, respectively, after 0.1 s of power flow controller action.

E. Transmission Line Fault

The simulation results of the power flow controller in case of a ground fault on Line 1 are shown in Fig. 15. When $t < t_f$, the IDCPFC controls the currents in Lines 1 and 2 to be 0.7 and 1.5 kA, respectively. When $t = t_f$, a short-circuit fault to ground occurs in Line 1. After the system detects the fault at t_1, opens BS_1, BS_3 as well as BS_5, and closes switches Q_{11}∼Q_{32}. After a delay period, switches BS_2, BS_4, and BS_6 are closed so that the fault current is transferred to the fault transfer branch at t_2. At t_3

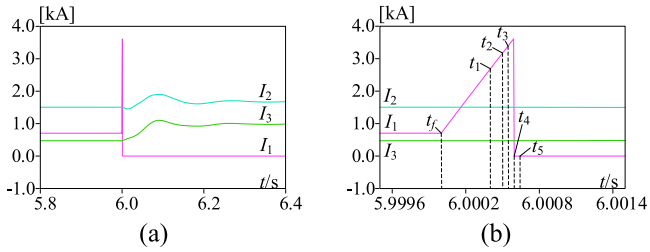

Fig. 15. Simulation results of transmission line fault. (a) I_1, I_2, and I_3. (b) Amplified I_1, I_2, and I_3.

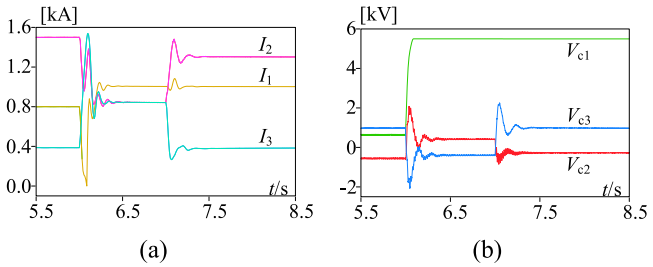

Fig. 16. Simulation results of switch fault. (a) I_1, I_2, and I_3. (b) V_{c1}, V_{c2}, and V_{c3}.

and t_4, the IDCPFC switches and DCCBs of the faulty line are opened, respectively. Finally, switches BS_2, BS_4, and BS_6 are opened and the other lines return to normal operation.

Fig. 15(a) gives the line currents from the occurrence of a fault to the time when the fault is removed. The line currents of the amplified fault handling section are given in Fig. 15(b).

F. Switch Fault

Fig. 16 shows the simulation results when switch Q_{11} or Q_{12} has an open-circuit fault. When $t < 6$ s, the IDCPFC controls the currents in Lines 1 and 2 to be 0.8 and 1.5 kA, respectively. When $t = 6$ s, an open-circuit fault occurs at switch Q_{11} or Q_{12} of Line 1, the switches of Lines 2 and 3 will be in the equal duty cycle alternating operation mode after detecting the fault and then enter the protection state. Line 1 will continue to charge C_1 due to switch disconnection until the current I_1 equals to 0 A. At this moment, switch BS_1 is disconnected and switch BS_2 is closed so that the current in Line 1 is followed by BS_2. For Line 1, this treatment is equivalent to bypassing the IDCPFC. When $t = 7$ s, the current I_2 is controlled to be 1.3 kA, and the current reaches the given value after a short fluctuation, which proves the good independence between the lines of the power flow controller.

Fig. 16(a) and (b) give the line currents and capacitor voltages from the occurrence of a fault to the time when the IDCPFC is put back into operation. As can be seen from Fig. 16(b), the capacitor voltage is stabilized at less than 6 kV. Besides, in order to achieve the power flow reversal condition, the capacitor voltage needs to operate at 8 kV or even higher, which means that the capacitor operates within the tolerance range during the fault handling process.

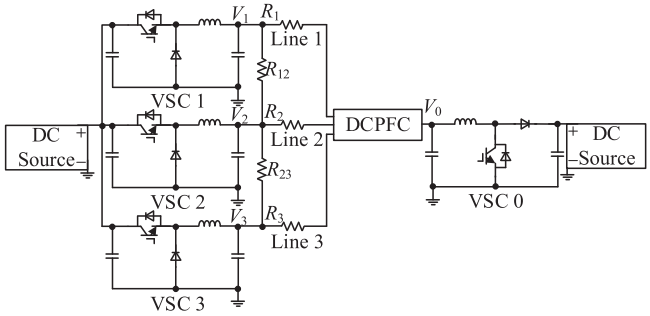

Fig. 17. Equivalent circuit of a four-terminal DC grid.

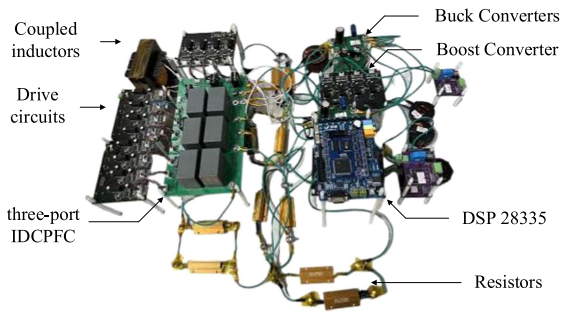

Fig. 18. Image of three-port IDCPFC.

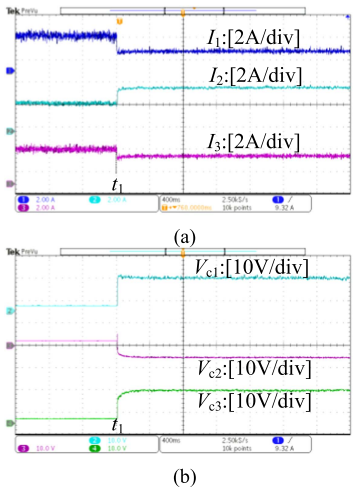

Fig. 19. Experimental results when the IDCPFC is inserted. (a) Waveforms of controlled line currents. (b) Waveforms of V_{c1}, V_{c2}, and V_{c3}.

V. Experiment Verification

To verify the operation of the proposed IDCPFC, a four-terminal dc grid consisting of a three-port IDCPFC has been built in the laboratory. The equivalent circuit and the prototype are shown in Figs. 17 and 18. The output power of VSC 1, VSC 2, and VSC 3 is 90, 160, and 70 W, respectively. The voltage V_0 of VSC 0 is 30 V. The line resistances R_1, R_2, and R_3 are 2.5, 5, and 1 Ω, respectively. For the three-port IDCPFC, $L_1 = L_2 = 100\ \mu$ H, and $C_1 = C_2 = C_3 = 300\ \mu$ F.

The experimental results of the case when the IDCPFC is inserted into the grid are shown in Fig. 19, and the reference

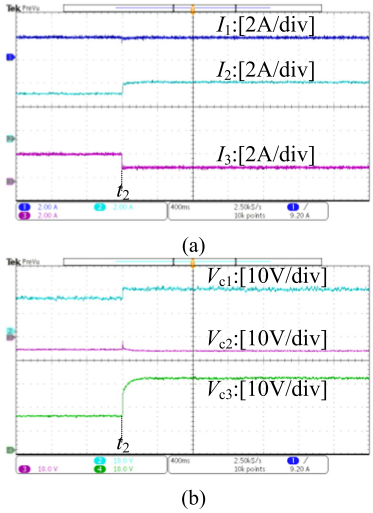

Fig. 20. Experimental results of changing I_1 while keeping I_3 unchanged. (a) Waveforms of controlled line currents. (b) Waveforms of V_{c1}, V_{c2}, and V_{c3}.

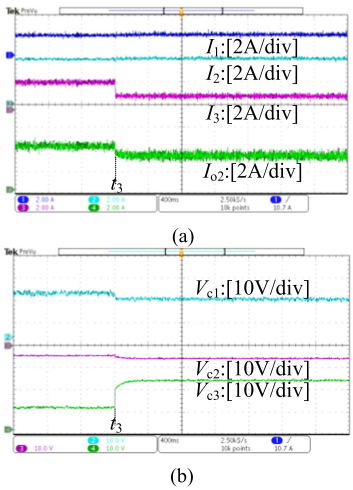

Fig. 21. Experimental results of changing I_1 while keeping I_3 unchanged while the output power VSC 2 is changed. (a) Waveforms of controlled line currents and output current of VSC 2. (b) Waveforms of V_{c1}, V_{c2}, and V_{c3}.

values of I_1 and I_2 are 1.8 and 4 A, respectively. Before t_1, the IDCPFC is bypassed, and the current I_1 and I_2 are 3.1 and 2.4 A, respectively. Under the regulation of IDCPFC, I_1 and I_2 quickly reach to their reference values, and I_3 is decreased. Fig. 19(b) shows the voltage waveforms of the inserted capacitors. The voltage of the three capacitors increases from 0 to a stable value.

Fig. 20 shows the experimental waveforms of changing the reference value of current I_2 while maintaining current I_1 unchanged. The reference values of current I_1 and I_3 before t_2 are 1.8 and 4 A, respectively, and at instant t_2, the reference value of current I_2 is set to 4.8 A. After a short transition, current I_2 quickly stabilizes to a new reference value, and current I_1 quickly remains at 1.8 A after a slight fluctuation. The voltages of inserted capacitors change from one steady state to another, as shown in Fig. 20(b).

Fig. 21 shows the experimental waveforms when the output power of VSC 2 is decreased (I_{o2} is the output current of VSC 2)

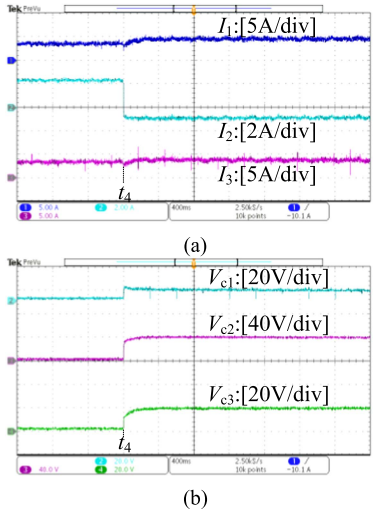

Fig. 22. Experimental results when power flow of Line 2 is reversed. (a) Waveforms of controlled line currents. (b) Waveforms of V_{c1}, V_{c2}, and V_{c3}.

and the reference values of I_1 and I_2 are still set to 1.8 and 4 A, respectively. It can be seen from the Fig. 21(a) that at instant t_3, the output power of VSC 2 decreases and I_1 and I_2 stabilize at the given values after a short fluctuation. In Fig. 21(b), the capacitor voltages change due to the drop of the output power of VSC 2.

Fig. 22 shows the experimental results when power flow of Line 2 is reversed. The reference values of current I_1 and I_2 are 4.5 and -1 A, respectively. Before t_4, the IDCPFC is bypassed, and I_1 and I_2 are 3.1 and 2.4 A, respectively. After t_4, the power flow of Line 2 is reversed under the regulation of IDCPFC. In Fig. 22(a), I_2 is controlled to -1 A, and I_1 is controlled to be 4.5 A at the same time. Fig. 22(b) shows the voltages of inserted capacitors. In all, Fig. 22 verifies the power flow reversal capability of the proposed power flow controller.

VI. Conclusion

An expandable IDCPFC is proposed in this article for meshed HVdc grids, which has the advantages of stronger expandability, less active switching devices, simpler control, and wider adjustment range. For an n-port IDCPFC, $(n-1)$-port power flow can be controlled actively. The operation principle, characteristics, and control strategy are analyzed in detail. Simulation tests on a three-port IDCPFC has been carried out in a four-terminal HVdc grid through four simulation scenarios, including steady-state operation, power injection step down, active control, and power flow reversal. The fault redundancy structure proposed in Section III is validated by line fault as well as switch fault simulations. In order to verify the performance of IDCPFC, a meshed four-terminal dc grid empirical system, as well as an IDCPFC prototype have been established in the laboratory. Experimental results verify that the proposed power flow controller has the characteristics of multiport independent control, outstanding dynamic performance, and is able to cope with power flow reversal conditions.

REFERENCES

[1] M. K. Bucher, R. Wiget, G. Andersson, and C. M. Franck, "Multi-terminal HVDC networks—What is the preferred topology?," *IEEE Trans. Power Del.*, vol. 29, no. 1, pp. 406–413, Feb. 2014.

[2] A. Nami, J. Liang, F. Dijkhuizen, and G. D. Demetriades, "Modular multilevel converters for HVDC applications: Review on converter cells and functionalities," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 18–36, Jan. 2015.

[3] E. Kontos, R. T. Pinto, S. Rodrigues, and P. Bauer, "Impact of HVDC transmission system topology on multiterminal DC network faults," *IEEE Trans. Power Del.*, vol. 30, no. 2, pp. 844–852, Apr. 2015.

[4] J. Yang, Z. He, H. Pang, and G. Tang, "The hybrid-cascaded DC–DC converters suitable for HVDC applications," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5358–5363, Oct. 2015.

[5] Y. Li, X. Shi, B. Liu, W. Lei, F. Wang, and L. M. Tolbert, "Development, demonstration, and control of a testbed for multiterminal HVDC system," *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 6069–6078, Aug. 2017.

[6] D. Jovcic, M. Hajian, H. Zhang, and G. Asplund, "Power flow control in DC transmission grids using mechanical and semiconductor based DC/DC devices," in *Proc. 10th Inst. Eng. Technol. Int. Conf. AC DC Power Transmiss.*, 2012, pp. 1–6.

[7] D. Jovcic, "Bidirectional, high-power DC transformer," *IEEE Trans. Power Del.*, vol. 24, no. 4, pp. 2276–2283, Oct. 2009.

[8] K. Natori, H. Obara, K. Yoshikawa, B. C. Hiu, and Y. Sato, "Flexible power flow control for next-generation multi-terminal DC power network," in *Proc . IEEE Energy Convers. Congr. Expo.*, 2014, pp. 778–784.

[9] G. J. Kish and P. W. Lehn, "A modular bidirectional DC power flow controller with fault blocking capability for DC networks," in *Proc. IEEE 14th Workshop Control Model. Power Electron.*, 2013, pp. 1–7.

[10] S. Kenzelmann, A. Rufer, D. Dujic, F. Canales, and Y. R. de Novaes, "Isolated DC/DC structure based on modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 89–98, Jan. 2015.

[11] T. Zhang, C. Li, and J. Liang, "A thyristor based series power flow control device for multi-terminal HVDC transmission," in *Proc. 49th Int. Univ. Power Eng. Conf.*, 2014, pp. 1–5.

[12] L. Yao, H. Cui, J. Zhuang, G. Li, B. Yang, and Z. Wang, "A DC power flow controller and its control strategy in the DC grid," in *Proc. IEEE 8th Int. Power Electron. Motion Control Conf.*, 2016, pp. 2609–2614.

[13] X. Zhong, M. Zhu, Y. Chi, S. Liu, and X. Cai, "Composite DC power flow controller," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 3530–3542, Apr. 2020.

[14] S. Kim, S. Cui, and S.-K. Sul, "Modular multilevel converter based on full bridge cells for multi-terminal DC transmission," in *Proc. 16th Eur. Conf. Power Electron. Appl.*, 2014, pp. 1–10.

[15] X. Zhang, J. Jin, Y. Ye, and X. Yang, "Analysis of a series-parallel-connected type DC power flow controller in multiterminal grids," *IEEE Trans. Power Electron.*, vol. 37, no. 6, pp. 7400–7410, Jun. 2022.

[16] Y. Ye, X. Zhang, J. Jin, Y. Wang, and X. Yang, "A multiport current flow controller for meshed multiterminal DC grids," *IEEE Trans. Power Electron.*, vol. 38, no. 4, pp. 5479–5489, Apr. 2023.

[17] V. Hofmann, A. Schön, and M.-M. Bakran, "A modular and scalable HVDC current flow controller," in *Proc. 17th Eur. Conf. Power Electron. Appl.*, 2015, pp. 1–9.

[18] C. D. Barker and R. S. Whitehouse, "A current flow controller for use in HVDC grids," in *Proc. 10th Inst. Eng. Technol. Int. Conf. AC DC Power Transmiss.*, 2012, pp. 1–5.

[19] N. Deng, P. Wang, X. Zhang, G. Tang, and J. Cao, "A DC current flow controller for meshed modular multilevel converter multiterminal HVDC grids," *CSEE J. Power Energy Syst.*, vol. 1, no. 1, pp. 43–51, 2015.

[20] J. Sau-Bassols, E. Prieto-Araujo, O. Gomis-Bellmunt, and F. Hassan, "Series interline DC/DC current flow controller for meshed HVDC grids," *IEEE Trans. Power Del.*, vol. 33, no. 2, pp. 881–891, Apr. 2018.

[21] W. Chen, X. Zhu, L. Yao, X. Ruan, Z. Wang, and Y. Cao, "An interline DC power-flow controller (IDCPFC) for multiterminal HVDC system," *IEEE Trans. Power Del.*, vol. 30, no. 4, pp. 2027–2036, Aug. 2015.

[22] W. Chen et al., "A novel interline DC power-flow controller (IDCPFC) for meshed HVDC grids," *IEEE Trans. Power Del.*, vol. 31, no. 4, pp. 1719–1727, Aug. 2016.

[23] M. Ranjram and P. W. Lehn, "A multiport power-flow controller for DC transmission grids," *IEEE Trans. Power Del.*, vol. 31, no. 1, pp. 389–396, Feb. 2016.

[24] J. Sau-Bassols, R. Ferrer-San-José, E. Prieto-Araujo, and O. Gomis-Bellmunt, "Multiport interline current flow controller for meshed HVDC grids," *IEEE Trans. Ind. Electron.*, vol. 67, no. 7, pp. 5467–5478, Jul. 2020.

[25] J. Yi, M. Zhu, X. Zhong, H. Wang, and X. Cai, "An improved triple interline DC power flow controller for bidirectional power control," in *Proc. IEEE Region 10 Conf.*, 2020, pp. 1301–1306.

[26] X. Zhong, M. Zhu, Y. Li, S. Wang, H. Wang, and X. Cai, "Modular interline DC power flow controller," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 11707–11719, Nov. 2020.

[27] A. Mokhberdoran, J. Sau-Bassols, E. Prieto-Araujo, O. Gomis-Bellmunt, N. Silva, and A. Carvalho, "Fault mode operation strategies for dual H-bridge current flow controller in meshed HVDC grid," *Electric Power Syst. Res.*, vol. 160, pp. 163–172, 2018.

[28] S. Balasubramaniam, C. E. Ugalde-Loo, J. Liang, T. Joseph, R. King, and A. Adamczyk, "Experimental validation of dual H-bridge current flow controllers for meshed HVdc grids," *IEEE Trans. Power Del.*, vol. 33, no. 1, pp. 381–392, Feb. 2018.

[29] A. Mokhberdoran, O. Gomis-Bellmunt, N. Silva, and A. Carvalho, "Current flow controlling hybrid DC circuit breaker," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1323–1334, Feb. 2018.

[30] O. Cwikowski et al., "Integrated HVDC circuit breakers with current flow control capability," *IEEE Trans. Power Del.*, vol. 33, no. 1, pp. 371–380, Feb. 2018.

[31] S. Zhang, G. Zou, X. Wei, and C. Zhang, "Combined hybrid DC circuit breaker capable of controlling current flow," *IEEE Trans. Ind. Electron.*, vol. 68, no. 11, pp. 11157–11167, Nov. 2021.

[32] C. Zhang, G. Zou, S. Zhang, C. Xu, and W. Sun, "Multiport hybrid DC circuit breaker with current flow control for MTDC grids," *IEEE Trans. Power Electron.*, vol. 37, no. 12, pp. 15605–15615, Dec. 2022.

Hao Guo was born in Shaanxi, China, in 1999. He received the B.S. degree in new energy science and engineering from the Hohai University, Jiangsu, China, in 2021. He is currently working toward the M.S. degree in electrical engineering from Southeast University, Nanjing, China.

His research interests include HVdc and dc power flow controller.

Wu Chen (Senior Member, IEEE) was born in Jiangsu, China, in 1981. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2003, 2006, and 2009, respectively.

From 2009 to 2010, he was a Senior Research Assistant with the Department of Electronic Engineering, City University of Hong Kong, Hong Kong. In 2010 and 2011, he was a Postdoctoral Researcher with Future Electric Energy Delivery and Management Systems Center, North Carolina State University, Raleigh, NC, USA. Since September 2011, he has been an Associate Research Fellow with the School of Electrical Engineering, Southeast University, Nanjing, where he has been a Professor since 2016. His main research interests include soft-switching converters, power delivery, and power electronic system integration.

Dr. Chen is an Associate Editor for IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, *Journal of Power Electronics*, and *CPSS Transactions on Power Electronics and Applications*.

Yiqing Zhu was born in Jiangsu, China, in 2000. She received the B.S. degree in electrical engineering from the Nanjing Normal University, Jiangsu, China, in 2022. She is currently working toward the M.S. degree in electrical engineering with Southeast University, Nanjing, China.

Her research interests include high-power high-voltage converters and power flow controller.

Miao Zhu (Senior Member, IEEE) received the B.Sc. degree from Southeast University, Nanjing, China, in 2001, and the Ph.D. degree from Nanyang Technological University, Singapore, in 2009, both in electrical engineering.

During 2001–2002, he was an Assistant Engineer with Wuxi Power Supply Company, State Grid of China. From 2008 to 2009, he was with Meiden Asia Pte Ltd, Singapore, as an R&D Engineer. After that, he had been a Scientist in the Experimental Power Grid Centre, A∗STAR, Singapore. In Aug. 2012, he joined Shanghai Jiao Tong University (SJTU), China, as a Distinguished Researcher. He is currently the Professor of Electrical Engineering Department, SJTU, and the Vice Director of State Energy Smart Grid (Shanghai) R&D Center. Since 2018, he has been the Vice Chairman of both IEEE PELS Shanghai Chapter and IEEE IES Shanghai Chapter. His research interests include power converters, renewable energy generation, dc distributed power system, and dc grid.