Active Power Enhancement Control Strategy of Grid-Forming Inverters Under Asymmetrical Grid Faults

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***Abstract*—Due to the simple implementation and good dynamic response, the current-limiting gain control strategy (CLGCS) is widely utilized to limit the overcurrent of grid-forming inverters under asymmetrical grid faults. However, it will curtail the transmission capability of the active power (AP), which has not been investigated in detail before. In this article, its AP curtailment issue is first elaborated based on sequence networks. To enhance the transmission capability of the AP and ride-through asymmetrical grid faults simultaneously, an AP enhancement control strategy (APECS), including the proposed voltage-limiting gain control strategy (VLGCS) plus negative-sequence current feedback-based voltage compensation (NSCFVC) and the CLGCS, is proposed. The inverter output overvoltage and overcurrent are automatically limited by the proposed VLGCS and CLGCS without any fault detection. The transmission capability of the AP is enhanced with the proposed NSCFVC by eliminating negative-sequence fault currents. Consequently, the maximum inverter output phase voltage and current as well as the AP with both the CLGCS and the proposed APECS are comparatively analyzed based on sequence networks. The fault ride-through ability and enhanced transmission capability of the AP with the proposed APECS are verified by theoretical and experimental results.**

***Index Terms*—Active power (AP), asymmetrical grid faults, fault ride-through, Grid-forming (GFM) inverter, sequence network.**

NOMENCLATURE

GFM	Grid-forming.
GFL	Grid-following.
p.u.	Per-unit.
FRT	Fault ride-through.
VCM	Voltage control mode.
CCM	Current control mode.
CLG	Current-limiting gain.
CLGCS	Current-limiting gain control strategy.
AP	Active power.
APECS	Active power enhancement control strategy.
VLG	Voltage-limiting gain.
VLGCS	Voltage-limiting gain control strategy.
STRF	Stationary reference frame.
NRF	Neutral reference frame.
SRF	Synchronous reference frame.
NSCFVC	Negative-sequence current feedback-based voltage compensation.
SLG	Single line-to-ground.
LL	Line-to-line.
LLG	Line-to-line-to-ground.
$v^*_{Cp\alpha/\beta}$	Positive-sequence voltage reference in the STRF, generated from the droop control.
$v^*_{Cn\alpha/\beta}$	Negative-sequence voltage reference in the STRF, generated from NSCFVC.
$v^*_{C\alpha/\beta}$	Inner voltage reference in the STRF (input of the VLG).
$v^*_{C\alpha/\beta 1}$	Inner voltage reference in the STRF (output of the VLG).
$i^*_{\alpha/\beta}$	Inner current reference in the STRF (input of the CLG).
$i^*_{\alpha/\beta 1}$	Inner current reference in the STRF (output of the CLG).
$\dot{V}_{Cp/n}$	Internal positive-/negative-sequence phase voltage (p.u.).
$\dot{V}_{invp/n}$	Positive-/negative-sequence phase voltage of the GFM inverter (p.u.).
$\dot{V}_{fp/n/z}$	Positive-/negative-/zero-sequence phase voltage at the fault location (p.u.).
$\dot{I}_{op/n/z}$	Output positive-/negative-/zero-sequence current of the GFM inverter.
$\dot{I}_{fp/n/z}$	Fault positive-/negative-/zero-sequence current.
$\dot{V}_g/V_g$	Grid voltage (p.u.)/grid voltage magnitude (V).
Z_v	Virtual impedance (p.u.).
Z_T	Transformer impedance (p.u.).
Z_g	Grid impedance (p.u.).
Z_f	Fault impedance (p.u.).
I_{th}/V_{th}	Current threshold (A)/voltage threshold (V).
$I^*_{\max}$	Maximum magnitude of $i^*_{\alpha/\beta}$ transferred in the NRF (A).
$I_{\max}$	Maximum magnitude of GFM inverter output currents (A).
K_I/K_V	CLG/VLG.

Manuscript received 11 April 2023; revised 22 July 2023 and 28 August 2023; accepted 29 September 2023. Date of publication 4 October 2023; date of current version 6 December 2023. This work was supported in part by the Natural Sciences and Engineering Research Council of Canada and in part by the Major Innovation Fund from the Government of Alberta. Recommended for publication by Associate Editor Y. Tang. *(Corresponding author: Cheng Xue.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3322042.

Digital Object Identifier 10.1109/TPEL.2023.3322042

P_{inv} Inverter output AP during the fault (p.u.).
$V_{\max}$ Maximum phase voltage magnitude (V).
$V^*_{C\max}$ Maximum magnitude of $v^*_{C\alpha/\beta}$ transferred in the NRF (V).

I. Introduction

RENEWABLE energy sources, such as wind and photovoltaics, are widely integrated into the power system via voltage source converters (VSCs) to relieve global warming caused by carbon dioxide emissions [1]. Among these VSCs, GFM inverters are gradually favored and adopted because they can operate in both grid-connected and islanded modes thanks to their voltage source behavior [2]. In addition, compared with GFL inverters, GFM inverters can be connected to weak grids stably [3].

The common asymmetrical grid faults that include SLG, LL, and LLG faults are shown in Fig. 1. Unlike traditional synchronous generators, which can tolerate 5–7 p.u. of overcurrent under asymmetrical grid faults, GFM inverters can only handle up to 1.2–1.5 p.u. of overcurrent owing to the low thermal inertia of semiconductor switches [4], [5]. Traditionally, GFM inverters can be tripped to protect the power system and themselves from overcurrent, but in the modern power-electronics-based power system with critical loads, GFM inverters are required to remain connected to the power system and ride through grid faults. Therefore, FRT strategies for current limiting are vital in the modern power system.

The FRT strategies of the GFM inverter can be classified into indirect and direct current-limiting strategies according to the regulation manner of the current references. Indirect current-limiting strategies can prevent overcurrent by modifying voltage references of outer voltage loops, or power references. For example, the traditional virtual impedance, which is utilized to prevent power coupling and improve stability [6], is designed to limit overcurrent under grid faults [7], [8], [9], [10], [11], [12], [13], [14]. However, the virtual impedance design usually considers the most severe condition (symmetrical grid faults) [14]. This will limit the fault current to a quite low value under asymmetrical grid faults, which may deteriorate the rapid detection and fault clearance of the protection system. In addition to virtual impedance, the positive-negative-zero-sequence limiting with stability-enhanced *P-f* droop control is proposed to limit inverter output current and voltage under grid faults [15], [16], but the parameter design is complicated, and the control speed is not fast since it operates in the outer voltage loop. The disadvantages of indirect current-limiting strategies are that the control design is complicated, and the control bandwidth is low.

Compared with indirect current-limiting strategies, direct current-limiting strategies modify current references directly under grid faults, and control modes are transferred from the VCM into the CCM. The simplest current-limiting strategy is instantaneous current limiting [17], [18], [19]. However, it is abandoned owing to the manifest drawback that it will clip the crest of sinusoidal references, causing harmonic distortion and even instability. The latched current-limiting strategy is that a predetermined current reference will replace the prefault current reference when the current is higher than a threshold [14], [17], [19], [20], [21]. The disadvantages of this scheme are that the set and reset signals and mode switching procedures should be carefully designed, otherwise the latch-up issue will arise. Consequently, the CLGCS is proposed based on the magnitudes of current references without causing harmonic distortion [10], [19], [22], [23], [24]. Moreover, the control mode can be switched to CCM automatically without any fault detection, hence avoiding set and reset signals. Therefore, the direct current-limiting strategies are simple and rapid control strategies can prevent overcurrent under grid faults.

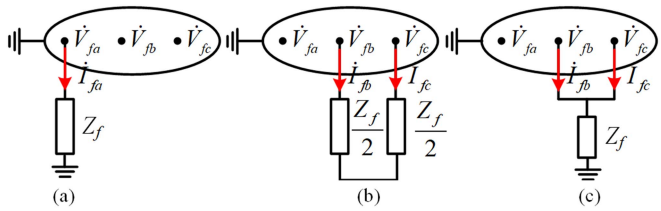

Fig. 1. Representation of a system under three asymmetrical grid faults. (a) SLG fault. (b) LL fault. (c) LLG fault.

In this article, the CLGCS is utilized to limit the overcurrent of GFM inverters under asymmetrical grid faults thanks to its simple implementation and good dynamic response [19]. However, the AP curtailment issue with the CLGCS under asymmetrical grid faults exists but has not been well investigated before. Moreover, according to the newest IEEE Standard 2800-2022, the inverter-based resource unit can operate in active current priority mode or reactive current priority mode required by the system operator [25]. Some FRT strategies in reactive current priority have been proposed, but FRT schemes in active current priority mode are seldom researched [26], [27]. In addition, the AP enhancement will be beneficial to improving the *P–δ* relation of the GFM inverter that synchronizes with the grid through AP control, which has not been analyzed before. Therefore, to fill this gap, this article elaborates on the AP curtailment issue with the CLGCS under asymmetrical grid faults based on the sequence networks first. Subsequently, the APECS is proposed to enhance the AP under asymmetrical grid faults. The contributions of this article and the proposed APECS are highlighted as follows.

1) The AP curtailment issue under various asymmetrical grid faults, including SLG faults, LL faults, and LLG faults, with the CLGCS is well investigated based on sequence networks, which has not been analyzed in detail before. In addition, the transmission capability of the AP is significantly enhanced with the proposed APECS because the negative-sequence currents are eliminated by the proposed NSCFVC of the proposed APECS, which fills the gap of existing works. Moreover, the AP enhancement will help improve the *P–δ* relation of the GFM inverter that synchronizes with the grid via AP control.

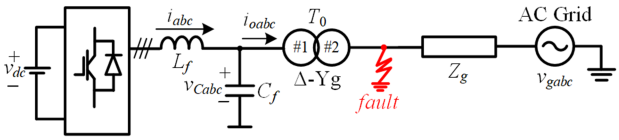

Fig. 2. Single-line diagram of a grid-connected GFM inverter.

2) The voltage source behavior can be maintained during the steady-state fault period when the proposed APECS can reduce the maximum inverter output current below the current threshold I_{th} of the CLGCS. In this scenario, the current-limiting ability of the CLGCS is achieved by the proposed APECS, hence the control is in VCM.
3) The proposed APECS shows high flexibility because it can be activated automatically under grid faults without any fault detection requirement. In addition, this control strategy is independent of network impedances, fault locations, and fault types.

II. System Configuration and Control

A. System Configuration

The single-line diagram of a grid-connected GFM inverter is shown in Fig. 2, where v_{dc} denotes the dc voltage, L_f denotes the inverter-side filter inductor, C_f denotes the filter capacitor, and L_T denotes the leakage inductor of the transformer T_0. These three components constitute an *LCL* filter to attenuate switching ripples. The grid is represented by a voltage source v_{gabc} and its Thevenin equivalent impedance Z_g. Besides, i_{abc}, i_{oabc}, and v_{Cabc} denote inverter-side currents, grid-side currents, and capacitor voltages, respectively. The asymmetrical grid faults occur at the *Yg* side of the transformer T_0.

B. Control System

The block diagram of the control system of the GFM inverter is shown in Fig. 3. The capacitor voltages v_{Cabc}, grid-side currents i_{oabc}, and inverter-side currents i_{abc} are transferred into signals in the STRF via *Clarke* transformation. The active and reactive powers are calculated in the STRF and filtered by low-pass filters, the cutoff angular frequency of which is ω_c. The typical *P-f* and *Q-V* droop controls are utilized to generate the inner voltage reference and frequency reference. The corresponding droop control parameters are listed in Table I. The transient stability enhanced control (TSEC) is adopted here to prevent the transient instability problem under asymmetrical grid faults, where the *q*-axis capacitor voltage v_{Cq} is derived from *Park* transformation, as shown in Fig. 3. The voltage v_{Cq}, multiplied by the feedback gain k_{oq}, is added with the fundamental angular frequency setpoint ω_0 and $m(P_0-P)$ to obtain the reference angular frequency ω^*. The feedback gain k_{oq} of the TSEC is selected as 0.4 in this article [28].

The proposed APECS is comprised of the proposed NSCFVC, the proposed VLGCS, and the CLGCS three schemes, which will be introduced in Sections IV and V in detail. The virtual inductance is used to decouple the active and reactive droops [6]. The voltage references $v^*_{C\alpha 1}$ and $v^*_{C\beta 1}$ are fed to the inner voltage control loop. The signals are in the STRF; hence, proportional-resonant (PR) controllers are adopted to realize zero steady-state error at the fundamental frequency. The nonideal PR controller considering the frequency deviation is written as [29]

$$H_{PRv}(s) = K_{pv} + R_v(s) = K_{pv} + \frac{K_{rv}s}{s^2 + 2\omega_i s + \omega_0^2} \quad (1)$$

where K_{pv} is the proportion gain of the PR controller; K_{rv} is the resonant gain of the PR controller; ω_i is the bandwidth of the resonant part; ω_0 is the fundamental angular frequency. In addition, a tracking integration antiwindup scheme is adopted here to prevent the windup of the voltage controller [17], [23], where g_1 is the antiwindup gain, chosen as 1.5 in this article.

TABLE I
Experimental Parameters

Symbol	Description	Value
S_b	Rated power	500 VA
V_{dc}/V_n	DC Voltage/Grid Voltage (LL, RMS)	250 V/104 V
L_f/C_f	Inverter filter inductance/capacitance	3 mF/30 μF
Z_T	Inductance of transformer T_0 ($D1$-Yg)	0.042 pu
L_v	Virtual inductance	2 mH
L_g	Grid inductance	5 mH/1 mH
K_{pv}/K_{rv}	Proportional/Resonant gain of voltage controller	0.1/80
K_{pi}/K_{ri}	Proportional/Resonant gain of current controller	15/500
K_{Pl}/K_{Ii}	Proportional/Integral gain of NSCFVC	4/200
m/n	Droop gain	0.01/0.1
P_0	AP setting value	500 W
Q_0	Reactive power setting value	0 Var
ω_0	Frequency setting value	377 rad/s
V_0	Voltage setting value	84.85 V
f_{sw}	Switching frequency	10 kHz
ω_c	Cut-off angular frequency	2π20 rad/s
ω_i	Bandwidth of the resonant part	π rad/s
k_{oq}	Proportional gain of TSEC	0.4
Z_f	Fault resistance	3.9/1/6.8 Ω

III. Sequence Network Modeling Under Different Asymmetrical Grid Faults

To obtain a general form for the faulty system, the GFM inverter system during asymmetrical grid faults can be illustrated in sequence networks, as shown in Fig. 4 [16], [30].

In Fig. 4, the equivalent positive-sequence, negative-sequence, and zero-sequence impedance can be deduced as

$$Z_p = (Z_v + Z_T)\,||\,Z_g,\ Z_n = (Z_v + Z_T)\,||\,Z_g,\ Z_z = Z_g||Z_T/2. \quad (2)$$

Then, the equivalent positive-sequence phase voltage $\dot{V}_p$ can be calculated as

$$\dot{V}_p = \frac{Z_g}{Z_g + Z_T + Z_v}\dot{V}_{Cp}b + \frac{Z_T + Z_v}{Z_g + Z_T + Z_v}\dot{V}_g \quad (3)$$

where $b = e^{j\pi/6}$ for the *D1-Yg* transformer. The equivalent negative-sequence phase voltage $\dot{V}_n$ can be derived as

$$\dot{V}_n = \frac{Z_g}{Z_v + Z_T + Z_g}\dot{V}_{Cn} \cdot c \quad (4)$$

where $c = e^{-j\pi/6}$ for the *D1-Yg* transformer.

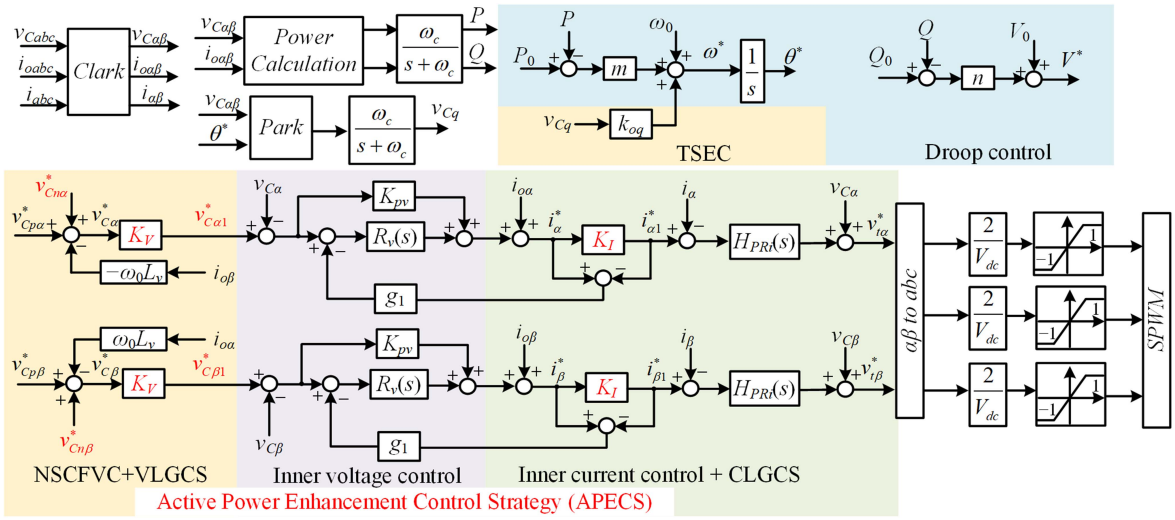

Fig. 3. Block diagram of the control system.

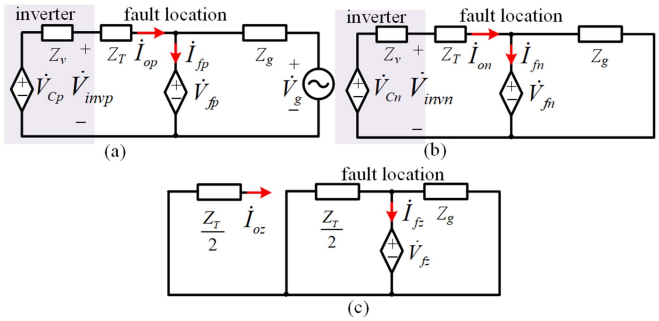

Fig. 4. Sequence networks of the GFM inverter. (a) Positive sequence. (b) Negative sequence. (c) Zero sequence.

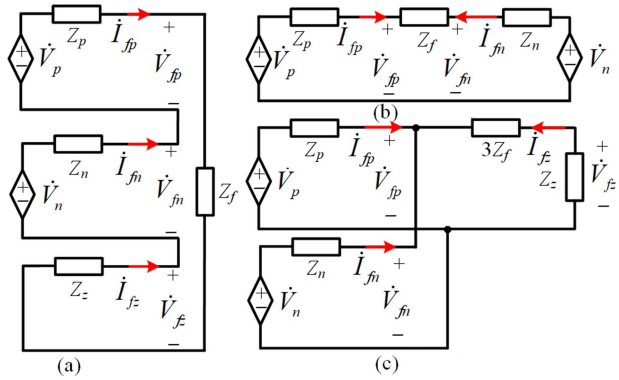

Fig. 5. Interconnected sequence networks under different asymmetrical grid faults. (a) SLG fault. (b) LL fault. (c) LLG fault.

According to Fig. 2, the voltages and currents at the fault location under various asymmetrical grid faults are expressed as

$$\begin{cases} \dot{I}_{fb}=\dot{I}_{fc}=0, \dot{V}_{fa}=Z_f\dot{I}_{fa}. & \text{SLG fault} \\ \dot{I}_{fb}=-\dot{I}_{fc}, \dot{V}_{fb}-\dot{V}_{fc}=Z_f I_{fb}, I_{fa}=0. & \text{LL fault} \\ \dot{I}_{fa}=0, \dot{V}_{fb}=\dot{V}_{fc}, \dot{V}_{fb}=Z_f\left(\dot{I}_{fb}+\dot{I}_{fc}\right). & \text{LLG fault} \end{cases} \tag{5}$$

The quantities in (5) can also be transferred to the quantities in the sequence domain under different asymmetrical grid faults, the specific deduction process can refer to Glover et al. [30], which is omitted for page limitation. The consequent equation in the sequence domain is written as

$$\begin{cases} \dot{I}_{fp}=\dot{I}_{fn}=\dot{I}_{fz}=0, \dot{V}_{fp}+\dot{V}_{fn}+\dot{V}_{fz}=3Z_f\dot{I}_{fp}. & \text{SLG} \\ \dot{I}_{fz}=0, \dot{I}_{fp}=-\dot{I}_{fz}, \dot{V}_{fp}-\dot{V}_{fn}=Z_f\dot{I}_{fp}. & \text{LL} \\ \dot{I}_{fp}+\dot{I}_{fn}+\dot{I}_{fz}=0, \dot{V}_{fz}-\dot{V}_{fp}=3Z_f\dot{I}_{fz}, \dot{V}_{fp}=\dot{V}_{fn}. & \text{LLG} \end{cases} \tag{6}$$

Combining (2)–(6) and Fig. 4, the interconnected sequence networks under various asymmetrical grid faults are depicted in Fig. 5.

Consequently, substituting (2)–(4) into (6), the phase voltages $\dot{V}_{fp}$, $\dot{V}_{fn}$, and $\dot{V}_{fz}$ at the fault location and fault currents $\dot{I}_{fp}$, $\dot{I}_{fn}$, and $\dot{I}_{fz}$ in the sequence domain can be calculated. Subsequently, the phase voltages $\dot{V}_{invp/n}$ and phase currents $\dot{I}_{op/n/z}$ can de deduced in Fig. 4; thus, phase voltages and phase currents in the NRF can be derived from the following equation:

$$\begin{bmatrix} X_a \\ X_b \\ X_c \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ a^2 & a & 1 \\ a & a^2 & 1 \end{bmatrix} \begin{bmatrix} X_p \\ X_n \\ X_z \end{bmatrix} \tag{7}$$

where X_{abc} denotes phase voltages or phase currents in the NRF. To simplify the calculation, all variables in this article are expressed in per unit values.

Using the parameters in Table I, the maximum inverter output phase current without any FRT strategy under the SLG, LL, and LLG faults with the increasing fault resistance can be obtained in (7) and depicted in Fig. 6. In this article, 1.5 p.u. is selected as the maximum inverter output phase current threshold I_{th} under asymmetrical grid faults. It is shown that the maximum inverter output phase current is significantly higher than the current threshold I_{th} under asymmetrical grid faults. As the fault resistance increases, the maximum inverter output current decreases under SLG and LL faults. However, as the fault resistance rises, the maximum inverter output current under the

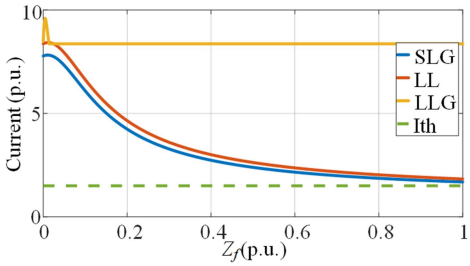

Fig. 6. Maximum inverter output phase current without any FRT strategy under the SLG, LL, and LLG faults as the fault resistance increases.

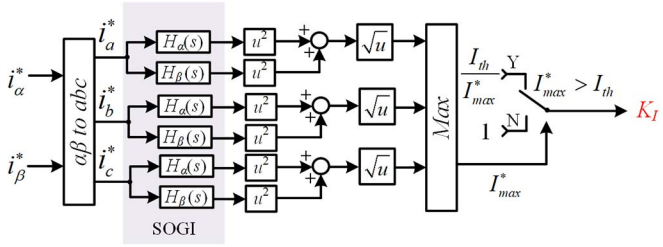

Fig. 7. Block diagram of the CLGCS.

LLG fault maintains a high value. This is because two phases are directly connected, as shown in Fig. 1. Compared with LL and LLG faults, the overcurrent is more severe under the LLG fault.

IV. Current-Limiting Gain Control Strategy and Its AP Curtailment Issue

A. Current-Limiting Gain Control Strategy (CLGCS)

To protect the GFM inverter from overcurrent, current-limiting FRT strategies are necessary under various grid faults. Compared with the virtual impedance, which depends on the fault location, fault types, and network impedances, the CLGCS is a simpler FRT control scheme that operates directly in the inner current control loop [10], [23]. The block diagram of the CLGCS is shown in Fig. 7.

As shown in Fig. 7, the inner current references in the STRF are transferred into signals in the NRF. To obtain the magnitude of each current reference, the second-order generalized integrator (SOGI) is utilized to generate one signal with the same phase and magnitude as the input signal, and another signal with the same magnitude but delayed phase by one-quarter period as the input signal [31]. The transfer functions of $H_\alpha(s)$ and $H_\beta(s)$ are given as

$$H_\alpha(s) = \frac{k\omega_1 s}{s^2 + k\omega_1 s + \omega_1^2}, H_\beta(s) = \frac{k\omega_1^2}{s^2 + k\omega_1 s + \omega_1^2} \quad (8)$$

where k is the SOGI proportional gain. Then, the square root of the sum of squares of two current signals from the SOGI is the magnitude of the current reference in the NRF. When $I^*_{\max}$ is no more than the threshold I_{th}, K_I is 1. When $I^*_{\max}$ is larger than I_{th}, K_I is defined by $I_{th}/I^*_{\max}$. The CLGCS directly operates in the current control loop with a short transient response time, which is as fast as the virtual admittance in the inner current control loop [7], [27], [32] and more rapid than the traditional virtual impedance in the inner voltage control loop [33]. In addition, it is effective for all types of grid faults, and the fault detection procedure is not required.

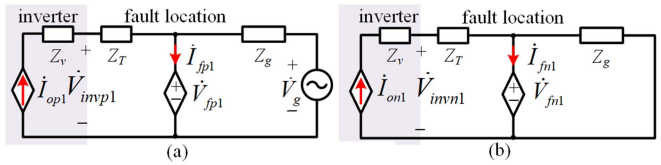

Fig. 8. Sequence networks of the GFM inverter with the CLGCS. (a) Positive sequence. (b) Negative sequence.

B. AP Curtailment Issue

The AP of the GFM inverter under asymmetrical grid faults can be calculated by

$$P_{inv} = \mathrm{Re}\left(\dot{V}_{invp} \cdot \bar{\dot{I}}_{op}\right) + \mathrm{Re}\left(\dot{V}_{invn} \cdot \bar{\dot{I}}_{on}\right) \quad (9)$$

where $\bar{\dot{I}}_{op}$ and $\bar{\dot{I}}_{on}$ are conjugate values of $\dot{I}_{op}$ and $\dot{I}_{on}$, respectively. When the maximum inverter output phase current during the fault is higher than I_{th}, it will be scaled down by the CLGCS to I_{th}. Unfortunately, negative-sequence currents will cause a severe imbalance in three phases and increase the current magnitude in one phase. Hence, currents at other phases will also be scaled down much lower than the threshold, thereby reducing the AP significantly. This will be verified by the following calculation. When no current-limiting strategy is applied, $\dot{V}_{invp}$, $\dot{I}_{op}$, $\dot{V}_{invn}$, and $\dot{I}_{on}$ can be obtained from the sequence network in Figs. 4 and 5 under different asymmetrical grid faults. However, when the CLGCS is applied, the control mode is switched from the VCM to the CCM. Thus, the sequence networks of the GFM inverter with the CLGCS are shown in Fig. 8, where the zero-sequence diagram is omitted because of no change.

Assuming the phase angle of the inverter output phase current with the CLGCS is unchanged when the fault occurs and the inverter-side currents i_{abc} are closed to grid-side currents i_{oabc}, the positive-sequence and negative-sequence controlled current sources are derived as

$$\dot{I}_{op1} = \dot{I}_{op} \cdot K_I, \dot{I}_{on1} = \dot{I}_{on} \cdot K_I. \quad (10)$$

Then, the equivalent positive-sequence and negative-sequence voltage sources in Fig. 4 can be deduced as

$$\dot{V}_p = \dot{I}_{op1} \cdot Z_g \cdot b, \dot{V}_n = I_{on1} \cdot Z_g \cdot c. \quad (11)$$

In addition, the equivalent positive-sequence, negative-sequence, and zero-sequence impedance can be calculated as

$$Z_p = Z_g, Z_n = Z_g, Z_z = Z_z. \quad (12)$$

Consequently, adopting the parameters in Table I, the AP with the CLGCS under asymmetrical grid faults is plotted in Fig. 9 for various fault resistances.

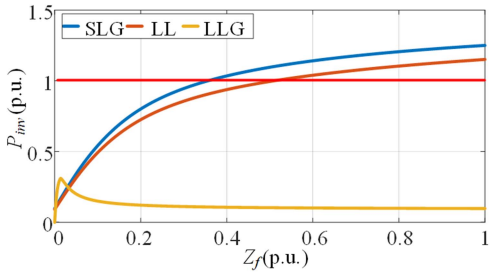

Fig. 9. AP with the CLGCS under asymmetrical grid faults.

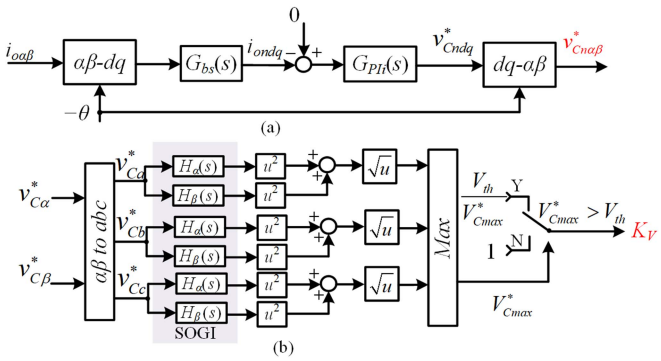

Fig. 10. Block diagram. (a) NSCFVC. (b) VLGCS.

As shown in Fig. 9, the LLG fault is the most severe fault because two phases are directly connected and then grounded via fault resistances. Therefore, the AP is much less than 1 p.u. during the fault and stays at a low value although the fault resistance increases. In addition, the AP under the SLG fault and LL fault with small fault resistances is also less than 1 p.u., and the LL fault is more severe than the SLG fault. Therefore, the AP is significantly curtailed under asymmetrical grid faults.

V. Proposed APECS

The AP is significantly curtailed because the CLGCS scales down the inner current references i^*_α and i^*_β based on the maximum inverter output phase current magnitude. If these references can be reduced before they are input into K_I, K_I will be higher, and the inner current references $i^*_{\alpha 1}$ and $i^*_{\beta 1}$ will not be significantly scaled down. In addition, the negative-sequence components of inverter output currents will also increase the maximum inverter output current magnitude; thus, K_I will be lower, and the AP will be curtailed. Therefore, if the negative-sequence components of i^*_α and i^*_β can be eliminated under asymmetrical grid faults, $I^*_{\max}$ can be reduced, and K_I will be enhanced. Consequently, the AP can be improved.

A. Proposed NSCFVC Plus VLGCS

To enhance the AP and prevent overvoltage, NSCFVC and VLGCS are simultaneously proposed and shown in Fig. 10(a) and (b).

The control objective of the proposed NSCFVC is to eliminate negative-sequence components of inverter output phase currents and subsequently enhance the AP. Specifically, a virtual

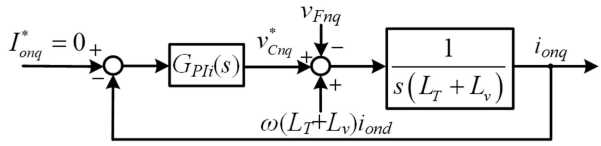

Fig. 11. Block diagram of the NSCFVC in the d-axis.

negative-sequence voltage source $\dot{V}_{Cn}$, as shown in Fig. 4(b), can be injected in the voltage control loop. When $\dot{V}_{Cn}$ is equal to $\dot{V}_{fn}$, the negative-sequence component of the inverter output current $\dot{I}_{on}$ is zero. The value of $\dot{V}_{Cn}$ can be calculated in the sequence network as

$$\dot{V}_{Cn} = \begin{cases} Z_n / \left[ck_4 \left(Z_p + Z_n + Z_Z + Z_f\right)\right] \dot{V}_p, \text{SLG} \\ Z_n / \left[ck_4 \left(Z_p + Z_n + Z_Z + Z_f\right)\right] \dot{V}_p, \text{LL} \\ k_5 / \left[cZ_p \left(1 - k_5 k_3 / Z_n\right)\right] \dot{V}_p, \text{LLG} \end{cases} \tag{13}$$

where

$$\begin{cases} k_3 = Z_g / \left(Z_g + Z_T + Z_v\right) \\ k_4 = 1 - k_3 + Z_n k_3 / \left(Z_p + Z_n + Z_f\right) \\ k_5 = 1 / \left[1/Z_p + 1/Z_n + 1/\left(3Z_f + Z_z\right)\right] \end{cases}. \tag{14}$$

However, in practical situations, the line impedance, fault location, and fault types are unknown. Thus, the virtual negative-sequence voltage source can be obtained by eliminating the negative-sequence current via a feedback control, as shown in Fig. 10(a). The NSCFVC can be activated in the normal condition because in the normal condition, the negative-sequence current i_{ondq} is zero, hence the virtual negative-sequence voltage $v^*_{Cn\alpha\beta}$ is zero, without impacting on the normal operation of the system. When the fault happens, the negative-sequence current i_{ondq} is eliminated by the NSCFVC, reducing the maximum output phase current of the GFM inverter.

In Fig. 10(a), the inverter output currents $i_{o\alpha\beta}$ in the STRF are transferred into currents in the SRF through *Park* transformation with $-\theta$. The notch filters are used to block second frequency signals. Then, the negative-sequence inverter output currents are obtained in the SRF. The transfer function of the notch filter is shown as

$$G_{bs}(s) = \frac{s^2 + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{15}$$

where the neutral angular frequency $\omega_n = 2\pi \cdot 120$ rad/s; the damping ratio $\zeta = 0.707$. The current reference is zero, and the differences between the reference and negative-sequence inverter output currents are regulated by proportional-integral (PI) controllers. The output signals are transferred into signals in the STRF through inverse *Park* transformation. The NSCFVC control loop in the d-axis is shown in Fig. 11, where v_{Fnd} is the d-axis negative-sequence voltage at the fault location.

To simplify the analysis, v_{Fnd} and $\omega(L_T+L_v)i_{onq}$ can be regarded as disturbances and neglected. Then, the open-loop transfer function can be obtained. The PI controller is easy to be designed and omitted here.

However, the virtual negative-sequence voltage compensation $v^*_{Cn\alpha\beta}$ in the proposed NSCFVC may increase the inverter output phase voltage. Therefore, the proposed VLGCS

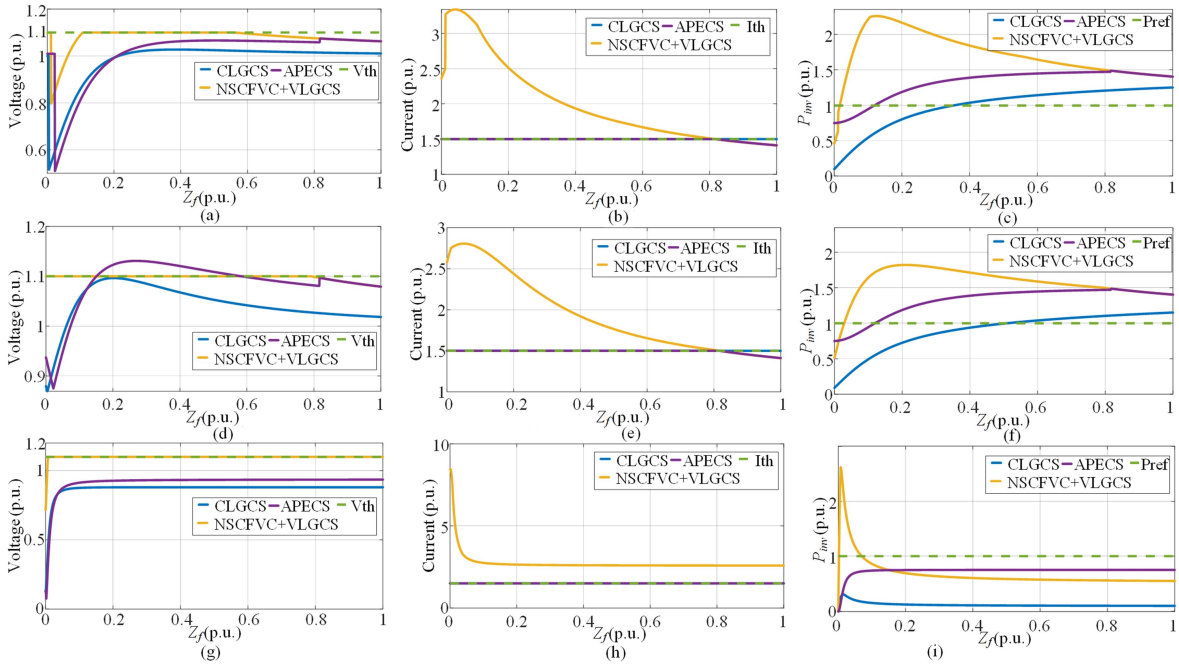

Fig. 12. Maximum inverter output phase voltage, current, and AP with the CLGCS, the proposed NSCFVC+VLGCS, and the proposed APECS under different asymmetrical grid faults as the fault resistance increases. (a) Voltage under SLG fault. (b) Current under SLG fault. (c) AP under SLG fault. (d) Voltage under LL fault. (e) Current under LL fault. (f) AP under LL fault. (g) Voltage under LLG fault. (h) Current under LLG fault. (i) AP under LLG fault.

is utilized to reduce the inner voltage references $v^*_{C\alpha/\beta}$, as shown in Fig. 10(b), in case of inverter output overvoltage. The reference voltages $v^*_{C\alpha}$ and $v^*_{C\beta}$ in the STRF are transferred into signals v^*_{Ca}, v^*_{Cb}, and v^*_{Cc} in the NRF. The maximum magnitude of v^*_{Ca}, v^*_{Cb}, and v^*_{Cc} is calculated and denoted as v^*_{Cmax}. And the voltage threshold V_{th} is set as 1.1 p.u of the nominal voltage magnitude [34]. When V^*_{Cmax} is larger than V_{th}, K_V is V_{th}/V^*_{Cmax}, otherwise K_V is 1. Consequently, as shown in Fig. 3, the new voltage references $v^*_{C\alpha1}$ and $v^*_{C\beta1}$ are generated by multiplying old voltage references $v^*_{C\alpha}$ and $v^*_{C\beta}$ with the voltage-limiting gain K_V. Therefore, the inverter output overvoltage can be mitigated by the proposed VLGCS. In addition, compared with the inverter output phase voltage mitigation control scheme in [16], the proposed VLGCS is very simple to operate and independent of the fault types, fault locations, and types of transformer winding connection.

Substituting (13) and (14) into Figs. 4 and 5, $v^*_{C\alpha\beta}$ and other variables can be also derived. Consequently, the positive-sequence and negative-sequence components of GFM inverter output phase voltages can be replaced by

$$\dot{V}_{Cp} = K_V \cdot \dot{V}_{invp}, \dot{V}_{Cn} = K_V \cdot \dot{V}_{invn}. \tag{16}$$

Then, the maximum inverter output phase voltage, current, and AP with the CLGCS and proposed NSCFVC+VLGCS under asymmetrical grid faults are plotted in Fig. 12(a)–(i). Compared with the CLGCS, the AP is significantly enhanced with the proposed NSCFVC+VLGCS. However, the overcurrent still exists in the proposed NSCFVC+VLGCS. This is because the proposed NSCFVC+VLGCS has no strong current-limiting ability. The maximum phase voltage is limited at the voltage threshold V_{th} in the proposed NSCFVC+VLGCS, which verifies its overvoltage-limiting ability.

B. Proposed APECS

To limit the overcurrent and improve the AP under asymmetrical grid faults, the proposed NSCFVC+VLGCS is combined with the CLGCS, and the three schemes constitute the proposed APECS. The proposed NSCFVC+VLGCS operates at the inner voltage control loop with a low bandwidth. On the contrary, the CLGCS operates in the current control loop under asymmetrical grid faults with a high bandwidth. Therefore, the CLGCS has a strong current-limiting ability and good dynamic performance. However, the proposed NSCFVC+VLGCS enhances the AP under asymmetrical grid faults. Therefore, the proposed APECS, which includes three schemes, can not only mitigate overcurrent and overvoltage but also enhance the AP under asymmetrical grid faults.

To compare the FRT ability and transmission capability of the AP, maximum inverter output phase voltage, current, and AP under various asymmetrical grid faults with the CLGCS, the proposed NSCFVC+VLGCS, and the proposed APECS are plotted in Fig. 12(a)–(i).

In terms of the maximum inverter output phase voltage, the CLGCS and the proposed NSCFVC+VLGCS will not result in overvoltage under any asymmetrical grid fault. Additionally, there is no overvoltage with the proposed APECS under SLG and LLG faults except a little overvoltage under the LL fault. However, the maximum overvoltage is 1.13 p.u. (0.03 p.u. higher than the voltage threshold V_{th}) with the proposed APECS, which is not severe for the system.

In terms of the maximum inverter output phase current, the proposed NSCFVC+VLGCS will cause more severe overcurrent than the CLGCS and the proposed APECS under different asymmetrical grid faults since the proposed NSCFVC+VLGCS has no strong current-limiting ability. On the contrary, the maximum inverter output phase current with the CLGCS is limited at *I*th under any asymmetrical grid fault. In addition, the maximum inverter output phase current with the proposed APECS is limited at the current threshold *I*th under the SLG fault and the LL fault when the fault resistance is small; hence, the control is in CCM. However, as the fault resistance increases, the maximum inverter output phase current may fall below the current threshold *I*th. In this scenario, the CLGCS is deactivated, and the control mode is switched from the CCM to the VCM. Moreover, under the LLG fault, the maximum inverter output phase current is limited at the current threshold with the proposed APECS.

In terms of the maximum AP, the AP with the CLGCS falls more significantly under the LLG fault than other faults. In addition, compared with the CLGCS, the proposed NSCFVC+VLGCS and the proposed APECS enhance the AP significantly under various asymmetrical grid faults. Although the proposed NSCFVC+VLGCS has a better AP enhancement capability than the proposed APECS, it will cause severe overcurrent.

In summary, the proposed APECS has better overvoltage and overcurrent-limiting abilities than the proposed NSCFVC+VLGCS. Moreover, it has a better AP enhancement capability than the CLGCS under different asymmetrical grid faults.

C. P–δ Relation Improvement Analysis

Compared with the CLGCS, voltages at the fault location with the proposed APECS alter slightly. Therefore, the AP flows into the fault location with both the CLGCS and the proposed APECS is approximate. However, the AP of the GFM inverter during asymmetrical grid faults with the proposed APECS is significantly enhanced; hence, the excessive AP generated by the GFM inverter with the proposed APECS will be delivered to the power grid.

The GFM inverter synchronizes with the power grid through the *P-f* droop control (AP control), as shown in Fig. 3. Assuming the TSEC is deactivated during faults, the derivative of the internal angle can be deduced as

$$\dot{\delta} = \omega^* - \omega = m\left(P_0 - P\right) \tag{17}$$

where δ is the virtual power angle (VPA) between the capacitor voltage and grid voltage; P_0 is the AP setting value. Under grid faults, if the maximum AP of the GFM inverter is not lower than P_0, the derivative of VPA δ can equal zero. Consequently, the VPA δ can maintain a constant value, and the system is stable. This phenomenon can be illustrated in the VPA curve, as shown in Fig. 13. Under normal conditions, the maximum AP $P_{\max}$ of the GFM inverter is much higher than P_0; hence, in steady state, the VPA of the GFM inverter is maintained at δ_0. However, under faulty conditions, the AP of the GFM inverter with the CLGCS is significantly curtailed, as analyzed in Section IV. The maximum AP $P_{\max 2}$ of the GFM inverter with the CLGCS may be lower than P_0, as shown in Fig. 13. Due to no stable equilibrium point (SEP) existing, the GFM inverter with the CLGCS will lose synchronization with the power grid and turn into transient instability. However, under faulty conditions, with the proposed APECS, the AP of the GFM inverter is significantly improved. As a result, the maximum AP $P_{\max 1}$ may be larger than P_0, as shown in Fig. 13. One SEP at δ_1 exists, and the system can maintain its transient stability during the fault.

Therefore, the *P*–δ relation of the GFM inverter under asymmetrical grid faults will be improved with the proposed APECS since the AP is enhanced.

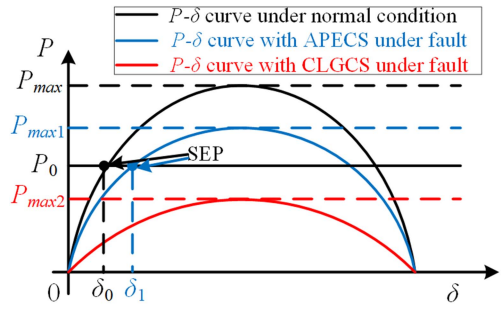

Fig. 13. VPA curves under different operating conditions.

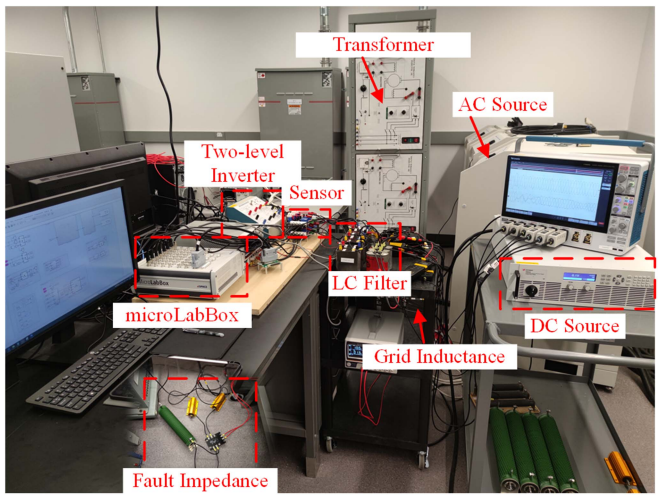

Fig. 14. Experimental setup of the grid-connected GFM inverter system.

VI. Experimental Verifications

To verify the FRT ability and AP enhancement capability of the proposed APECS, an experimental platform is set up in the laboratory, as shown in Fig. 14. The dSPACE MicroLabBox DS1202 is adopted as the digital controller. The fault impedance is cut in via the solid-state relay SSR3-D48100ZK. The experimental parameters are listed in Table I.

A. FRT Performance of the Proposed APECS

The FRT current-limiting performance under various asymmetrical grid faults is verified for two different short-circuit

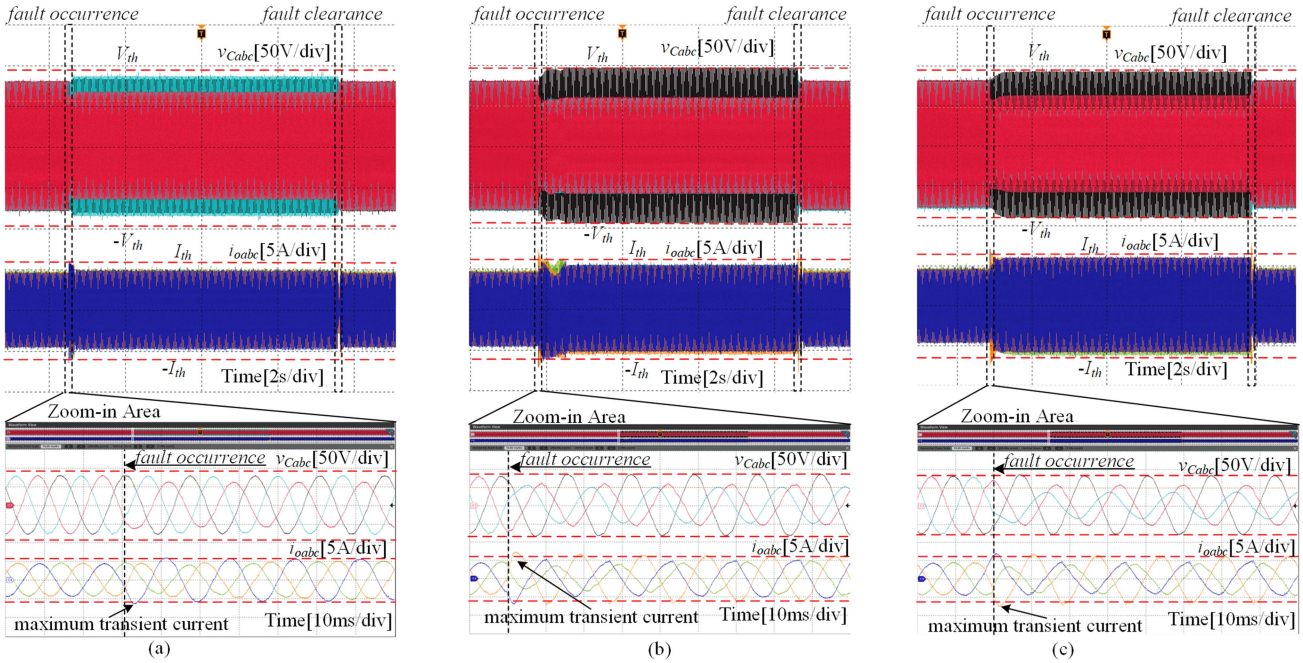

Fig. 15. Experimental results of inverter output phase voltages and currents with the proposed APECS under different asymmetrical grid faults at the 5-mH grid inductance. (a) APECS under SLG fault. (b) APECS under LL fault. (c) APECS under LLG fault.

TABLE II
EXPERIMENTAL RESISTANCES

L_g	SCR	SLG	LL	LLG
5 mH	5.85	3.9 Ω	3.9 Ω	1 Ω/3.9 Ω
1 mH	9.9	3.9 Ω	6.8 Ω	1 Ω/6.8 Ω

ratios (SCRs), and the specific fault resistances under different conditions are listed in Table II. In the SLG fault experiment, the fault resistor in Table II is utilized to connect one phase with the ground. In the LL fault experiment, the fault resistor is in Table II utilized to connect two phases. In the LLG fault experiment, for safety considering, two 1-Ω resistors are adopted to connect two phases in case of direct connection, and another resistor in Table II is utilized to connect the midpoint of the two 1-Ω resistors with the ground.

Fig. 15 shows the experimental results of inverter output phase voltages and currents with the proposed APECS under the SLG, LL, and LLG faults at the 5-mH grid inductance. The waveforms around the fault occurrence are zoomed in for a clear view of the transient voltage and current-limiting performance. As shown in Fig. 15, both inverter output phase voltages and currents during various asymmetrical grid faults are limited under the voltage and current thresholds, respectively. There exists a dynamic process around the fault occurrence due to the operation of the proposed NSCFVC+VLGCS with a low bandwidth for different asymmetrical grid faults. However, the transient overcurrent is well limited by the CLGCS. As shown in Fig. 15(a), at the SLG fault occurrence, there is only a little transient overcurrent peak, which exists for approximately 1 ms in the first fundamental period. As shown in Fig. 15(b), at the LL fault occurrence, there are two small transient overcurrent peaks, which exist for around 2 ms and cannot be avoided. As shown in Fig. 15(c), at the LLG fault occurrence, there are two little transient overcurrent peaks, which exist for about 2 ms. However, they all are smoothly mitigated under the current threshold by the CLGCS. During the steady-state fault period, the maximum currents are all lower than the current threshold since the proposed NSCFVC+VLGCS operates in steady state. The current-limiting gain K_I of CLGCS is 1, the control is in VCM, and the voltage source behavior is maintained.

Therefore, both the whole period waveforms and the zoom-in waveforms when the fault happens can verify the fault-ride-through performance with the proposed APECS under different fault types at the 5-mH grid inductance.

Fig. 16 shows the experimental results of inverter output phase voltages and currents with the proposed APECS under SLG, LL, and LLG faults at the 1-mH grid inductance. As shown in Fig. 15(a), during the SLG fault period, the phase voltages and phase currents are both below the voltage and current thresholds, respectively. The zoom-in area around the fault occurrence is also shown in Fig. 16(a). It is clear that maximum transient current peak is lower than the current threshold around the fault occurrence and all phase voltages are lower than the voltage threshold. As shown in Fig. 16(b), during the LL fault period, the phase voltages and phase currents are both below the voltage and current thresholds, respectively. The zoom-in area around the fault occurrence is also shown in Fig. 16(b). The transient current peak at the fault occurrence is still lower than the current threshold. In addition, the phase voltages are lower than the voltage threshold. As shown in Fig. 16(c), during the LLG fault period, the phase voltages and phase currents are both below the voltage and current thresholds, respectively. The zoom-in area around the fault occurrence is also shown in Fig. 16(c).

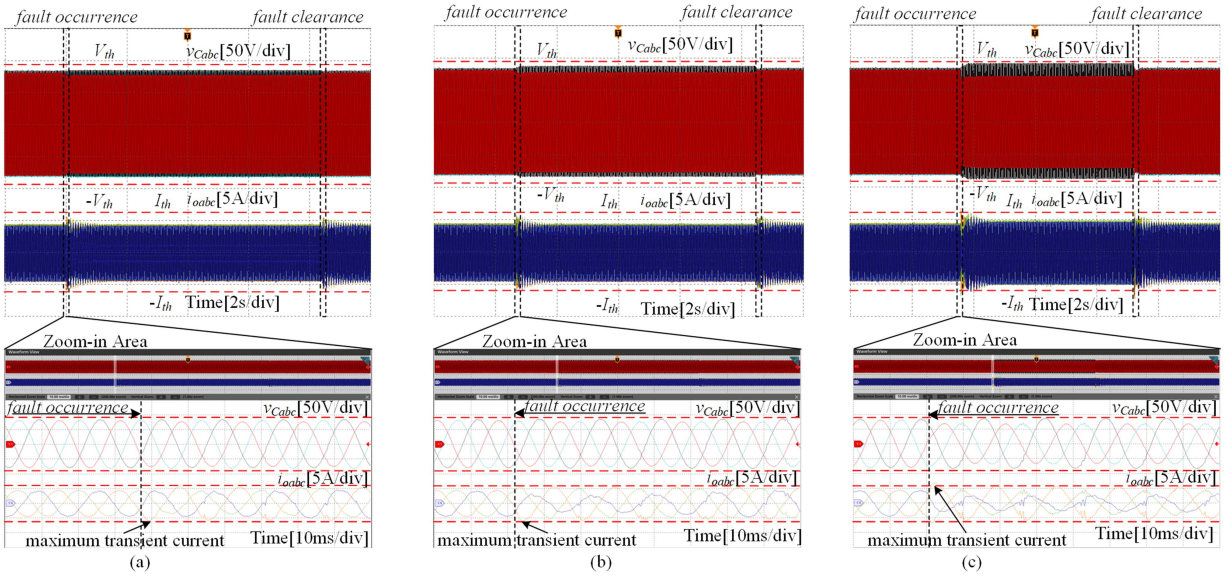

Fig. 16. Experimental results of inverter output phase voltages and currents with the proposed APECS under different asymmetrical grid faults at the 1-mH grid inductance. (a) APECS under SLG fault. (b) APECS under LL fault. (c) APECS under LLG fault.

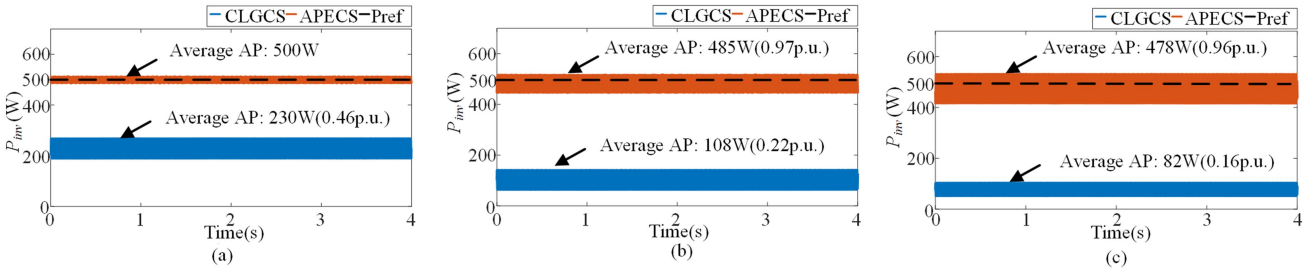

Fig. 17. Experimental results of the AP with the CLGCS and the proposed APECS under different asymmetrical grid faults. (a) AP under SLG fault. (b) AP under LL fault. (c) AP under LLG fault.

There is a little transient overcurrent peak at the fault occurrence, but it falls smoothly under the current threshold in the second fundamental period. Besides, all phase voltages are lower than the voltage threshold. There are obvious periodic spikes in the inverter phase currents around the fault occurrence. This is induced by the operation of the solid-state relay. Consequently, all the experiments under different fault types can verify that the proposed APECS is also effective under a large SCR condition.

In summary, the experimental results can verify the effectiveness of the proposed APECS under different asymmetrical grid faults and various SCRs for current and voltage limiting.

B. AP Enhancement of the Proposed APECS

The AP with the CLGCS and the proposed APECS under different asymmetrical grid faults at 5-mH grid inductance is compared to verify the AP enhancement of the proposed APECS.

Fig. 17(a) shows the experimental results of the AP during the steady-state fault period under the SLG fault with the CLGCS and the proposed APECS. When the SLG fault occurs, the AP during the steady-state fault period with the CLGCS is 230 W(0.46 p.u.) much lower than the reference AP $P_{\text{ref}} = 500$ W. However, with the proposed APECS, the AP is maintained at the reference power $P_{\text{ref}} = 500$ W. Comparing the experiment results of the inverter output phase voltages and currents with the CLGCS under the SLG fault in Fig. 18(a) and with the proposed APECS under the SLG fault in Fig. 19(a), the magnitudes of phase voltages are closed. However, the inverter output phase currents are balanced with the proposed APECS. On the contrary, the current in one phase is reduced to a low value with the CLGCS, thus the AP is curtailed. This is why the proposed APECS can significantly enhance the AP under the SLG fault.

Fig. 17(b) shows the experimental results of the AP under the LL fault with the CLGCS and the proposed APECS. When the LL fault happens, the AP during the steady-state fault period with the CLGCS is 108 W (0.22 p.u.) much lower than the reference AP 500 W. However, with the proposed APECS, the AP is maintained at 485 W (0.97 p.u.). Comparing Figs. 18(b) and 19(b), the inverter output phase currents are more balanced with the proposed APECS than with the CLGCS under the LL fault. Therefore, the proposed APECS can significantly enhance the AP under the LL fault.

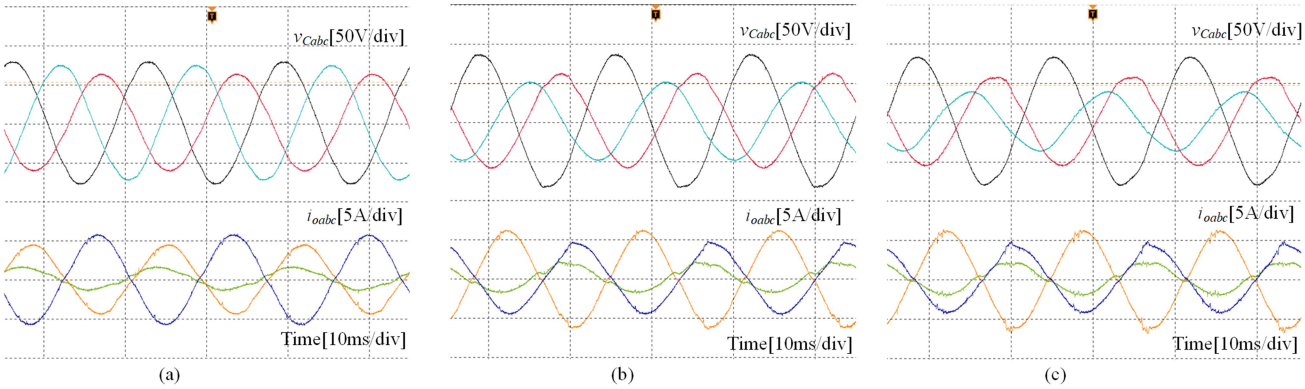

Fig. 18. Experimental results of the inverter output phase voltages and currents with the CLGCS during the steady-state fault period under different asymmetrical grid faults. (a) SLG fault. (b) LL fault. (c) LLG fault.

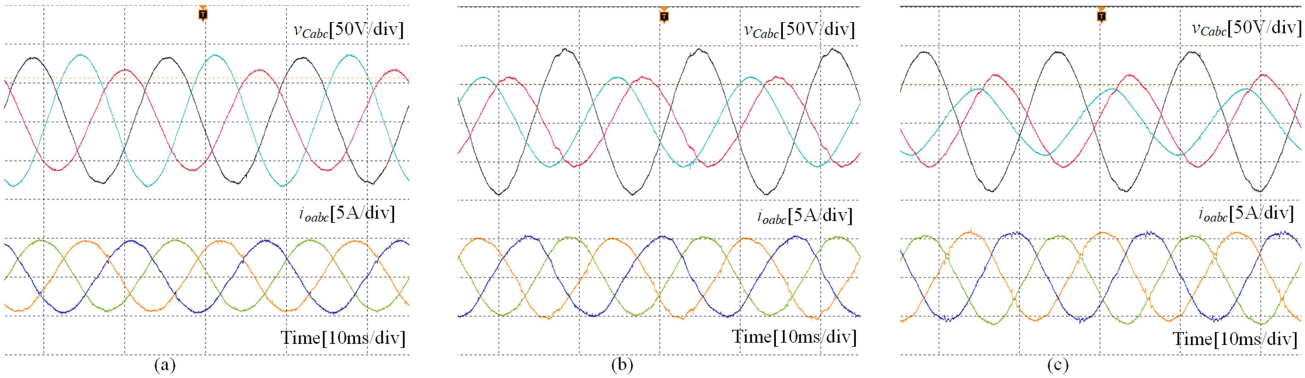

Fig. 19. Experimental results of the inverter output phase voltages and currents with the proposed APECS during the steady-state fault period under different asymmetrical grid faults. (a) SLG fault. (b) LL fault. (c) LLG fault.

Fig. 17(c) shows the experimental results of the AP during the steady-state fault period under the LLG fault with the CLGCS and the proposed APECS. When the LLG fault happens, the AP during the steady-state fault period with the CLGCS is 82 W (0.16 p.u.) much lower than the reference AP 500 W. However, the AP with the proposed APECS is maintained at 478 W (0.96 p.u.). Comparing Figs. 18(c) and 19(c), the inverter output phase currents are more balanced with the proposed APECS than with the CLGCS under the LLG fault. Therefore, the proposed APECS can significantly enhance the AP under the LLG fault.

In summary, the AP during the steady-state fault period with the CLGCS falls significantly below the reference AP under different asymmetrical grid faults. This phenomenon is consistent with the AP curtailment issue analysis in Section IV and Fig. 12(c), (f), and (i). In addition, the AP curtailment is more severe under the LLG fault than the SLG fault and the LL fault, which complies with the calculation result in Fig. 12(c), (f), and (i). Moreover, compared with the CLGCS, the AP during steady-state fault period with the proposed APECS is significantly enhanced to approximate the reference power, which verifies the AP enhancement capability of the proposed APECS. Comparing the inverter output phase voltages and currents under various asymmetrical grid faults in Fig. 19 with Fig. 18, it is found that the voltage magnitudes with these two control schemes are similar, but the inverter output phase currents are balanced with the proposed APECS. The negative-sequence fault currents are eliminated by the proposed APECS. This is why the inverter with the proposed APECS can produce higher AP during the different asymmetrical faults.

VII. Conclusion

The AP curtailment issue of the CLGCS under different asymmetrical grid faults has not been well investigated before, but it is analyzed in this article based on sequence networks. The negative-sequence currents during the asymmetrical grid faults limit the transmission capability of the AP with the CLGCS. Therefore, the APECS in this article is proposed to not only ride-through different asymmetrical grid faults but also enhance the transmission capability of the AP. The proposed APECS limits overvoltage by the proposed VLGCS and prevent overcurrent by the CLGCS without any fault detection method. In addition, the proposed APECS enhance the transmission capability of the AP with the proposed NSCFVC by eliminating negative-sequence fault currents. Theoretical calculation based on the sequence networks in terms of the maximum inverter output phase voltage, current, and AP can verify the FRT ability and transmission capability enhancement of the AP with the proposed APECS. These contributions are also verified by experimental results.

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