Letters

A TM-APSM SIMO Buck Converter With Ultralow Quiescent Current and Fast-Transient Response for IoT Applications

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***Abstract*—This letter presents a time-multiplexing adaptive pulse-skip modulation (TM-APSM) single-inductor multiple-output (SIMO) buck converter for Internet of Things (IoT) applications. The converter generates 0.8, 1.2, and 1.8 V independent supply voltages from 2.4–4.2 V battery. The proposed successive approximation frequency modulator (SAFM) improves transient response without extra quiescent current. Also, the implemented ADC-based adaptive on-time (AOT) generator suppresses the output ripple under a wide range of input and output voltages. The chip fabricated in the 55-nm CMOS process achieves 93.2% peak efficiency within 0.3 μA to 12 mA total load range. It consumes only 33 nA quiescent current and achieves 150 μs output recovery time at 0-to-4 mA load transition. A decent efficiency of 70% is also obtained under 3 μA ultralight load condition.**

***Index Terms*—Adaptive on-time (AOT), buck converter, high efficiency, Internet of Things (IoT), low quiescent current, single-inductor multiple-output (SIMO).**

I. Introduction

BENEFITTING from the rapid development of the Internet of Things (IoT) and miniaturization of the electronics, the systems-on-chip (SoC) integrating diverse function modules are now widely deployed in IoT applications. To create independent supply voltage domains for internal analog and digital blocks in SoCs, a combination of single dc-dc followed by multiple low-dropout voltage regulators (LDOs) is implemented. However, the total power efficiency is reduced, leading to a short life span of a small-volume battery. The ultralow power (ULP) converter array is able to improve efficiency, whereas the bulk inductors introduce cost and area overhead. Therefore, the single-inductor-multi-output (SIMO) converters that provide customized supply voltages with shared inductor are extremely desirable as power management circuits. Due to the power demand of SoCs typically ranges from nano-watts to milli-watts [1], it is challenging for the SIMO converter to improve the transient response speed with limited standby power. Furthermore, the analog front-end (AFE) circuits in SoCs are sensitive to the ripple noise. It is essential to minimize both the cross-regulation issue between different outputs and output ripple to ensure optimal performance.

In the prior-art SIMO converters, single discharge control (SDC) is proposed in [2], in which four outputs are charged successively and recycling the remaining energy in one period. However, this approach suffers from the cross-regulation issue and the double conversion loss. An output-aware control technique is presented in [3], achieving 0.016 mV/mA cross-regulation. Unfortunately, it lacks a zero-current detector (ZCD) in discontinuous conduction mode (DCM), reducing the conversion efficiency. Adaptive and hysteretic control techniques have been proposed in [4] and [5], respectively, aiming to achieve ultra-low quiescent current. However, both approaches result in slower transient response time due to limitations imposed by the feedback-loop bandwidth. When the load switches from light to heavy conditions, a large undershoot of the output voltage may disable the subsequent circuits.

To address these existing issues, this letter presents a time-multiplexing adaptive pulse-skip modulation (TM-APSM) SIMO buck converter. In this converter, three outputs are regulated using DCM in a time-multiplexing manner, effectively alleviating the cross-regulation issue. In addition, the transient response speed is enhanced by the successive approximation frequency modulator (SAFM) without sacrificing the quiescent power. Furthermore, the ADC-based adaptive on-time (AOT) generator reduces the output ripple over a wide input and output range.

II. Architecture of the Proposed SIMO Converter

Fig. 1 shows the overall block diagram of the proposed SIMO buck converter. The power stage contains a pull-up power transistor M_P, a pull-down power transistor M_N, and output power transistors M_{S1}-M_{S3}. Three independent outputs are generated from V_{BAT} by utilizing a shared inductor. In the target IoT applications, where the load condition is relatively light, the converter only operates in the DCM. The latch-type comparators

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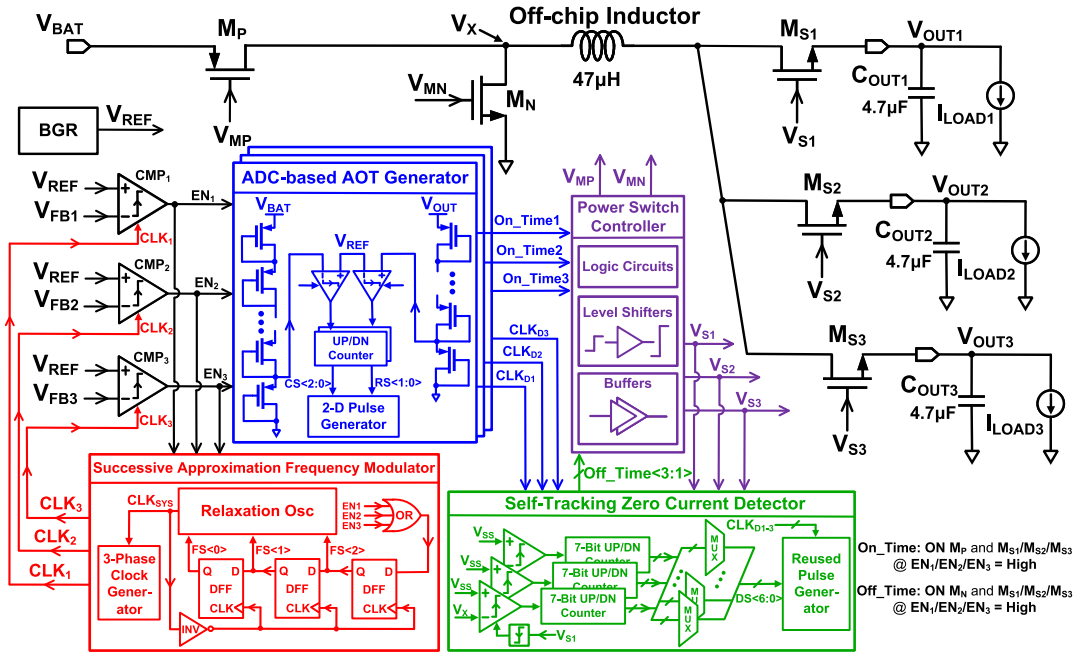


Fig. 1. Overall block diagram of the proposed SIMO buck converter.

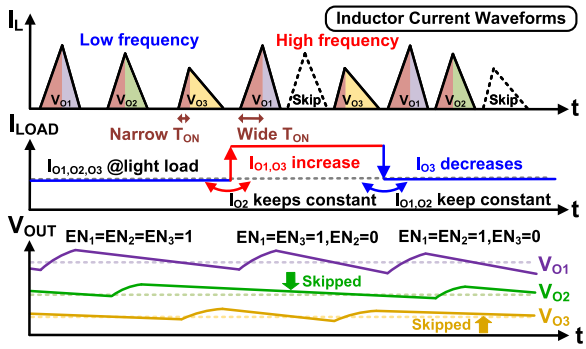


Fig. 2. Operational waveforms of the SIMO TM-APSM strategy.

CMP_1-CMP_3 compare the divided voltages V_{FB1}-V_{FB3} with the reference voltage V_{REF} at the rising edges of the corresponding clock CLK_1-CLK_3. The ADC-based AOT generators provide the appropriate on-time period (T_{ON}) triggered by the enable signals EN_1-EN_3. The off-time period (T_{OFF}) is determined by the the self-tracking zero-current detector (ST-ZCD) to avoid the reverse inductor current. The power switch controller contains the logic circuits and buffers, driving the corresponding power switches.

Fig. 2 illustrates the operation of the TM-APSM. At the beginning, three outputs are charged sequentially in a time-multiplexing manner. A lower switching frequency is selected to accommodate the light load condition. Now suppose I_{O1} and I_{O3} increase, whereas I_{O2} keeps unchanged, the switching frequency is boosted adaptively to satisfy the load requirements of V_{OUT1} and V_{OUT3}. At the same time, the charging period of V_{OUT2} is skipped with $EN_2 = 0$ to keep the output voltage. Similarly, the switching operation of V_{OUT3} is also skipped when I_{O3} is decreasing. Thanks to the proposed TM-APSM control strategy, architectural reduction of crosstalk between three outputs becomes possible. The ADC-based AOT generator adjusts the T_{ON} corresponding to the input and output voltages. The transient performance is also enhanced with the successive approximation frequency modulation technique.

III. Circuit Implementation

A. Successive Approximation Frequency Modulator

In the ULP IoT applications, the power consumption of the clock generator needs to be reduced for a long battery lifespan. However, both transient response speed and load range are limited due to the restricted switching frequency. A current mirror-based load detector is proposed to modulate the switching frequency in [4], but it introduces relatively large quiescent power overhead. In this letter, we introduced an SAFM to accommodate the load condition, as shown in Fig. 3(a). It consists of a 3-b shift register, an ULP relaxation oscillator (Rx. Osc) and a 3-phase clock generator. The frequency of main clock CLK_{SYS} is modulated by the registers FS<2:0>. Three time-interleaving clock signals CLK_1-CLK_3 are further generated from CLK_{SYS}. Each of these signals operates at 1/3 the frequency of CLK_{SYS}. In the event that any of EN_1–EN_3 signal transitions to 1 due to an escalating load condition, the most significant bit (MSB) FS<2> is subsequently set to 1. This action triggers a significant and corresponding step increase in the frequency of CLK_{SYS}. If EN remains at 1 in the next period, FS<2:0> is updated to 110 through the successive approximation process. Unlike the frequency modulator in [6], the proposed SAFM achieves faster response speed compared to the hill-climbing operation. Consequently, the large undershoot observed in [6] can be completely eliminated. Conversely, when all EN_1-EN_3

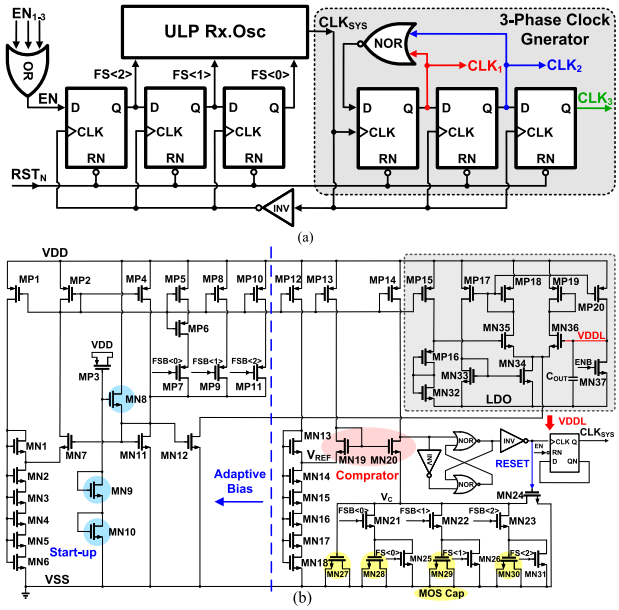


Fig. 3. Successive approximation frequency modulator. (a) Block diagram. (b) Schematic of the ULP relaxation oscillator.

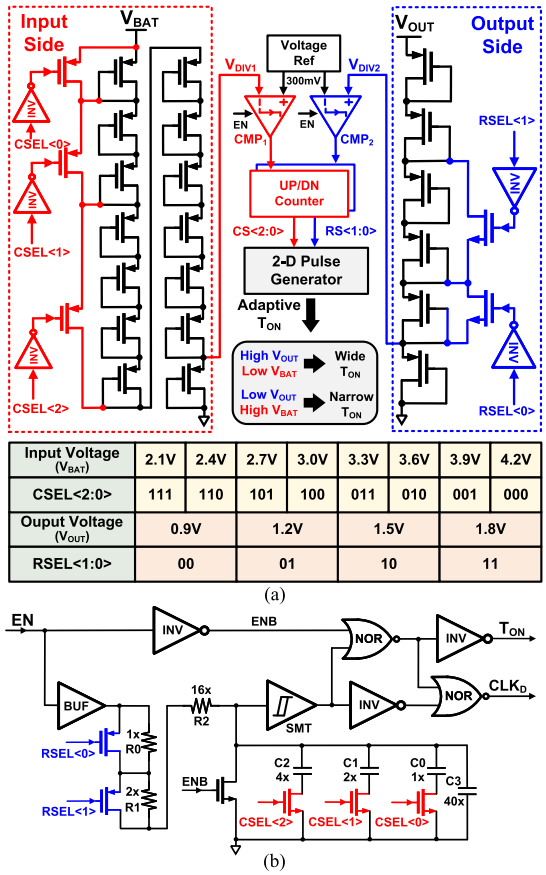
signals become 0 at heavy-to-light load transition, the MSB promptly switches to 0, leading to a slower CLK_{SYS}. As a result, the proposed SAFM can search for the optimum switching frequency within fewer iteration steps, while consuming lower quiescent power. Fig. 3(b) shows the schematic of the implemented ULP Rx. Osc. The bias current and charging capacitance are adaptively adjusted by FS<2:0>. 1–120 kHz CLK_{SYS} is generated with 6–182 nA average current, well accommodating 0.3 μA–12 mA load ranges.

B. ADC-Based AOT Generator

On-time control is usually employed in DCM operation by adjusting the peak inductor current (I_{PEAK}) when the input or output voltage varies. In this letter, we proposed an ADC-based AOT generator featuring of low power and wide tuning range. Fig. 4(a) shows the circuit diagram, which consists of input and output side diode-divider, comparators, up/down counters, and a pulse generator. The divided voltages V_{DIV1} and V_{DIV2} are generated from V_{BAT} and V_{OUT}, respectively. The dynamic comparators CMP_1 and CMP_2 compare V_{DIV1} and V_{DIV2} with the 300 mV reference voltage, the comparison results are transferred to the corresponding UP/DN counter. Thus, the level of V_{BAT} and V_{OUT} are quantized to the digital counterparts CS<2:0> and RS<1:0>, which further modulate T_{ON} through the 2-D pulse generator. Fig. 4(b) shows its schematic. Wider T_{ON} is generated with decreasing V_{BAT} or increasing V_{OUT}, and vice versa, which can be further explained with the following equations. The peak inductor current is expressed as

$$I_{PEAK} = \frac{V_{BAT} - V_{OUT}}{L} \cdot T_{ON} = \frac{V_{OUT}}{L} \cdot T_{OFF}. \quad (1)$$

Assuming output voltage ripple ΔV_O caused by the load consuming is negligible in short switching period, the delivered



Input Voltage (V_{BAT})	2.1V	2.4V	2.7V	3.0V	3.3V	3.6V	3.9V	4.2V
CSEL<2:0>	111	110	101	100	011	010	001	000
Ouput Voltage (V_{OUT})	0.9V		1.2V		1.5V		1.8V	
RSEL<1:0>	00		01		10		11	

Fig. 4. ADC-Based AOT generator. (a) Circuit diagram and digital encoding. (b) Schematic of the 2-D pulse generator.

energy ΔE_{OUT} can be expressed as

$$\Delta E_{OUT} = \frac{1}{2} \cdot I_{PEAK} \cdot (T_{ON} + T_{OFF}) \cdot V_{OUT} \quad (2)$$

$$= \frac{1}{2} C_{OUT} (V_{OUT} + \Delta V_O)^2 - \frac{1}{2} C_{OUT} V_{OUT}^2. \quad (3)$$

By combining (1)–(3), ΔV_O is derived as

$$\Delta V_O \approx \frac{V_{BAT} \cdot (V_{BAT} - V_{OUT})}{2 \cdot L C_{OUT} \cdot V_{OUT}} \cdot T_{ON}^2. \quad (4)$$

Therefore, when V_{BAT} or V_{OUT} varies, T_{ON} can be adaptively adjusted to stabilize ΔV_O. By implementing the proposed AOT generator, T_{ON} is modulated in terms of the predefined lookup table. The relationship between supply and demand can be well balanced. Moreover, the 3-nA diode-dividers and voltage reference in the proposed circuitry significantly reduces the quiescent current.

C. Self-Tracking Zero Current Detector

ZCD is the requisite module in DCM operation to determine T_{OFF} by detecting the zero current crossing point of inductor current. In this work, ST-ZCD is employed for its low quiescent power [1]. Considering the chip area overhead, the pulse generator is reused to serve three independent outputs, as shown in Fig. 1. Node voltage V_X is compared to ground at the end

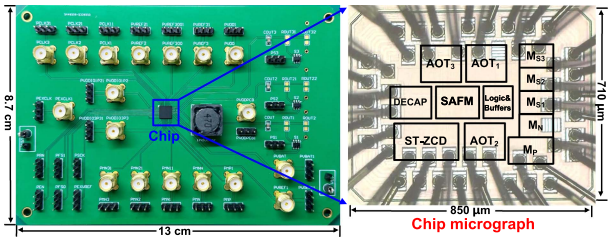


Fig. 5. Test PCB and chip micrograph.

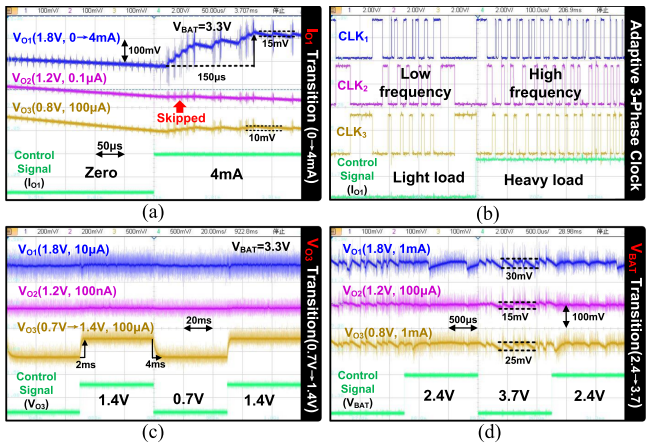


Fig. 6. Measured transient waveforms of (a) V_{O1}-V_{O3} when V_{O1} has load change. (b) adaptive 3-phase clock. (c) V_{O1}-V_{O3} when V_{O3} has voltage step-change. (d) V_{O1}-V_{O3} when V_{BAT} has voltage step-change.

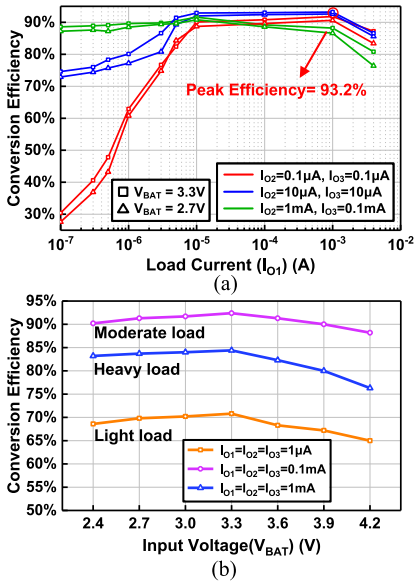


Fig. 7. Measured conversion efficiency versus. (a) Load current (I_{O1}). (b) Input voltage (V_{BAT}).

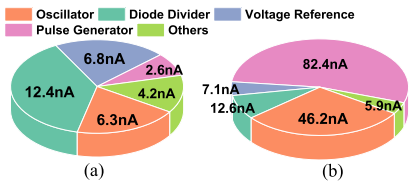


Fig. 8. Simulated quiescent current breakdown at (a) no load condition, (b) peak efficiency point.

of the corresponding T_{OFF}. DS<6:0> are generated through the respective 7-b UP/DN counter according to the comparison results. The reused pulse generator is implemented with similar structure in Fig. 4(b). A 150 ns tuning resolution is implemented to ensure the detection accuracy by 7-b capacitor array.

IV. Experimental Results

Fig. 5 shows the chip micrograph of the proposed SIMO converter and its test PCB. The chip was fabricated in 55-nm CMOS process with an active area of 0.85 × 0.71 mm^2. The off-chip components are the 47 μH inductor and three 4.7 μF output capacitors.

Fig. 6(a) presents the measured transient waveforms of V_{O1}–V_{O3} when I_{O1} changes from 0 to 4 mA. Three output voltages are set to 1.8, 1.2, and 0.8 V with a 3.3 V input voltage. Under a zero load condition, a lower switching frequency is selected to keep the voltage. When I_{O1} changes to 4 mA, V_{O1} is charged with a higher switching frequency while the output recovery time is 150 μs. In this condition, V_{O2} and V_{O3} are not affected thanks to the TM-APSM technique. Cross-regulation is not observed as well. Fig. 6(b) shows the corresponding 3-phase clock, which is modulated adaptively to accommodate the load conditions. Fig. 6(c) and (d) depicts the transient behaviors when output and input voltages change. In Fig. 6(c), V_{O3} changes between 0.7 and 1.4 V within 2 and 4 ms, respectively. The transient response time can be further improved by decreasing C_{OUT} at the cost of increased voltage ripple. Meanwhile, V_{O1} and V_{O2} keep constant with 3.3 V input voltage. When V_{BAT} varies between 2.4 and 3.7 V as shown in Fig. 6(d), the ripples of three outputs are kept below 30 mV benefiting from the proposed AOT circuits.

Fig. 7 shows the measured efficiency with V_{O1}–V_{O3} setting to 1.8, 1.2, and 0.8 V. The converter achieves a wide load range from 0.1 μA to 4 mA per channel. A peak efficiency of 93.2% is obtained at I_{O1}=1 mA. Furthermore, a decent efficiency around 70% is achieved under 3 μA light load condition as shown in Fig. 7(b). Fig. 8 shows the quiescent current breakdown among main blocks. At no load condition, the oscillator maintains the lowest frequency with total 33 nA quiescent current, while the pulse generator dominates the power consumption at peak efficiency point.

Table I summarizes the performance in comparison with the prior SIMO converters. This work achieves lower quiescent current (compared to [4], [5], and [6]) or higher peak efficiency (compared to [2], [5], and [6]). Cutting-edge figure of merit (FOM) value is therefore obtained, representing higher conversion efficiency over wider load range.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH PRIOR WORKS

	[2] TPEL'18	[4] JSSC'22	[5] TIE'23	[6] SSCL'21	This letter
Technology	0.18-μm BCD	0.153-μm CMOS	0.5-μm BCD	0.18-μm BCD	**55-nm CMOS**
Input voltage (V)	2.7-3.7	1-5	2.1-5.5	3-5	**2.4-4.2**
Output voltage (V)	1/1.2/1.5/1.8	0.8/1.2/1.8/3.6	0.8/1.8/20	1.8/0.8/12	**0.8/1.2/1.8**
L(μH)/C_{OUT}(μF)	10or4.7/10	10/2.2	4.7/10	4.7/N.A	**47/4.7**
Control method	SDC	ASCD	Hysteretic	PSK	**TM-APSM**
Operating mode	CCM / DCM	CCM / DCM	DCM	DCM	**DCM**
Peak efficiency (%)	73	94.3	92.3	86	**93.2**
Load range of single channel	500μA-66mA*	1mA-400mA*	200μA-10mA*	1μA-1mA*	**0.1μA-4mA**
Efficiency @light-load	20%*@1mA	85%*@1mA	63%*@600μA	55%@1μA	**70%@3μA**
Quiescent current	N/A	185nA	<1μA	217nA	**33nA**
AOT for Diff. V_{OUT}	No	No	No	Yes	**Yes**
Output ripple	30mV@1V	28mV@1.8V	45mV*@1.8V	<50mV@1.8V	**30mV@1.8V**
Switching frequency	1MHz	1.5MHz	0-2.1MHz	3-18kHz	**1-120kHz**
Output recover time @load transition	50μs* @0-100mA	8μs* @100m-400mA	N/A	≤1ms @0-1mA	**150μs @0-4mA**
FOM (pA/%)**	N/A	550	24000	285	**1.1**

*: Calculated/Observed from the paper.
**: FOM [1] = $I_{LOAD,min} \times I_q/(I_{LOAD,max} \times$Eff@1mA), the smaller is better.

V. CONCLUSION

This letter presents the implementation of a TM-APSM SIMO buck converter fabricated in a 55-nm CMOS process, incorporating SAFM, ADC-based AOT generator, and ST-ZCD. The converter yields three independent outputs characterized by improved transient response and reduced output ripple. The achieved peak efficiency stands at 93.2%, while maintaining a quiescent current of 33 nA and accommodating a total load range of 0.3 μA to 12 mA. These results demonstrate its potential suitability for integration into power management circuits for IoT applications.

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