A Modulation Strategy to Operate Five-Level HC Inverter at Wide Power Factors With Enhanced Neutral Point Voltage Balancing Capability

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***Abstract*—Clamped multilevel inverters suffer significantly from neutral point (NP) voltage unbalancing in low power factor applications, which will lead to severe device overvoltage problems and affect its output performance. The five-level hybrid clamped (HC) inverter is a state-of-the-art topology with additional redundant switching states, which makes it possible to suppress the NP low-frequency voltage ripples better. Therefore, a novel and simple modulation for five-level HC inverter with enhanced NP voltage balancing capability is proposed. Based on the influence of NP currents on the dc-link capacitor voltages, the different switching states combinations with capacitor voltages naturally balancing constraints are analyzed comprehensively, and the relationship between the duty ratio of average NP currents and the reference modulation voltage is designed as a bi-triangular function to minimize the currents flowing out of the NPs. Compared with traditional modulation, the equivalent adjustment ability of NP currents is greatly enhanced by the zero-sequence voltage injection, and the low-frequency voltage ripples of DC-link capacitors are suppressed significantly at whole power factors. Moreover, the active balancing methods are explored to achieve independent and decoupling control of all capacitor voltages. Simulations and experiments verify the viability of the modulation strategy and the capacitor voltage balancing method.**

***Index Terms*—Capacitor voltage balancing, modulation strategy, multilevel inverter, zero-sequence voltage (ZSV).**

I. Introduction

MULTILEVEL inverters are more suitable for high-power industrial applications, such as motor drives, renewable energy power generation, and flexible ac transmission systems [1], [2], [3], [4]. Three basic multilevel topologies, neutral point clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB) are academically accepted topologies and have been successfully commercialized [5], [6]. In these topologies, the drawbacks gradually show up with the expansion of voltage and power levels. FC inverter requires numerous floating capacitors, which increases the complexity of the capacitor voltage balancing, and the application of CHB inverter is limited due to the massive independent dc power supplies being required [7]. In comparison, NPC inverter is much easier to expand beyond three voltage levels [8].

As the voltage level increases, the NPC inverter will suffer from severe NP voltage unbalancing problems, which only allows the NPC inverter to operate in limited power factors and modulation indexes under classic phase disposition pulse-width modulation (PD-PWM) or nearest-three-vector modulation [9], [10]. In order to tackle such problems, additional voltage balancing circuits or virtual-space-vectors-based PWM are proposed in [11] and [12]. However, these methods increase the overall cost or computational complexity of the system. Space vector modulation with active capacitor voltage balancing and model-predictive control are another ways to ensure that the NPC inverter operates at a high power factor and high modulation index [13], [14]. But similar to virtual-space-vectors-based PWM, they are very complex and difficult to implement. A novel modulation method named carrier-overlapped PWM (COPWM) is proposed in [15], which utilizes the carrier-based PWM method for four-level NPC. On the basis of this, a generalized COPWM method for arbitrary voltage levels of NPC is developed in [10]. The triangular carriers are unevenly distributed and overlapped with each other. In this way, the average NP currents are the same for one carrier period while equal to zero for one fundamental period. The NP unbalanced voltage will cause low-frequency voltage ripples in the dc-link upper and lower capacitors. Therefore, the active ZSV injection method is also employed to regulate NP currents and suppress low-frequency voltage fluctuations of dc-link upper and lower capacitors.

Similarly, the COPWM method has been applied to other clamped inverters, such as four-level active NPC (ANPC) inverter [16] and four-level T-Type inverter [17]. The COPWM method is based on carriers and easily implemented in engineering. But the line voltage level jumps increase as the voltage level expands to five or more, and it is not applicable to five-level ANPC inverter [18], [19], HC inverter [20], [22], five-level nested neutral-point piloted (NNPP) inverter [23], and other clamped inverter with floating capacitors. The unbalancing

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voltage of NPs is related to the power factor angle, current amplitude, and modulation index [23]. However, this conclusion comes from the hybrid carrier modulation method. With such carrier-based modulation, a fixed combination of switching states is selected, so that the relationship between duty ratio of average NP currents and the reference modulation voltage is determined. This means that the ability of the ZSV method to manage the NP currents is also determined with a fixed modulation index and load impedance. Wang et al. [24] proved the relationship between duty ratio of average NP currents and the reference modulation voltage as a triangular function when the COPWM method is employed in the NPC inverter. At high power factors, the power factor angle is small and the phase of the reference modulation voltage is similar to the phase of the inverter output current. In this situation, the maximum and minimum values of the triangle function correspond to the minimum and maximum values of the output current, respectively, the absolute value of the slope between the output current and the reference modulation voltage is relatively large, which provides considerable NP currents regulation capability by ZSV method at high modulation indexes. In contrast, the out current lags reference modulation voltage by close to $\pm\pi/2$ at low power factors. The maximum value of the triangle function corresponds to the maximum value of the output current, the absolute value of the slope between the output current and the reference modulation voltage is minimum, combined with the fact that the zero-sequence voltage (ZSV) injection range is constrained by the linear modulation at high modulation indexes. The adjustment ability of NP currents is greatly weakened, and the low-frequency voltage ripple of dc-link upper and lower capacitors will not be suppressed [24]. Similar to NPC inverter, the carrier-based five-level ANPC inverter [25], five-level NNPC inverter [23], and five-level stacked multicell (SM) inverter [26] are also triangular function relations. This implies that these clamped inverters still face the problem of NP voltage unbalancing at low power factors and high modulation indexes.

The HC inverter is an excellent and practical candidate in medium and high power applications [27]. Compared with the ANPC inverter, the HC inverter has equal blocking voltages across the switches and fewer devices. Although the HC inverter has a complex capacitor voltage balancing strategy, the additional switching states support higher flexible voltage balancing schemes and modulation methods. In addition, the HC inverter has certain advantages over the other existing inverters such as MMC, NPC, FC, SMC, and NNPC [22]. The traditional phase-shifted PWM (PS-PWM) with ZSV injection method is first employed to achieve the voltage balancing of dc-link capacitors [20], but the low-frequency voltage ripples are not considered. On top of that, an improved common-mode voltage is applied to address the low-frequency voltage ripples, but it requires relatively complex closed-loop control of common-mode voltage [28]. In [29], the mathematical model of the common-mode voltage is derived, which can be calculated in the open-loop. It needs three loops to identify the optimal common-mode voltage, which also has complex computation. Some more complex and un-carrier-based methods, such as selected switching states [30] and unified selective harmonic elimination control [27], are also used to solve this problem. In terms of the five-level HC inverter, the main concern is the optimization of the floating capacitor size [31] and the optimized total harmonic distortion [32]. The low-frequency voltage ripple problem seems to be ignored. Additionally, some similar inverter topologies have been developed as a variant of the HC inverter but different voltage values in the dc-link capacitors and FCs, which are named as hybrid flying-capacitor (HFC) inverters [33], [34], [35], [36]. HFC inverters have excellent output power quality, lower power losses, and competitive device count compared to the same level of classical topologies [35]. However, different voltage values in capacitors cause uneven distribution of voltage stress across the devices, serial connection of switches is unavoidable, and additional auxiliary circuitry is required to suppress the low-frequency voltage ripples of dc-link capacitors. In [37], a modulation concept similar to COPWM is introduced, the switching states of adjacent voltage levels are considered, and thus, the auxiliary circuit is removed and the ZSV method can be used to guarantee voltage balancing of the dc-link capacitors, the drawbacks are similar to COPWM, the low-frequency problems cannot be solved. A novel dc-link capacitor voltage control scheme is proposed by [38], which discarded the principle of minimizing voltage stress of switches in five-level HFC inverter, and then the auxiliary dc-Link balancing circuit is excluded, the capacitor voltages can be maintained within the allowable range by PS-PWM. This method ensures capacitor voltage balancing but does not demonstrate competitive suppression of low-frequency voltage ripples, and the blocking voltages of certain switches rise to 1.5 times. In summary, no matter whether HC inverters or HFC inverters, the voltage balance of the dc-link capacitors is the key issue. The voltages of dc-link capacitors can be balanced with different approaches, the PS-PWM is the most suitable one due to the natural voltage balancing of capacitors, simplicity to realize, and no additional auxiliary circuits [32]. The HC inverter faces serious NP voltage unbalancing problems under conventional PS-PWM, especially at low power factors. Therefore, this article proposes a novel PS-PWM method which has a more competitive advantage in suppressing low-frequency voltage fluctuations without increasing the computational burden.

Essentially, the imbalance problem of NP voltage is significantly influenced by the relationship between the duty ratio of average NP currents and the reference modulation voltage. The trapezoidal function relationship of conventional PS-PWM generates large NP currents at low power factors, combined with the small slope between the reference modulation voltage and the output current, which corresponds to the zero slope region of the trapezoidal function. The selection of ZSVs is limited at high modulation indexes, this results in limited regulation of NP current, and the low-frequency fluctuations of the dc-link capacitors cannot be suppressed. The five-level HC inverter has sufficient redundant switching states, which makes it possible to explore new carrier-based modulation strategies to enhance NP voltage balancing capability and suppress low-frequency fluctuations of NP voltage. Therefore, a novel SP-PWM is explored in this article with a bi-triangular function relationship, which reduces NP currents greatly at low power factors and

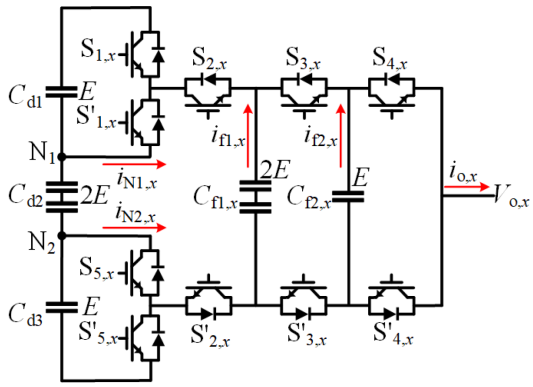

Fig. 1. Single phase circuit of the five-level HC inverter.

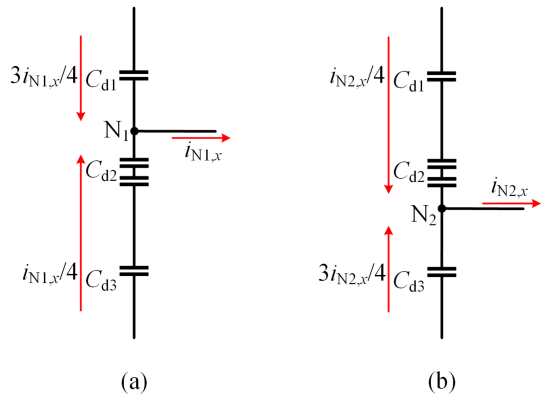

Fig. 2. NP currents distribution of DC-link capacitors. (a) $i_{\mathrm{N1},x}$, (b) $i_{\mathrm{N2},x}$.

without zero slope region. this means that the regulation of the NP current by the ZSV method is also stronger compared with conventional PS-PWM, the low-frequency voltage fluctuations of the dc-link capacitors can be further suppressed. The main contributions of the article are summarized as follows:

1) A novel and simple carrier-based modulation is proposed in this article with only two carriers phase shifted by π, and it ensures the natural voltage balancing of floating capacitors and dc-link center capacitor within one carrier period to minimize the capacitor voltage ripples.
2) The duty ratio of average NP currents and the reference modulation voltage are designed as a bi-triangular functional relationship by proposed PS-PWM. Compared with traditional PS-PWM, it reduces NP currents greatly at low power factors and without zero slope region. Therefore, it has considerable NP current regulation capability by the ZSV method, even at high modulation indexes, and the low-frequency voltage ripples of dc-link upper and lower capacitors are almost suppressed completely. Finally, the verification is carried out by simulation and experiment.

The rest of the article is organized as follows. Section II presents a novel carrier-based modulation, then a comprehensive ability of the different modulations to adjust the NP current is compared. Capacitor voltage balancing method is given in Section III. Sections IV and V show the simulation results and experimental results respectively. Finally, Section VI concludes the article.

II. Five-Level HC Inverter and Proposed Modulation Strategy

A. Five-Level HC Inverter

The single phase circuit of the five-level HC inverter is shown in Fig. 1. The normal voltages of the dc-link capacitors C_{d1}, C_{d2}, C_{d3} are E, $2E$, E, respectively, and the normal voltages of the floating capacitors $C_{\mathrm{f1},x}$, $C_{\mathrm{f2},x}$ are $2E$, E, respectively. $i_{\mathrm{N1},x}$ and $i_{\mathrm{N2},x}$ represent the currents flowing out of the NPs N_1 and N_2, respectively. $i_{\mathrm{f1},x}$ and $i_{\mathrm{f2},x}$ represent the currents flowing out of the floating capacitors $C_{\mathrm{f1},x}$ and $C_{\mathrm{f2},x}$. $i_{o,x}$ is the output phase current. $V_{o,x}$ is the instantaneous output phase voltage. Where underscript symbol x represent phase a, b or c.

According to the principle of minimum voltage stress of switches, the switching states can be obtained as listed in Table I, and the following operating rules need to be included.

1) The switches $\mathrm{S}_{1,x}$–$\mathrm{S}_{5,x}$ are complementary to the corresponding switches $\mathrm{S}'_{1,x}$–$\mathrm{S}'_{5,x}$.
2) The switch $\mathrm{S}_{1,x}$ shares an identical gate signal with $\mathrm{S}_{5,x}$.

If E is selected as the base voltage, and the negative terminal of the dc-link is used as the zero voltage potential. Defining the switching functions of switches $\mathrm{S}_{1,x}$–$\mathrm{S}_{4,x}$ are $f_{1,x}$–$f_{4,x}$, respectively. According to the above operating principle and switching states in Table I, the $V_{o,x}$ of five-level HC inverter can be expressed as follows:

$$V_{o,x} = (f_{1,x} + f_{2,x} + f_{3,x} + f_{4,x}) \cdot E. \tag{1}$$

Equation (1) implies that the instantaneous output voltage of the inverter is equal to the sum of the switching functions, and moreover, the control of the switches is independent of each other. Therefore, the traditional PS-PWM method can be employed to control the five-level HC inverter [22].

Based on the switching states in Table I, the relationship between the NP currents and the switching functions are as follows:

$$i_{\mathrm{N1},x} = f_{2,x}(1 - f_{1,x}) \cdot i_{o,x} \tag{2a}$$

$$i_{\mathrm{N2},x} = f_{1,x}(1 - f_{2,x}) \cdot i_{o,x} \tag{2b}$$

$$i_{\mathrm{N},x} = i_{\mathrm{N1},x} + i_{\mathrm{N2},x} = |f_{1,x} - f_{2,x}| \cdot i_{o,x}. \tag{2c}$$

The currents flowing out of the floating capacitors can be written as follows:

$$i_{\mathrm{f1},x} = (f_{3,x} - f_{2,x}) \cdot i_{o,x} \tag{3a}$$

$$i_{\mathrm{f2},x} = (f_{4,x} - f_{3,x}) \cdot i_{o,x}. \tag{3b}$$

Suppose the capacitance values of dc-link are $C_{\mathrm{d1}} = 2C_{\mathrm{d2}} = C_{\mathrm{d3}} = C_{\mathrm{d}}$, according to the circuit topology of five-level HC inverter, the NP currents distribution of dc-link capacitors are given in Fig. 2. Then, the NP currents over a carrier period versus the dc-link capacitor voltages can be expressed as follows:

$$\Delta u_{\mathrm{d1},x} = \left[\int_0^{T_c} (-3i_{\mathrm{N1},x}/4 - i_{\mathrm{N2},x}/4)dt\right] / C_{\mathrm{d}} \tag{4a}$$

TABLE I
SWITCHING STATES OF FIVE-LEVEL HC INVERTER

$S_{1,x}$	$S_{2,x}$	$S_{3,x}$	$S_{4,x}$	$S_{5,x}$	$i_{N1,x}$	$i_{N2,x}$	$i_{f1,x}$	$i_{f2,x}$	$V_{o,x}$	switching states
0	0	0	0	0	0	0	0	0	0	V_0
0	0	0	1	0	0	0	0	$i_{o,x}$	E	V_1
0	0	1	0	0	0	0	$i_{o,x}$	-$i_{o,x}$	E	V_2
0	1	0	0	0	$i_{o,x}$	0	-$i_{o,x}$	0	E	V_3
1	0	0	0	1	0	$i_{o,x}$	0	0	E	V_4
0	0	1	1	0	0	0	$i_{o,x}$	0	$2E$	V_5
0	1	0	1	0	$i_{o,x}$	0	-$i_{o,x}$	$i_{o,x}$	$2E$	V_6
0	1	1	0	0	$i_{o,x}$	0	0	-$i_{o,x}$	$2E$	V_7
1	0	0	1	1	0	$i_{o,x}$	0	$i_{o,x}$	$2E$	V_8
1	0	1	0	1	0	$i_{o,x}$	$i_{o,x}$	-$i_{o,x}$	$2E$	V_9
1	1	0	0	1	0	0	-$i_{o,x}$	0	$2E$	V_{10}
0	1	1	1	0	$i_{o,x}$	0	0	0	$3E$	V_{11}
1	0	1	1	1	0	$i_{o,x}$	$i_{o,x}$	0	$3E$	V_{12}
1	1	0	1	1	0	0	-$i_{o,x}$	$i_{o,x}$	$3E$	V_{13}
1	1	1	0	1	0	0	0	-$i_{o,x}$	$3E$	V_{14}
1	1	1	1	1	0	0	0	0	$4E$	V_{15}

$$\Delta u_{d2,x} = \left[\int_0^{T_c} (i_{N1,x}/2 - i_{N2,x}/2)dt\right]/C_d \tag{4b}$$

$$\Delta u_{d3,x} = \left[\int_0^{T_c} (i_{N1,x}/4 + 3i_{N2,x}/4)dt\right]/C_d \tag{4c}$$

where T_c is a carrier period time, $\Delta u_{d1,x}$, $\Delta u_{d2,x}$, Δu_{d3} denote the voltage deviation of dc-link capacitors C_{d1}, C_{d2}, C_{d3} caused by NP currents, respectively.

Equation (4) shows that the voltage of C_{d2} is naturally balanced when the integrals of $i_{N1,x}$ and $i_{N2,x}$ are equal in a carrier period, on the contrary, the unbalanced voltages of C_{d1} and C_{d3} are related to the integral of the sum of $i_{N1,x}$ and $i_{N2,x}$, which can be written as follows:

$$\Delta u_{d3,x} - \Delta u_{d1,x} = \left[\int_0^{T_c} (i_{N1,x} + i_{N2,x})dt\right]/C_d. \tag{5}$$

The average-value model is employed to eliminate the integral term and simplify the operation in a carrier period, so that the influence of average NP currents on the dc-link capacitors can be rewritten as follows:

$$\Delta u_{d2,x} = T_c \cdot (\bar{i}_{N1,x}/2 - \bar{i}_{N2,x}/2)/C_d \tag{6a}$$

$$\Delta u_{d3,x} - \Delta u_{d1,x} = T_c \cdot (\bar{i}_{N1,x} + \bar{i}_{N2,x})/C_d. \tag{6b}$$

B. Influence of Traditional PS-PWM Method on NP Currents

The PS-PWM can ensure the voltage natural balance of the dc-link center capacitor and floating capacitors of the five-level HC inverter under ideal conditions. The PS-PWM method for five-level HC inverter is shown in Fig. 3. The reference modulation voltage $u_{r,x}$ of each switch is the same and is compared with the four symmetrical triangle carriers $C_{r1,x}$–$C_{r4,x}$ to obtain the corresponding gate signals. The carriers are phase shifted by $\pi/2$ or -$\pi/2$ between each other, corresponding to the switches $S_{4,x}$–$S_{1,x}$, respectively. It is worth noting that the switching states of five-level HC inverter are symmetric, so the case of $0.5 \le u_{r,x} \le 1$ can be obtained by analogy from the case of $0 \le u_{r,x} \le 0.5$.

Defining the duty ratio of switches $S_{1,x}$–$S_{4,x}$ as $d_{1,x}$–$d_{4,x}$. When the PS-PWM method is used for five-level HC inverter, it is easy to obtain

$$u_{r,x} = d_{1,x} = d_{2,x} = d_{3,x} = d_{4,x} \tag{7a}$$

$$u_{r,x} = u_{o,x}/4E \tag{7b}$$

where $u_{o,x}$ is average output phase voltage which is the average value of $V_{o,x}$ in a carrier period.

The five-level HC inverter has five voltage levels which are 0, E, $2E$, $3E$, and $4E$. Therefore, the average output phase voltage of HC inverter is in the range of [0, $4E$]. Between two adjacent voltage levels, the combination of switching states is fixed, and thus, $u_{o,x}$ is divided into four ranges which are $0 \le u_{o,x} < E$, $E \le u_{o,x} < 2E$, $2E \le u_{o,x} < 3E$, and $3E \le u_{o,x} \le 4E$. This categorization can be referred to [22]. According to (7b), $u_{r,x}$ also can be divided into four ranges which are $0 \le u_{r,x} < 0.25$, $0.25 \le u_{r,x} < 0.5$, $0.5 \le u_{r,x} < 0.75$, and $0.75 \le u_{r,x} \le 1$.

It is assumed that the carrier frequency is much larger than the fundamental frequency, then $i_{o,x}$ can be equivalent to a constant within one carrier period. Equation (2c) implies that $i_{N,x}$ depends on the nonoverlapping region between the on-time of $S_{1,x}$ and $S_{2,x}$. Fig. 3 shows the traditional PS-PWM method for five-level HC inverter. When $0 \le u_{r,x} < 0.25$, as shown in Fig. 3(a), the on-time of $S_{1,x}$ and $S_{2,x}$ do not overlap with each other. Therefore, based on (7a), the sum of the single-phase average NP currents can be written as follows:

$$\bar{i}_{N,x} = \bar{i}_{N1,x} + \bar{i}_{N2,x} = (d_{1,x} + d_{2,x}) \cdot i_{o,x} = 2u_{r,x} \cdot i_{o,x}. \tag{8}$$

When $0.25 \le u_{r,x} < 0.5$, as shown in Fig. 3(b), the on-time region of $S_{1,x}$ and $S_{2,x}$ are overlapped partially, and the carriers are symmetrical and evenly distributed. Based on (2c) and (7a), the nonoverlapping region between the on-time of $S_{1,x}$ and $S_{2,x}$ are constant. the sum of the single-phase average NP currents

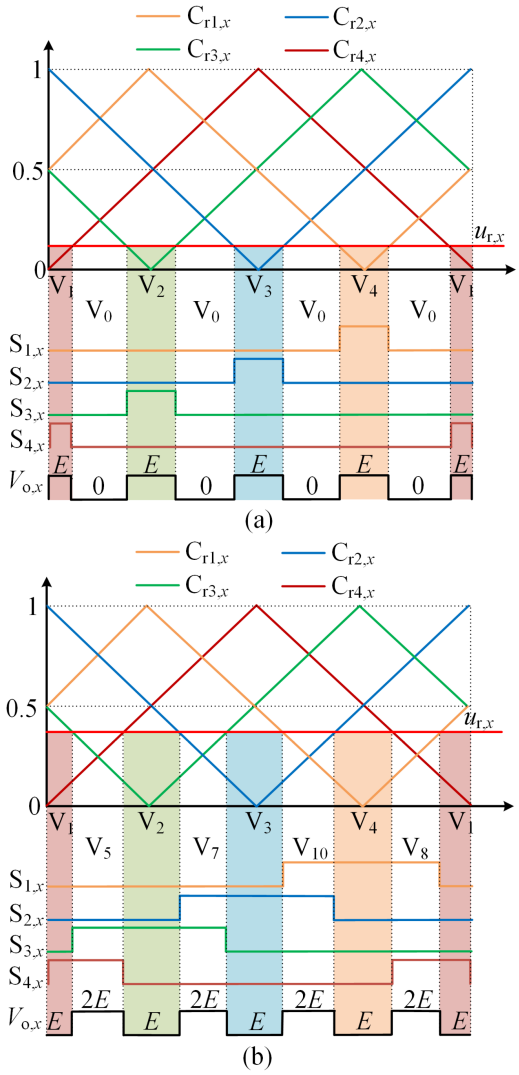

Fig. 3. Traditional PS-PWM method for five-level HC inverter, (a) $0 \le u_{\mathrm{r},x} < 0.25$, (b) $0.25 \le u_{\mathrm{r},x} < 0.5$.

can be written as follows:

$$\bar{i}_{\mathrm{N},x} = (1/4 + 1/4) \cdot i_{o,x} = i_{o,x}/2. \tag{9}$$

When $0.5 \le u_{\mathrm{r},x} \le 1$, the same analytical approach can be employed to obtain the sum of the single-phase average NP currents. When $0.5 \le u_{\mathrm{r},x} < 0.75$, the expression for the average NP currents is the same as (9). When $0.75 \le u_{\mathrm{r},x} \le 1$, the average NP currents can be written as follows:

$$\bar{i}_{\mathrm{N},x} = [(1 - d_{1,x}) + (1 - d_{2,x})] \cdot i_{o,x} = 2(1 - u_{\mathrm{r},x}) \cdot i_{o,x}. \tag{10}$$

It is worth noting that the above functional relationship is derived on the premise that carriers $\mathrm{C}_{r1,x}$ and $\mathrm{C}_{r2,x}$ are phase shifted by $\pi/2$ or -$\pi/2$. In this case, the switching states combination (V_5, V_{10}, V_7, V_8) or (V_5, V_{10}, V_6, V_9) with complementary currents is selected, which depends on the different phase shift directions between $\mathrm{C}_{r3,x}$ and $\mathrm{C}_{r4,x}$. Further, when $\mathrm{C}_{r1,x}$ and $\mathrm{C}_{r2,x}$ are phase shifted by π or -π, only the switching states combination (V_7, V_8, V_6, V_9) is selected. The relationship

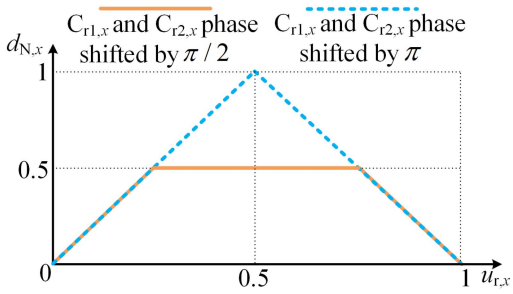

Fig. 4. Relationship between $u_{\mathrm{r},x}$ and $d_{\mathrm{N},x}$ which is based on different phase shifts of $\mathrm{C}_{1,x}$ and $\mathrm{C}_{2,x}$.

between duty ratio of average NP currents and reference modulation voltage is the same as ANPC [19], NNPC [23], and SM [26], which can be expressed as: $\bar{i}_{\mathrm{N},x} = 2u_{\mathrm{r},x} \cdot i_{o,x}$ $(0 \le u_{\mathrm{r},x} < 0.5)$ and $\bar{i}_{\mathrm{N},x} = 2(1 - u_{\mathrm{r},x}) \cdot i_{o,x}$ $(0.5 \le u_{\mathrm{r},x} \le 1)$.

Defining $d_{\mathrm{N},x}$ as the duty ratio of average NP currents, then (8)–(10) can be rewritten as follows:

$$\bar{i}_{\mathrm{N},x} = 2\bar{i}_{\mathrm{N1},x} = 2\bar{i}_{\mathrm{N2},x} = d_{\mathrm{N},x} \cdot i_{o,x}. \tag{11}$$

Equation (11) demonstrates that the average NP current is related to $d_{\mathrm{N},x}$ and $i_{o,x}$, $i_{o,x}$ depends on the characteristics of load, and cannot be modified actively. $d_{\mathrm{N},x}$ is related to $u_{\mathrm{r},x}$, and thus, the functional relationship between $u_{\mathrm{r},x}$ and $d_{\mathrm{N},x}$ plays an important role on the influence of the average NP current. In addition, the functional relationship between $u_{\mathrm{r},x}$ and $d_{\mathrm{N},x}$ is determined by the different phase shifts of $\mathrm{C}_{r1,x}$ and $\mathrm{C}_{r2,x}$, therefore, the phase shifts of $\mathrm{C}_{r1,x}$ and $\mathrm{C}_{r2,x}$ affect the NP current, and consequently the balance of the NP voltage. Based on (8)–(11), the relationship between $u_{\mathrm{r},x}$ and $d_{\mathrm{N},x}$ which $\mathrm{C}_{r1,x}$ and $\mathrm{C}_{r2,x}$ phase shifted by $\pi/2$ can be easily obtained. Similarly, when $\mathrm{C}_{r1,x}$ and $\mathrm{C}_{r2,x}$ phase shifted by π, the relationship between $u_{\mathrm{r},x}$ and $d_{\mathrm{N},x}$ can be expressed as: $d_{\mathrm{N},x} = 2u_{\mathrm{r},x}$ $(0 \le u_{\mathrm{r},x} < 0.5)$, $d_{\mathrm{N},x} = 2(u_{\mathrm{r},x} - 1)$ $(0.5 \le u_{\mathrm{r},x} \le 1)$. Finally, the relationship between $u_{\mathrm{r},x}$ and $d_{\mathrm{N},x}$ based on different phase shifts of $\mathrm{C}_{r1,x}$ and $\mathrm{C}_{r2,x}$ is shown in Fig. 4. The area enclosed by $\mathrm{C}_{r1,x}$ and $\mathrm{C}_{r2,x}$ phase shifted by $\pi/2$ is the smallest, which has smaller NP currents and lower dc-link capacitor voltage fluctuations. Furthermore, the complementary switching states V_6 and V_9 have the worst output performance due to $i_{o,x}$ flowing through more floating capacitors. Therefore, switching states combination (V_5, V_{10}, V_7, V_8) is the appropriate choice, when the SP-PWM method is used with symmetrical triangle carriers.

C. Proposed Modulation Strategy With Enhanced NP Voltage Balancing Capability

The five-level HC is a state-of-the-art topology with multiple switching states, which provides flexibility in terms of switching state combinations. However, the existing modulation method is a modification of the action time or action sequence of the switching states, which is still based on the symmetrical triangular carrier PS-PWM method [31], [32]. And the combination of switching states is limited. Therefore, this section explores a

sawtooth triangle carrier-based modulation with a more reasonable combination of switching states, which enhances the NP voltage balancing capability.

When the instantaneous output voltage $V_{o,x}$ of the five-level HC inverter is E, the switching states V_1–V_4 must be selected to ensure the voltage natural balance of the floating capacitors $C_{\mathrm{f1},x}$, $C_{\mathrm{f2},x}$, and dc-link center capacitor C_{d2}. When the instantaneous output voltage $V_{o,x}$ is $2E$, the switching state combinations (V_5, V_{10}), (V_7, V_8), (V_6, V_9) and their recombinations all have capacitor voltage natural balancing capability. Here are a variety of alternatives, but it is easy to get that the switching state combination (V_5, V_{10}) is optimal due to the absence of NP currents and the unaffected voltage of floating capacitor $C_{\mathrm{f2},x}$.

Based on the above analysis, the proposed modulation method with sawtooth triangle carriers is shown in Fig. 5. The sawtooth carriers $\mathrm{C}_{\mathrm{r1},x}$ and $\mathrm{C}_{\mathrm{r3},x}$ with the same shape and phase shift are used jointly by switches $\mathrm{S}_{1,x}$ and $\mathrm{S}_{3,x}$. In contrast, the sawtooth carriers $\mathrm{C}_{\mathrm{r2},x}$ and $\mathrm{C}_{\mathrm{r4},x}$ with a phase shift of π are applied to switches $\mathrm{S}_{2,x}$ and $\mathrm{S}_{4,x}$. In addition, in order to obtain the switching state combination (V_5, V_{10}), the duty ratio of switches $\mathrm{S}_{2,x}$ and $\mathrm{S}_{3,x}$ should be changed in the opposite direction to that of switches $\mathrm{S}_{1,x}$ and $\mathrm{S}_{4,x}$. Then, the reference modulation voltages of switches $\mathrm{S}_{2,x}$ and $\mathrm{S}_{3,x}$ should be modified accordingly

$$\begin{cases} u_{\mathrm{r1},x} = d_{1,x} = u_{\mathrm{r},x} \\ u_{\mathrm{r2},x} = 1 - d_{2,x} = 1 - u_{\mathrm{r},x} \\ u_{\mathrm{r3},x} = 1 - d_{3,x} = 1 - u_{\mathrm{r},x} \\ u_{\mathrm{r4},x} = d_{4,x} = u_{\mathrm{r},x} \end{cases} \tag{12}$$

where $u_{\mathrm{r1},x}$–$u_{\mathrm{r4},x}$ represents the reference voltages of switches $\mathrm{S}_{1,x}$–$\mathrm{S}_{4,x}$. The reference modulation voltages of the switches can be regarded as constant within one carrier period. Therefore, the switching states sequence depends mainly on the shape of the carriers and the phase shift between the carriers. The proposed PS-PWM method utilizes sawtooth triangle carriers with identical shape, $\mathrm{C}_{r1,x}$ and $\mathrm{C}_{r3,x}$ share one carrier, while $\mathrm{C}_{r2,x}$ and $\mathrm{C}_{r4,x}$ share the other carrier, the phase shift between $\mathrm{C}_{r1,x}$ and $\mathrm{C}_{r2,x}$ is π. When $u_{\mathrm{r1},x}$ and $u_{\mathrm{r4},x}$ are greater than the corresponding carriers, the corresponding switches are ON, and conversely the switches are OFF. For $u_{\mathrm{r2},x}$ and $u_{\mathrm{r3},x}$, their operating rules are reversed. Under such a set of carriers and operating rules, the switching states sequence that is configured can be obtained. Similarly, in the simulations and experiments, the key to obtaining the required sequence of switching states is to set up the carriers and operating rules. The PLECS software and RT-BOX controller have configurable carrier modules, which includes carrier shape, phase shift, and operating rules. This ensures that a set switching sequence can be generated in simulation and experimentation. Finally, the proposed modulation method for obtaining instantaneous output voltage $V_{o,x}$ is shown in Fig. 6. In the three-phase five-level HC inverter, the carriers are required to be phase-shifted collectively by 0, $-3\pi/2$, and $3\pi/2$ for phases a, b, and c, respectively, which helps to reduce the total harmonic distortion of the line voltage.

Based on the proposed modulation method in Fig. 5, the average currents flowing out of the floating capacitors can be

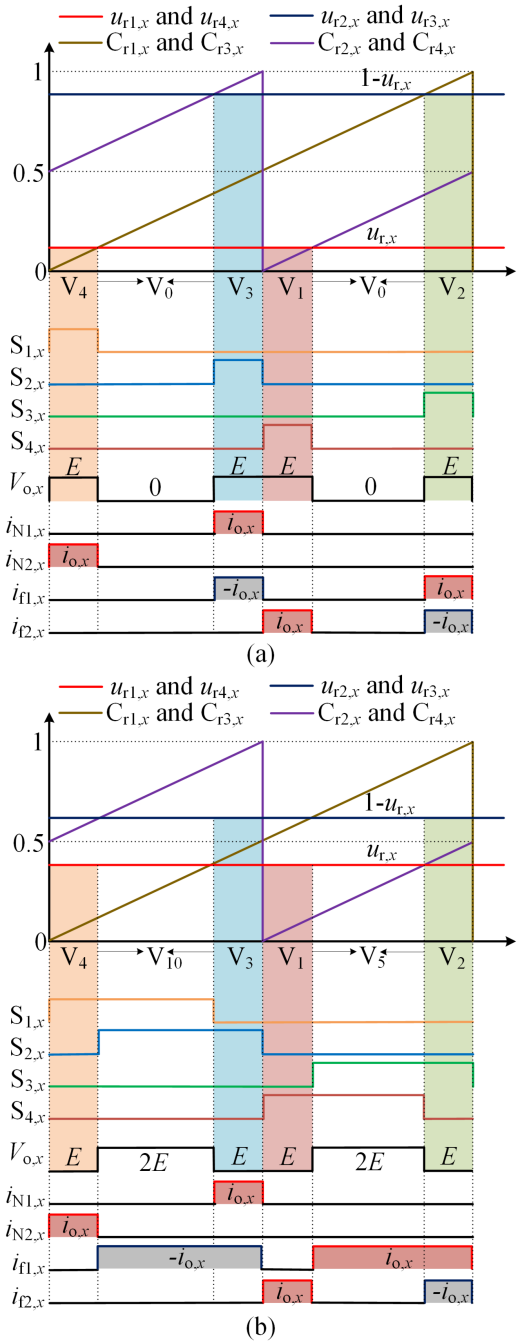

Fig. 5. Proposed modulation method with sawtooth triangle carriers, (a) $0 \le u_{\mathrm{r},x} < 0.25$, (b) $0.25 \le u_{\mathrm{r},x} < 0.5$.

written as follows:

$$\bar{i}_{\mathrm{f1},x} = (d_{3,x} - d_{2,x}) \cdot i_{o,x} \tag{13a}$$

$$\bar{i}_{\mathrm{f2},x} = (d_{4,x} - d_{3,x}) \cdot i_{o,x}. \tag{13b}$$

The difference between $\bar{i}_{\mathrm{N1},x}$ and $\bar{i}_{\mathrm{N2},x}$ can be expressed as follows:

$$\bar{i}_{\mathrm{N1},x} - \bar{i}_{\mathrm{N2},x} = (d_{2,x} - d_{1,x}) \cdot i_{o,x}. \tag{14}$$

According to (6) and (12)–(14), it can be derived that the average currents $\bar{i}_{\mathrm{f1},x}$, $\bar{i}_{\mathrm{f2},x}$, and $\bar{i}_{\mathrm{N1},x} - \bar{i}_{\mathrm{N2},x}$ are equal to zero

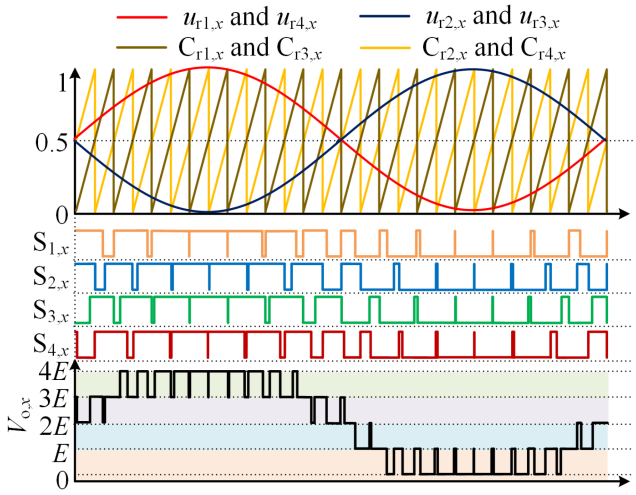

Fig. 6. Proposed modulation method for obtaining instantaneous output voltage $V_{o,x}$.

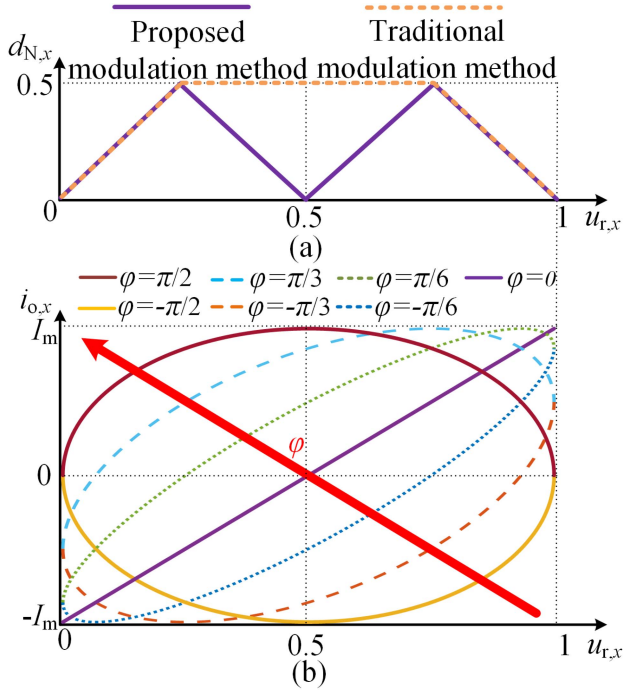

Fig. 7. Relationship between $u_{r,x}$ and different variables, (a) $d_{N,x}$, (b) $i_{o,x}$.

in a carrier period. This indicates that the proposed modulation method can maintain the natural voltage balance of the floating capacitors $C_{f1,x}$, $C_{f2,x}$ and DC-link center capacitor C_{d2} under ideal conditions. Further, the switching state combination (V_5, V_{10}, V_7, V_8) is replaced by (V_5, V_{10}), which reduces the currents flowing out of the NPs and floating capacitor $C_{f2,x}$. As a result, the voltage ripples of the dc-link capacitors C_{d2} and the floating capacitor $C_{f2,x}$ are reduced, which only sacrifices the voltage performance of the floating capacitor $C_{f1,x}$.

For the dc-link upper and lower capacitors C_{d1}, C_{d3}, the $d_{N,x}$ can be obtained according to the different ranges of $u_{r,x}$. When $0 \le u_{r,x} < 0.25$ or $0.75 \le u_{r,x} \le 1$, the expression of $d_{N,x}$ can be referred to (8) or (10), respectively. When $0.25 \le u_{r,x} < 0.5$, the $d_{N,x}$ is rewritten due to the modification of the switch state combination in Fig. 5(b), the nonoverlapping region between the on-time of $S_{1,x}$ and $S_{2,x}$ depends on duty cycle, $d_{N,x}$ can be written as follows:

$$d_{N,x} = (1/2 - d_{1,x}) + (1/2 - d_{2,x}) = 1 - 2u_{r,x}. \tag{15}$$

Correspondingly, when $0.5 \le u_{r,x} < 0.75$, due to the symmetry of the switching state combinations, $d_{N,x}$ is rewritten as follows:

$$d_{N,x} = (d_{1,x} - 1/2) + (d_{2,x} - 1/2) = 2u_{r,x} - 1. \tag{16}$$

Three-phase reference modulation voltages and the corresponding output phase currents can be expressed respectively as follows:

$$\begin{cases} u_{r,a} = 1/2 + m \cdot \sin(\theta)/2 \\ u_{r,b} = 1/2 + m \cdot \sin(\theta - 2\pi/3)/2 \\ u_{r,c} = 1/2 + m \cdot \sin(\theta + 2\pi/3)/2 \end{cases} \tag{17a}$$

$$\begin{cases} i_{o,a} = I_m \cdot \sin(\theta + \varphi) \\ i_{o,b} = I_m \cdot \sin(\theta - 2\pi/3 + \varphi) \\ i_{o,c} = I_m \cdot \sin(\theta + 2\pi/3 + \varphi) \end{cases} \tag{17b}$$

where m denotes modulation index, θ denotes the phase angle of the output voltage, I_m denotes the amplitude of the output current, and φ denotes the power factor angle.

Based on (8)–(11), (15) and (16), the relationship between $u_{r,x}$ and $d_{N,x}$ can be obtained as shown in Fig. 7(a). Meanwhile, based on (17), φ is taken to be $\pm\pi/2$, $\pm\pi/3$, $\pm\pi/6$, 0, respectively, and then calculating the $u_{r,x}$ and $i_{o,x}$, where θ varies between 0 and 2π, and then taking $u_{r,x}$ as the x-axis and $i_{o,x}$ as the y-axis, the relationship between $u_{r,x}$ and $i_{o,x}$ is shown in Fig. 7(b). From the (11), it can be derived that $\bar{i}_{Nx}$ is influenced by $d_{N,x}$ and $i_{o,x}$ simultaneously, $i_{o,x}$ is a function of the power factor angle φ. Combined with (6), $\bar{i}_{Nx}$ determines the unbalanced voltage between the upper and lower capacitors. Therefore, the power factor angle φ has a certain impact on the voltage balance of the dc-link capacitors. When φ is 0, the absolute value of the slope between $u_{r,x}$ and $i_{o,x}$ is relatively large. Both modulations have similar NP currents regulation capability, but the proposed modulation method has a smaller NP currents integration area resulting in a smaller NP voltage unbalancing. However, with the change of φ, the relationship between $u_{r,x}$ and $i_{o,x}$ changes from linear to elliptical. The worst case occurs at $\varphi = \pm\pi/2$. For traditional modulation, the maximum point of the trapezoidal function corresponds to the maximum $i_{o,x}$, and the strongest NP unbalanced voltage is generated here. However, the slope between $u_{r,x}$ and $i_{o,x}$ is minimal, which means that the regulation of the NP currents is greatly weakened with ZSV method, and the NP unbalanced voltage is difficult to be suppressed. As for the proposed modulation, the minimum point of the bi-triangular function corresponds to the maximum $i_{o,x}$, there is a considerable reduction in the unbalanced voltage caused by the maximum $i_{o,x}$, which significantly improves

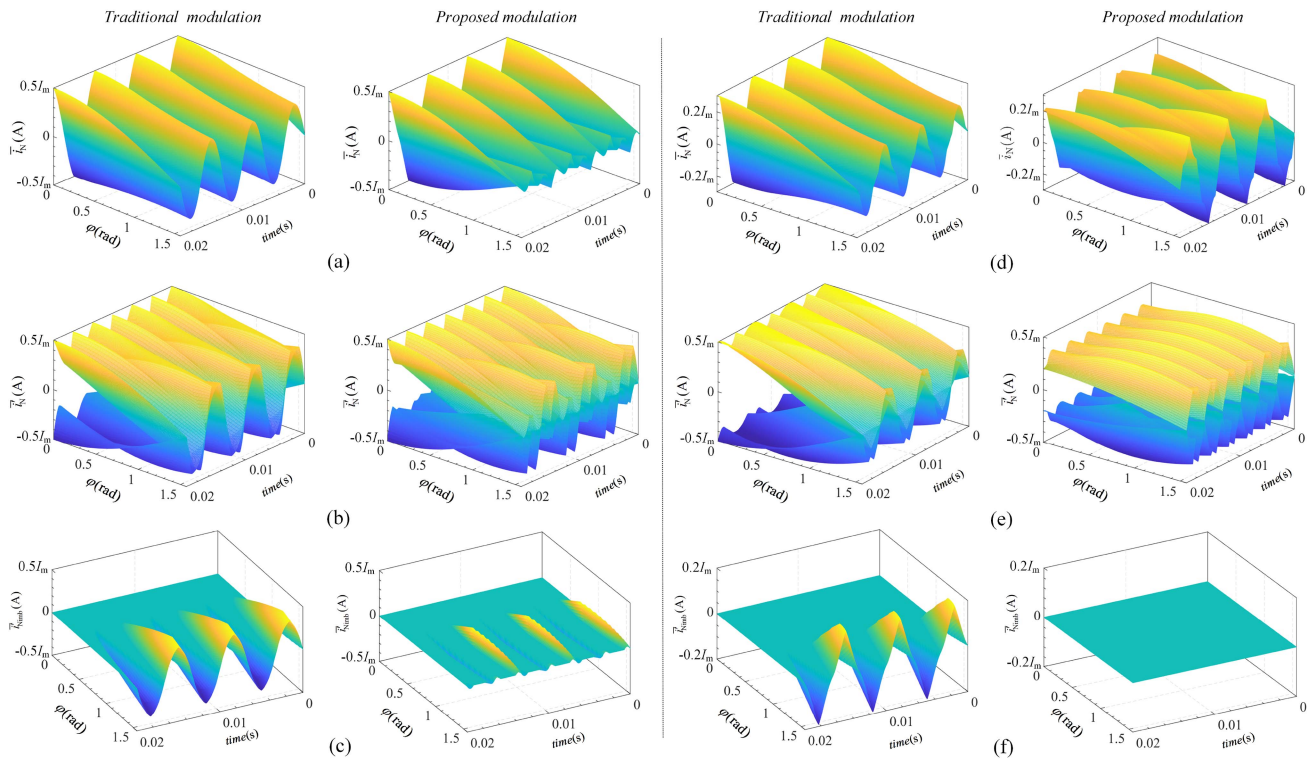

Fig. 8. Comprehensive comparison of different modulation methods on three-phase average NP currents, (a) $\bar{i}_{\mathrm{N}}$ without ZSV method, $m = 1$, (b) adjustable maximum and minimum value of $\bar{i}'_{\mathrm{N}}$ with ZSV method, $m = 1$, (c) imbalanced value of $\bar{i}'_{\mathrm{N}}$ with ZSV method, $m = 1$, (d) $\bar{i}_{\mathrm{N}}$ without ZSV method, $m = 0.8$, (e) adjustable maximum and minimum value of $\bar{i}'_{\mathrm{N}}$ with ZSV method, $m = 0.8$, (f) imbalanced value of $\bar{i}'_{\mathrm{N}}$ with ZSV method, $m = 0.8$.

the equivalent adjustment of the NP currents. This allows the five-level HC inverter to operate well over a wide range of power factors.

NP unbalanced voltage will cause low-frequency voltage ripples in the dc-link upper and lower capacitors. The capacitor voltages can be naturally balanced within a fundamental period. But under nonideal conditions, the capacitor voltages will diverge if not controlled. Therefore, ZSV is commonly used as an active balancing method to suppress low-frequency voltage fluctuations and voltage deviations of the dc-link capacitors. However, when the power factor is low and the modulation index is relatively large, the available ZSV range is limited significantly, which can only ensure the nondivergence of the capacitor voltage at the dc-link, but cannot suppress the low-frequency voltage fluctuation. The bi-triangular functional relationship between $u_{\mathrm{r},x}$ and $d_{\mathrm{N},x}$ is more helpful to eliminate the low-frequency voltage fluctuation, which will be explained in the subsequent content.

The voltage difference between capacitors C_{d3} and C_{d1} is impacted by the three-phase total average NP current

$$\bar{i}_{\mathrm{N}} = \bar{i}_{\mathrm{N,a}} + \bar{i}_{\mathrm{N,b}} + \bar{i}_{\mathrm{N,c}} = d_{\mathrm{N,a}} \cdot i_{\mathrm{o,a}} + d_{\mathrm{N,b}} \cdot i_{\mathrm{o,b}} + d_{\mathrm{N,c}} \cdot i_{\mathrm{o,c}}. \tag{18}$$

When the ZSV method is employed, the reference modulation voltage can be rewritten as follows:

$$u'_{\mathrm{r},x} = u_{\mathrm{r},x} + u_{\mathrm{z}} \tag{19}$$

ZSV method is constrained by the linear modulation range

$$-\min(u_{\mathrm{r},x}) \le u_{\mathrm{z}} \le 1 - \max(u_{\mathrm{r},x}). \tag{20}$$

When ZSV is injected, (18) is modified to

$$\bar{i}'_{\mathrm{N}} = d'_{\mathrm{N,a}} \cdot i_{\mathrm{o,a}} + d'_{\mathrm{N,b}} \cdot i_{\mathrm{o,b}} + d'_{\mathrm{N,c}} \cdot i_{\mathrm{o,c}}. \tag{21}$$

Based on (15)–(18), three-phase total average NP current $\bar{i}_{\mathrm{N}}$ is jointly influenced by the power factor angle φ, modulation index m, amplitude of the output current I_{m}, and the phase angle of the output voltage θ. A comprehensive comparison of the proposed modulation method and the traditional modulation method is given to further analyze the impact on $\bar{i}_{\mathrm{N}}$ by holding constant value of m. The influence of different modulation methods on $\bar{i}_{\mathrm{N}}$ for $m = 1$ is given in Fig. 8(a). When the power factor angle is small, $\bar{i}_{\mathrm{N}}$ displays triple-frequency fluctuations with an amplitude of $0.5I_{\mathrm{m}}$, which is similar for both two modulation methods. However, in inductive/capacitive load-dominated applications with larger power factor angle, the advantages of the proposed modulation method are obvious, the fluctuation amplitude of $\bar{i}_{\mathrm{N}}$ is extremely small and the fluctuation frequency is nine times. This means that the voltage ripples in the upper and lower capacitors of the dc-link are drastically reduced without the influence of the ZSV method. When $m = 0.8$, this advantage is not obvious, the two modulation methods have similar $\bar{i}_{\mathrm{N}}$ throughout the power factor range, which can be derived from Fig. 8(d).

Equations (19)–(21) imply that three-phase total average NP current can be actively adjusted by ZSV method. However, $d_{\mathrm{N},x}$

is a segmented function, which makes it complicated to obtain the analytic equations for the maximum and minimum values of $\bar{i}'_{\rm N}$ [20]. A simple solution is to take the ZSVs equidistantly according to the constraint range of (20), then $\bar{i}'_{\rm N}$ is calculated from the corresponding ZSVs, the maximum and minimum values of $\bar{i}'_{\rm N}$ are identified. The adjustable range of $\bar{i}'_{\rm N}$ which is based on the ZSV method is shown in Fig. 8(b) and (e). When $m = 1$, both modulation methods have a wide $\bar{i}'_{\rm N}$ adjustment range at low power factor angle. Comparatively, at high power factor angle, the proposed method still has an appreciable $\bar{i}'_{\rm N}$ adjustment range, and it is extended further at $m = 0.8$. For traditional modulation methods, the adjustment range of $\bar{i}'_{\rm N}$ is limited significantly, which leads to considerable voltage ripples, and this situation is not alleviated even at $m = 0.8$.

The selective range of ZSV is limited because of the constraint of linear modulation range. Thus, NP current cannot be balanced at each carrier period, the imbalance of $\bar{i}'_{\rm N}$ needs to be explored. Defining the imbalanced value of $\bar{i}'_{\rm N}$ as $\bar{i}'_{\rm Nimb}$, when $\bar{i}_{\rm N}$ can be fully suppressed by the ZSV method, the value of $\bar{i}'_{\rm Nimb}$ is expressed as zero, otherwise, $\bar{i}'_{\rm Nimb}$ is expressed as maximum or minimum value of $\bar{i}'_{\rm N}$, which can be expressed as follows:

$$\bar{i}'_{\rm Nimb} = \begin{cases} 0, & \text{if } \bar{i}_{\rm N} \geq 0 \text{ and } \bar{i}'_{\rm Nmin} \leq 0 \\ \bar{i}'_{\rm Nmin}, & \text{else if } \bar{i}_{\rm N} \geq 0 \text{ and } \bar{i}'_{\rm Nmin} > 0 \\ 0, & \text{else if } \bar{i}_{\rm N} < 0 \text{ and } \bar{i}'_{\rm Nmax} \geq 0 \\ \bar{i}'_{\rm Nmax}, & \text{otherwise} \end{cases} \tag{22}$$

where $\bar{i}'_{\rm Nmax}$ and $\bar{i}'_{\rm Nmin}$ are adjustable maximum and minimum value of $\bar{i}'_{\rm N}$ with ZSV method, respectively. Fig. 8(c) and (f) demonstrates the imbalanced value of $\bar{i}'_{\rm N}$ with ZSV method. $\bar{i}'_{\rm Nimb}$ equals zero at a small power factor angle, which indicates that the imbalanced $\bar{i}'_{\rm N}$ are well suppressed and NP unbalanced voltage eliminated completely by ZSV method. As the power factor angle increases, the ability of the ZSV method to suppress $\bar{i}'_{\rm Nimb}$ is diminished and $\bar{i}'_{\rm Nimb}$ grows with the increase of the power factor angle. When power factor angle is large, the traditional modulation method shows triple-frequency fluctuations in $\bar{i}'_{\rm Nimb}$ whether m is 1 or 0.8, this causes enormous voltage ripples of the dc-link capacitors and cannot be eliminated with ZSV method. In comparison, the proposed modulation method has a extremely small region and amplitude of $\bar{i}'_{\rm Nimb}$ at $m = 1$, and $\bar{i}'_{\rm Nimb}$ is completely suppressed at $m = 0.8$.

In summary, the proposed modulation method only increases the voltage ripple of $C_{{\rm f}1,x}$, while all other capacitor voltage ripples are reduced, and a more significant advantage is that the proposed modulation method has a stronger NP currents balancing capability relative to the traditional modulation method, then the low-frequency frequency voltage ripples of the dc-link upper and lower capacitors can be better suppressed and potential device damage is avoided. Further, the unbalanced NP current and the output current are related, this advantage is more obvious in low power factor applications with higher current. Therefore, the proposed modulation method enhances the voltage balancing capability of NPs significantly, which makes up for the shortcomings of traditional modulation methods with limited modulation index and power factor range. The low-frequency voltage ripples of dc-link capacitors are mainly third harmonic component. Generally, the carrier frequency is much larger than the fundamental frequency, and the low-frequency voltage fluctuations of the dc-link capacitors is related to the fundamental frequency. The switching frequency only affects the voltage ripple at the carrier frequency, not the low-frequency voltage ripples of dc-link capacitors. Therefore, the performance achieved by the proposed method is mainly dependent on the suppression of low-frequency voltage ripples.

III. Capacitor Voltage Active Balancing Strategy for Proposed Modulation Method

The proposed modulation method can ensure the natural balance of the capacitor voltages, however, they will still diverge under the influence of nonideal conditions such as dead time, load conditions, and inverter parameters. The capacitor voltage balance issues of the five-level HC inverter mainly include the voltage balance issue of the floating capacitors and dc-link center capacitor, and the voltage balance issue between the dc-link upper and lower capacitors. Therefore, the impact of the duty ratio on the voltage ripples of $C_{{\rm f}1,x}$, $C_{{\rm f}2,x}$, $C_{\rm d2}$, the ZSV method on voltage difference between $C_{\rm d1}$ and $C_{\rm d3}$ need to be analyzed for achieving the active balancing of capacitor voltages and ensuring the safe operation of five-level HC inverter.

A. Voltage Balance of $C_{{\rm f}1,x}$, $C_{{\rm f}2,x}$ and $C_{\rm d2}$

Assuming that the duty ratio adjustments $\Delta d_{1,x}$, $\Delta d_{2,x}$, $\Delta d_{3,x}$, and $\Delta d_{4,x}$ are added to the duty ratios $d_{1,x}$, $d_{2,x}$, $d_{3,x}$, and $d_{4,x}$, respectively. When $0 \leq u_{{\rm r},x} < 0.5$, the effects on the average currents are listed in Table II, and the similar conclusions can be obtained due to the symmetry of the circuit when $0.5 \leq u_{{\rm r},x} \leq 1$. Then, the average current of the single-phase outflow the dc-link center capacitor which is based on (12) and (14) can be expressed as follows:

$$\bar{i}_{{\rm N}1,x}/4 - \bar{i}_{{\rm N}2,x}/4 = (\Delta d_{2,x} - \Delta d_{1,x}) \cdot i_{{\rm o},x}/4. \tag{23}$$

The average currents flowing out of the floating capacitors can be expressed as follows:

$$\bar{i}_{{\rm f}1,x} = (\Delta d_{3,x} - \Delta d_{2,x}) \cdot i_{o,x} \tag{24a}$$

$$\bar{i}_{{\rm f}2,x} = (\Delta d_{4,x} - \Delta d_{3,x}) \cdot i_{o,x}. \tag{24b}$$

In order to unaffect the average output phase voltage, the following condition needs to be met:

$$\Delta d_{1,x} + \Delta d_{2,x} + \Delta d_{3,x} + \Delta d_{4,x} = 0. \tag{25}$$

According to the voltage ripple model of $C_{\rm d2}$ and (23), the required duty ratio adjustment to suppress the unbalanced voltage of $C_{\rm d2}$ in the next carrier period can be written as follows:

$$\Delta d_{{\rm d}2,x} = (\Delta d_{2,x} - \Delta d_{1,x}) = \frac{2C_{\rm d} \cdot (u_{\rm d2} - 2E)}{3T_{\rm c} \cdot i_{{\rm o},x}} \tag{26}$$

where $u_{\rm d2}$ represents the voltage of $C_{\rm d2}$.

Similarly, for the floating capacitors, the required duty ratio adjustment in the next carrier period can be expressed as follows:

$$\Delta d_{{\rm f}1,x} = (\Delta d_{3,x} - \Delta d_{2,x}) = \frac{C_{{\rm f}1,x} \cdot (u_{{\rm f}1,x} - 2E)}{T_{\rm c} \cdot i_{{\rm o},x}} \tag{27a}$$

TABLE II
EFFECTS OF DUTY RATIO ADJUSTMENTS ON AVERAGE CURRENTS

The range of $u_{\mathrm{r},x}$	Duty ratios	$\bar{i}_{\mathrm{N1},x}$	$\bar{i}_{\mathrm{N2},x}$	$\bar{i}_{\mathrm{f1},x}$	$\bar{i}_{\mathrm{f2},x}$
$0 \le u_{\mathrm{r},x} < 0.25$	$d_{1,x}+\Delta d_{1,x}$	0	$\Delta d_{1,x}\cdot i_{\mathrm{o},x}$	0	0
	$d_{2,x}+\Delta d_{2,x}$	$\Delta d_{2,x}\cdot i_{\mathrm{o},x}$	0	$-\Delta d_{2,x}\cdot i_{\mathrm{o},x}$	0
	$d_{3,x}+\Delta d_{3,x}$	0	0	$\Delta d_{3,x}\cdot i_{\mathrm{o},x}$	$-\Delta d_{3,x}\cdot i_{\mathrm{o},x}$
	$d_{4,x}+\Delta d_{4,x}$	0	0	0	$\Delta d_{4,x}\cdot i_{\mathrm{o},x}$
$0.25 \le u_{\mathrm{r},x} < 0.5$	$d_{1,x}+\Delta d_{1,x}$	$-\Delta d_{1,x}\cdot i_{\mathrm{o},x}$	0	0	0
	$d_{2,x}+\Delta d_{2,x}$	0	$-\Delta d_{2,x}\cdot i_{\mathrm{o},x}$	$-\Delta d_{2,x}\cdot i_{\mathrm{o},x}$	0
	$d_{3,x}+\Delta d_{3,x}$	0	0	$\Delta d_{3,x}\cdot i_{\mathrm{o},x}$	$-\Delta d_{3,x}\cdot i_{\mathrm{o},x}$
	$d_{4,x}+\Delta d_{4,x}$	0	0	0	$\Delta d_{4,x}\cdot i_{\mathrm{o},x}$

$$\Delta d_{\mathrm{f2},x} = (\Delta d_{4,x} - \Delta d_{3,x}) = \frac{C_{\mathrm{f2},x}\cdot(u_{\mathrm{f2},x}-E)}{T_{\mathrm{c}}\cdot i_{\mathrm{o},x}} \tag{27b}$$

where $C_{\mathrm{f1},x}$ and $C_{\mathrm{f2},x}$ denote the capacitances. $u_{\mathrm{f1},x}$ and $u_{\mathrm{f2},x}$ represent the voltages of corresponding floating capacitors.

Based on (25)–(27), the following system of voltage control equations can be obtained:

$$\begin{cases} \Delta d_{2,x} - \Delta d_{1,x} = \Delta d_{\mathrm{d2},x} \\ \Delta d_{3,x} - \Delta d_{2,x} = \Delta d_{\mathrm{f1},x} \\ \Delta d_{4,x} - \Delta d_{3,x} = \Delta d_{\mathrm{f2},x} \\ \Delta d_{1,x} + \Delta d_{2,x} + \Delta d_{3,x} + \Delta d_{4,x} = 0 \end{cases}. \tag{28}$$

Independent decoupling control of each capacitor voltage can be achieved by setting two values of the three variables $\Delta d_{\mathrm{d2},x}$, $\Delta d_{\mathrm{f1},x}$, $\Delta d_{\mathrm{f2},x}$ to zero.

When the values of $\Delta d_{\mathrm{f1},x}$ and $\Delta d_{\mathrm{f2},x}$ are zero, the voltage of C_{d2} can be controlled independently and the solution of (28) can be expressed as follows:

$$\begin{cases} \Delta d_{1,x} = -3\Delta d_{\mathrm{d2},x}/4 \\ \Delta d_{2,x} = \Delta d_{\mathrm{d2},x}/4 \\ \Delta d_{3,x} = \Delta d_{\mathrm{d2},x}/4 \\ \Delta d_{4,x} = \Delta d_{\mathrm{d2},x}/4 \end{cases}. \tag{29}$$

Analogously, the solutions for the voltage balance control of $C_{\mathrm{f1},x}$ and $C_{\mathrm{f2},x}$ are expressed as (30a) and (30b), respectively

$$\begin{cases} \Delta d_{1,x} = -\Delta d_{\mathrm{f1},x}/2 \\ \Delta d_{2,x} = -\Delta d_{\mathrm{f1},x}/2 \\ \Delta d_{3,x} = \Delta d_{\mathrm{f1},x}/2 \\ \Delta d_{4,x} = \Delta d_{\mathrm{f1},x}/2 \end{cases} \tag{30a}$$

$$\begin{cases} \Delta d_{1,x} = -\Delta d_{\mathrm{f2},x}/4 \\ \Delta d_{2,x} = -\Delta d_{\mathrm{f2},x}/4 \\ \Delta d_{3,x} = -\Delta d_{\mathrm{f2},x}/4 \\ \Delta d_{4,x} = 3\Delta d_{\mathrm{f2},x}/4 \end{cases}. \tag{30b}$$

Then, the modified reference modulation voltages with voltage balancing capability are obtained by (12) and (29)–(30)

$$\begin{cases} u'_{\mathrm{r1},x} = u_{\mathrm{r},x} - \frac{3}{4}\Delta d_{\mathrm{d2},x} - \frac{1}{2}\Delta d_{\mathrm{f1},x} - \frac{1}{4}\Delta d_{\mathrm{f2},x} \\ u'_{\mathrm{r2},x} = 1 - \left(u_{\mathrm{r},x} + \frac{1}{4}\Delta d_{\mathrm{d2},x} - \frac{1}{2}\Delta d_{\mathrm{f1},x} - \frac{1}{4}\Delta d_{\mathrm{f2},x}\right) \\ u'_{\mathrm{r3},x} = 1 - \left(u_{\mathrm{r},x} + \frac{1}{4}\Delta d_{\mathrm{d2},x} + \frac{1}{2}\Delta d_{\mathrm{f1},x} - \frac{1}{4}\Delta d_{\mathrm{f2},x}\right) \\ u'_{\mathrm{r4},x} = u_{\mathrm{r},x} + \frac{1}{4}\Delta d_{\mathrm{d2},x} + \frac{1}{2}\Delta d_{\mathrm{f1},x} + \frac{3}{4}\Delta d_{\mathrm{f2},x} \end{cases}. \tag{31}$$

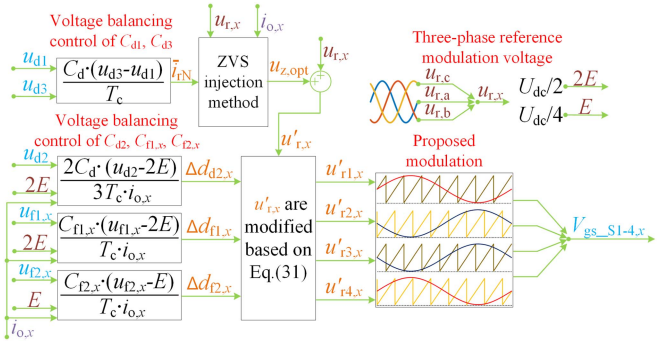

Fig. 9. Block diagram of capacitor voltage balancing control.

B. Voltage Balance of C_{d1} and C_{d3}

ZSV injection method is used to balance voltages of C_{d1} and C_{d3}, the required three-phase total average NP current can be written as followws:

$$\bar{i}_{\mathrm{rN}} = \frac{C_{\mathrm{d}}\cdot(u_{\mathrm{d3}}-u_{\mathrm{d1}})}{T_{\mathrm{c}}}. \tag{32}$$

The same philosophy of ZSV injection is used for proposed PS-PWM and traditional PS-PWM simultaneously. According to (19)–(21) and (32), when $\bar{i}_{\mathrm{rN}} = \bar{i}'_{\mathrm{N}}$, the optimal ZSV $u_{\mathrm{z,opt}}$ can be solved. However, the relationship between $d_{\mathrm{N},x}$ and $u_{\mathrm{r},x}$ is a segmental function, it is difficult to solve the optimal ZSV directly [20]. Therefore, an alternative way to obtain an approximate $u_{\mathrm{z,opt}}$, and then, to achieve the voltage balance of the dc-link capacitors can be divided into the following steps:

Step I: According to (20), the range of u_{z} is determined. Then, k equidistant ZSVs are selected and labeled as $u_{\mathrm{z},k}$.

Step II: Taking $u_{\mathrm{z},k}$ into (19) and (21) to calculate $\bar{i}'_{\mathrm{N},k}$, while $\bar{i}_{\mathrm{rN}}$ is obtained according to (32).

Step III: Comparing $\bar{i}'_{\mathrm{N},k}$ with $\bar{i}_{\mathrm{rN}}$ and choosing the $u_{\mathrm{z},k}$, which produces the closest $\bar{i}'_{\mathrm{N},k}$ to $\bar{i}_{\mathrm{rN}}$ as $u_{\mathrm{z,opt}}$.

Whether the traditional method or the proposed method, they both use *Step I–Step III* to solve for the optimal ZSV, and thus, their solution concept of ZSV is the same. The block diagram of the capacitor voltage balance control is shown in Fig. 9. The ZSV method is used to achieve voltage balance between C_{d1} and C_{d3}, while the reference modulation voltages are modified to achieve voltage balance of $C_{\mathrm{f1},x}$, $C_{\mathrm{f2},x}$, and C_{d2}, in order to avoid the voltage harmonics caused by the excessive duty ratio

TABLE III
CIRCUIT PARAMETERS USED IN THE SIMULATION

Parameters	Value
Rated volume	1 MVA
DC-link voltage	U_{dc} = 4.8 kV
DC-link capacitors	C_{d1} = C_{d3} = 560 μF, C_{d2} = 280 μF
Floating capacitors	$C_{\mathrm{f1},x}$ = 560 μF, $C_{\mathrm{f2},x}$ = 280 μF
Carriers frequency	f_{c} = 10 kHz
Fundamental frequency	f = 50 Hz
R-L load	R = 2.5 Ω, L = 32 mH

adjustments, the range of $\Delta d_{\mathrm{d2},x}$, $\Delta d_{\mathrm{f1},x}$, and $\Delta d_{\mathrm{f2},x}$ should be restricted. Finally, the reference modulation voltages are compared with the corresponding sawtooth triangle carriers to obtain the gate signals of the switches. With this method, all capacitor voltages can be controlled independently and decoupled from each other. It is worth noting that the voltage balancing control in Fig. 9 modifies the reference voltage slightly, and then affects the action time of the switching states, which does not change the defined sequence of switching states.

IV. SIMULATION RESULTS

Five-level HC multilevel inverter is attractive for medium and high power applications [22]. Therefore, a 1MVA five-level HC inverter has been modeled in simulation environment, and R = 2.5 Ω, L = 32 mH are chosen to verify the advantages of the proposed modulation method at a low power factor of 0.241. The circuit parameters used for simulation are listed in Table III. The ZSV injection must be performed to maintain the voltage balance of the dc-link capacitors, otherwise, the five-level HC inverter will not work properly. Therefore, the same ZSV injection philosophy is applied to each experiment, and combined with modulation methods for comparison studies.

A comprehensive comparison of different modulation indexes and modulation methods is shown in the Fig. 10. In the simulation, the optimal ZSV is injected after 0.2 s. When m = 1, the line voltage and phase voltage waveforms under the traditional modulation method have obvious low-frequency voltage ripples, which are not effectively suppressed after the ZSV injection method is adopted. In contrast, the low-frequency voltage ripples in the output waveforms are not obvious when the proposed modulation is implemented. At $m = 0.8$, the voltage ripples of the traditional modulation method are alleviated, but the phase voltage level jump is more serious. In comparison, the proposed modulation method still has a good output performance. Due to the large inductive load, the phase currents of both methods show highly sinusoidal waveforms with almost no difference. For three-phase reference modulation voltages and ZSVs, the three-phase modulated voltage generated by the traditional modulation method is severely limited to the linear modulation range of [0,1]. Meanwhile, the optimal ZSV is severely constrained by the maximum and minimum value of ZSVs. All of this means that it is not possible to find the optimal ZSV to suppress the voltage ripples of the dc-link upper and lower capacitors at m = 1. However, the three-phase reference modulation voltage of the proposed modulation method is much less affected by the constraint of the linear modulation range, which is helpful to find the optimal ZSV. When $m = 0.8$, traditional modulation method is still strongly constrained by the linear modulation range, while the proposed modulation method is almost unconstrained. For the dc-link capacitors and floating capacitors, both modulation methods have similar effects on voltage ripples, but the impacts on the low-frequency voltage ripples of dc-link upper and lower capacitors are completely different. when $m = 1$ and the traditional modulation method is implemented, the difference between low-frequency voltage ripples of dc-link upper and lower capacitors is 180 V, which is reduced to 160 V after ZSV injection. when $m = 0.8$, the difference of low-frequency voltage ripples is 96 V, and it reduced to 60 V after the ZSV is injected. In comparative terms, the proposed modulation method has obvious advantages, the difference of low-frequency voltage ripples is 56 V at $m = 1$, which becomes 26 V after ZSV injection and voltage ripples reduced by nearly six times. When $m = 0.8$, the low-frequency voltage ripple of 110 V is completely suppressed by the ZSV method. Thus, the proposed modulation method alleviates the power switch overvoltage problem in low power factor applications, which avoids the potential damage caused by the five-level HC inverter being out of the safe operating area.

Fig. 11 shows the line voltage FFT analysis of different modulations at $m = 1$. The total harmonic distortion of the line voltage for the traditional modulation is 22.28%, while proposed modulation is better for 21.51%. Further, the traditional modulation has the four times equivalent switching frequency, while the proposed modulation has the twice equivalent switching frequency, this can be due to the fact that only two triangular carriers shifted by π are implemented in the proposed modulation method.

Fig. 12 shows the three-phase current and capacitor voltage ripples at a high power factor and high modulation index, R = 15 Ω, L = 5 mH are chosen to compare different modulation methods with a power factor of 0.994 and $m = 1$. After ZSV injection, the low-frequency voltage ripples of both modulations are suppressed completely, and both modulation methods have shown excellent performance at a high power factor and high modulation index.

Fig. 13 shows the variable voltage and variable frequency(VVVF) control of five-level HC inverter, the modulation index changes from 0 to 1 within 1 s, while the fundamental frequency changes from 0 to 50 Hz, which is similar to the start-up process of the motor. When the traditional modulation method is implemented, the low-frequency voltage ripples of the dc-link upper and lower capacitors cannot be balanced after $m = 0.6$ and rise sharply with the increasing of the modulation index. For the proposed modulation, all capacitor voltages remain well balanced over the whole modulation index range and fundamental frequency.

In Fig. 14, the c-phase load resistance is modified from 2.5 Ω to 11 Ω to verify the voltage balancing capability of different modulations at $m = 1$. In the traditional modulation, the difference of low-frequency voltage ripples of dc-link upper and lower capacitors changes from 160 to 230 V, while the difference of

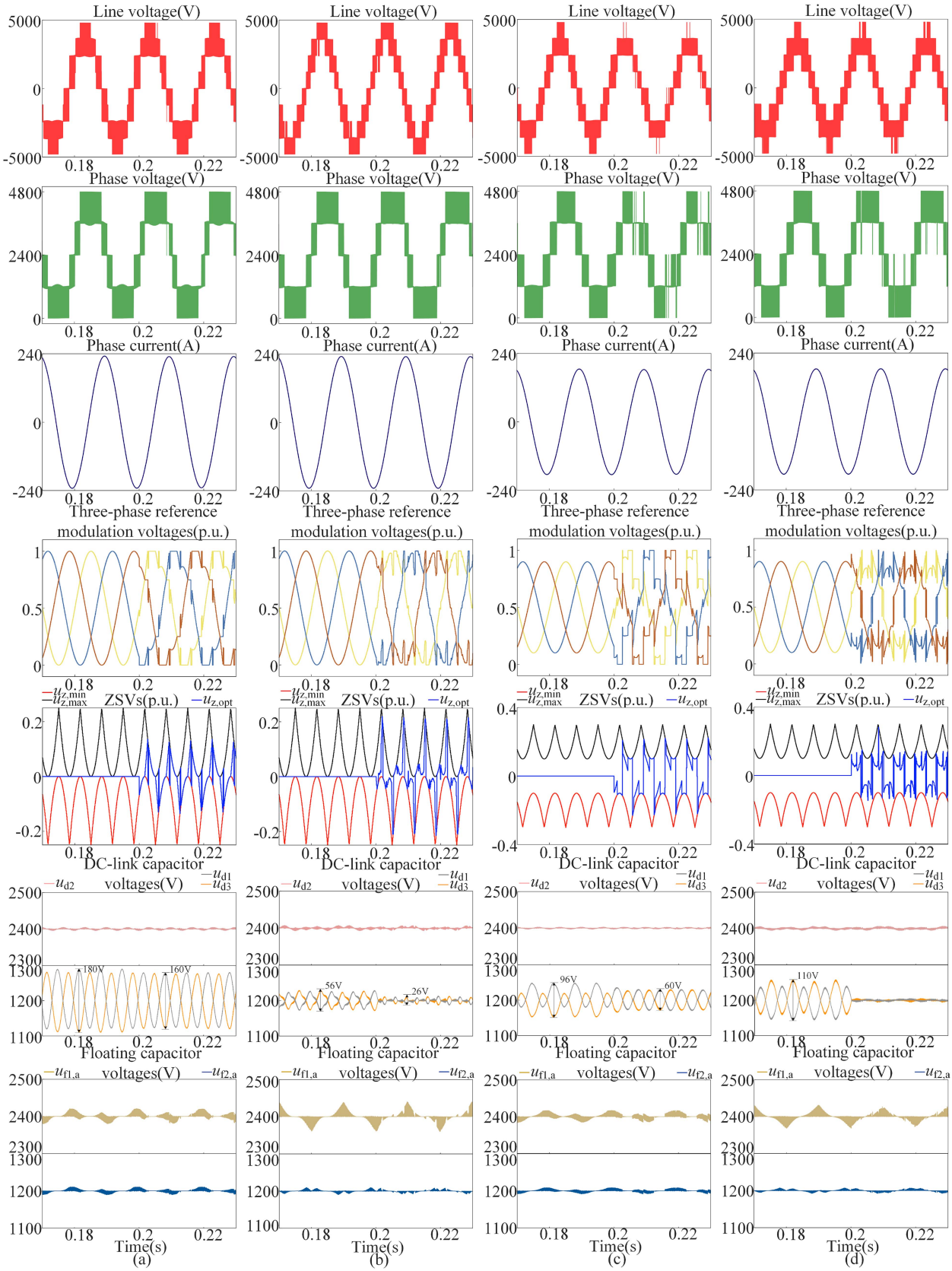

Fig. 10. Comprehensive comparison of different modulation indexes and modulation methods. (a) Traditional modulation and $m = 1$. (b) Proposed modulation and $m = 1$. (c) Traditional modulation and $m = 0.8$. (d) Proposed modulation and $m = 0.8$.

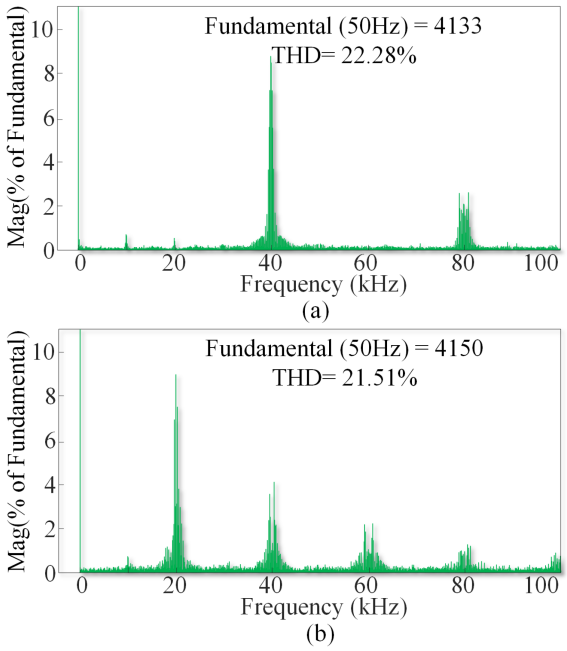

Fig. 11. FFT analysis of line voltages. (a) Traditional modulation. (b) Proposed modulation.

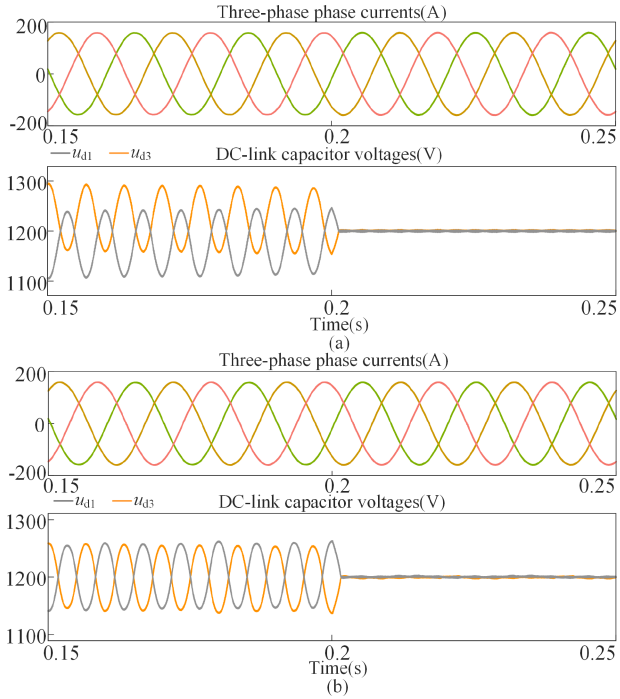

Fig. 12. Three-phase current and capacitor voltage ripples at a high power factor and high modulation index. (a) Traditional modulation. (b) Proposed modulation.

low-frequency voltage ripples changes from 26 to 30 V, which is less affected by three-phase unbalanced loads in the proposed modulation method.

Fig. 15 shows the output performance with 1.5 kHz in the simulation. As the modulation index increases from 0.2 to 1, the voltage ripples become more noticeable. For the proposed

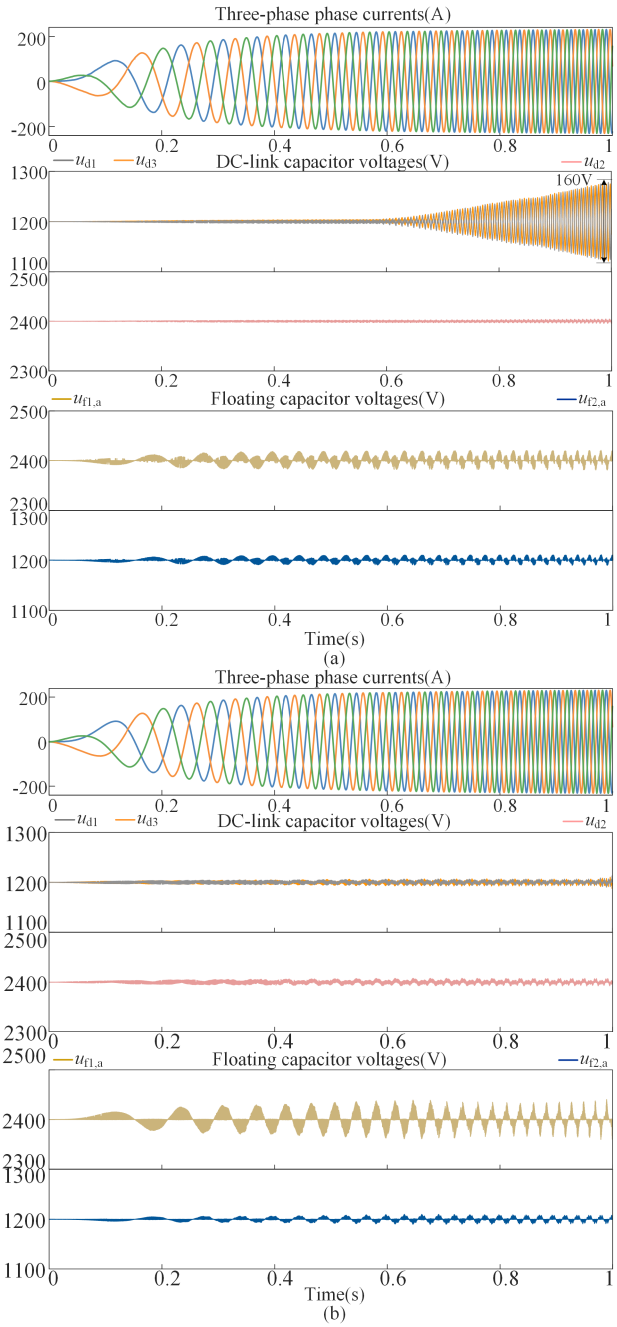

Fig. 13. Voltage ripples of capacitors under VVVF control. (a) Traditional modulation. (b) Proposed modulation.

method, all capacitors are maintained at the reference voltage value well, while the voltage of dc-link capacitors cannot be kept balanced and has a large low-frequency harmonic component under the traditional modulation. Therefore, the proposed method presents a stronger voltage balance of dc-link capacitors.

In order to verify the capacitors voltage independent and decoupling control of the proposed modulation method, Fig. 16 shows the simulation results when the voltage reference values of the capacitors are suddenly modified. In Fig. 16(a), the reference value of the voltage difference between the dc-link upper and lower capacitors is suddenly modified to 400 V at $t = 0.2$ s,

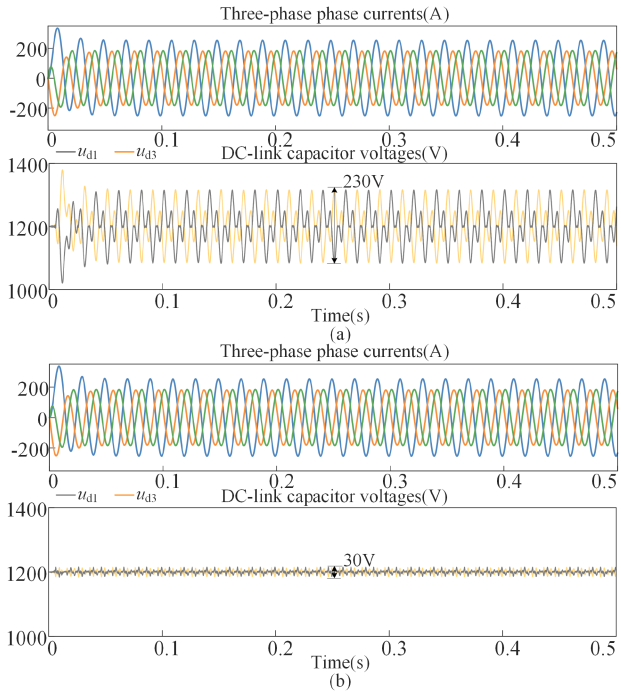

Fig. 14. Unbalanced loads. (a) Traditional modulation. (b) Proposed modulation.

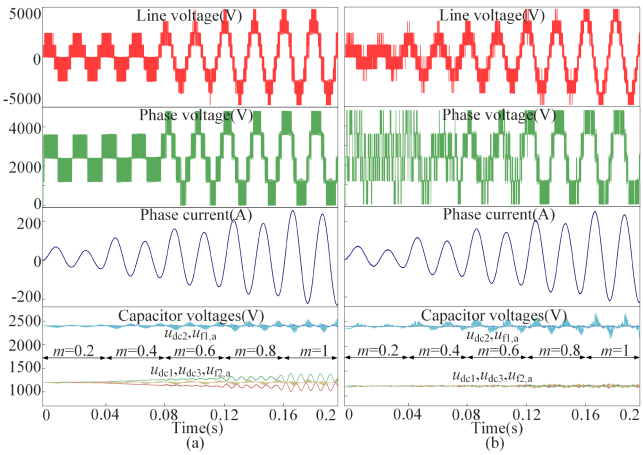

Fig. 15. Output performance with 1.5 kHz. (a) Traditional modulation. (b) Proposed modulation.

and this is modified back to zero at $t = 0.3$ s. Under the action of the capacitor voltage balancing controller, the voltages of DC-link upper and lower capacitors rise by 200 and -200 V, respectively, and the voltage difference is 400 V, after $t = 0.3$ s, the voltages of the two capacitors are balanced once again. During this process, the voltage of dc-link center capacitor is kept in balance consistently. Similarly, in Fig. 16(b), the voltage reference value of dc-link center capacitor is modified to 2100 V at $t = 0.2$ s and reset to 2500 V at $t = 0.3$ s, voltage of dc-link center capacitor follows the reference value dropping 400 V, and then rising 400 V to return to its normal voltage value. Accordingly, the voltages of upper and lower capacitors first rise by 200 V and then fall by 200 V, and their voltages are kept

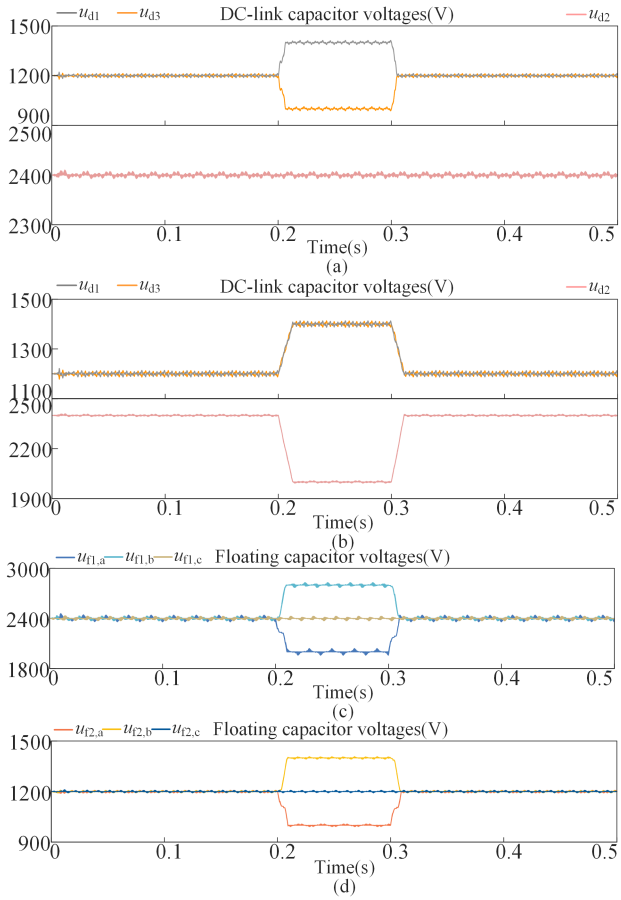

Fig. 16. Independent control of different capacitor voltages. (a) u_{d1} and u_{d2}. (b) u_{d2}. (c) $u_{\mathrm{f1},x}$. (d) $u_{\mathrm{f2},x}$.

synchronized. Fig. 16(c) and (d) demonstrates the independent control of the voltages of the floating capacitors. In Fig. 16(c), the voltage reference values of $C_{\mathrm{f1,a}}$ and $C_{\mathrm{f1,c}}$ are modified to 2000 and 2800 V, respectively, in a similar way, the voltage reference values of $C_{\mathrm{f2,a}}$ and $C_{\mathrm{f2,c}}$ are modified to 1000 and 1400 V in Fig. 16(d), respectively, all floating capacitor voltages vary according to the voltage reference values. Therefore, all capacitor voltages can be controlled independently.

V. Experimental Results

A. Experimental Verification

A low-power five-level HC inverter prototype is built to verify the proposed modulation and capacitor voltage control methods in the low power factor experimental environment, which is shown in Fig. 17. The experimental circuit parameters are listed in Table IV, the capacitor capacitances, carriers frequency, fundamental frequency, and *R–L* load are all consistent with the simulation, the dc-link voltage is changed to 100 V. Thus, the five-level HC inverter output performance and capacitor voltage ripple characteristics are similar to simulation. In the experiment, Plexim's RT-BOX, which embeds FPGA into the CUP core is used as the real-time controller. It measures the

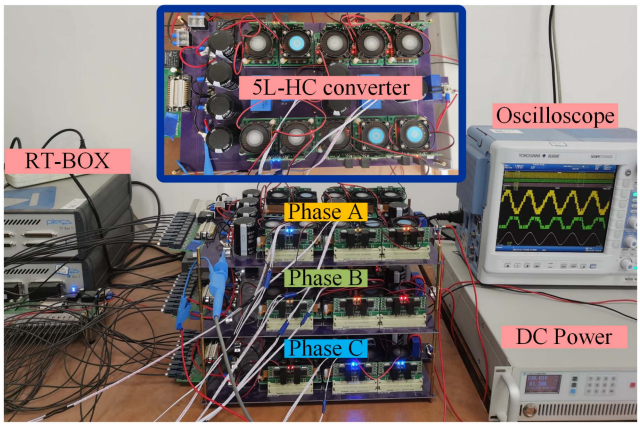

Fig. 17. Experimental prototype of the five-level HC inverter.

TABLE IV
CIRCUIT PARAMETERS USED IN THE EXPERIMENT

Parameters	Value
Rated volume	1 MVA
DC-link voltage	$U_{\rm dc}$ = 4.8 kV
DC-link capacitors	$C_{\rm d1}$ = $C_{\rm d3}$ = 560 μF, $C_{\rm d2}$ = 280 μF
Floating capacitors	$C_{{\rm f}1,x}$ = 560 μF, $C_{{\rm f}2,x}$ = 280 μF
Carriers frequency	$f_{\rm c}$ = 10 kHz
Fundamental frequency	f = 50 Hz
R-*L* load	R = 2.5 Ω, L = 32 mH

voltage and current signals in the five-level HC inverter prototype and generates the gate signals of the power switches through the capacitor voltage balancing control algorithm and the proposed modulation method. Then, the gate signals are transmitted back to the five-level HC inverter via optical fibers. Finally, the gate driver IXDI614YI drives the power switches CI60N120SM according to the gate signals.

Fig. 18 shows the comprehensive comparison of different modulation indexes and modulation methods in the experiment. Similar to the results of the simulation, the voltage ripples of the floating capacitors and the dc-link center capacitor are similar under the two different modulations. When the traditional method is implemented and $m = 1$, the low-frequency voltage ripples difference between the dc-link upper and lower capacitors is 4.5 V, while the difference between the low-frequency voltage ripples of the proposed modulation is a much smaller of 1.5 V. When $m = 0.8$, the range of ZSV becomes wider and the low-frequency voltage ripples of the dc-link upper and lower capacitor are further reduced. The low-frequency voltage ripples of the traditional modulation is 2.2 V, while the proposed modulation is 1 V, which is relatively similar to the voltage ripple caused by the carriers frequency. Therefore, the proposed modulation method has better low-frequency voltage ripple suppression of the upper and lower dc-link capacitors, the low-frequency voltage fluctuation amplitudes reduced from 9% to 3% at $m = 1$, while the low-frequency voltage fluctuation amplitudes reduced from 4.5% to 2% at $m = 0.8$. It can be derived from Figs. 3 and 5 that the phase voltages of the two different modulation methods are not the same. In addition, the optimal ZSV calculated by the two modulation methods are different, and thus, their reference modulation voltages are also different. Therefore, there is a difference in their phase voltage. Further, although the ZSV does not affect line voltage, but affects the pulse distribution of phase voltage, the line voltage can be expressed as the difference between the phase voltages, so the difference in phase voltage is noticeable.

A comparison of the line voltage fast Fourier transform (FFT) analysis is given in Fig. 19. Both methods have a carrier frequency of 10 kHz and $m = 1$, for the traditional modulation, the first band of the harmonic is 40 kHz, while the first harmonic band of the proposed method is 20 kHz. The first harmonic band of the traditional method is twice that of the proposed method, however, the total harmonic distortion (THD) of the traditional method is higher as 26.02%, while the proposed method is lower as 25.17%. In order to make the first band of the harmonic appear at the same frequency, the carrier frequency of the proposed method is increased to 20 kHz so that the first band of the harmonic is the same as in the traditional method. As shown in Fig. 19(c), the THD of proposed method is further reduced to 24.64%, which is more preferable to traditional method.

Fig. 20 shows the output performance at a high power factor of 0.98 and $m = 1$ in the experiment, the parameters of the three-phase load are $L = 10$ mH, $R = 15\Omega$. Both the conventional modulation method and the proposed modulation method demonstrate excellent output performance, the low-frequency voltage ripples of the dc-link upper and lower capacitors are suppressed completely.

Fig. 21 shows the voltage ripples of capacitors under VVVF control in the experimental setup. Within one second, the modulation index increases from 0 to 1 linearly, while the fundamental frequency increases from 0 to 50 Hz. During this period, capacitor voltages are maintained at steady-state values, the capacitor voltage ripples are similar for both modulations, except for the dc-link upper and lower capacitors. For traditional modulation, the low-frequency voltage ripples of the upper and lower dc-link capacitors are more noticeable with the increase of time. In comparison, the low-frequency voltage ripples of the proposed method are suppressed significantly.

Three-phase unbalanced loads experiment as shown in Fig. 22. The c-phase resistance is changed from 2.5Ω to 11Ω, which is the same as the simulation, the three-phase current has a significant imbalance. For traditional modulation, the low-frequency voltage ripple difference of upper and lower dc-link capacitors is further extended to 5.5 V. By contrast, the advantages of the proposed modulation method are more obvious with the low-frequency voltage ripple difference of 2 V.

Fig. 23 shows independent control of different capacitor voltages in the experimental setup. In Fig. 23(a), the reference value of the voltage difference between the dc-link upper and lower capacitors is suddenly changed to 10 V and returns to zero after 0.5 s. With the implementation of the ZSV method, the voltages of the dc-link upper and lower capacitors reach steady-state values of 20 and 30 V, respectively, and return to 25 V after 0.5 s. The dc-link center capacitor voltage is not affected by the ZSV and remains balanced. In Fig. 23(b), the voltage reference

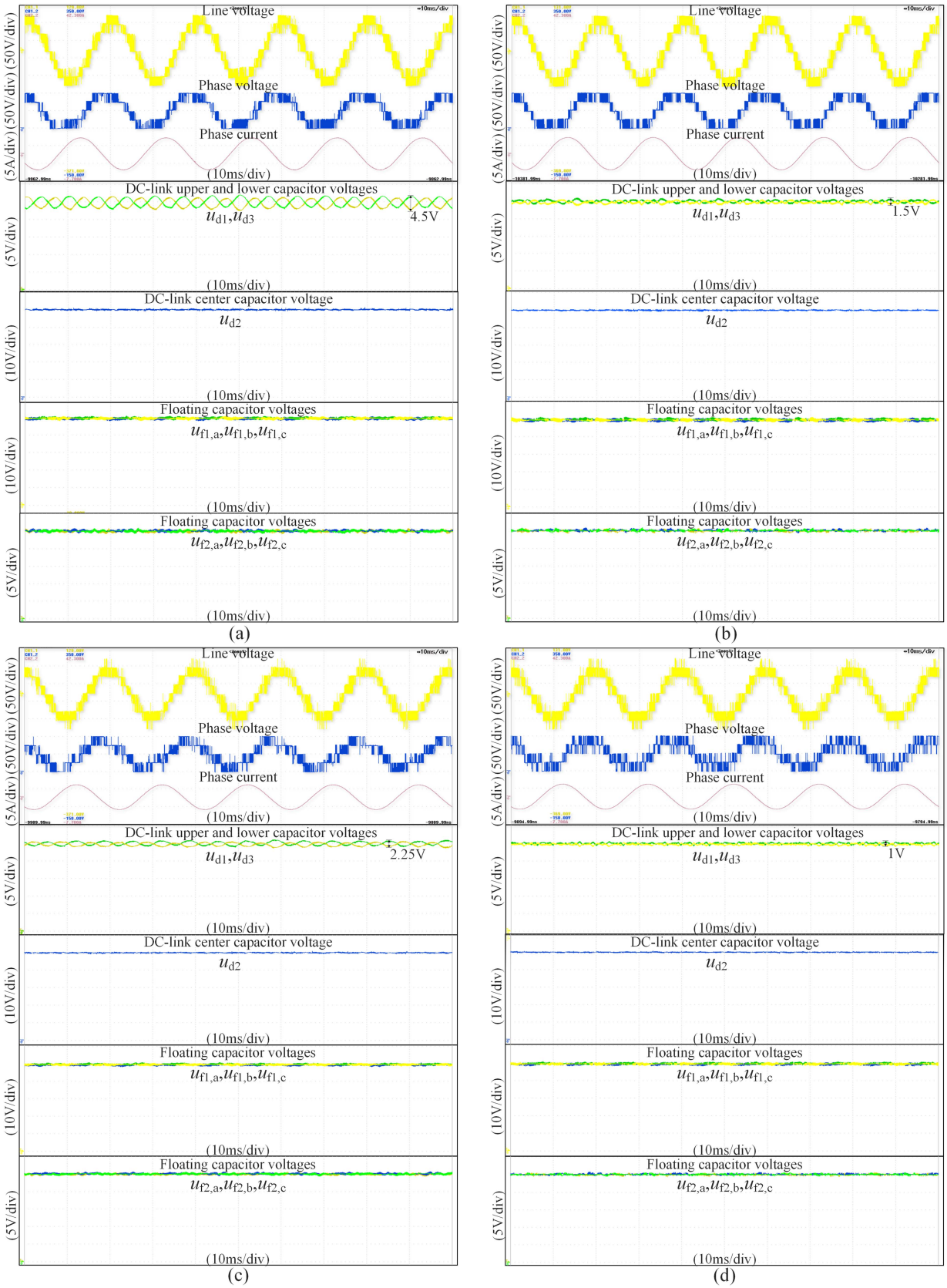

Fig. 18. Comprehensive comparison of different modulation indexes and modulation methods in the experiment. (a) Traditional modulation and $m = 1$. (b) Proposed modulation and $m = 1$. (c) Traditional modulation and $m = 0.8$. (d) Proposed modulation and $m = 0.8$.

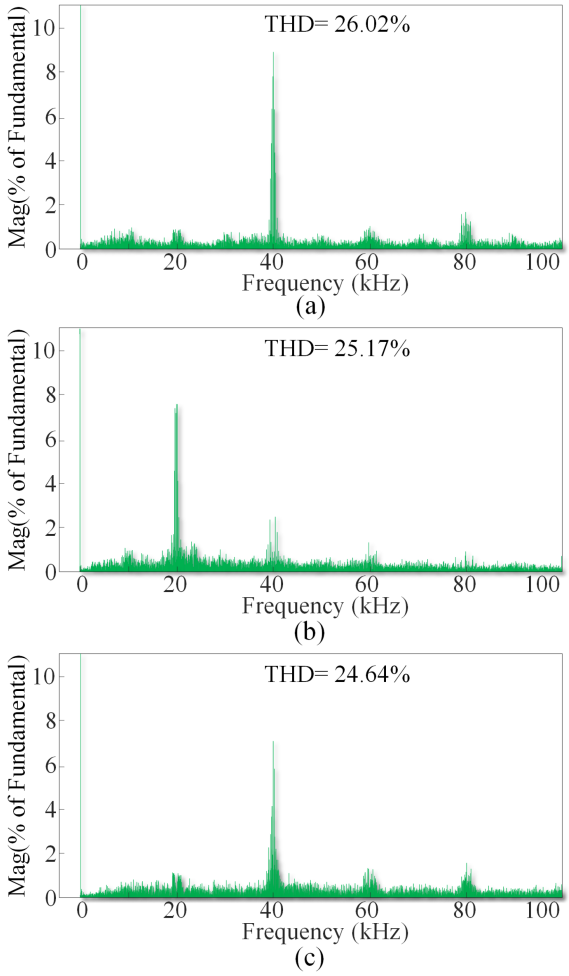

Fig. 19. FFT analysis of line voltages in the Experiment. (a) Traditional modulation with 10 kHz. (b) Proposed modulation with 10 kHz. (c) Proposed modulation with 20 kHz.

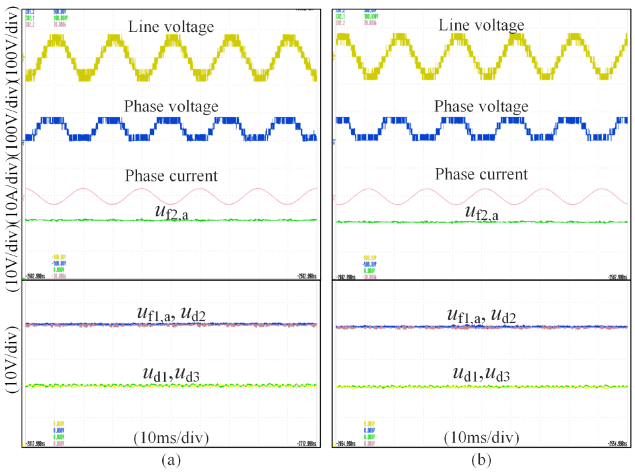

Fig. 20. Output performance at a high power factor of 0.98 in the experiment in the experiment. (a) Traditional modulation. (b) Proposed modulation.

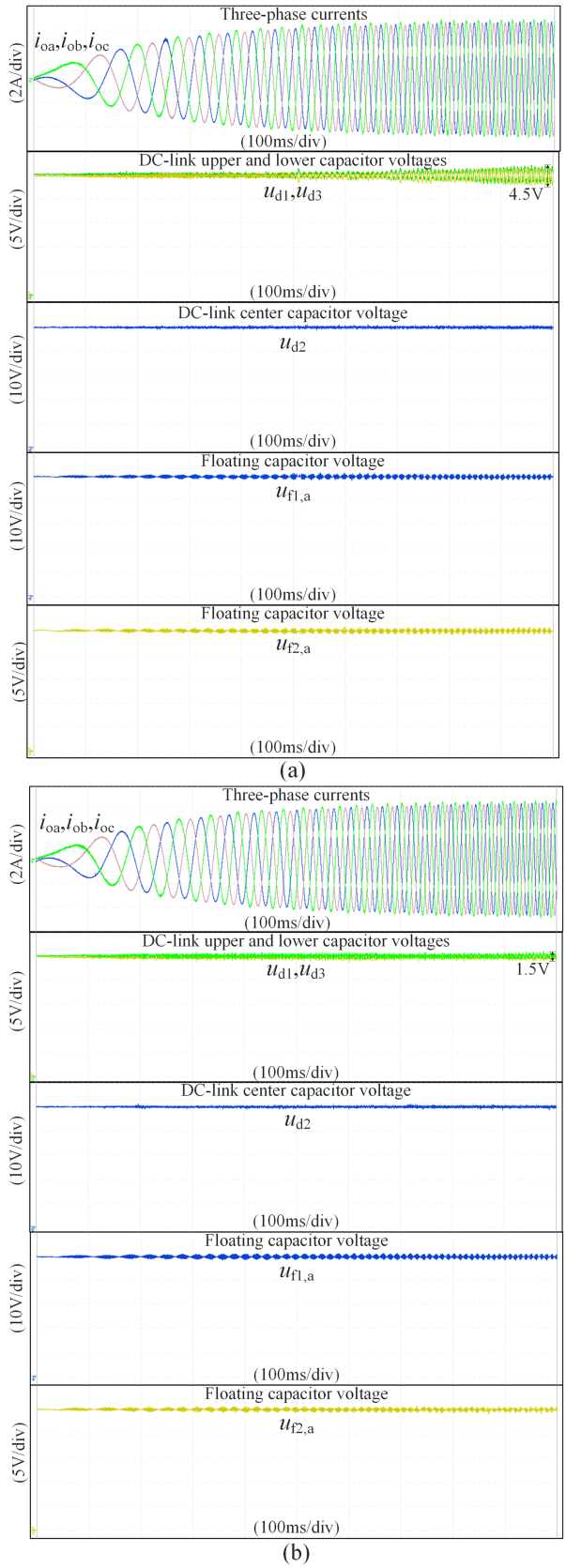

Fig. 21. Voltage ripples of capacitors under VVVF control in the experiment. (a) Traditional modulation. (b) Proposed modulation.

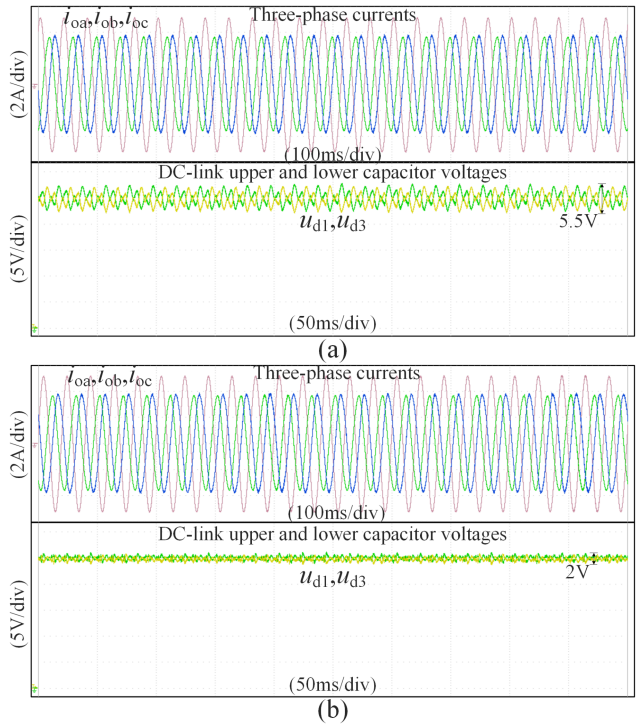

Fig. 22. Unbalanced loads in the experiment. (a) Traditional modulation. (b) Proposed modulation.

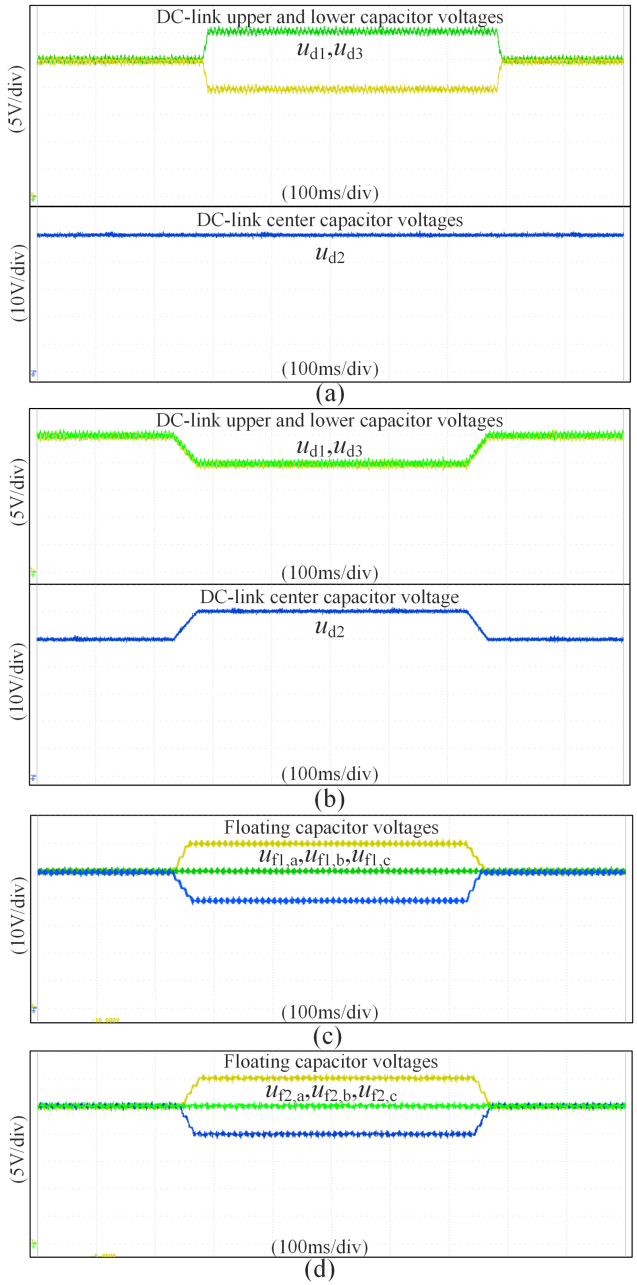

Fig. 23. Independent control of different capacitor voltages in the experiment. (a) u_{d1} and u_{d2}. (b) u_{d2}. (c) $u_{\mathrm{f1},x}$. (d) $u_{\mathrm{f2},x}$.

value of the dc-link center capacitor is suddenly modified to 60 V, then it modifies to the normal value after 0.5 s. The dc-link center capacitor voltage is controlled to rise to 60 V first and then return to 50 V, which corresponds to the voltage reference value. In this process, the voltages of dc-link upper and lower capacitors are kept consistent, and the ZSV method is performed appropriately. Fig. 23(c) shows independent control of $C_{\mathrm{f1,a}}$, $C_{\mathrm{f1,b}}$, and $C_{\mathrm{f1,c}}$, the voltage reference values of $C_{\mathrm{f1,a}}$ and $C_{\mathrm{f1,c}}$ are modified to 60 and 40 V, respectively, which are modified to the normal voltage reference value of 50 V after 0.5 s. The voltages of $C_{\mathrm{f1,a}}$ and $C_{\mathrm{f1,c}}$ go up and down by 10 V, respectively, and balance again to 50 V after 0.5 s. Similarly, the voltage reference values of $C_{\mathrm{f2,a}}$ and $C_{\mathrm{f2,c}}$ are changed to 30 and 20 V, respectively, and then revise to 25 V. The voltages of $C_{\mathrm{f2,a}}$, $C_{\mathrm{f2,b}}$, and $C_{\mathrm{f2,c}}$ always follows the voltage reference values. Thus, all capacitor voltages can be controlled independently.

Fig. 24 shows the start-up process of the five-level HC inverter at the experimental setup. The dc-link voltage is supplied at the initiation of the start-up, the capacitors share the dc-link voltage based on the capacitance value and then remain stable at the voltage reference values, respectively. For floating capacitors, $u_{\mathrm{f1,a}}$ and $u_{\mathrm{f2,a}}$ charge from 0 to the voltage reference values and reach the steady states simultaneously. During the start-up process, the line voltage shows a distinct stepped wave gradually and the phase current is highly sinusoidal.

Fig. 25 shows the different modulation indexes with 10 kHz in the experimental setup. The modulation indexes vary from 1 to 0.2, the line voltage level and phase current decreases with modulation indexes, while the amplitude of common-mode voltage keeps rising. At high modulation indexes, the common mode voltage of the proposed modulation method is larger than that of the traditional method, and relatively, at low modulation indexes, the common mode voltage performance of the proposed method is better. For capacitor voltage ripples, the proposed method has small voltage ripples over the entire modulation index range, in contrast, the traditional method has significant low-frequency voltage ripples in dc-link capacitors at high modulation indexes, The voltage ripples are not significantly suppressed until $m = 0.4$ and below. Therefore, the proposed modulation method presents a stronger capability of low-frequency voltage suppression.

Fig. 26 shows variable modulation index with 1.5 kHz in the experiment. Both modulation methods have higher voltage

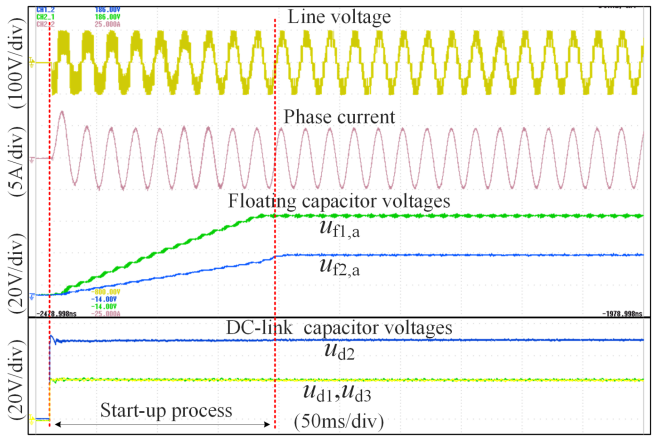

Fig. 24. Start-up process of the inverter in the experiment.

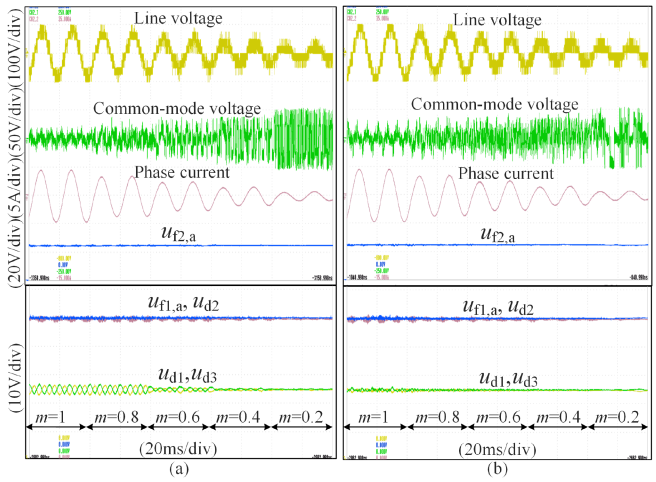

Fig. 25. Variable modulation index with 10 kHz in the experiment. (a) Traditional modulation. (b) Proposed modulation.

ripples compared to 10 kHz, and the low-frequency voltage ripples of the dc-link capacitor are more difficult to suppress due to the longer ZSV injection time interval. Nevertheless, the proposed modulation still has better low-frequency voltage ripples suppression of dc link upper and lower capacitors at a lower switching frequency and low power factor.

The output performance in the experiment with 1 kHz is shown in Fig. 27. In order to avoid the large voltage ripples skewing the measured signal at low carrier frequency, and resulting in a slight offset in the floating capacitor voltage, measured voltage signals are periodically averaged over the carrier period. Whether at high or low power factor, the proposed modulation method has excellent output performance at 1 kHz, and the capacitor voltages are well balanced, which be derived from Fig. 27(a) and (b). For traditional modulation, the capacitor voltages are maintained in balance at high power factor of 0.98. However, at a low power factor of 0.24, traditional modulation cannot achieve voltage balance of dc-link capacitors. Because, the ZSV is injected once per carrier cycle, which depends on the frequency of the carrier. When the carrier frequency is relatively high, the NP voltage deviation caused by nonideal conditions

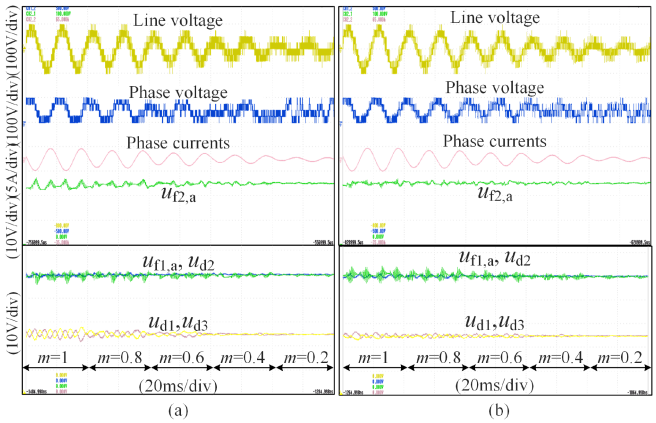

Fig. 26. Variable modulation index with 1.5 kHz in the experiment. (a) Traditional modulation. (b) Proposed modulation.

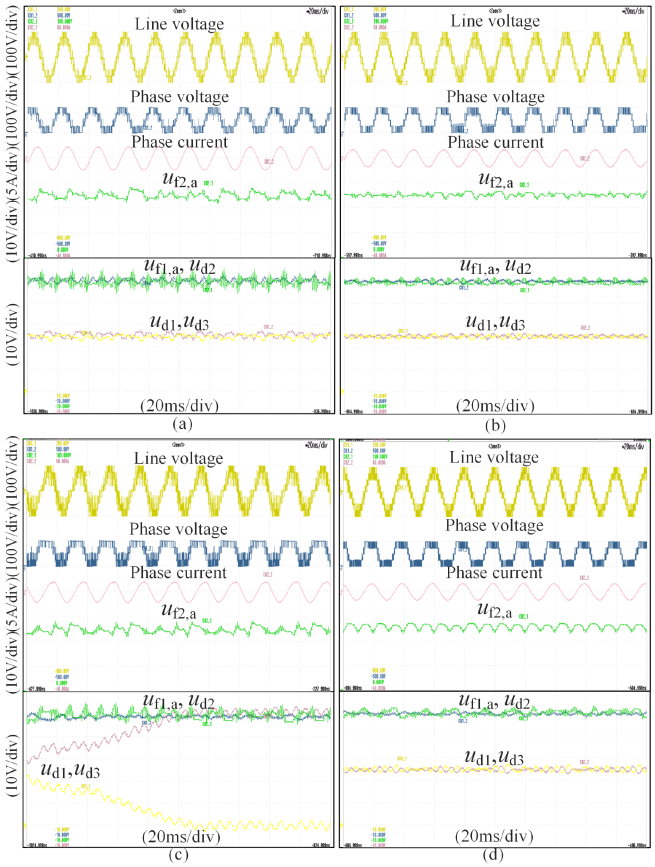

Fig. 27. Output performance with 1 kHz in the experiment. (a) Proposed modulation with a power factor of 0.24. (b) Proposed modulation with a power factor of 0.98. (c) Traditional modulation with a power factor of 0.24. (d) Traditional modulation with a power factor of 0.98.

is relatively small in a carrier period, and dc-link capacitor's voltage can be kept balanced by adjusting the NP current with ZSV. When the carrier frequency is low, the NP voltage deviation caused by nonideal conditions becomes larger within a unit carrier period, the active regulation of NP current by ZSV is not sufficient enough to eliminate the NP voltage dispersion

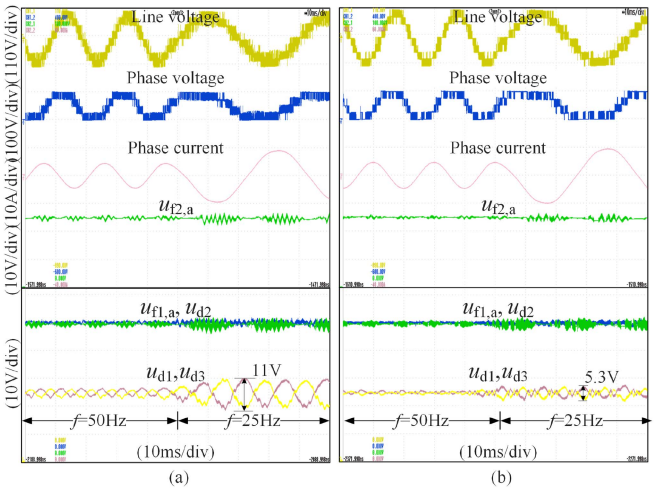

Fig. 28. Variable fundamental frequency in the experiment. (a) Traditional modulation. (b) Proposed modulation.

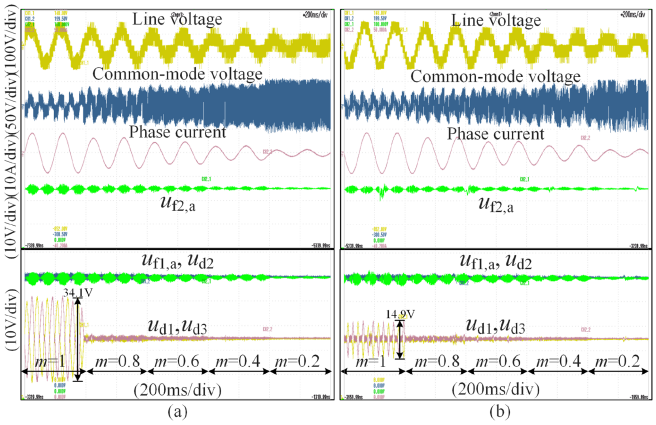

Fig. 29. Low fundamental frequency of 5 Hz in the experiment. (a) Traditional modulation. (b) Proposed modulation.

problem caused by nonideal conditions. In summary, the traditional PS-PWM provides a weak regulation of the NP current at low power factors, while the low switching frequency further reduces the frequency of the ZSV injection, which makes it impossible to suppress the voltage deviation of dc-link capacitor caused by nonideal conditions. For the proposed PS-PWM, the NP current can be bipolar regulated within a wide range, which allows a better suppression of voltage divergence due to nonideal conditions at low power factors and low carrier frequencies.

The output performance in the experiment with different fundamental frequencies is shown in Fig. 28, the fundamental frequency suddenly changed from 50 to 25 Hz, the power factor changes from 0.245 to 0.445 as the fundamental frequency is transformed, low-frequency voltage fluctuations of the dc-link capacitors depend on the fundamental frequency, which also drop by half. The low-frequency voltage fluctuations of the traditional method is about 11 V, while the proposed method is a much lower 5.3 V.

Fig. 29 provides the experimental results with a low fundamental frequency of 5 Hz, $R = 2.5\ \Omega$, $L = 152$ mH, and power factor of 0.46. The capacitor voltages are well balanced at low modulation indices for both PS-PWMs. However, at a high modulation index of 1, the difference in low-frequency voltage ripples of the dc-link capacitor is evident. For traditional modulation, the voltage ripple between the upper and lower capacitors on the dc-link is 34.1 V, and the line voltage shows significant distortion. Comparatively, the voltage ripple of the proposed method is 14.9 V, which demonstrates more competitive voltage ripple performance at low fundamental frequencies.

B. Comparison of Different Methods

The PS-PWM method is easy to implement and the switching frequency of all switches is distributed evenly, which also can maintain the natural voltage balance of floating capacitors and dc-link central capacitor under ideal condition. A simple voltage balancing method combined with PS-PWM can improve voltage balancing performance significantly. By contrast, the triangular carriers of PD-PWM feature a different phase position, which leads to inconsistent switching frequency and conduction time among the switches. Further, the auxiliary voltage balancing circuits or complex redundant switching states selection methods are employed to enhance the voltage balancing performance of the capacitors, which will increase the system cost and the switching transitions. Therefore, PS-PWM method is more advantageous for five-level HC inverter. In order to compare the performance of the proposed PS-PWM in terms of efficiency, voltage ripple, and THD comprehensively. Traditional PS-PWM [22], IPS-PWM [32], MPS-PWM with $\varphi = 0.066\pi$ (MPS-PWM1), and MPS-PWM with $\varphi = 0.266\pi$ (MPS-PWM2) [31] are carried out as comparison experiments among different switching frequencies, fundamental frequencies, and power factors.

The single-phase five-level HC inverter has four independent switches $S_{1,x}$–$S_{4,x}$, and $S_{1,x}$, $S_{5,x}$ share a common control signal. Therefore, four triangle carriers are required to correspond to each individual switch when PS-PWM is implemented. PS-PWM is a fixed switching frequency modulation method, where the carriers are shifted relative to each other and correspond to the switches, and duty cycle correction and ZSV injection are calculated only once in a carrier period. Therefore, each switch is switched once in one carrier period. Each phase of the five-level HC inverter has 10 switches, which means that the number of total switchings of the three-phase in half of the fundamental period is $15f_c/f$. For the traditional PS-PWM, as shown in Fig. 3, the four symmetrical triangular carriers are distributed evenly so that the generated pulses are not linked or overlapped completely. IPS-PWM is a collective phase shift of carriers located in different reference modulation voltage intervals, which is based on the traditional PS-PWM, and the carriers are still uniformly distributed. Therefore, the phase voltage equivalent switching frequency of traditional PS-PWM and IPS-PWM are $4f_c$. For MPS-PWM1 and MPS-PWM2, although the four carriers are not uniformly distributed, there are no pulses that overlap each other or are linked at the

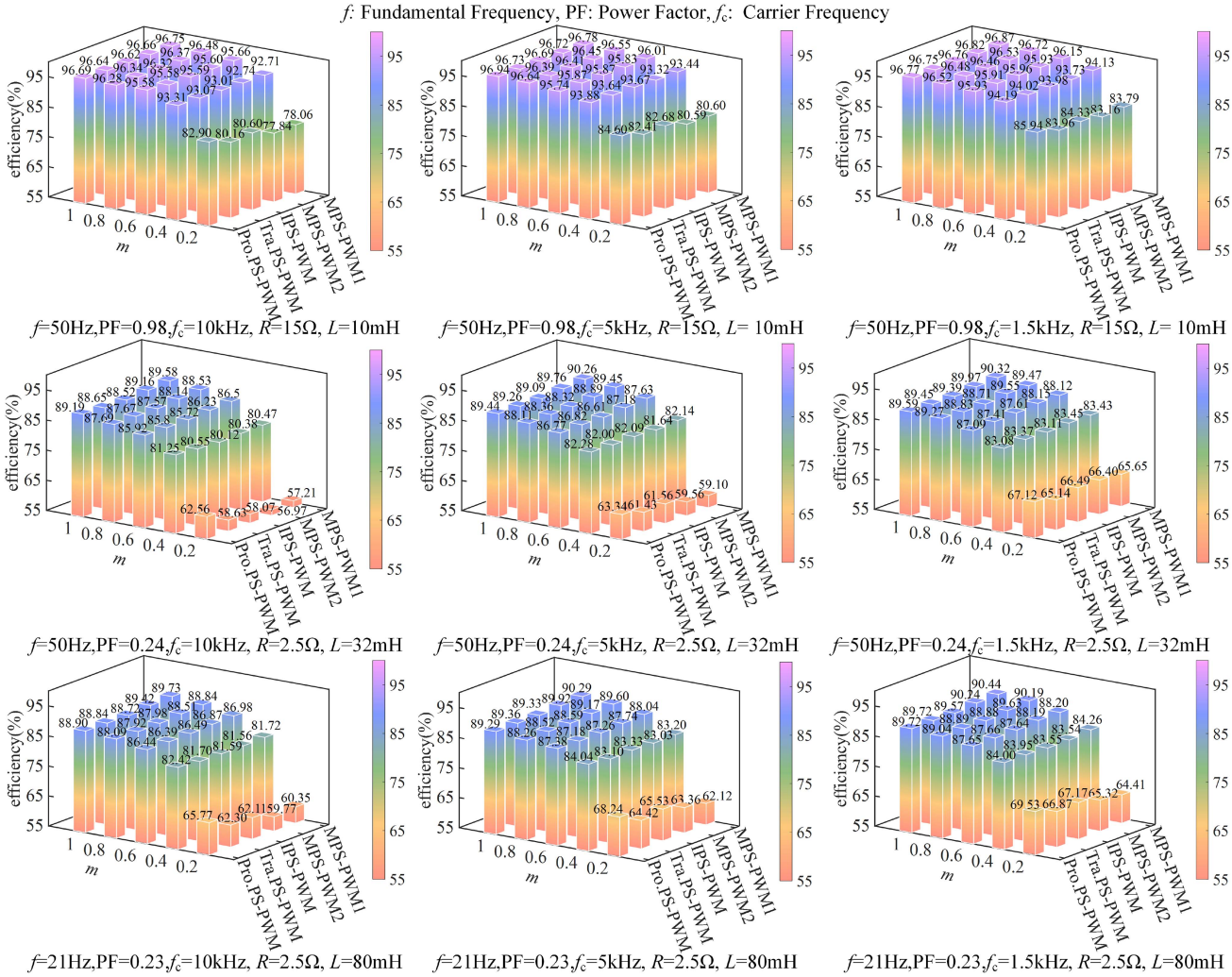

Fig. 30. Efficiencies of different methods in terms of switching frequencies, power factors and fundamental frequencies in the experiment.

first and last. Therefore, the same as traditional PS-PWM and IPS-PWM, the phase voltage equivalent switching frequency of MPS-PWM1 and MPS-PWM2 is $4f_c$. This is different in the proposed PS-PWM, as shown in Fig. 5, the carrier waves overlap each other two-by-two, and the generated pulses are connected at the beginning and end. Thus, the phase voltage equivalent switching frequency is $2f_c$, which is half of the other PS-PWM.

The efficiencies of the different methods in terms of switching frequencies, power factors, and fundamental frequencies are shown in Fig. 30 and the efficiencies are measured by PA2000mini power analyzer. Overall, the efficiencies of all PS-PWM methods increase as the switching frequency decreases, at a low power factor of 0.24, the overall efficiency is 10% to 20% lower than at a high power factor of 0.98. The efficiencies at different fundamental frequencies are relatively approximate. For a certain PS-PWM method, MPS-PWM1 and MPS-PWM2 seem to have the best efficiency at high modulation indexes, while the efficiencies are the worst at low modulation indexes. In contrast, IPS-PWM and traditional PS-PWM perform moderately well in terms of efficiency. For the proposed method, the efficiencies are not impressive at high modulation indexes, but it has an overwhelming efficiency advantage at low modulation indexes.

The line voltage THDs of the different methods in terms of switching frequencies, power factors and fundamental frequencies in the experiment are shown in Fig. 31. In general, the line voltage THDs increase as the switching frequencies decrease, but not significantly. In comparison, line voltage THDs rise dramatically as the modulation indexes become lower, and the difference is not obvious at different fundamental frequencies. IPS-PWM shows the best line voltage THDs under different experimental conditions, while MPS-PWM1 and MPS-PWM2 almost present the worst performance. IPS-PWM method tackles the problem of line voltage level overlap, which provides better THD at low modulation indices and low switching frequencies, and this case is most significant at $f=50$ Hz, PF $= 0.98$, $R = 15\Omega$, $L = 10$ mH. When $f_c = 10$ kHz and $m = 0.4$, the line voltage THD of proposed method is 68.61%, while that of IPS-PWM is 67.81%. When $f_c = 1.5$ kHz and $m = 0.4$, the line voltage THD of proposed method is 73.73%, while that of IPS-PWM is 70.70%. The THD of the proposed method increases more than

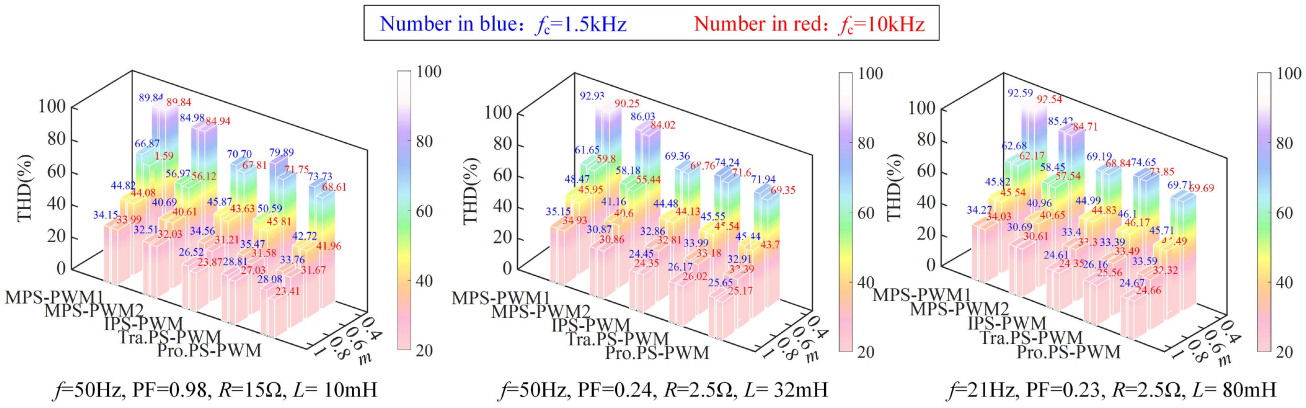

Fig. 31. Line voltage THDs of the different methods in terms of switching frequencies, power factors and fundamental frequencies in the experiment.

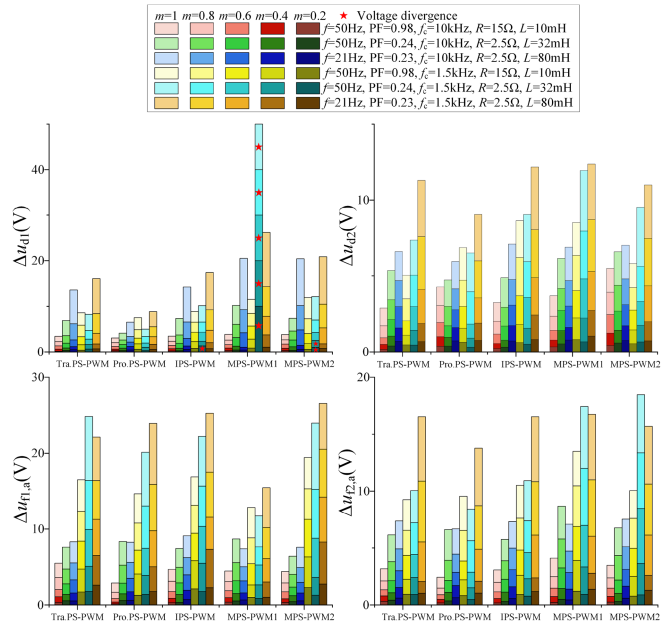

Fig. 32. Capacitor voltage ripples of the different methods in terms of switching frequencies, power factors and fundamental frequencies in the experiment.

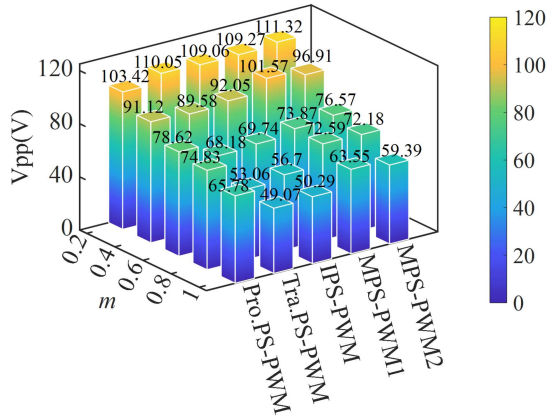

Fig. 33. Comparison of inverter common mode voltage in the experiment.

that of IPS-PWM, and the proposed method has higher THD compared to IPS-PWM at lower modulation indices and low switching frequencies. In summary, The proposed PS-PWM is inferior to the IPS-PWM, which presents a relatively competitive THD performance among all methods.

The voltage ripples of upper and central dc-link capacitors Δu_{d1}, Δu_{d2}, and the voltage ripples of floating capacitors $\Delta u_{\mathrm{f1,a}}$, $\Delta u_{\mathrm{f2,a}}$, which in terms of switching frequencies, power factors, and fundamental frequencies in the experiment are shown in Fig. 32. As a whole, the voltage ripples increase as the switching frequency decreases, all PS-PWM methods exhibit outstanding voltage balancing performance at high power factors, but there are significant differences at low power factors. For Δu_{d1}, the proposed method demonstrates the best voltage ripple performance with arbitrary power factor and fundamental frequency, while MPS-PWM1 shows significant capacitor voltage divergence at PF $=$ 0.24, f $=$ 50 Hz, f_{c} $=$ 1.5 kHz. The voltage dispersion phenomenon is also revealed in IPS-PWM and MPS-PWM2, the capacitor voltage drifts slightly, but returns to stabilization eventually. For Δu_{d2}, $\Delta u_{\mathrm{f1,a}}$, and $\Delta u_{\mathrm{f2,a}}$, there is no significant difference in voltage ripples among all methods, excluding that the MPS-PWM1 is distinctly competitive on the $\Delta u_{\mathrm{f1,a}}$. In summary, the proposed method is effective in reducing Δu_{d1}, and thus, the low-frequency voltage ripple of dc-link capacitor can be suppressed to a relatively small degree, which avoids device damage and output harmonics caused by low-frequency voltage ripple or even voltage dispersion.

Fig. 33 shows the experimental results of common-mode voltage comparison for different methods. Voltage peak-to-peak (Vpp) of the common-mode voltage is considered as a comparison with f_{c} $=$ 10 kHz, f $=$ 50 Hz and power factor of 0.24. In the range of modulation indices from 0.4 to 1, the traditional PS-PWM demonstrates the smallest common-mode voltage among all the methods. In contrast, the proposed PS-PWM increases the common-mode voltage dramatically at high modulation indices, and the competitive common-mode voltage performance can only be achieved with low modulation indices of 0.2 and 0.4.

VI. Conclusion

In this article, a novel and simple carrier-based modulation method to operate five-level HC inverter at wide power factors

with enhanced NP voltage balancing capability is proposed. Similar to the traditional methods, it achieves a natural voltage balancing of floating capacitors and the dc-link center capacitor without additional voltage balancing circuits. On the basis of this, voltage ripple models are derived to enable the voltage independent control of all capacitors. Experiments and simulations show that the proposed modulation can avoid the potential damage and impact of capacitor low-frequency voltage disturbance on the device and output waveform, which improves the ability of the five-level HC inverter to operate at low power factor and low fundamental frequency applications. In comparison with the traditional methods, the proposed method has the following pros and cons:

1) The proposed PS-PWM can significantly improve the NP voltage balancing capability over a wide power factor range. This avoids the problem of insufficient NP current regulation, resulting in low-frequency fluctuations or voltage dispersion in dc-link capacitors compared to other methods, and this advantage is more obvious at low power factors and low carrier frequencies.
2) MPS-PWM1 and MPS-PWM2 demonstrate best efficiency at high modulation indexes, while the efficiencies are the worst at low modulation indexes. Comparatively, the efficiencies of proposed PS-PWM are not impressive at high modulation indexes, but it has an overwhelming efficiency advantage at low modulation indexes.
3) Although the proposed method greatly increases the common-mode voltage at high modulation index, it has the smallest common-mode voltage at low modulation index, which also demonstrates its competitive ability relative to traditional PS-PWM.
4) IPS-PWM method tackles the problem of line voltage level overlap, and thus, it provides the best THD performance among the five different methods. In particular at lower modulation indices and low switching frequencies, the line voltage THD of IPS-PWM grows at a lower rate than that of the proposed method. On the whole, the proposed PS-PWM is inferior to the IPS-PWM, but it is better than other methods.

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