Letters

A Hybrid Current Reference Control Method for PFC Converter in Server Power Supply

Jae-Sang Kim, *Student Member, IEEE*, Taewoo Kim, *Student Member, IEEE*, Juhyun Bae, *Student Member, IEEE*, Jung-Kyu Han, *Member, IEEE*, and Gun-Woo Moon, *Member, IEEE*

***Abstract*—Server power supply has to maintain output power even under abnormal input voltage conditions for stable operation of the server. Input-voltage-based current reference control has been widely used for power factor correction converter in server power supply because it can instantly generate a current reference and maintain a stable output. However, because harmonics and noise in the input voltage directly influence the current reference, the input current total harmonic distortion (THD) increases. On the other hand, phase-locked loop (PLL) based control can achieve lower current THD due to its excellent noise and harmonic filtering capabilities, but it cannot respond to sudden changes in the input voltage. In this letter, a hybrid current reference control method is proposed to achieve stable operation of the server power supply. The proposed method ensures continuous operation under abnormal input voltages by utilizing input-voltage-based control. Therefore, in normal input condition, the PLL bandwidth design can be alleviated to achieve a lower current THD. To determine the effectiveness of the proposed control method, steady-state operation and abnormal input condition operation were confirmed through a 47–64 Hz/90–264 V_{rms} 3-kW prototype converter.**

***Index Terms*—Digital control, server power supply, totem-pole bridgeless power factor correction converter.**

I. Introduction

THE implementation of international harmonic regulations, such as IEC61000-3-2, aims to prevent the degradation of power quality caused by input current harmonics [1]. In server systems, redundant power supply units are necessary to ensure continuous server operation in case of power supply failure. As a result, numerous front-end power supply units operate simultaneously, making it important to maintain high input current quality to reduce reactive power and interference.

Manuscript received 29 April 2023; revised 7 August 2023 and 7 September 2023; accepted 1 October 2023. Date of publication 10 October 2023; date of current version 6 December 2023. This work was supported by the National Research Foundation of Korea grant funded by the Korea government (MSIT) (2021R1A5A1031868). *(Corresponding author: Gun-Woo Moon.)*

Jae-Sang Kim, Taewoo Kim, Juhyun Bae, and Gun-Woo Moon are with the Department of Electrical Engineering, Korea Advanced Institute of Science and Technology, Daejeon 34141, South Korea (e-mail: jaesangkim@kaist.ac.kr; fptmvj@kaist.ac.kr; wngus7158@kaist.ac.kr; gwmoon@kaist.ac.kr).

Jung-Kyu Han is with the Department of Electronic Engineering, Hanbat National University, Daejeon 34158, South Korea (e-mail: jkhan@hanbat.ac.kr).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3323555.

Digital Object Identifier 10.1109/TPEL.2023.3323555

Active power factor correction (PFC) converters are widely adopted to comply with harmonic regulations, and recently, digital-signal-processor-based totem-pole bridgeless PFC converters have gained attention in the industry for achieving high efficiency [2], [3]. However, the bandwidth (BW) of digital current controllers is lower than that of analog controllers due to limitations in sampling frequency and calculation delay, resulting in increased total harmonic distortion (THD) of the input current [4].

The server power supply has to maintain output even under harsh input voltage conditions, such as voltage sag, distortion, phase jump, and frequency jump. Input-voltage-based current reference control generates a current reference identical to the sensed input voltage waveform. Therefore, a continuous input current reference can be formed even during sudden input voltage changes [5]. However, in cases where noise and harmonics are present in the input voltage, the input-voltage-based method can degrade the quality of the input current.

The phase-locked loop (PLL) based control method is a widely adopted control method in grid-connected inverters and bidirectional applications [6], [7], [8], [9], [10]. By forming the current reference through the filtered phase information, the impact of the noise and harmonic can be significantly reduced. Therefore, stable input current quality can be achieved. However, if the BW of the PLL is designed to be high for fast phase tracking, it can lead to grid instability due to low input impedance in the low-frequency domain [9]. Thus, there are limitations in applying the PLL-based control to a server power supply that requires immediate recovery and continuous output even under abnormal input voltage conditions [10].

In PFC converters, when employing a synchronous rectifier in the unfolder leg to enhance efficiency, a current spike may arise if the input voltage phase is sensed in the opposite direction. Moreover, current spike can make the converter operation unstable. Therefore, a dead-zone, also known as blanking time, is necessary to stop all switches around the zero-crossing for stable PFC converter operation [11]. Fig. 1 illustrates the determination of dead-zones according to the control method. As seen in Fig. 1(a), the input-voltage-based method defines the dead-zone based on a fixed threshold voltage. As a result, the dead-zone varies depending on the magnitude of the input voltage. This leads to an excessive extension of the dead-zone under low-line

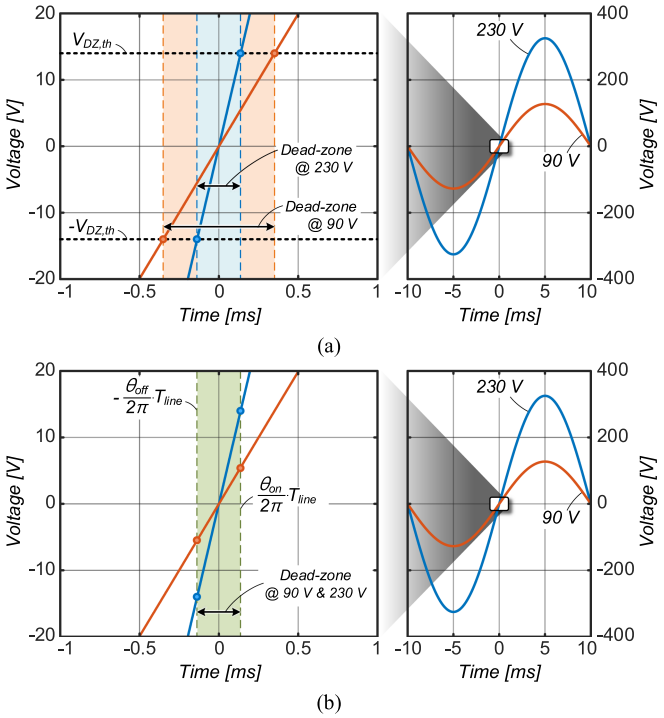

Fig. 1. Illustration of dead-zone determination according to control method at 90 V_{rms} and 230 V_{rms}. (a) Input-voltage-based control method using dead-zone threshold voltage $V_{DZ,th}$, and (b) PLL-based control method using dead-zone ON/OFF phase θ_{on}/θ_{off}.

conditions and results in a high current THD. Furthermore, when using a digital controller, which is more sensitive to noise compared to an analog controller, a higher dead-zone threshold voltage is set for clear phase distinction. On the other hand, the PLL-based dead-zone setting is depicted in Fig. 1(b). The phase of the input voltage can be accurately obtained through the PLL. In PLL-based control, the dead-zone is determined based on the phase, allowing for a consistent dead-zone width regardless of input voltage conditions.

This letter proposes a hybrid control method that uses both input-voltage-based and PLL-based control to achieve stable operation of a server power supply. The proposed method achieves low current THD through PLL-based control during steady-state operation, and it can respond immediately through input-voltage-based control when abnormal input occurs. Therefore, the PLL can be designed with a low BW, which can significantly increase the input impedance of the PFC converter, thereby enhancing grid stability. This letter is organized as follows. In Section II, the concept of the proposed control method will be explained. Section III shows experimental results of a 3 - kW totem-pole bridgeless PFC converter under the steady-state conditions and abnormal input conditions. Finally, Section IV concludes this letter.

II. Proposed Hybrid Control Method

A. Concept of Proposed Hybrid Control Method

The key concept of the proposed hybrid current reference control method is to select between input-voltage-based and PLL-based references depending on the input voltage conditions. Fig. 2 shows the totem-pole bridgeless PFC converter and control block diagram of the proposed control method. As depicted in Fig. 2(a), the proposed method is implemented based on the dual-loop control of the conventional PFC converter. In steady state, the phase of the input can be obtained through the second-order generalized integrator-based PLL (SOGI-PLL), as shown in Fig. 2(b), which utilizes the current reference and low-frequency switch control. In contrast, under abnormal input conditions, the input voltage is divided by the peak value of the input voltage to obtain a phase of input voltage.

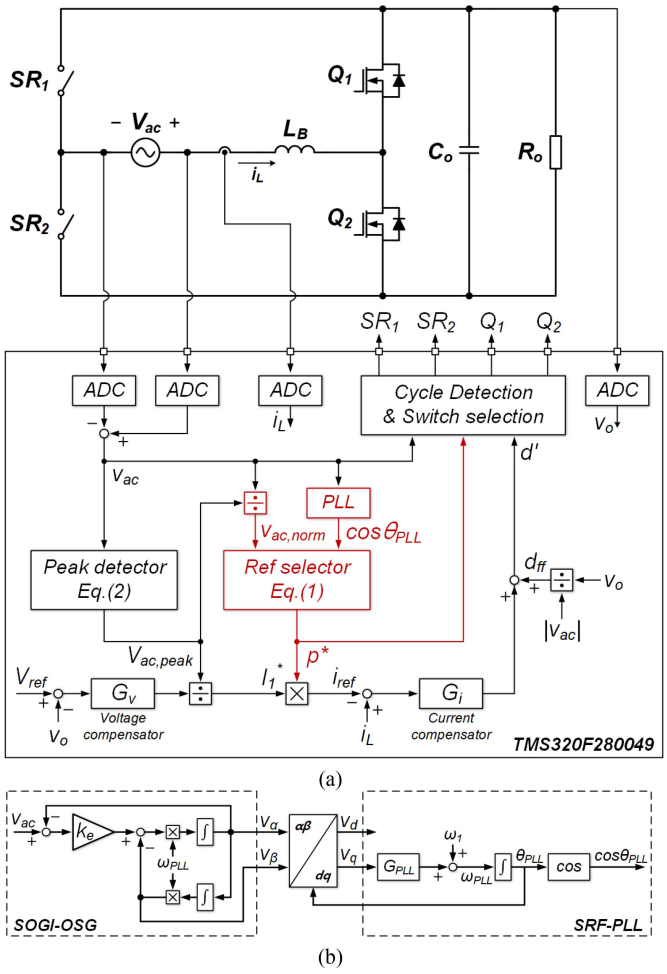

Fig. 2. Structure of totem-pole bridgeless PFC converter. (a) Control block diagram of the proposed hybrid current refence control method. (b) Block diagram of SOGI-PLL.

Fig. 3 shows the operating concept waveforms of the proposed method. Under normal input condition, the proposed controller controls the current reference and dead-zone based on the PLL. Therefore, the PFC converter can achieve low input current THD using a narrow dead-zone and a current reference in which harmonics and noise have been rejected. When a sudden abnormal input voltage occurs at t_0, the controller switches to the input-voltage-based controller, which can operate immediately regardless of the phase. Thus, it can ensure a continuous PFC operation. While the converter operates as the input voltage controller and the PLL starts to accurately track the phase, the

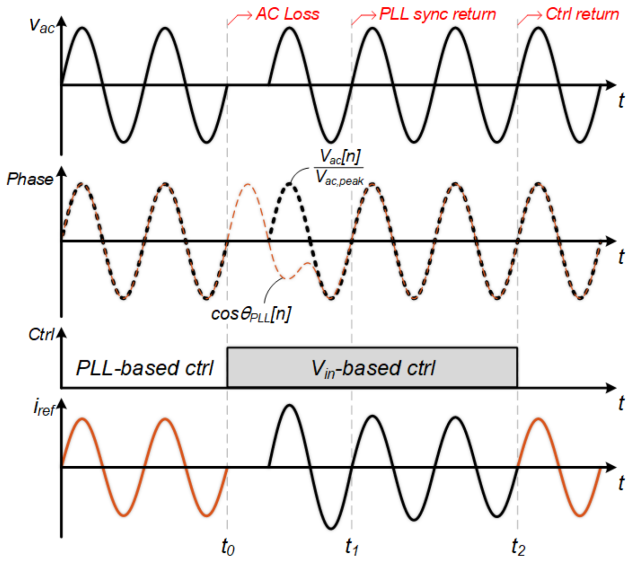

Fig. 3. Control concept waveform of the proposed hybrid current reference control method when an abnormal input voltage condition occurs at t_0.

proposed controller switches back to PLL-based control after several line cycles to prevent malfunction.

B. Criterion for Abnormal Input Voltage Detection

The proposed control method determines the state of the input based on whether the PLL is synchronized with the normalized input voltage, and the normal input condition can be expressed by the following equation:

$$\left| \frac{v_{\text{ac}}[n]}{V_{\text{ac,peak}}} - \cos\theta_{\text{PLL}}[n] \right| < \frac{\Delta V_{\text{sync}}}{V_{\text{ac,peak}}} \tag{1}$$

where v_{ac} is an input voltage, $V_{\text{ac,peak}}$ is the peak of input voltage at fundamental frequency, θ_{PLL} is the phase from PLL, and ΔV_{sync} is a threshold voltage.

Once stable synchronization is confirmed over several line cycles, a PLL-based control that can focus on the input current quality is selected as the current reference. On the other hands, if desynchronization occurs even once, it is considered an abnormal input condition, and output voltage is maintained through input-voltage-based control.

The PLL operates based on the fundamental frequency of the input voltage. Therefore, $V_{\text{ac,peak}}$ must detect the peak of fundamental frequency to accurately identify abnormal input voltages, using (1), even in the presence of harmonic distortions in the input voltage. To minimize distortion caused by harmonics, $V_{\text{ac,peak}}$ is detected using the following equation:

$$V_{\text{ac,peak}} = \frac{\pi}{2} \langle |v_{\text{ac}}| \rangle \tag{2}$$

where $\langle \cdot \rangle$ represents the average operator. The average can be implemented through the low-pass filter (LPF), designed with a BW of 1 Hz. This design allows for avoiding interference with the output voltage controller, which operates at 10 Hz.

Moreover, when the input voltage contains harmonics, the LPF can effectively attenuate their effects. If the harmonic component is significantly smaller than the fundamental, the error can be determined by the following equation:

$$e_{\text{ac,peak}} \leq \sum_{k=3}^{\text{odd}} \frac{V_{\text{ac,peak},k}}{k} \tag{3}$$

where $e_{\text{ac,peak}}$ is the error in the peak voltage of the fundamental frequency, and $V_{\text{ac,peak},k}$ is the peak voltage of the kth harmonic. As a result, a lower error can be achieved compared to the simple peak value storing method.

Under input-voltage-based control, slow peak voltage detection can lead to significant fluctuations in the current reference during abrupt input voltage changes, and it causes overcharging or discharging of the link capacitor. Therefore, a nonlinear gain control is used, which increases the gain of the voltage controller nonlinearly according to output voltage error [12]. As a result, due to the instantaneous voltage controller compensation, the output voltage can be maintained stably.

ΔV_{sync} should be set to a greater value than the lowest condition of the dead-zone threshold voltage. The maximum value of ΔV_{sync} can be obtained through the following equation:

$$\Delta V_{\text{sync}} > \sqrt{2} \cdot V_{\text{ac,min}} \cdot \cos\theta_{\text{off}} \tag{4}$$

where $V_{\text{ac,min}}$ is the lowest input rms value, and θ_{off} is the phase angle entering the dead-zone. In addition, for uninterruptable power supply of data center, the output ensures a voltage THD less than 3% under a resistive load. Therefore, ΔV_{sync} is set to 12 V, which is 3% of the maximum input voltage peak, and is greater than 5.1 V, as (4).

C. Input Impedance According to Current Reference Control

The PLL-based control is implemented using SOGI-PLL, which is widely used due to harmonic rejection performance and simple implementation. Fig. 2(b) shows the control diagram of the SOGI-PLL. In the design of the SOGI-OSG, k_e is a critical parameter that determines the bandwidth and harmonic rejection performance of the PLL and has the following relationship between input and output:

$$G_\alpha(s) \equiv \frac{v_\alpha(s)}{v_{\text{ac}}(s)} = \frac{k_e\omega_1 s}{s^2 + k_e\omega_1 s + \omega_1^2} \tag{5}$$

$$G_\beta(s) \equiv \frac{v_\beta(s)}{v_{\text{ac}}(s)} = \frac{k_e\omega_1^2}{s^2 + k_e\omega_1 s + \omega_1^2} \tag{6}$$

where ω_1 is the fundamental angular frequency of input. A higher k_e can achieve fast dynamic characteristics, which can reduce the settling time. However, it also broadens the bandpass filter of SOGI-OSG, leading to a deterioration in harmonic rejection performance. On the contrary, a low k_e can obtain a high input impedance through good harmonic rejection. However, the settling time of the PLL is prolonged. For the design of the PLL loop compensator, SOGI can be expressed as follows through a simple linearization [13]:

$$\frac{v_q(s)}{\theta_{\text{PLL}}(s)} \approx \frac{V_{\text{ac,peak}}}{\tau_p s + 1} \tag{7}$$

where $\tau_p = 2/k_e\omega_1$ is the time constant.

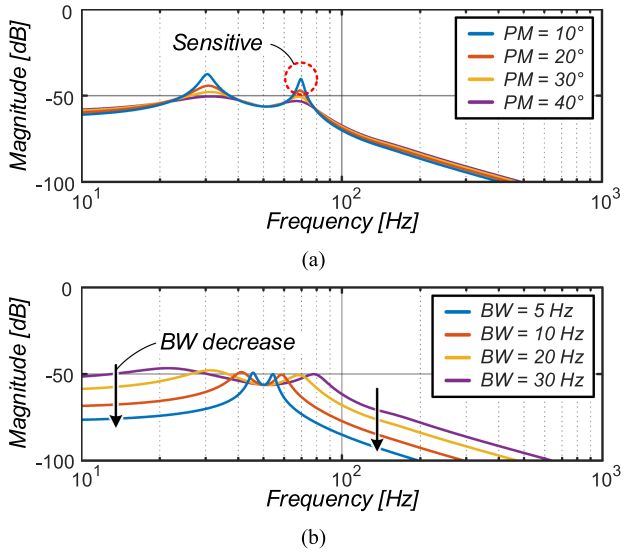

Fig. 4. Magnitude plots of the small-signal model of SOGI-PLL with different PLL parameter. (a) According to PW. The BM and k_e are designed with the same at 20 Hz and 1.414, and (b) according to BW. The PM and k_e are designed with the same at 10 Hz and 1.414.

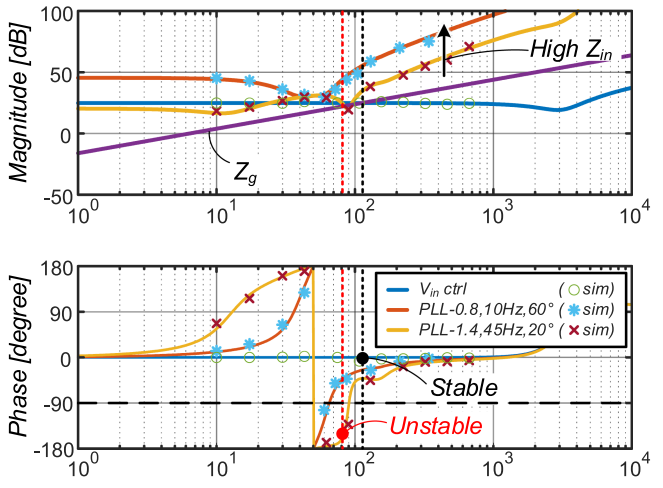

Fig. 5. Bode plots of the input impedance of PFC converter according to current reference control method, and grid impedance.

An additional issue with PLL-based control is grid instability in the low frequency due to frequency coupling. Disturbance signal of frequency f_p on the input voltage generates frequency components of $f_p + mf_1$ ($m \in N$) through the PLL loop. These components induce a low input impedance of the PFC converter around the fundamental frequency, which can cause grid instability under weak grid conditions [9].

To analyze grid stability, modeling of PLL in response to input disturbances must be carried out. For a simplified analysis, the effects of the input EMI filter are not considered. The small-signal model of the PLL to input disturbances, when modeled through harmonic linearization, can be represented by the following revised equation [9], [14]:

$$G_{\mathrm{SOGI}}(s) \equiv \frac{i_{\mathrm{ref}}(s)}{I_1^* v_{\mathrm{ac}}(s)} = \frac{1}{2j}\left[G_p(s - j\omega_1) - G_n(s + j\omega_1)\right] \tag{8}$$

where $i_{\mathrm{ref}}(s)$ is the small-signal of current reference, I_1^* is magnitude of a current reference, and $G_p(s)$ and $G_n(s)$ are given in Appendix.

The design of the SOGI-PLL relies on parameters, such as k_e, BW, and phase margin (PM), each of which contributes differently to its performance. Fig. 4(a) shows the small-signal model of PLL according to the PM = 10°, 20°, 30°, and 40°, respectively. The BM and k_e are designed with the same at 20 Hz and 1.414. As shown in Fig. 4(a), a smaller PM implies a higher sensitivity to input disturbances, which in turn is a primary cause of instability in weak grids. Fig. 4(b) displays a PM of 30°, with varying PLL BW = 5, 10, 20, and 30 Hz. With the PM kept constant, lower BW achieve lower dc and high-frequency gain. In conclusion, a PLL design with lower k_e, BW, and higher PM tends to deliver better harmonic rejection performance, which is a critical factor in enhancing grid stability.

The input impedance and grid stability of single-phase grid-tied inverters or PFC have been studied through various previous research [9], [14], [15]. For a simple analysis, the effect of output voltage control is not considered in this letter. Considering the input feed-forward, the input impedance of the PFC can be expressed as following equation:

$$Z_{\mathrm{in}}(s) = \frac{sL_B + V_o G_{ic}(s)}{A(s) V_o G_{ic}(s)} \tag{9}$$

$$A(s) = \begin{cases} I_1^* \frac{1}{v_{\mathrm{ac,peak}}} & , V_{\mathrm{in}}\ ctrl \\ I_1^* G_{\mathrm{SOGI}}(s), & PLL\ ctrl \end{cases}. \tag{10}$$

Fig. 5 depicts the bode plots of input impedance based on control method. The validity of the model was verified through MATLAB/Simulink simulations. In input-voltage-based control, the input impedance has resistive characteristics. As a result, grid stability can be maintained even when the grid impedance increases. However, in the mid-frequency range, the low input impedance can lead to large harmonic currents, potentially increasing the current THD. In contrast, in PLL-based control, the high input impedance effectively reduces harmonic currents. However, when the PLL BW is designed to be wide for fast tracking of input voltage changes, there is a potential risk of grid instability due to the increased capacitive characteristics of the input impedance. As illustrated in Fig. 5, the PLL-based control with a BW of 45 Hz and a low PM of 20° has capacitive input impedance around 80 Hz. Thus, when $L_g = 25$ mH, it fails to meet the GMPM criteria, which can lead to grid instability [16]. Conversely, a PLL with a BW of 10 Hz and a PM of 60° can maintain grid stability owing to its narrow capacitive range and a high input impedance.

The proposed hybrid control can address the input voltage variation through input-voltage-based control. Therefore, a lower BW design of the PLL is passible and high grid stability can be achievable.

TABLE I
EXPERIMENT SPECIFICATIONS AND DESIGNED PARAMETERS

Input voltage	47-63 Hz/90-264 V_{rms}
Output voltage and power	390 V/1 kW for low line 390 V/ 3kW for high line
High-frequency switches	GS66516B
Low-frequency switches	IPP60R022S7
Inductor	640 µH
Output Capacitor	980 µF
Switching frequency	64 kHz
Digital signal processer	TMS320F280049PZT
Sampling frequency	64 kHz

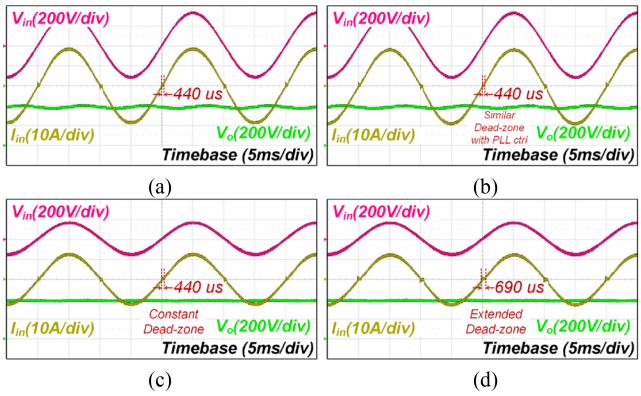

Fig. 6. Experimental waveforms of 50-Hz steady-state operation. (a) PLL-based control at 230 V_{rms}/3 kW, (b) input-voltage-based control at 230 V_{rms}/3 kW, (c) PLL-based control at 115 V_{rms}/1 kW, and (d) input-voltage-based control at 115 V_{rms}/1 kW.

III. EXPERIMENTAL RESULTS

In order to verify the feasibility of the proposed hybrid current reference control method, the steady-state operation of the PFC converter and the operation at an abnormal input voltage were tested. The PFC converter used in the experiment was designed with 47–64 Hz/90–264 V_{rms} input, 390 V/1 kW for low line, and 3 kW for high line. Table I summarizes the list of components of the prototype.

Fig. 6 illustrates a steady-state waveform comparison according to the control method. Fig. 6(a) and (b) depicts the experimental waveforms under 230-V_{rms} input and 3-kW output condition. The PLL-based control is set with a phase threshold of 0.04 and has a dead-zone of 440 μs, and the dead-zone threshold voltage of input-voltage-based control was set to 12 V to achieve the same dead-zone period. Fig. 6(c) and (d) shows the experimental waveforms under 115-V_{rms} input and 1-kW output low-line condition. The dead-zone of PLL-based control is determined based on the phase, hence it remains the same as in high-line condition, as shown in Fig. 3(c). On the other hand, the input-voltage-based control expands to 690 μs due to the decreased input, which increase THD.

Fig. 7 illustrates the results of the experiment under abnormal input voltage conditions. Fig. 7(a) and (b) demonstrates the operational waveforms when the input voltage phase experiences

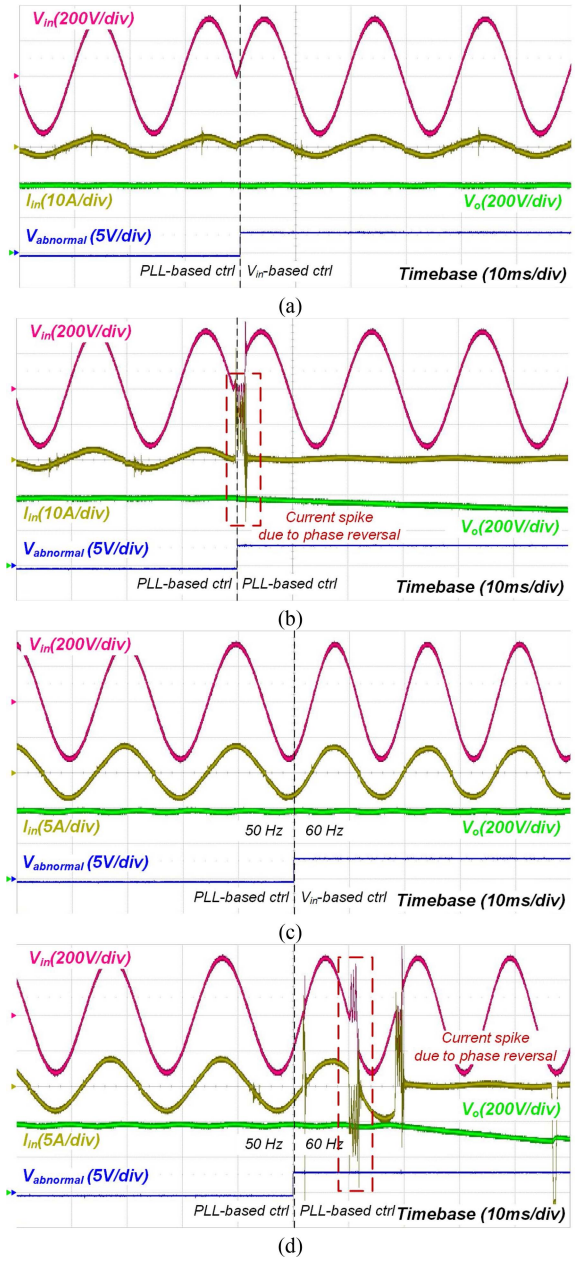

Fig. 7. Experimental waveforms of the abnormal input conditions, such as phase jump under (a) proposed hybrid control, (b) PLL-based control, and frequency jump from 50 to 60 Hz under (c) proposed hybrid control, and (d) PLL-based control.

a 180° jump. The proposed controller is capable of continuous operation using input-voltage-based control upon detecting an abnormal input voltage. In contrast, as shown in Fig. 7(b), the switch operation inverts with PLL-based control, leading to considerable spikes in the inductor and input current, subsequently halting the converter due to a fault condition. Fig. 7(c) and (d) presents the experimental waveform where the input frequency experiences a swift jump from 50 to 60 Hz. It is indicated that the proposed hybrid control method can continually supply output power, despite changes to the input voltage frequency of 10 Hz or more. However, PLL-based control faces difficulties in

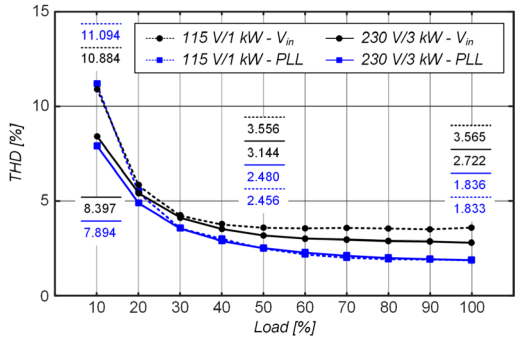

Fig. 8. Measured results of input current THD under sinusoidal input voltage condition based on current reference control method.

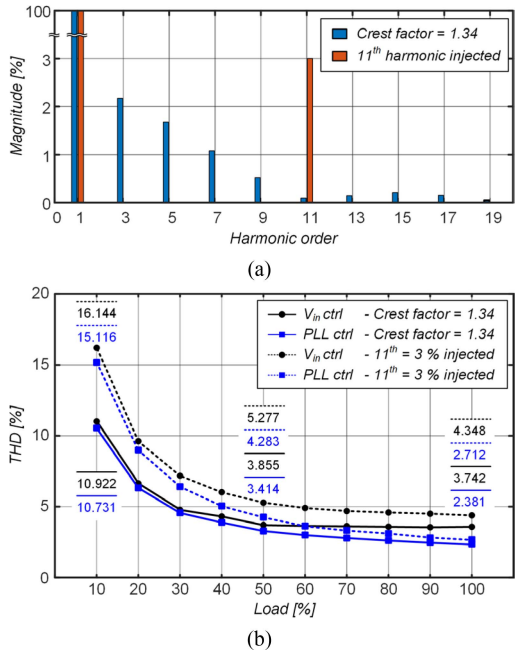

Fig. 9. Measured results under distorted input voltage condition of 230 V_{rms} with voltage THD = 3%. (a) Harmonic components of the distorted input voltage. (b) Input current THD based on the control method.

maintaining continuous operation as it generates large current spikes at each phase reversal region.

Fig. 8 presents the measurement results for input current THD under normal sinusoidal input voltage conditions, obtained using the Yokogawa WT-1802E. Although there is no difference in dead-zone period between both control methods under high-line condition, the current reference of the PLL-based control is less affected by input voltage sensing noise, allowing low input current THD. In addition, the dead-zone interval difference affects THD under low-line condition. Therefore, the THD of the PLL-based control method is reduced by 2.7% under the maximum load condition.

Fig. 9 shows the measurement results under input voltage conditions of 230-V_{rms} with a 3% voltage THD. The harmonic spectrum of the input voltage used in the experiment is shown in Fig. 9(a). The input voltage, which has a peak limited to 309 V and a crest factor of 1.34, contains low-order harmonics of 3rd, 5th, and 7th, at 2.17%, 1.68%, and 1.08%, respectively. Additionally, to validate the effects of higher order harmonic, experiments were conducted under input voltage conditions where the 11th harmonic was injected at 3%. While the input-voltage-based control leads to high current THD throughout the entire load due to distortion in the current reference, the PLL-based current reference can reduce the THD through filtering of input voltage harmonics. Since higher order harmonics can be filtered more than the lower order harmonics, under the input voltage condition where the 11th harmonic is injected, it achieves a more improved THD reduction of 1.63% compared to 1.46% for a crest factor of 1.34. Moreover, at full-load conditions, PLL-based control achieved a current THD of 2.3% and 2.7%, lower than the 3% distortion of the input voltage. As a result, the proposed control method can achieve low input THD even in the harmonic distortion in the input.

IV. Conclusion

In this letter, a hybrid current reference control method for a digital totem-pole bridgeless PFC converter is proposed. The proposed control method improves the steady-state input current THD through PLL-based control, which has a constant dead-zone and a noise and harmonic-filtered current reference. An abnormal input voltage can be detected by comparing the PLL output with the normalized input voltage. Upon detection, the controller immediately changes to input-voltage-based control to ensure continuous operation. The proposed control method can reduce current THD by 0.9% at 230-V_{rms} input and 2.7% at 115-V_{rms} input. Furthermore, even with a 3% voltage THD in the input voltage, a 1.4% current THD reduction can be achieved under 230-V_{rms} input. The proposed hybrid control method is excellent candidate for a server power supply, which maintains output power even at a hush input voltage.

Appendix

The transfer function for the small-signal model of SOGI-PLL [9]

$$G_p(s) = \frac{T_{\text{PLL}}(s)\left[-jG_\alpha(s+j\omega_1)+G_\beta(s+j\omega_1)\right]}{2-sT_{\text{PLL}}(s)\left[-jP_\alpha(s)+jN_\alpha(s)+P_\beta(s)+N_\beta(s)\right]} \tag{11}$$

$$G_n(s) = \frac{T_{\text{PLL}}(s)\left[jG_\alpha(s-j\omega_1)+G_\beta(s-j\omega_1)\right]}{2-sT_{\text{PLL}}(s)\left[-jP_\alpha(s)+jN_\alpha(s)+P_\beta(s)+N_\beta(s)\right]} \tag{12}$$

$$T_{\text{PLL}}(s) = \frac{G_{\text{PLL}}(s)}{s+v_{\text{ac,peak}}G_{\text{PLL}}(s)} \tag{13}$$

$$P_\alpha(s) = -\frac{v_{\text{ac,peak}}}{jk_e\omega_1}G_\alpha(s+j\omega_1) \tag{14}$$

$$P_\beta(s) = -\frac{v_{\text{ac,peak}}}{jk_e\omega_1}G_\beta(s+j\omega_1)+\frac{v_{\text{ac,peak}}}{j2\omega_1} \tag{15}$$

$$N_\alpha\ (s) = \frac{v_{\text{ac,peak}}}{jk_e\omega_1}\, G_\alpha\left(s - j\omega_1\right) \tag{16}$$

$$N_\beta\ (s) = \frac{v_{\text{ac,peak}}}{jk_e\omega_1}\, G_\beta\left(s - j\omega_1\right) - \frac{v_{\text{ac,peak}}}{j2\omega_1}. \tag{17}$$

REFERENCES

[1] *Limits for Harmonic Current Emissions (Equipment Input Current <16A per Phase)*, IEC International Standard 1000–3–2, 2001.

[2] Y.-D. Lee, G.-W. Moon, J. Baek, and C.-E. Kim, "A reconfigurable totem-pole PFC rectifier with light load optimization control strategy and soft-switching capability," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 4371–4382, Apr. 2021.

[3] M.-H. Park, J. Baek, Y. Jeong, and G.-W. Moon, "An interleaved totem-pole bridgeless boost PFC converter with soft-switching capability adopting phase-shifting control," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 10610–10618, Nov. 2019.

[4] H.-S. Youn, J.-S. Park, K.-B. Park, J.-I. Baek, and G.-W. Moon, "A digital predictive peak current control for power factor correction with low-input current distortion," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 900–912, Jan. 2016.

[5] J. Baek, J.-B. Lee, and J.-K. Kim, "Effective hold-up time extension method using fan control in server power systems," *IEEE Trans. Ind. Electron.*, vol. 67, no. 7, pp. 5820–5824, Jul. 2020.

[6] P. Lamo, F. López, A. Pigazo, and F. J. Azcondo, "An efficient FPGA implementation of a quadrature signal-generation subsystem in SRF PLLs in single-phase PFCs," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3959–3969, May 2017.

[7] S. Golestan, J. M. Guerrero, A. Abusorrah, M. M. Al-Hindawi, and Y. Al-Turki, "An adaptive quadrature signal generation-based single-phase phase-locked loop for grid-connected applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 4, pp. 2848–2854, Apr. 2017.

[8] F. Xiao, L. Dong, L. Li, and X. Liao, "A frequency-fixed SOGI-based PLL for single-phase grid-connected converters," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 1713–1719, Mar. 2017.

[9] J. Xu, H. Qian, Q. Qian, and S. Xie, "Modeling, stability, and design of the single-phase SOGI-based phase-locked loop considering the frequency feedback loop effect," *IEEE Trans. Power Electron.*, vol. 38, no. 1, pp. 987–1002, Jan. 2023.

[10] S. Golestan, J. M. Guerrero, and J. C. Vasquez, "Single-phase PLLs: A review of recent advances," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9013–9030, Dec. 2017.

[11] J.-Y. Lee, "Single-stage AC/DC converter with input-current dead-zone control for wide input voltage ranges," *IEEE Trans. Ind. Electron.*, vol. 54, no. 2, pp. 724–732, Apr. 2007.

[12] A. R. Gautam, K. Gourav, J. M. Guerrero, and D. M. Fulwani, "Ripple mitigation with improved line-load transients response in a two-stage DC–DC–AC converter: Adaptive SMC approach," *IEEE Trans. Ind. Electron.*, vol. 65, no. 4, pp. 3125–3135, Apr. 2018.

[13] S. Golestan, M. Monfared, F. D. Freijedo, and J. M. Guerrero, "Dynamics assessment of advanced single-phase PLL structures," *IEEE Trans. Ind. Electron.*, vol. 60, no. 6, pp. 2167–2177, Jun. 2013.

[14] J. Lin, M. Su, Y. Sun, D. Yang, and S. Xie, "Recursive SISO impedance modeling of single-phase voltage source rectifiers," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 1296–1309, Feb. 2022.

[15] M. Chen and J. Sun, "Feedforward current control of boost single-phase PFC converters," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 338–345, Mar. 2006.

[16] B. Wen, D. Boroyevich, R. Burgos, P. Mattavelli, and Z. Shen, "Inverse Nyquist stability criterion for grid-tied inverters," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1548–1556, Feb. 2017.