Letters

A High-Speed Synchronous Rectifier With Improved Dead Time Compensation and Suitable for High-Voltage Applications

Minggang Chen, Yongjia Li, *Senior Member, IEEE*, Jiawei Shi, Song Ding, Zhongyuan Fang, Shen Xu, *Member, IEEE*, Qinsong Qian, *Member, IEEE*, and Weifeng Sun, *Senior Member, IEEE*

***Abstract*—$V_{\rm DS}$ (drain–source voltage)-based synchronous rectifiers (SRs) are widely used due to their simplicity and low cost. However, there are still three obvious issues. 1) The premature turn-OFF caused by parasitic inductance under high frequency. 2) The turn-ON propagation delay is typically tens of nanoseconds. 3) Commercial SRs usually have a limited $V_{\rm DS}$ rating of about 200 V. To solve the above problems, a high-speed SR (including a customized SR IC and a peripheral circuit) is proposed. A high-speed comparator together with a slope detection circuit is proposed to reduce the turn-ON delay, and the proposed fully integrated SR IC is implemented in a 1-μm bipolar process with a die area of 1.47 $\times$ 1.98 mm^2. The peripheral circuit contains the improved dead time compensation circuit, the self-driven high-voltage isolation circuit, and the power supply circuit for SR IC, and the component count is reduced by device reuse. In a 200-W Double clamp zero voltage switching (DCZVS) buck–boost converter prototype, the proposed SR can achieve a switching frequency of more than 700 kHz with minimal dead time, the turn-ON propagation delay including peripheral circuits and SR IC is reduced to 8.1 ns, the isolated drain–source voltage is limited to within 10 V, and the peak efficiency is 93.6%.**

***Index Terms*—Double clamp zero voltage switching (DCZVS) buck–boost converter, high-voltage blocking, synchronous rectifier (SR), $V_{\rm DS}$-sensing.**

I. Introduction

SYNCHRONOUS rectifiers (SRs) are usually adopted to replace the diodes in isolated power converters [1], [2], [3], [4] for higher efficiency. There is a variety of ways to implement SR [5], and they have significant differences in technical solutions, costs, and applications. Among them, $V_{\rm DS}$-sensing [7], [8], [9], [10] is the most promising choice and is more popular with commercial SR ICs for its robustness and simplicity [7], [8], [9], [10]. However, there are still three obvious issues remaining to be resolved for commercial SR ICs, as shown in Fig. 1.

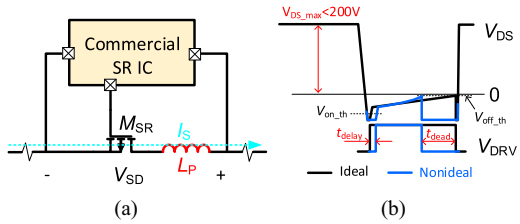

Fig. 1. Nonideality of commercial SR ICs. (a) Parasitic Inductance of SR. (b) Three kinds of nonideality.

First, due to the parasitic inductance (L_P) caused by the packaging of power MOS or PCB wiring, SR can be turned OFF prematurely at high switching frequency, as follows:

$$V_{\rm DS} = -\left(I_S \times R_{\rm ON} + L_P \frac{dI_s}{dt}\right) \tag{1}$$

where $V_{\rm DS}$ is the drain–source voltage, I_S is the secondary current through synchronous rectification MOS, and $R_{\rm ON}$ is the ON-resistance of SR MOS. During the dead time ($t_{\rm dead}$), the current goes through the body diode, causing large power loss. Although RC-based compensation [11], [12] is proposed, the accuracy is influenced by temperature and gate–source voltage ($V_{\rm GS}$). Adaptive control methods [2] are also proposed to alleviate this problem, but dynamic degradation is inevitable.

Second, commercial SR ICs [6], [7], [8], [9], [10] have large turn-ON propagation delay ($t_{\rm delay}$) due to the limited performance of the turn-ON circuit, and this will increase power loss, especially for converters with peak current at the beginning of energy transfer stage (such as ACF [13], DCZVS buck–boost [4]).

Finally, since the BCD technologies are usually adopted to implement the ICs for their maturity and low cost, the maximum rating drain–source voltage ($V_{\rm DS\_max}$) is typically less than 200 V. Therefore, commercial ICs are not suitable for high-voltage applications (more than 200 V). To expand the voltage range, some research [14], [15] has been reported. Yu et al. [14] use a blocking FET to isolate high voltage, but an

Manuscript received 20 June 2023; revised 2 August 2023 and 21 August 2023; accepted 1 September 2023. Date of publication 5 September 2023; date of current version 6 December 2023. This work was supported in part by the Youth Program of the Natural Science Foundation of Jiangsu Province under Grant BK2022048-3, in part by the Southeast University Startup Funding under Grant 4006012308, and in part by the programs of the National Natural Science Foundation of China under Grants 52177172, 62234005, 62174030, 5706002301, and 52207192. *(Corresponding authors: Qinsong Qian; Weifeng Sun.)*

The authors are with the National ASIC System Engineering Research Center, Southeast University, Nanjing 210096, China (e-mail: chen_mg@seu.edu.cn; yongjia.li@ieee.org; 1029148862@qq.com; songding1996@foxmail.com; 101013415@seu.edu.cn; xus@seu.edu.cn; qianqinsong@seu.edu.cn; swffrog@seu.edu.cn).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3312132.

Digital Object Identifier 10.1109/TPEL.2023.3312132

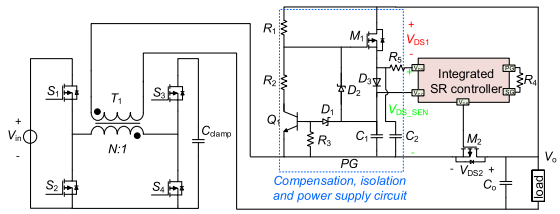

Fig. 2. Power topology and architecture of the proposed SR.

external capacitor is required to mitigate the impact of high *dv/dt*, which introduces an additional sampling delay. Zhang et al. [15] propose a self-driven SR drain-to-source voltage sensing circuit, which provides a low-impedance bypassing path for the current introduced by high *dv/dt*. However, digital isolators and filters also introduce additional delay. Furthermore, Yu et al. [14] and Zhang et al. [15] do not present the power supply circuits of the proposed SRs.

In this letter, a high-speed SR IC together with a peripheral circuit is proposed and verified. The proposed SR IC is implemented in a bipolar process for low delay and high driving current density [16]. The novel peripheral circuit can almost eliminate the dead time, isolate the high voltage, and power up the SR IC at the same time.

II. Analysis and Design of Proposed SR

A. Architecture of Proposed SR

The proposed SR and the topology of the power converter are shown in Fig. 2. The proposed SR is composed of a peripheral circuit (compensation, isolation, and power supply circuit) and an integrated SR controller. Specifically, M_1 has the following three functions. 1) M_1 and C_2 form the compensation network. 2) M_1 is also the high-voltage blocking switch. 3) R_1, R_2, R_3, C_1, D_1, D_2, D_3, M_1, and Q_1 form the power supply circuit. M_1 is the power transistor, D_1 and Q_1 form the voltage reference, and Q_1, R_1, and R_2 form the error amplifier. The integrated SR controller turns SR MOS ON or OFF by sampling $V_{\rm DS}$, and a detailed description will be given later. Fig. 2 shows the configuration of high-side SR, the proposed SR can also be configured to the low side.

B. High-Voltage Isolation Sampling and Power Supply Circuit

To improve the $V_{\rm DS}$ rating of SR and power up the SR IC, a power supply and high-voltage isolation circuits are proposed, as depicted in Fig. 2. To illustrate the working principle, key waveforms are shown in Fig. 3. The working principle of the DCZVS buck–boost converter can be found in [4].

t_0–t_1: Both M_1 and M_2 are OFF. $V_{\rm GS2}$ keeps low, and $V_{\rm DS2}$ rises to V_o by t_1. $V_{\rm DS1}$ increases with $V_{\rm DS2}$, and $V_{\rm DS\_SEN}$ keeps constant. C_1 is discharged and $V_{\rm CC}$ is reduced.

t_1–t_2>: Both M_1 and M_2 are OFF. $V_{\rm DS1}$ follows $V_{\rm DS2}$, $V_{\rm DS\_SEN}$ keeps at maximum value unchanged, and the high voltage is isolated by M_1.

t_2–t_3>: Both M_1 and M_2 are OFF. $V_{\rm DS1}$ decreases with $V_{\rm DS2}$, and $V_{\rm DS1}$ reaches -0.7 V by t_3 and is clamped due to the conduction of the body diode of M_1.

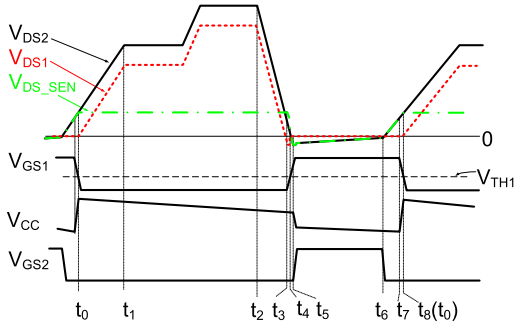

Fig. 3. Key waveforms of the proposed sampling and supply circuit.

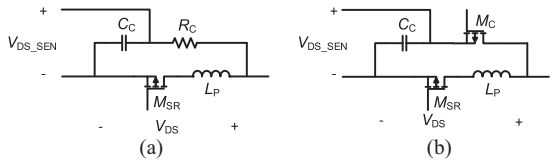

Fig. 4. Simplified compensation circuit. (a) Conventional. (b) Proposed.

t_3–t_4>: Both M_1 and M_2 are OFF. Since $V_{\rm DS1}$ is clamped to -0.7 V, $V_{\rm DS\_SEN}$ decreases with $V_{\rm DS2}$. $V_{\rm GS1}$ increases due to the decrease of $V_{\rm DS\_SEN}$, and $V_{\rm GS1}$ reaches $V_{\rm TH1}$ by t_4, and then M_1 is turned ON.

t_4–t_5>: M_1 is ON and M_2 is OFF. Since M_1 is ON, $V_{\rm DS1}$ is zero and $V_{\rm DS\_SEN}$ decreases with $V_{\rm DS2}$. $V_{\rm DS\_SEN}$ reaches the turn-ON threshold of SR at t_5, and then, M_2 is turned ON. More energy is needed to turn M_2 ON, so $V_{\rm CC}$ is reduced sharply at this moment.

t_5–t_6>: Both M_1 and M_2 are ON, and $V_{\rm DS\_SEN}$ equals $V_{\rm DS2}$ and reaches the turn-OFF threshold of SR at t_6, and then M_2 is turned OFF.

t_6–t_7>: M_1 is ON and M_2 is OFF, $V_{\rm DS\_SEN}$ increases with $V_{\rm DS2}$ and reaches ($V_{\rm CC}$+$V_{\rm DON3}$) by t_7.

t_7–t_8(t$_0$)>: M_1 is ON and M_2 is OFF. D_3 is ON and C_1 is charged, and $V_{\rm CC}$ is increased. Since $V_{\rm CC}$ is increased, $I_{\rm CQ1}$ is increased, and $V_{\rm GS1}$ is decreased. And $V_{\rm GS1}$ reaches $V_{\rm TH1}$ by $t_8(t_0)$, and then M_1 is OFF. A new cycle begins after t_8.

C. Dead Time Compensation Circuit

Since parasitic inductance (L_P) caused by the packaging of power MOS or PCB wiring will lead to the phase lead of $V_{\rm GS2}$, RC-based compensation was presented and extensively used for its simplicity and low cost [11], [12], as shown in Fig. 4(a). The s-domain expression for $V_{\rm DS\_SEN}$ can be obtained with (1) and Fig. 4(a)

$$V_{\rm DS\_SEN} = -I_S R_{\rm ON}\left(1+s\frac{L_P}{R_{\rm ON}}\right)\left(\frac{1}{1+sR_CC_C}\right) \quad (2)$$

where $V_{\rm DS\_SEN}$ is the sensed source–drain voltage, R_C is the compensation resistor, and C_C is the compensation capacitor. To compensate for the phase lead caused by L_P, R_C, and C_C should satisfy

$$R_CC_C = \frac{L_P}{R_{\rm ON}}. \quad (3)$$

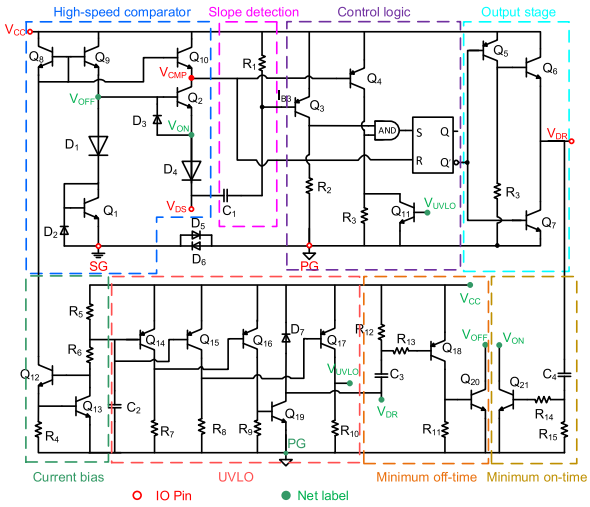

Fig. 5. Circuit of the proposed SR IC.

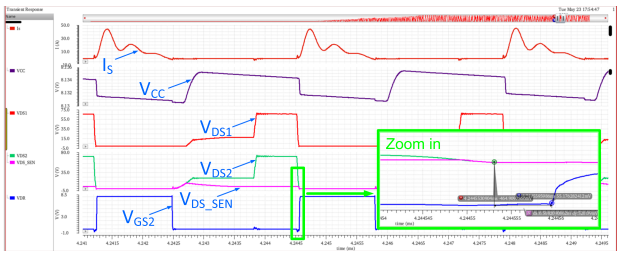

Fig. 6. Key simulation waveforms of the proposed SR IC.

The methods in [11] and [12] have two issues: 1) $R_{\rm ON}$ varies with gate–source voltage and temperature; (b) an additional reset circuit is needed to keep the initial value of C_C. To solve the above two issues, the proposed compensation circuit is shown in Fig. 4(b), of which the resistor R_C is implemented by a MOSFET M_C (M_1 in Fig. 2), and the drive circuit of M_C is shown in Fig. 2. If M_C is chosen the same as $M_{\rm SR}$ and driven by the same gate–source voltage, R_C should be the same as $R_{\rm ON}$. When laying out the PCB, make M_C as close as possible to $M_{\rm SR}$ to eliminate the impact of temperature on $R_{\rm ON}$. As also shown in Figs. 2 and 3, D_2 is ON when $V_{\rm DS2}$ is low, thus $V_{\rm GS1}$ is equal to $V_{\rm CC}$. As described in Section II-B, due to the conduction of M_1 between t_4 and t_8, $V_{\rm DS\_SEN}$ varies between positive and negative values and thus be reset cycle by cycle.

D. High-Speed SR IC

Since the bipolar process has better current efficiency [16], the proposed SR IC is implemented with bipolar technology, as shown in Fig. 5 . The driver IC is composed of a high-speed comparator, slope detection, control logic, output stage, current bias, UVLO, minimum ON-time control, and minimum OFF-time control, and detailed analysis of high-speed comparator, slope detection, and minimum ON/OFF-time control is presented.

1) High-Speed Comparator: As shown in Fig. 5, the comparator includes Q_1, Q_2, Q_8, Q_9, Q_{10}, D_1, D_2, D_3, and D_4. Q_8, Q_9, and Q_{10} form the current mirror and provide the current bias

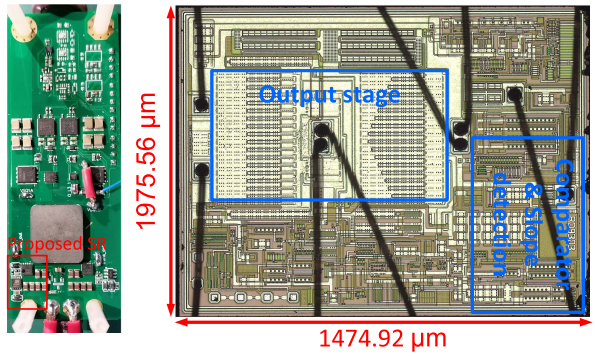

Fig. 7. (a) Testing setup. (b) Die photograph of the proposed SR IC.

of the input path and the reference path. D_1, D_2, and Q_1 form the reference path, and the reference voltage is zero. D_3, D_4, and Q_2 form the input path, and the output of the comparator is $V_{\rm CMP}$. When $V_{\rm DS} > 0$, $V_{\rm CMP}$ is high; when $V_{\rm DS} < 0$, $V_{\rm CMP}$ is low. The ideal reference voltage is 0, but this can be violated by the mismatch between Q_9 and Q_{10}, and the mismatch between the input path and reference path. This violation can be minimized by matching the design of the layout, and this violation can be further removed by R_4 or R_5 of Fig. 2. The current bias generated by Q_9 and Q_{10} will go through R_4 and R_5 of Fig. 2, respectively. The configurable threshold of the comparator is expressed by

$$\left.\begin{aligned} V_{\rm TH} &= 0 + I_B R_4 \\ V_{\rm INCMP} &= V_{\rm DS} + I_B R_5 \end{aligned}\right\} \tag{4}$$

where $V_{\rm TH}$ and $V_{\rm INCMP}$ are the reference voltage and the input voltage of the proposed comparator, respectively, and I_B is the bias current generated by Q_9 and Q_{10}.

When $R_4 > R_5$, the reference voltage of the comparator will be increased. And when $R_4 < R_5$, the reference voltage of the comparator will be decreased. R_4 and R_5 can also be used to adjust the ON/OFF threshold voltage of SR MOS. Therefore, the effect of the parameter's tolerance on the comparator can be compensated and ignored.

2) Slope Detection: As shown in Fig. 5, R_1 and C_1 form the slope detection circuit. The falling slope of $V_{\rm DS}$ determines the current through R_1. When C_1 is determined, the larger the falling slope of $V_{\rm DS}$, the greater the current flowing through R_1. And the maximum current of R_1 is $V_{\rm EB3}/R_1$. When the falling slope of $V_{\rm DS}$ meets with the following equation:

$$\frac{dV_{\rm DS}}{dt} \geq \frac{V_{\rm EB3}}{R_1 C_1} + \frac{I_{\rm B3}}{C_1}. \tag{5}$$

Q_3 is ON, and one input of the AND gate is high. The slope detection circuit is designed to avoid the wrong opening. To avoid parameter deviation and the accuracy of slope detection, R_1 is designed to be adjustable with trim.

3) Minimum Off-Time: As shown in Fig. 5, Q_{18}, Q_{20}, R_{11}, R_{12}, R_{13}, and C_3 form the minimum OFF-time control circuit. As described before, slope detection is designed to avoid wrong openings, but this is not enough. At the moment, when SR MOS is turned OFF, $V_{\rm DS}$ is usually accompanied by a large high-frequency voltage ringing, which may also cause a wrong opening. To avoid this risk, a blanking time is usually set to

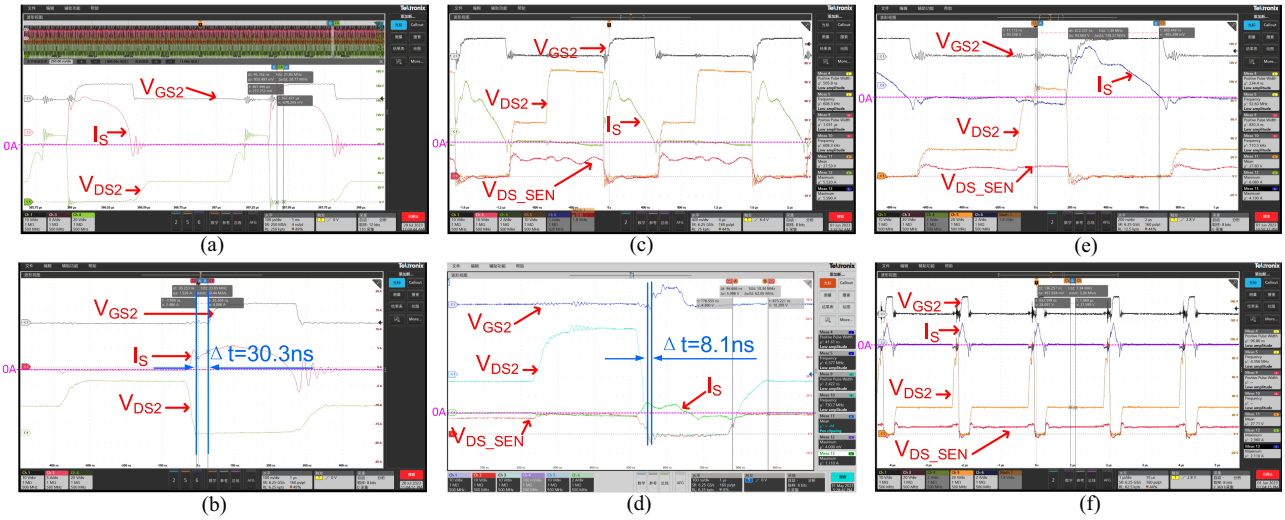

Fig. 8. Transient test waveforms. (a) With NCP4306 ($V_{\rm in}$ = 400 V, V_o = 28 V, P_o = 200 W). (b) With NCP4306 ($V_{\rm in}$ = 170 V, V_o = 28 V, P_o = 20 W). (c) With the proposed SR driver ($V_{\rm in}$ = 170 V, V_o = 28 V, P_o = 200 W). (d) With the proposed SR driver ($V_{\rm in}$ = 170 V, V_o = 28 V, P_o = 0 W). (e) With the proposed SR driver ($V_{\rm in}$ = 400 V, V_o = 28 V, P_o = 200 W). (f) With the proposed SR driver ($V_{\rm in}$ = 400 V, V_o = 28 V, P_o = 20 W).

the input signal S of the SR trigger. In this work, a blanking time (typically 50 ns) determined by C_3 and R_{12} is added to the circuit. At the falling edge of $V_{\rm DR}$

$$C_3\frac{dV_{\rm DR}}{dt}=\frac{V_{\rm EB18}}{R_{12}}+I_{\rm B18}. \tag{6}$$

When ignoring the base current of Q_{18}, the minimum OFF-time can be got

$$t_{\rm min\_off}=\frac{V_{\rm DR}}{V_{\rm EB18}}R_{12}C_3 \tag{7}$$

where $t_{\rm min\_off}$ is designed to avoid wrong openings, and there are no high requirements for its accuracy, and it can also be trimmed by R_{12}.

4) Minimum On-Time: As shown in Fig. 5, Q_{21}, R_{14}, R_{15}, and C_4 form the minimum ON-time control circuit. It functions at the rising edge of $V_{\rm DR}$ to prevent wrong turning OFF. The principle is similar to that of *minimum OFF-time.*

The key simulation waveforms of the proposed SR IC are shown in Fig. 6, which is consistent with the theoretical waveforms in Fig. 3. To illustrate the impact of parameter tolerance on the turn-ON delay, simulations were conducted at different process corners and temperature, and the simulation results are shown Table I. The turn-ON delay is between 5.9 ns and 11.5 ns, and the typical turn-ON propagation delay is 6.5 ns.

III. Experimental Verification and Comparison

The experimental prototype is shown in Fig. 7(a), the die photo of the proposed SR IC is shown in Fig. 7(b), and the key parameters of the experimental prototype are listed in Table II. Fig. 8 presents the waveforms of the DCZVS power converter with NCP4306 and with the proposed SR driver under different input voltages and loads. Fig. 8(a) shows the waveforms of full load and high input voltage for NCP4306, and Fig. 8(b) shows the light load and low input voltage for NCP4306. It can be seen from Fig. 8(b) that the turn-ON delay of NCP4306 is about 30.3 ns and the late turn-OFF leads to a significant negative current. Fig. 8(c)–(f) shows the waveforms of the proposed SR driver. As theoretically analyzed before, when $V_{\rm DS2}$ is high, $V_{\rm DS\_SEN}$ is always maintained at around $V_{\rm CC}$; when $V_{\rm DS2}$ is at a low level, $V_{\rm DS\_SEN}$ can accurately follow $V_{\rm DS2}$. Fig. 8(c) and (d) shows the waveforms of 200 W and 0 W under the input of 170 V, respectively. It can be seen from Fig. 8(d) that the turn-ON delay is only 8.1 ns, and the turn-OFF is almost at zero current. Fig. 8(e) and (f) shows the waveforms 200 W and 20 W under the input of 400 V, respectively. With self-driven MOS-and-capacitor-based compensation, our SR has minimal dead time after M_2 is turned OFF and is not affected by temperature and driving voltage. By comparing Fig. 8(b) and (d), the turn-ON propagation delay ($t_{\rm delay}$) of the proposed SR driver is 8.1 ns and is slightly larger than the simulation result of 6.5 ns, which is much smaller than the turn-ON delay of NCP4306. The efficiency of the DCZVS power converter with the proposed SR, NCP4306, and without SR is shown in Fig. 9. Thanks to the fast turn-ON and compensation for turn-OFF, the proposed SR driver achieves a peak efficiency of 93.6%, which is higher than 91.6% of NCP4306 and 90% of without SR. The performance of the proposed SR is summarized and compared to other state-of-the-art SRs in Table III. With

TABLE I
Turn-ON Delay Under Different Process Corners and Temperature

	TT	SS	FF	SF	FS
-40 ℃	5.9 ns	6.6 ns	6 ns	6 ns	5.9 ns
27 ℃	6 ns	7.8 ns	6.5 ns	6.8 ns	6.4 ns
125 ℃	9.8 ns	9.8 ns	11.5 ns	9.2 ns	10.8 ns

TABLE II
Key Parameters of the Experimental Prototype

Components	Parameters
Input voltage $V_{\rm in}$	170–400 V
Output voltage $V_{\rm o}$	28 V
$P_{\rm o}$	200 W
Switching frequency $f_{\rm s}$	700 kHz
Transformer	N=$N_{\rm P}$:$N_{\rm S}$=6:1, $L_{\rm P}$=15 μH, $L_{\rm S}$=50 nH
$M_{\rm SR}$, $M_{\rm C}$	BSZ240N12NS3G

TABLE III
PERFORMANCE SUMMARY AND COMPARISON

	TPEL[11]	TPEL[12]	JESTPE[14]	JESTPE[15]	This work	
SR scheme	Discrete	IR1168	NCP4303	Discrete	**NCP4306**	**Customized IC**
f_s	1000 kHz	170 kHz	300 kHz	500 kHz	**700 kHz**	**700 kHz**
P_o	1000 W	600 W	1000 W	3300 W	**200 W**	**200 W**
Peak efficiency	96.3%	95.8%	N/A	97.6%	**91.6%**	**93.6%**
t_{delay}	75 ns	60 ns*	60 ns*	60 ns	**30.3 ns**	**8.1 ns**
Improvement of dead time	RC-based, deteriorated by temperature and driving voltage	RC-based, deteriorated by temperature and driving voltage	N/A	N/A	**N/A**	**MOS and capacitor-based compensation**
VDS rating Extension of SR	N/A	N/A	Self-Driven Blocking MOSFET, with extra delay	Self-Biasing Blocking MOSFET, with extra delay	**N/A**	**Self-driven High-Voltage Blocking**
Component count	Low	Low	Low	High	**Low**	**Low**

* The delay of the compensation circuit is not included.
The boldface values to highlight "This work."

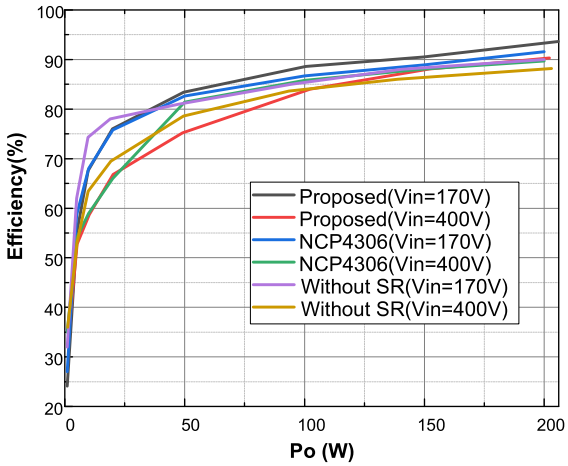

Fig. 9. Efficiency of the DCZVS buck–boost converter with different SR.

customized SR ICs and novel compensation/isolation/power supply circuits, the proposed SR can achieve the lowest turn-ON propagation delay. Besides, compensation for dead time and high-voltage isolation are achieved with a small number of peripheral devices.

IV. CONCLUSION

The proposed SR includes a customized IC and compensation/supply/isolation circuit. Implemented by the bipolar process, the proposed IC reduces the turn-ON propagation delay $t_{\rm delay}$ to only 8.1 ns, which is much smaller than conventional SR ICs. With the proposed MOS-and-C-based compensation scheme, the proposed SR can work at a high switching frequency (700 kHz) with nearly no dead time $t_{\rm dead}$, and it will not be affected by temperature and driving voltage compared to conventional methods. And in a 200-W experimental prototype, the peak efficiency of 93.6% is achieved. The compensation circuit and supply and isolation circuits reuse devices, which reduces the component count of the proposed SR. Although only verified in the DCZVS buck–boost converter, the proposed SR can also be applied to Flyback, QR-Flyback, *LLC*

REFERENCES

[1] C. Sun, Q. Sun, R. Wang, P. Zhang, L. Zhang, and P. Wang, "Universal synchronous rectification scheme for LLC resonant converter using primary-side inductor voltage," *IEEE Trans. Ind. Electron.*, vol. 70, no. 6, pp. 5747–5759, Jun. 2023.
[2] Q. Qian, Q. Liu, M. Zheng, Z. Zhou, S. Xu, and W. Sun, "An improved adaptive synchronous rectification method with the enhanced capacity to eliminate reverse current," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 1394–1410, Feb. 2022.
[3] H. Dong, X. Xie, and L. Zhang, "A new primary PWM control strategy for CCM synchronous rectification flyback converter," *IEEE Trans. Power Electron.*, vol. 35, no. 5, pp. 4457–4461, May 2020.
[4] S. Ding, T. Wang, Q. Liu, Y. Zhou, and Q. Qian, "A novel realization of ZVS and efficiency optimization for double-clamped ZVS buck-boost converter without current sampling," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2022, pp. 743–746.
[5] Y. Wei, Q. Luo, and H. A. Mantooth, "Synchronous rectification for LLC resonant converter: An overview," *IEEE Trans. Power Electron.*, vol. 36, no. 6, pp. 7264–7280, Jun. 2021.
[6] "UCC24630: Synchronous rectifier controller with ultra-low standby current," Texas Instruments Incorporated, Dallas, TX, USA, 2015. [Online]. Available: http://www.ti.com/product/UCC24630
[7] "UCC24612: High-frequency synchronous rectifier controller," Texas Instruments Incorporated, Dallas, TX, USA, 2018. [Online]. Available: https://www.ti.com/product/UCC24612
[8] "NCP4306, secondary side synchronous rectification driver for high-efficiency SMPS topologies," 2022. [Online]. Available: https://www.onsemi.com/download/data-sheet/pdf/ncp4306-d.pdf
[9] "LT8309: Secondary-side synchronous rectifier driver," Analog Devices, Inc., Wilmington, MA, USA, 2014. [Online]. Available: https://www.analog.com/media/en/technical-documentation/data-sheets/lt8309.pdf
[10] "MP6951: Fast turn-off rectifier for flyback converter with intelligent VDS ringing detection," Monolithic Power Syst., Inc., 2022. [Online]. Available: https://www.monolithicpower.com/en/documentview/productdocument/index/version/2/document_type/Datasheet/lang/en/sku/MP6951GJ/document_id/10923/
[11] D. Fu, Y. Liu, F. C. Lee, and M. Xu, "A novel driving scheme for synchronous rectifiers in LLC resonant converters," *IEEE Trans. Power Electron.*, vol. 24, no. 5, pp. 1321–1329, May 2009.
[12] D. Wang and Y.-F. Liu, "A zero-crossing noise filter for driving synchronous rectifiers of LLC resonant converter," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1953–1965, Apr. 2014.
[13] M. Chen, S. Xu, L. Huang, W. Sun, and L. Shi, "A digital adaptive control method for optimizing valley current of active clamp flyback converter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 5, pp. 5749–5761, Oct. 2022.
[14] O. Yu, C.-W. Chen, C.-S. Yeh, and J.-S. Lai, "Design and analysis of high-voltage blocking in drain–source synchronous rectifier controllers for kV operation," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 4, pp. 4406–4415, Dec. 2020.
[15] Z. Zhang, M. Wang, C. Liu, Y. Si, Y. Liu, and Q. Lei, "High-dv/dt-immune fine-controlled parameter-adaptive synchronous gate driving for GaN-based secondary rectifier in EV onboard charger," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 3, pp. 3302–3323, Jun. 2022.
[16] "Fundamentals of MOSFET and IGBT gate driver circuits," Texas Instruments Incorporated, Dallas, TX, USA, 2015. [Online]. Available: