Letters

A Fast-Transient Fully-Integrated Digital LDO With Current-Estimation Algorithm Based Coarse Loop

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***Abstract*—In this brief, a fully-integrated output-capacitor-free (OCF) digital low-dropout regulator (DLDO) is proposed utilizing a current-estimation algorithm (CEA)-based coarse loop controller to achieve fast voltage droop (V_{Droop}) recovery with improved line and load regulations. The proposed CEA-based controller quickly determines the target output switch-code by estimating the current-voltage ratio of power MOSFETs, enabling fast V_{Droop} recovery during load current (I_{LOAD}) transients. Complementing the CEA-based coarse loop, the proposed OCF-DLDO incorporates asynchronous and fine loops. The asynchronous loop supplies an instant dynamic current during I_{LOAD} transients, rapidly restoring the V_{OUT}, while the fine loop reduces output voltage ripples and quiescent current during steady-state of the DLDO. The proposed OCF-DLDO was fabricated in a 65-nm CMOS process with an active area of 0.075 mm^2. Measurement results demonstrate that the proposed DLDO operates with an input voltage range of 0.6−1.2 V. For a load current step of 26 mA at V_{DD} = 0.6 V, the proposed DLDO recovers a V_{Droop} of 140 mV within 95 ns achieving a figure-of-merit of 3.74 ns with a peak current efficiency of 99.6 %.**

***Index Terms*—Current-estimation algorithm, digital low-dropout regulator (LDO), fast transient, output-capacitor-free.**

I. Introduction

LOW-DROPOUT regulators (LDOs) are widely used in system-on-chips (SoCs) for efficient point-of-load (PoL) power delivery with fast transient response and small footprint [1]. Multiple LDOs can be integrated into SoCs without bulky passive components like inductors and capacitors in switching-mode regulators [2]. Digital versions of LDOs (DLDOs) have gained significant attention due to their design simplicity, scalability, and wide range of input (V_{DD}) and output voltages (V_{OUT}) while driving μA to sub-ampere load currents [3]. However, conventional DLDOs, as depicted in Fig. 1(a) utilizing a binary clocked comparator and an integral-controller based on bidirectional shift registers (SRs), rely on high clock frequency (F_{CLK}) for improved performance [1], [2], [3]. Yet, this high F_{CLK} incurs a large quiescent current (I_Q) which reduces the overall current and power efficiencies of a DLDO.

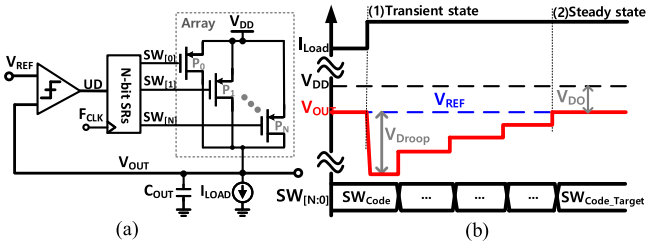

Fig. 1. Typical DLDO: (a) Circuit diagram and (b) load transient response.

Dual-feedback loop DLDOs [4], [5], [6], [7], [8], [9], [10] have effectively addressed the power-speed tradeoff of a typical DLDO. In dual-loop DLDOs [4], [8], [10], [11], a high-gain coarse loop controller with a higher F_{CLK} is implemented to quickly reduce the large voltage error during transient-state. Conversely, a high-resolution fine loop controller with a slower F_{CLK} is implemented for the steady-state operation of a dual-loop DLDO to reduce the I_Q and voltage ripples V_{RIPP}. It indicates that, even in the coarse loop, F_{CLK} influences the transient response of dual-loop DLDOs [4], [8], [10], [11]. Fig. 1(b) illustrates the load transient waveforms of DLDOs [4], [5], [10] using typical SRs-based digital controllers. These controllers recover the voltage droop (V_{Droop}) by adjusting their output codes ($SW_{[N:0]}$) at each rising edge of F_{CLK} until the target output code $SW_{Code[Target]}$ is achieved and V_{OUT} becomes equal to V_{REF}. This approach adjusts only one SW_{Code} per F_{CLK} period, resulting in prolonged recovery time (T_{REC}) of V_{Droop}. Notably, the T_{REC} of DLDOs [1], [4], [5], [10] increases with higher V_{Droop} at higher I_{LOAD} transients. Recently, we proposed a least-mean-square (LMS) algorithm-based controller which is equipped with adaptive-gain adjusting logics for fast

Manuscript received 16 August 2023; revised 24 September 2023 and 17 October 2023; accepted 25 October 2023. Date of publication 27 October 2023; date of current version 6 December 2023. This work was supported in part by the Research grant of Kangwon National University in 2022, and in part by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIT) under Grant RS-2023-00221494. The EDA tool was supported by the IC Design Education Center (IDEC) . *(Corresponding authors: Muhammad Abrar Akram; In-Chul Hwang.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3328065.

Digital Object Identifier 10.1109/TPEL.2023.3328065

accurate voltage recovery [12]. It successfully eliminated the T_{REC} dependence on the F_{CLK} like in typical DLDOs [4], [5], [6], [7], [8], [9], [10]. However, the LMS algorithm requires more computational time for adaptive-gain adjustment because it reduces the feedback errors by comparing the present and the previous errors which leads to longer T_{REC}.

To address these shortcomings, we propose a current-estimation algorithm (CEA)-based controller for the coarse loop of the proposed DLDO. This CEA-based controller updates its output (SW_{Code}) by estimating the current-voltage ratio of power MOSFETs, enabling quick determination of the $SW_{Code[Target]}$ and significantly reducing the T_{REC} of V_{Droop}, even during large I_{LOAD} transients. This quick determination of $SW_{Code[Target]}$ using CEA-controller improves the load transient response as compared to LMS algorithm-based controller [12]. The rest of this article is organized as follows. Section II derives the relationship between the controller's $SW_{Code[Target]}$, I_{LOAD}, and the dropout voltage (V_{DO}) of the DLDO. Section III discusses the proposed CEA-based coarse loop and compares its performance with existing typical SRs controllers. The proposed output-capacitor-free (OCF) DLDO is presented in Section IV. Section V presents the measurement results. Finally, Section VI concludes the article.

II. Relationship Between Target SW_{Code} and I_{LOAD}

DLDOs commonly use unary-weighted PMOS transistor sizing due to its high resolution [1], [4], [5], [10]. Fig. 1(a) shows a typical DLDO with a unary-weighted PMOS array. Here, the number of turned-ON transistors depends on the switch code $SW_{[N:0]}$ of the SRs controller, determined within the feedback loop operation to achieve $V_{OUT} = V_{REF}$ at a particular I_{LOAD}. PMOS transistors are turned-ON in the deep-triode region and function as r_{ON} resistors, while turned-OFF transistors behave like open circuits [Fig. 1(a)]. The turned-ON state of a PMOS in this switch array can be expressed as follows:

$$I_{PMOS} = \mu_p C_{ox} \frac{W_p}{L_p}(V_{SG} - |V_{thp}|)V_{SD}. \tag{1}$$

Similarly, I_{LOAD} can be calculated from the number of turned-ON PMOS transistors corresponding to the SW_{Code} value.

$$\begin{aligned} I_{LOAD} &= I_{PMOS} \times SW_{Code} \\ &= \mu_p C_{ox} \frac{W_p \times SW_{Code}}{L_p}(V_{SG} - |V_{thp}|)V_{SD} \\ &= k \times SW_{Code} \times V_{SD}. \end{aligned} \tag{2}$$

Coefficient (k) models the process parameters and voltage ($V_{SG} - |V_{thp}|$). V_{SD} indicates the voltage difference between V_{DD} and V_{OUT}, and it is called the dropout voltage (V_{DO}). During the load-transient state as shown in Fig. 1(b), V_{DO} becomes equivalent to V_{Droop} at a particular SW_{Code} and I_{Load}. Accordingly, (2) for the load-transient state is given as

$$I_{LOAD}(transient - state) = k \times SW_{Code} \times V_{Droop}. \tag{3}$$

Similarly, in the DLDO's steady-state, V_{Droop} is fully recovered after multiple iterations of SW_{Code} [Fig. 1(b)] and V_{OUT} equals V_{REF} at the target $SW_{Code[Target]}$. It provides the steady-state current equation of DLDO.

$$I_{LOAD}(steady - state) = k \times SW_{Code} \times V_{DO}. \tag{4}$$

Equations (3) and (4) provides the $SW_{Code[Target]}$ to achieve the steady-state of the DLDO.

$$SW_{Code[Target]} = \frac{SW_{Code} \times V_{Droop}}{V_{DO}}. \tag{5}$$

Equation (5) indicates that knowing the present SW_{Code} and V_{DO} enables an immediate estimation of the $SW_{Code[Target]}$ for the DLDO's the steady-state during I_{Load} transients. By deriving (5), we propose the CEA-based coarse loop, which promptly adjusts the V_{Droop} by estimating $SW_{Code[Target]}$. This leads to the significant reductions in V_{Droop} and T_{REC} during I_{Load} transients for the proposed OCF-DLDO.

III. Proposed CEA-Based Coarse Loop

Fig. 2(a) shows the simplified block diagram of the proposed CEA-based coarse loop implemented in the proposed OCF-DLDO. During start-up, the continuous-time ADC (CT-ADC) performs a non-uniform quantization and generates seven-thermometric bits DT[6:0]. Among these bits, DT[3] is considered at the V_{REF} level and changes its polarity when V_{OUT} is approximately equal to V_{REF}. DT[2] and DT[4] represent a voltage range ($V_{REF} \pm \Delta$) around the V_{REF}. Based on this voltage range, the operating mode of the proposed CEA is decided. The mode selector block generates the control signal CEA_{SEL} from DT[2] and DT[4] to select the operating mode of the CEA-based coarse loop. When the V_{OUT} is outside the voltage range $V_{REF} \pm \Delta$, CEA_{SEL} remains zero. However, when V_{OUT} enters the $V_{REF} \pm \Delta$ range, CEA_{SEL} changes its polarity from 0 to 1. CEA_{SEL} level determines which output bits of the two different operating modes of the CEA controller are used to control the PMOS transistors, as depicted in Fig. 2(a).

When $CEA_{SEL} = 0$, all DT[6:0] bits are passed to a look-up table (LUT) as shown in Fig. 2(a). The LUT generates the 20-bit binary-code RG[19:0]. These values are computed using the voltage difference ratio between V_{DD}, V_{OUT}, and V_{REF}, which can be expressed as follows:

$$RG[19:0] = \frac{V_{DD} - V_{OUT}}{V_{DD} - V_{REF}}. \tag{6}$$

As a result, LUT continually generates RG[19:0] until the voltage differences in (6) ($V_{DD} - V_{OUT}$) and ($V_{DD} - V_{REF}$) becomes equal. Subsequently, RG[19:0] is fed to a 20-bit multiplier, where the upper 7-bits represent the integer part, and the lower 13 bits represent the fractional part. The 7-bit integer part is then transformed into 128-bit thermometric code using a binary-to-thermometric (B-to-T) converter that controls the PMOS transistors and generates the current I_{CEA}. This current is adjusted to match I_{LOAD} for voltage regulation. The 13-bit fractional part is designed to reduce feedback voltage errors during arithmetic operations, specifically the quantizer (CT-ADC) errors. The fractional part significantly reduces the division errors. Its resolution is set to be $(1/2)^N$, where N is the number of bits in the fractional part. The maximum error

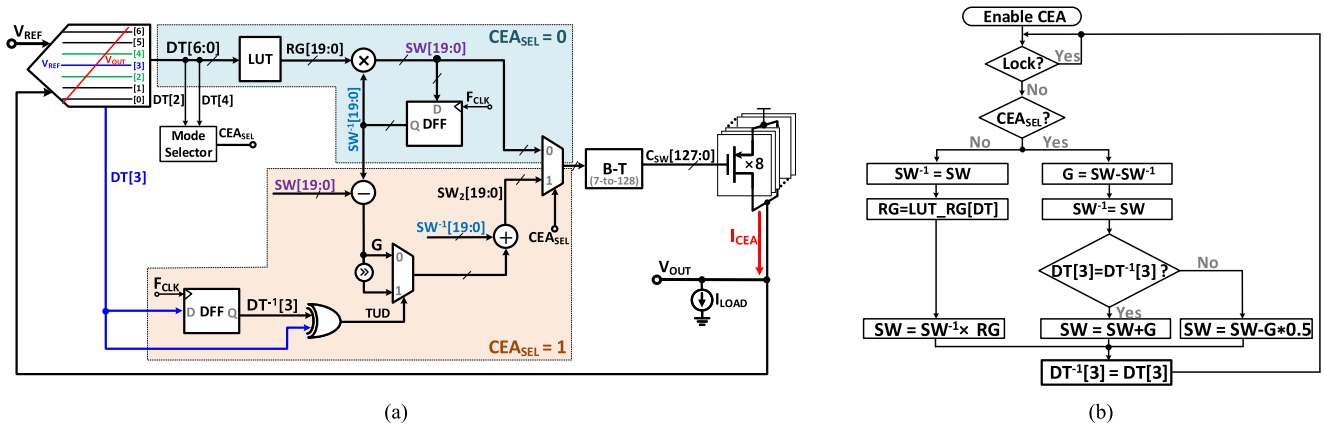


Fig. 2. Proposed CEA-based coarse loop. (a) Simplified block diagram. (b) Flow diagram.

may occur when the C_{SW} code is at its maximum value. If M is the number of bits in the integer part, the design constraint is $((2^M) - 1 \times (1/2)^N < 1)$. To ensure that the voltage error remains within acceptable limits, M should be less than N. The proposed CEA-based controller aims to keep the voltage error within 1.5 % of the C_{SW} code.

When $CEA_{SEL} = 0$ and V_{OUT} is out of $V_{REF} \pm \Delta$ range, the proposed CEA loop performs coarse-gain variations within one F_{CLK} cycle, to rapidly bring V_{OUT} within $V_{REF} \pm \Delta$ range, thus reducing the transient time. Contrarily, when V_{OUT} approaches the $V_{REF} \pm \Delta$ range CEA_{SEL} switches from low to high, the proposed CEA loop initiates its fine-gain iterations to precisely match V_{OUT} with V_{REF}. This reduces V_{OUT} fluctuations and achieves fine load regulation. The fine-gain variations start with the mid-bit DT[3] of DT[6:0], which is delayed by one F_{CLK} cycle, and then compared with DT^{-1}[3]. If DT[3] and DT^{-1}[3] are different, and $TUD = 1$, the gain (G) of the CEA is reduced to half of the current gain to achieve fine regulation. The feedback loop continues iterating and reducing the gain (G) by half in each F_{CLK} cycle until DT[3] and DT^{-1}[3] becomes equal, and the gain (G) of CEA is fixed. The overall operation of the proposed CEA-based coarse loop is depicted in a flow diagram in Fig. 2(b). In Fig. 2(b), *Lock* indicates the enabling of the CEA coarse loop of the DLDO, which is described in detail in Section IV.

Fig. 3 compares the load transient response of the proposed CEA-based coarse loop controller with our previously proposed LMS-based coarse loop controller [12] at $V_{OUT} = 1.15$ V, $F_{CLK} = 20$ MHz, and $\Delta I_{LOAD} = 15$ mA. Both coarse loop controllers demonstrate almost the same V_{Droop}, however, the LMS-based controller recovers the V_{Droop} within $T_{REC} = 310$ ns, while the proposed CEA-based controller recovers it within $T_{REC} = 50$ ns, reducing the T_{REC} by 83.87%.

Furthermore, we simulated the load transient response of the proposed CEA-based loop controller with a typical SRs-based loop controller at various I_{LOAD} conditions, and compared their V_{Droop} and T_{REC}, as shown in Fig. 4. As shown, with the increase of I_{LOAD}, V_{Droop} and T_{REC} of SRs-based loop significantly increases, due to its inherent speed limitations as described in Section I. Contrarily, with the proposed CEA-based

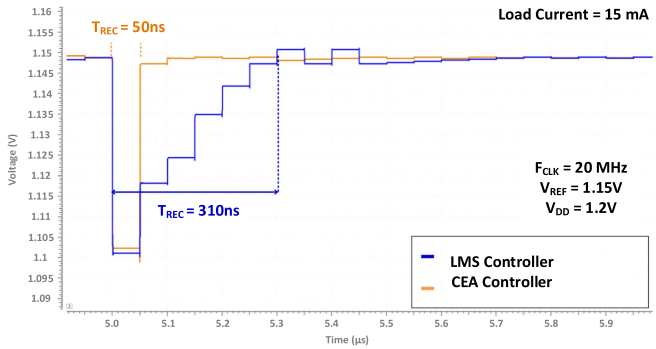


Fig. 3. Simulated load transient performance comparison of the LMS-based controller [12] with the proposed CEA-based controller.

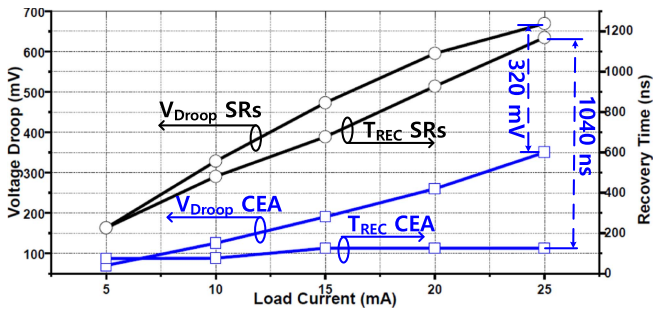
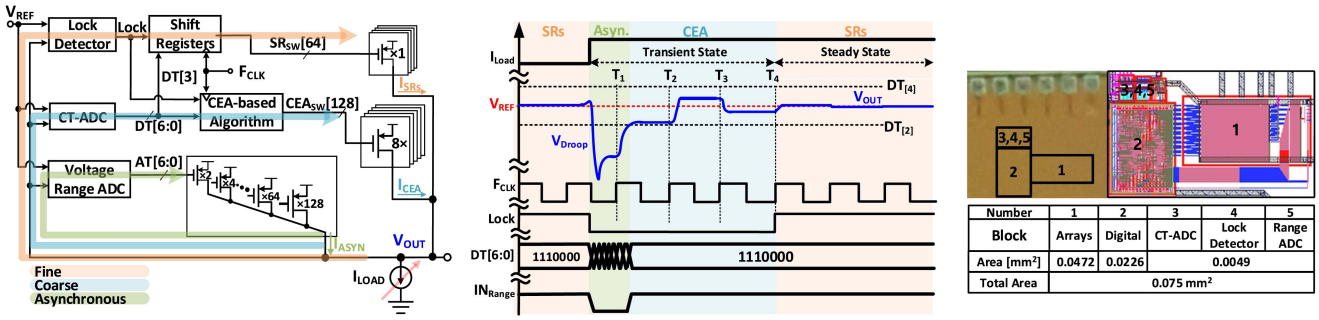


Fig. 4. Simulated V_{Droop} and T_{REC} comparison of typical SRs-based and the proposed CEA-based coarse loops at various I_{LOAD}.

loop, T_{REC} does not increase with an increase of V_{Droop} for a large I_{LOAD} step. Instead, it recovers the V_{Droop} within almost the same T_{REC} time. By using the proposed CEA-based loop, the overall V_{Droop} and T_{REC} of the DLDO are reduced by 320 mV and 1040 ns, respectively, as compared to SRs loop.

IV. Proposed Fast-Transient OCF-DLDO

Fig. 5(a) shows the detailed block diagram of the proposed OCF-DLDO. The OCF-DLDO consists of three loops: Two synchronous (F_{CLK} operated) loops and one asynchronous (clock-less) loop. The asynchronous loop functions as a fast



(a) (b) (c)

Fig. 5. Proposed OCF-DLDO. (a) Block diagram. (b) Operating waveforms. (c) Die micrograph and layout.

proportional (P-control) system, providing instant dynamic current I_{ASYN} similar to an output capacitor (C_{OUT}). It effectively suppresses V_{Droop} during load current transients. The loop is realized by directly connecting a 7-bit V_{OUT} range detector ADC to a binary-weighted PMOS array, as shown in Fig. 5(a). The V_{OUT} range detector ADC compares V_{OUT} with seven predefined voltage ranges centered around V_{REF}, spanning 30–200 mV. Each voltage range is represented by the respective output bit of AT[6:0]. AT[0] corresponds to the widest voltage range and AT[6] is the narrowest one. When V_{OUT} is sufficiently close to V_{REF} (i.e., <30 mV) during the DLDO's steady-state, all thermometric bits AT[6:0] become high, turning-OFF the binary-weighted power transistors. The asynchronous loop has been previously proposed in our tri-loop DLDO [12], and its operation principle and design considerations are detailed there. The proposed coarse loop consists of a continuous-time ADC (CT-ADC), a CEA-based controller, and a 128-bit unary-weighted PMOS array, as shown in Fig. 5(a). The CT-ADC employs seven logic-threshold-triggered comparators (LTTC) to perform non-uniform quantization. It generates skewed-threshold voltage levels in each LTTC and produces 7-thermometric bits (DT[6:0]) [12]. The employed CT-ADC ensures high steady-state accuracy of the proposed OCF-DLDO without compromising its speed during transient states. The CEA controller, based on DT[6:0], adaptively estimates the coarse loop current (I_{CEA}) to match to the load current I_{LOAD}. During start-up or load transient states, if the voltage difference between V_{OUT} and V_{REF} increases, the proposed CEA-based controller turns-ON/OFF a larger number of PMOS transistors within a F_{CLK} cycle. Conversely, as the voltage difference decreases, the CEA-based controller performs fine-regulation by halving the number of turned-on/off transistors in each F_{CLK} cycle until $V_{OUT} \approx V_{REF}$. The fine loop consists of a typical SRs-based controller and a small-sized unary-weighted PMOS array. It operates during the steady-state of the DLDO to reduce steady-state voltage ripples (V_{RIPP}) and quiescent current (I_Q).

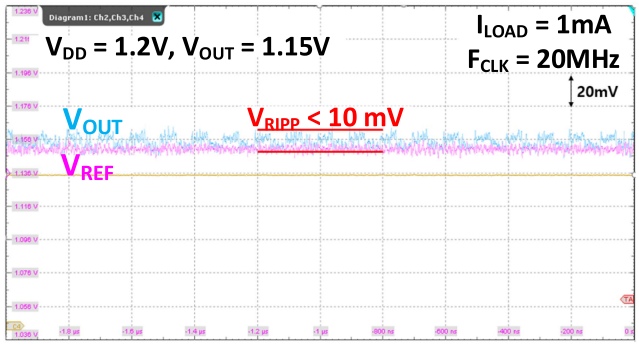
The switching between the coarse and fine loops is determined by the "$Lock$" signal generated by a lock detector as shown in Fig. 5(a). When V_{OUT} reaches within the pre-defined lock range (≈ 10 mV) of the lock detector, $Lock$ signal toggles from 0 to 1, transitioning the loop from coarse to fine. The switching process is further illustrated in Fig. 5(b). As shown, during a load-transient state (when I_{LOAD} steps-up), the asynchronous loop rapidly supplies I_{ASYN} to compensate for V_{Droop} before the synchronous CEA-based coarse loop responds. At the next rising of $F_{CLK}(T_1)$, the CEA-based controller recovers the V_{Droop} upto IN_{Range} ($DT_{[2]}$–$DT_{[4]}$), substantially reducing the voltage difference between V_{OUT} and V_{REF}. At T_2 and T_3, the CEA-based controller further reduces the voltage difference using fine current estimations, as discussed in Section III. Once, V_{OUT} enters the predefined lock range of lock detector, $Lock$ switches high, freezing the coarse loop and triggering the fine loop to reduce V_{RIPP} and I_Q.

V. Measurement Results

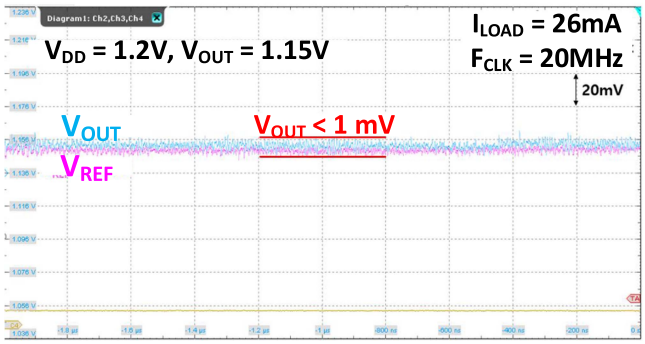
The proposed output-capacitor-free DLDO (OCF-DLDO) was designed in a 65-nm CMOS process and occupies an active area of 0.075 mm^2, as shown in Fig. 5(c). It generates V_{OUT} from 0.65–1.15 V using V_{DD} of 0.7–1.2 V, and supplies an I_{LOAD} of 1 to 26 mA. V_{RIPP} performance of the proposed OCF-DLDO is shown in Fig. 6 for minimum and maximum I_{LOAD} at $V_{OUT} = 1.15$ V. The OCF-DLDO exhibits 10 mV and 1 mV of V_{RIPP} at I_{LOAD} of 1 mA and 26 mA, respectively. Fig. 7(a) shows the dynamic voltage scaling accuracy of the proposed OCF-DLDO at $V_{DD} = 1.2$ V and $I_{LOAD} = 1$ mA. It accurately tracks the fast-changing V_{REF} from 0.95 to 1.15 V. Line transient performance of the proposed OCF-DLDO is shown in Fig. 7(b), when the V_{DD} is switched between 1.0 to 1.2 V at $V_{REF} = 0.9$ V and $I_{LOAD} = 1$ mA. The proposed OCF-DLDO achieves a line regulation of 0.05 mV/mV.

Fig. 8 shows the measured PSR of the proposed OCF-DLDO over the frequency range from 10 Hz to 1 MHz under two different I_{LOAD} conditions, i.e., 1 mA and 26 mA.

To measure the PSR at $V_{DD} = 1.2$ V $V_{REF} = 1.15$ V with V_{DO} of 50 mV, a small-signal ripple of 40 mV_{PP} was injected into V_{DD}, and V_{OUT} was measured. Although, the 40 mV_{PP} injection into 40 mV_{DD} reduced the V_{DO} to 30 mV, still the proposed DLDO maintains more than –25 dB PSR from 10 Hz to 10 kHz frequency range. Overall, the PSR increases from –33 dB at 10 Hz to –2.5 dB at 1 MHz for $I_{LOAD} = 1$ mA, and it is also within a similar range for $I_{LOAD} = 26$ mA. It indicates that the proposed OCF-DLDO does not show large PSR variations against I_{LOAD} variations.

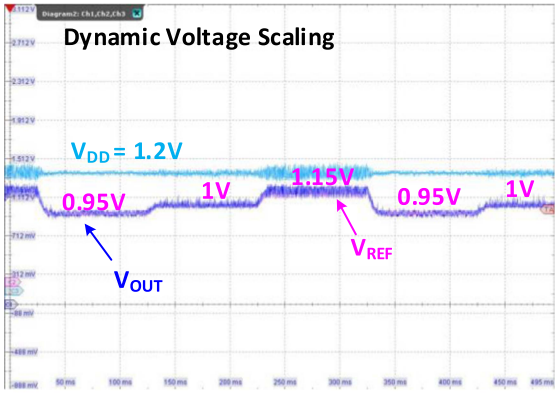


(a)



(b)

Fig. 6. Oscilloscope captures of V_{RIPP} of the proposed OCF-DLDO at (a) $I_{LOAD} = 1$ mA and (b) $I_{LOAD} = 26$ mA.



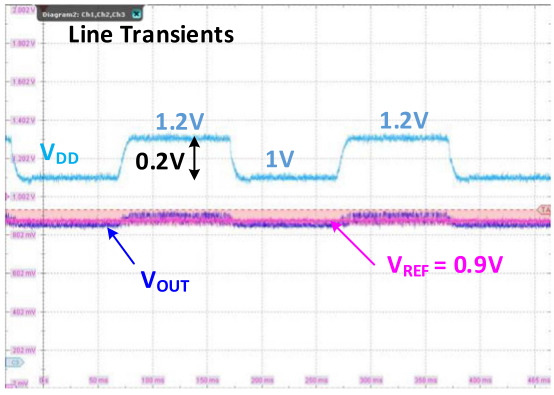


Fig. 7. Oscilloscope captures of (a) dynamic voltage scaling and (b) line transient performance of the proposed OCF-DLDO.

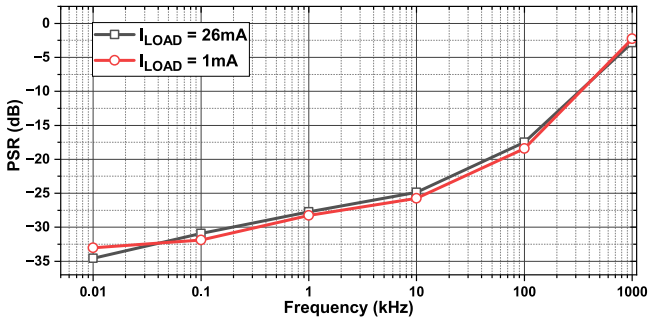
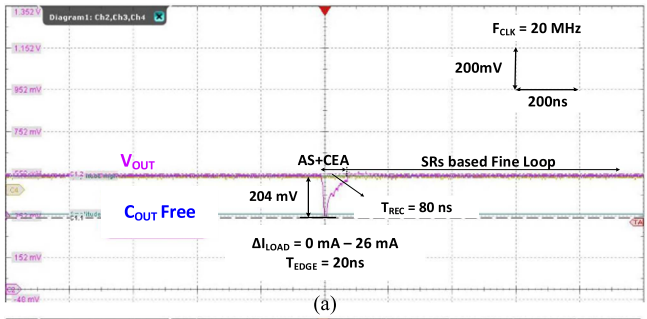
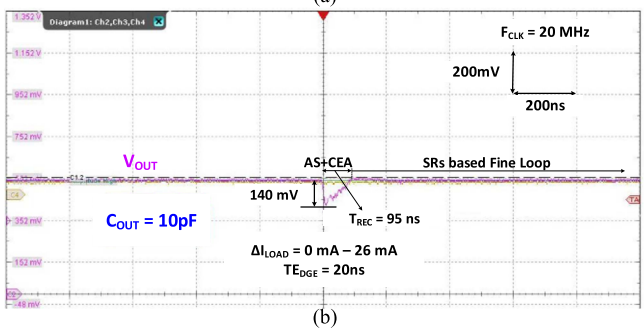


Fig. 8. Measured power supply rejection (PSR) of the proposed OCF-DLDO at $V_{DD} = 1.2$ V.



(a)



(b)

Fig. 9. Oscilloscope captures showing the load transient performance of the proposed OCF-DLDO at $V_{DD} = 0.6$ V, $V_{REF} = 0.55$ V, when (a) $C_{OUT} = 0$ and (b) $C_{OUT} = 10$ pF.

Figs. 9 and 10 exhibit the measured load transient responses of the proposed DLDO, comparing cases with and without C_{OUT} ($C_{OUT} = 0$ and $C_{OUT} = 10$ pF). These measurements were taken by switching the I_{LOAD} from 0 to 26 mA ($\Delta I_{LOAD} = 26$ mA) with $T_{EDGE} = 20$ ns. At $V_{DD} = 0.6$ V, $V_{OUT} = 0.55$ V, as shown in Fig. 9, the proposed DLDO shows a reduced V_{Droop} of 204 mV without using a C_{OUT} (i.e., $C_{OUT} = 0$) due to an instant dynamic current supply of asynchronous loop. V_{Droop} is recovered within T_{REC} of 80 ns. Adding $C_{OUT} = 10$ pF, reduces the V_{Droop} to 140 mV for the same load current (i.e., $\Delta I_{LOAD} = 26$ mA), and it is fully recovered in $T_{REC} = 95$ ns, as shown in Fig. 9(b). Similarly, at $V_{DD} = 1.2$ V, $V_{OUT} = 1.15$ V, as shown in Fig. 10(a), the proposed DLDO shows reduced V_{Droop} of 202 mV without using a C_{OUT}. Adding $C_{OUT} = 10$ pF [Fig. 10(b)] reduces V_{Droop} to 155 mV for the same load current, and it is fully recovered in $T_{REC} = 110$ ns.

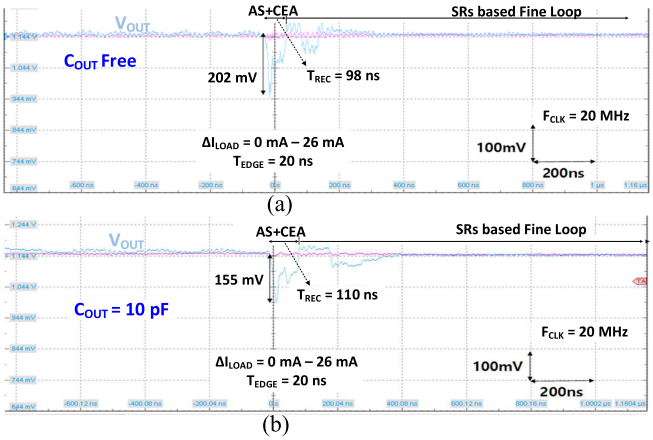


Fig. 10. Oscilloscope captures showing the load transient performance of the proposed DLDO at $V_{DD} = 1.2$ V, $V_{REF} = 1.15$ V, when (a) $C_{OUT} = 0$ and (b) $C_{OUT} = 10$ pF.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	This Work	[4]	[6]	[8]	[9]	[12]
Process [nm]	65	65	130	65	65	65
Topology	AS+CEA	SRs	PID	VCO	SRs	AS+LMS
V_{DD} [V]	0.6–1.2	0.6–1.2	0.5–1.22	0.9–1.2	0.6–1.0	0.6–1.2
V_{OUT} [V]	0.55–1.15	0.4–1.1	0.35–1.17	0.5–1.1	0.55–0.95	0.55–1.15
$I_{LOAD, MAX}$ [mA]	26	100	145	19	4.5	25
C_{OUT} [nF]	0–0.01	1	1.5	0.2	1	0.00084
V_{Droop} [mV] @ ΔI_{LOAD} [mA]	140@26*	55@98	280@40	80@3	118@4.4	96@24.5
T_{REC} [ns] @ V_{Droop} [mV]	95@140*	700@55	55@280	90@80	5900@118	900@96
ΔI_{LOAD} T_{EDGE} [ns]	20	20	0.1	5	10	20
Load Reg [mV/mA]	0.04	0.06	N/A	0.15	0.422	0.2
I_Q [µA]	102–167	82	3200	131	10.2	7.8–21.35
Current Eff. [%]	99.6	99.92	97.8	99.3	99.7	99.91
FOM_1 [ps]	39.4	8.836	844	342	73.7	8.71
FOM_2 [ns]	3.74	6.185	46.42	30.8	434	7.84
Area [mm^2]	0.075	0.01	0.18	0.059	0.09	0.041

*Measurements are performed using C_{OUT} = 0.01 nF at V_{DD} = 0.6V. N/A = Not Addressed.

$FOM_1 = \frac{C_{OUT} \times V_{Droop} \times I_Q}{\Delta I_{LOAD}^2} + \frac{T_{EDGE} \times I_Q}{2\Delta I_{LOAD}}$

$FOM_2 = FOM_1 \times T_{REC}$

Table I summarizes the performance of the proposed OCF-DLDO and its comparison with the state-of-the-art DLDOs. I_Q of the proposed DLDO is in the range of 102 to 167 μA for V_{DD} of 0.6 to 1.2 V, respectively. The reason for this I_Q range is the variation of static-current consumption at different V_{DD} in the level-triggered blocks i.e., (CT-ADC and voltage-range ADC). The proposed CEA-based coarse loop helps achieving the better load regulation as compared to referenced DLDOs. To fairly compare the overall load transient performance of the proposed and referenced DLDOs, we used a figure-of-merit (FOM_1) [(7)] introduced in [13] which specifically includes the edge-time (T_{EDGE}) information of changing I_{LOAD}.

$$FOM_1 = \frac{C_{OUT} \times V_{Droop} \times I_Q}{\Delta I_{LOAD}^2} + \frac{T_{EDGE} \times I_Q}{2\Delta I_{LOAD}}. \quad (7)$$

FOM_1, however, does not consider the T_{REC} which is significantly important in load transient performance of a DLDO. To include the T_{REC}, the FOM_2 was defined in [8] and it is given below

$$FOM_2 = FOM_1 \times T_{REC}, \quad (8)$$

Based on the FOM_1, as shown in the Table I, it is evident that the proposed DLDO exhibits superior performance when compared with DLDOs in [6], [8], and[9]. However, it is worth noting that [4] and LMS-based DLDO [12], outperform the proposed DLDO with regard to FOM_1. It is because, the I_{LOAD} driving capacity of [4] is large and in [12] the parasitic output capacitance is estimated instead of using a C_{OUT}. Nonetheless, when we consider the calculation of FOM_2 with T_{REC} inclusion, the proposed DLDO clearly outperforms both [4], [12] by achieving the minimum FOM_2. It is because of the significantly shorter T_{REC} as compared to [4] and [12]. The smaller FOM_2 of the proposed DLDO reflects the effectiveness of the proposed CEA-based controller which quickly determines the target switch-code to supply the I_{LOAD} without adversely affecting the other performance metrics of the DLDO, as compared to typical digital controllers [4], [6], [8], [9], [12].

VI. CONCLUSION

An output-capacitor-free DLDO with mitigated voltage droop (V_{Droop}) and fast-transient response is presented. The proposed CEA-based coarse loop enables fast V_{Droop} recovery during load current transients by quickly estimating the target switch code to activate exact number of PMOS transistors for load regulation. Fabricated DLDO in a 65-nm CMOS achieved a V_{Droop} recovery time (T_{REC}) dependent FOM of 3.74 ns with peak current efficiency of 99.6%.

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