A Counter-Based Open-Circuit Switch Fault Diagnostic Method for a Single-Phase Cascaded H-Bridge Multilevel Converter

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***Abstract*—A cascaded H-bridge multilevel converter (CHBMC), which is composed of power cells, is an attractive ac–dc converter for medium- and high-voltage applications in terms of its modularity, improved harmonic performance, and higher rated voltage withstand capability. Nevertheless, the overall operation and stability of the CHBMC can be affected by inevitable issues, such as the open-circuit (OC) switch fault. This issue causes adverse effects. Hence, it is vital to develop an effective but straightforward method to identify the OC switches. This article proposes an OC switch fault diagnostic method, which is based on counters. These counters are defined to have a one-to-one correspondence with the CHBMC switches. First, a fault feature variable is obtained based on a current residual generated from the estimated current model and the OC switch fault output voltage conditions. Subsequently, based on a postfault logic judgment process, the output voltage levels, the driving signal combinations, and the current polarity, the counters indicate the OC switch fault and its position. The proposed method is simple and voltage level-independent, making it ideal for diagnosing multiple OC switch faults for the CHBMC in a power cell and different cells. The effectiveness of the proposed method is verified by simulation and experimental results.**

***Index Terms*—Cascaded H-bridge multilevel converter (CHBMC), counter, current residual, fault diagnosis, open-circuit (OC) switch fault.**

NOMENCLATURE

n	Number of cascaded power cells.
e_{N}	Grid voltage.
i_{sN}	Grid current.
$L_{\mathrm{N}},\ R_{\mathrm{N}}$	Line inductor and line resistor.
W_{11} to W_{n4}	Switches in the CHBMC.
$\mathrm{D}_{\mathrm{d}11}$ to $\mathrm{D}_{\mathrm{d}n4}$	Diodes in the CHBMC.
$C_{\mathrm{dc}1}$ to $C_{\mathrm{dc}n}$	DC-link capacitors.
$R_{\mathrm{dc}1}$ to $R_{\mathrm{dc}n}$	DC-link resistors.
$u_{\mathrm{dc}1}$ to $u_{\mathrm{dc}n}$	DC-link voltages.
u_{dc}	Unified dc-link voltage.
$\overline{u}_{\mathrm{dc}1}$ to $\overline{u}_{\mathrm{dc}n}$	DC-link voltage mean values.
$\overline{U}_{\mathrm{dc}}$	Average of the dc-link voltage mean values.
U_{dc}^{*}	DC-link voltage reference.
g_{11} to g_{n4}	Driving signals.
p_{11} to p_{n4}	Control feedback signals.
u_1 to u_n	Actual port voltages.
c_{11} to c_{n4}	Counters.
D	Fault feature variable.
D_{11} to D_{n4}	Respective fault feature variables.
ω	Power angular frequency.
$\hat{u_1}$ to $\hat{u_n}$	Estimated port voltages.
u_{ab}	Actual total output voltage.
$u_{\hat{\mathrm{ab}}}$	Estimated total output voltage.
$\hat{i_{\mathrm{sN}}}$	Estimated grid current.
i_{sN}^{*}	Grid current reference.
u^{*}	Modulated voltage reference.
u_1^{*} to u_n^{*}	Respective modulated voltage references.
$cw_1,\ cw_2$	Carrier waves.
M_1 to M_n	Modulation waves.

I. INTRODUCTION

THE cascaded H-bridge multilevel converter (CHBMC) has gained significant attention for applications requiring high voltage and power, such as microgrid and traction railway systems [1], [2], [3], [4], [5]. Its modular structure provides control flexibility, scalability, and fault-tolerance. However, the reliability of the CHBMC operation is a topic of concern due to the presence of numerous power switches that are vulnerable to faults. Among these faults, the open-circuit (OC) switch fault is a potential risk that requires effective diagnostic methods [6], [7], [8], [9]. Hence, it is crucial to investigate effective diagnostic methods for the OC switch fault.

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Power switches are susceptible to two types of permanent failures, namely, short-circuit (SC) faults and OC faults. SC faults occur due to overvoltage, overheating, or wrong driving signals, which generate an overcurrent effect within approximately 10 μs, leading in the most severe case to an instantaneous breakdown of the converter [10]. Therefore, protection circuits are implemented to detect and isolate SC faults [11]. On the other hand, OC faults arise from lift-off bond wire or gate driver failure, which do not cause immediate converter breakdown but may result in a chain of failures due to thermal stress accumulation [12], [13]. Consequently, online OC switch diagnosis methods are crucial to prevent fault propagation and system shutdown.

Generally, identifying the specific causes of OC faults can be challenging as they can result in similar electrical behaviors in voltage/current measurements. The signal-based and model-based perspectives are two mainstreams of the OC switch fault diagnostic methods. In [14], a sampling theory is employed to obtain different switching sequences for an HB converter, which extracts postfault grid current information to identify the faulty switch. Similarly, in [15], the current slope and zero-voltage switching states are extracted to identify the fault location. However, these methods have a long diagnosis time of more than two current cycles and cannot detect multiple faults. To detect multiple faults, Kumar [16] analyzed the pulsewidth modulation (PWM) output voltage in prefault and postfault time-domain scenarios, enabling the identification of single/multiple faults in the CHBMC by analyzing switching states and comparing counters. Nonetheless, this approach requires additional voltage sensors and complex diagnostic criteria involving multiple threshold values. Furthermore, Wang et al. [17] used harmonic and principle component analysis (PCA) to obtain fault features of terminal voltages, but this method involves extra sensors and heavy computations.

Alternatively, model-based methods for OC switch fault diagnosis require accurate models and residual evaluations. From the current perspective, the authors in [18] and [19] employed a mixed logic dynamic model, which takes into account the diodes ON/OFF-state, to detect the fault current or voltage and identify the OC switch fault in the CHBMC. However, they are unable to detect multiple OC switch faults. To overcome this limitation, the authors in [20] and [21] used current residuals from different power cells and continuous updates of diagnostic matrices to identify multiple OC switch faults, but they require additional detection methods, such as dual current residuals-based detection and multiple iterated detection matrices. On the other hand, the authors in [22] and [23] utilized residual features between the estimated and measured terminal voltages for potential fault verification and modulation switching, enabling the identification of single or multiple faulty switches. However, these approaches involve additional voltage sensors and complex diagnostic procedures.

To address the aforementioned issues, this article proposes a counter-based OC switch fault diagnostic method. The diagnostic counter for each switch is specifically designed to perform a direct diagnosis of faulty switches based on the current residuals, postfault driving signal combinations, and current polarity, by judging the maximum counted value. Feature removal for detected faults and counter resetting help the method to continuously diagnose multiple faults. Compared with existing methods, a simple logic judgment with only one threshold is required. Moreover, the proposed method is level-independent and simply extends the diagnosis of the OC switch faults to more H-bridge power cells for the CHBMC, which ensures the application potential of the diagnostic method.

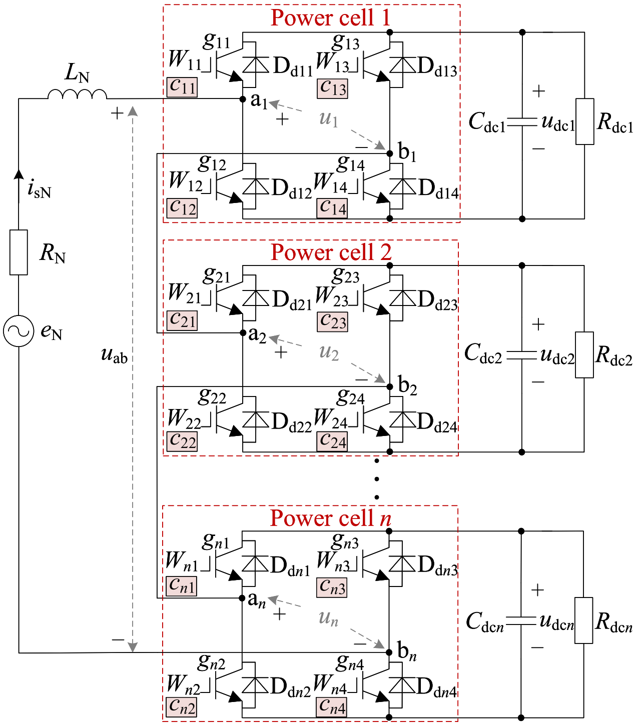


Fig. 1. CHBMC circuit diagram with n power cells.

II. Theory of the Proposed Method

The CHBMC comprises n cascaded power cells, as depicted in Fig. 1 [1], respectively, denoted as power cell 1 to power cell n. In Fig. 1, the electrical parameters are defined in the Nomenclature. Moreover, there exist n driving signal combinations, $\{g_{11}, g_{12}, g_{13}, g_{14}\}$ through $\{g_{n1}, g_{n2}, g_{n3}, g_{n4}\}$, which directly come from the controller. These driving signal combinations are utilized for two purposes: 1) driving the switches, i.e., W_{11} through W_{n4}, and 2) giving feedback to the controller and serving as input signals for the proposed OC switch fault diagnostic method. As will be clarified later, each switch depicted in Fig. 1 is also linked to counters, specifically c_{11} through c_{n4}, which serve to identify the position of the OC switch faults.

In terms of purpose 2), when the driving signal combinations $\{g_{11}, g_{12}, g_{13}, g_{14}\}$ through $\{g_{n1}, g_{n2}, g_{n3}, g_{n4}\}$ are fed back to the controller, they are redefined as the control feedback signal combinations, denoted by $\{p_{11}, p_{12}, p_{13}, p_{14}\}$ through $\{p_{n1}, p_{n2}, p_{n3}, p_{n4}\}$, respectively. These control feedback signal combinations are employed for model variable calculations. In cases where there are no OC switch faults, the $\{p_{n1}, p_{n2}, p_{n3}, p_{n4}\}$ are equal to $\{g_{n1}, g_{n2}, g_{n3}, g_{n4}\}$. However, they will not be equal if OC switch faults occur and are identified. Accordingly, some of $\{p_{n1}, p_{n2}, p_{n3}, p_{n4}\}$ are set as 0 to differentiate $\{g_{n1}, g_{n2}, g_{n3}, g_{n4}\}$. To distinguish the variables generated by $\{g_{11}, g_{12}, g_{13}, g_{14}\}$ through $\{g_{n1}, g_{n2}, g_{n3}, g_{n4}\}$ and $\{p_{11}, p_{12}, p_{13}, p_{14}\}$ through $\{p_{n1}, p_{n2}, p_{n3}, p_{n4}\}$, the following prerequisites are given.

1) The actual total output voltage u_{ab} is obtained by utilizing the driving signal combinations $\{g_{11}, g_{12}, g_{13}, g_{14}\}$ through $\{g_{n1}, g_{n2}, g_{n3}, g_{n4}\}$. On the other hand, the estimated total output voltage $\hat{u}_{\mathrm{ab}}$ is obtained utilizing the control feedback signal combinations, $\{p_{11}, p_{12}, p_{13}, p_{14}\}$ through $\{p_{n1}, p_{n2}, p_{n3}, p_{n4}\}$.
2) The actual total output voltage u_{ab} corresponds to the sum of all actual port voltages, i.e., $u_{\mathrm{ab}} = \sum_{i=1}^{n} u_i$. Similarly, the estimated total output voltage $\hat{u}_{\mathrm{ab}}$ is calculated as the sum of all estimated port voltages, i.e., $\hat{u}_{\mathrm{ab}} = \sum_{i=1}^{n} \hat{u}_i$.
3) The normalized forms of u_{ab} and $\hat{u}_{\mathrm{ab}}$ are defined as S_{ab} and $\hat{S}_{\mathrm{ab}}$, respectively. Specifically, S_{ab} is defined as the sum of actual port voltages divided by their respective dc-link voltages, as follows: $S_{\mathrm{ab}} = \sum_{i=1}^{n} (u_i/u_{\mathrm{dc}i}) = \sum_{i=1}^{n} S_i$, named as the actual total output level. Similarly, $\hat{S}_{\mathrm{ab}}$ is defined as the sum of estimated port voltages divided by their respective dc-link voltages: $\hat{S}_{\mathrm{ab}} = \sum_{i=1}^{n} (\hat{u}_i/u_{\mathrm{dc}i}) = \sum_{i=1}^{n} \hat{S}_i$, named as the estimated total output level. Here, S_1 to S_n and $\hat{S}_1$ to $\hat{S}_n$ represent the normalized forms of u_1 to u_n and $\hat{u}_1$ to $\hat{u}_n$, which are named as actual port levels and estimated port levels for power cells 1 to n, respectively.

Moreover, S_1 to S_n and $\hat{S}_1$ to $\hat{S}_n$ are normalized values that range from -1 to 1, since they are ratios of actual or estimated port voltages to the common dc-link voltage. S_{ab} and $\hat{S}_{\mathrm{ab}}$ are defined as the sum of the normalized port voltages, and thus, they are within the range of $[-n, n]$.

Here, the actual port level and the estimated port level S_n and $\hat{S}_n$ for the n power cell are taken as an example, then

$$\begin{cases} S_n = g_{n1}(1-x) + (1-g_{n2})x - g_{n3}x - (1-g_{n4})(1-x) \\ \hat{S}_n = p_{n1}(1-x) + (1-p_{n2})x - p_{n3}x - (1-p_{n4})(1-x) \end{cases} \tag{1}$$

where the variable x is defined as a logical variable [18] and the value of x belongs to $\{0, 1\}$. If $i_{\mathrm{sN}}>0$, then $x = 1$. Conversely, if $i_{\mathrm{sN}} < 0$, then $x = 0$.

For example, if $\{g_{n1}, g_{n2}, g_{n3}, g_{n4}\}$ and $\{p_{n1}, p_{n2}, p_{n3}, p_{n4}\}$ are both equal to $\{1,0,0,1\}$ and $i_{\mathrm{sN}}>0$, S_n and $\hat{S}_n$ are equal to 1 based on (1).

According to Fig. 1 and the Kirchhoff voltage law [2], the grid current deviation is obtained

$$\frac{\mathrm{d}i_{\mathrm{sN}}}{\mathrm{d}t} = -\frac{R_{\mathrm{N}}}{L_{\mathrm{N}}} i_{\mathrm{sN}} + \frac{1}{L_{\mathrm{N}}}(e_{\mathrm{N}} - S_{\mathrm{ab}} u_{\mathrm{dc}}). \tag{2}$$

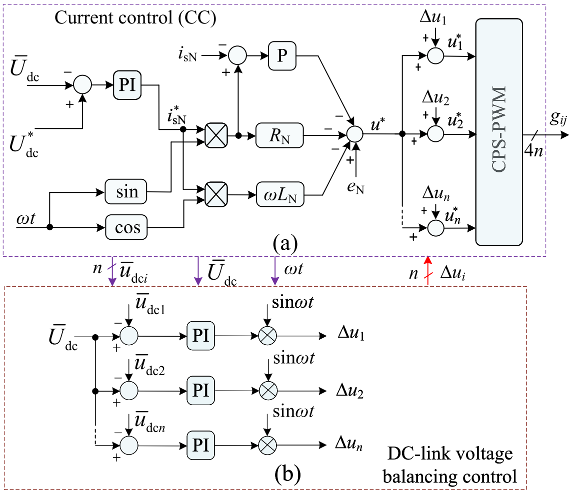


Fig. 2. PI-based control diagram of the (a) CC loop and (b) DC-link voltage balancing control loop [24], [25], [26].

Taking the discretization of the control system into account, based on (2), the actual grid current $i_{\mathrm{sN}}(k)$ and the estimated grid current $\hat{i}_{\mathrm{sN}}(k)$ at the k-instant are obtained by

$$\begin{cases} i_{\mathrm{sN}}(k) = (1 - \frac{R_{\mathrm{N}}T_{\mathrm{s}}}{L_{\mathrm{N}}})i_{\mathrm{sN}}(k-1) + \frac{T_{\mathrm{s}}}{L_{\mathrm{N}}}\{e_{\mathrm{N}}(k-1) \\ -S_{\mathrm{ab}}(k-1)u_{\mathrm{dc}}(k-1)\} \\ \hat{i}_{\mathrm{sN}}(k) = (1 - \frac{R_{\mathrm{N}}T_{\mathrm{s}}}{L_{\mathrm{N}}})i_{\mathrm{sN}}(k-1) + \frac{T_{\mathrm{s}}}{L_{\mathrm{N}}}\{e_{\mathrm{N}}(k-1) \\ -\hat{S}_{\mathrm{ab}}(k-1)u_{\mathrm{dc}}(k-1)\} \end{cases} \tag{3}$$

where T_s is the control loop period. $i_{\mathrm{sN}}(k-1)$, $u_{\mathrm{N}}(k-1)$, and $u_{\mathrm{dc}}(k-1)$ are the sampled values of the grid current, grid voltage, and dc-link voltage, respectively. $S_{\mathrm{ab}}(k-1)$ is the actual total output level at $(k-1)$ instant. $\hat{S}_{\mathrm{ab}}(k-1)$ is the estimated total output level based on (1) at $(k-1)$ instant. Note that achieving balanced dc-link voltages u_{dc1} to $u_{\mathrm{dc}n}$ is crucial both during normal operation and in the case of an OC switch fault occurrence. To address this concern, the current control (CC) strategy collaborates with the dc-link voltage balancing control, enabling both the unity power factor and balanced dc-link voltages operation of the CHBMC [24], [25], [26], as shown in Fig. 2. In the CC loop, the dc-link voltages u_{dc1} to $u_{\mathrm{dc}n}$ are filtered using second-order notch filters to obtain the dc-link voltage mean values, $\overline{u}_{\mathrm{dc1}}$ to $\overline{u}_{\mathrm{dc}n}$. The aggregate sum of $\overline{u}_{\mathrm{dc1}}$ to $\overline{u}_{\mathrm{dc}n}$, normalized by the system count n, gives rise to the average value of the dc-link voltage mean values, i.e., $\overline{U}_{\mathrm{dc}}$. Here, a reference for the dc-link voltage is defined as U^*_{dc}. The difference between $\overline{U}_{\mathrm{dc}}$ and U^*_{dc} is then fed into a proportional–integral (PI) controller for computing the grid current reference, i.e., i^*_{sN}. The resulting i^*_{sN} is further multiplied by sinωt and cosωt, respectively, being the active part fed into the current loop. Then, adding e_{N} generates the desired modulated voltage reference u^*.

Regarding the dc-link voltage balancing control loop, PI controllers address the deviation between $\overline{U}_{\mathrm{dc}}$ and the individual dc-link mean voltages ($\overline{u}_{\mathrm{dc1}}$ to $\overline{u}_{\mathrm{dc}n}$). Following this, the outputs of these controllers are added with u^* to obtain u^*_1 to u^*_n, which enter into the carrier phase shift pulsewidth modulation (CPS-PWM) block, yielding the driving signals essential for the balanced operation of the system under both normal and

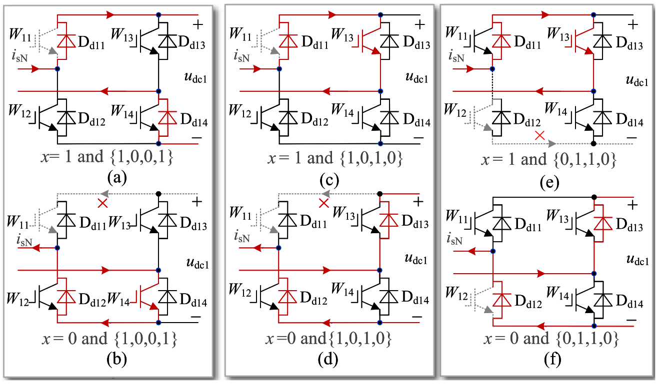


Fig. 3. Flow paths of the grid current under different driving signal combinations when the OC switch fault occurs in W_{11} and W_{12}: (a) $x = 1$ and $\{1,0,0,1\}$, (b) $x = 0$ and $\{1,0,0,1\}$, (c) $x = 1$ and $\{1,0,1,0\}$, (d) $x = 0$ $\{1,0,1,0\}$, and (e) $x = 1$ and $\{0,1,1,0\}$, and (f) $x = 0$ and $\{0,1,1,0\}$.

OC switch fault conditions. Consequently, unifying the dc-link voltages across the distinct H-bridges $u_{\mathrm{dc}1}$ to $u_{\mathrm{dc}n}$ into u_{dc}, as shown in (2) and (3), facilitates the process of fault modeling and diagnostic analysis hereinafter.

During practical operations, the current sensor directly samples $i_{\mathrm{sN}}(k)$, whereas $\hat{i}_{\mathrm{sN}}(k)$ is estimated using (3). If there is no OC switch fault at instant k, $\hat{S}_{\mathrm{ab}}$ will be equal to S_{ab}, and $i_{\mathrm{sN}}(k)$ will be equal to $\hat{i}_{\mathrm{sN}}(k)$. However, if an OC switch fault occurs at instant k, then $\hat{S}_{\mathrm{ab}}$ will not be equal to S_{ab}, causing a mismatch between $\hat{i}_{\mathrm{sN}}(k)$ and $i_{\mathrm{sN}}(k)$. Thus, the proposed diagnostic method for detecting and diagnosing OC switch faults based on this mismatch is described in the following sections.

A. OC Switch Fault Analysis

To clarify the OC switch fault possible conditions, one power cell is exemplified to discuss the OC switch fault criterion hereinafter.

Given that the actual port levels for a power cell are 1, 0, and -1, then the driving signal combination for the switches W_{11} to W_{14} are $\{1,0,0,1\}$, $\{1,0,1,0\}$/$\{0,1,0,1\}$, and $\{0,1,1,0\}$, respectively.

For the actual port level "1" with {1,0,0,1}: Assume that the OC switch fault occurs in the switch W_{11}, when $x = 1$, the generated actual port level "1" will not be affected, as shown in Fig. 3(a). Nevertheless, when $x = 0$, as shown in Fig. 3(b), the actual port level is changed from "1" to "0," which deteriorates the grid current quality. Similarly, if the OC switch fault occurs in the switch W_{14}, the actual port level keeps as "1" when $x = 1$. It will be changed from "1" to "0" when $x = 0$.

For the actual port level "0" with {1,0,1,0}: Assume that the OC switch fault occurs in the switch W_{11}, no change happens when $x = 1$, as shown in Fig. 3(c), whereas when $x = 0$, the actual port level is changed from "0" to "-1," which deteriorates the grid current quality, as shown in Fig. 3(d). A similar result holds for the other combination: $\{0,1,0,1\}$.

For the actual port level "-1" with {0,1,1,0}: Assume that the OC switch fault occurs in the switch W_{12}, when $x = 1$, the actual port level is changed from "-1" to "0," as shown in Fig. 3(e), which deteriorates the grid current quality. However, when $x = 0$, the generated actual port level "-1" is not affected, as shown in Fig. 3(f).

B. Fault Feature Variable Generation

As discussed before, when the OC switch fault occurs in a power cell, the actual total output level probably changes, resulting in a difference between the sampled grid current $i_{\mathrm{sN}}(k)$ and the estimated grid current $\hat{i}_{\mathrm{sN}}(k)$. This difference is defined as the grid current residual $E(k)$. Based on (3), $\hat{i}_{\mathrm{sN}}(k)$ is subtracted from $i_{\mathrm{sN}}(k)$ to obtain the grid current residual as follows:

$$\begin{aligned} E(k) &= i_{\mathrm{sN}}(k) - \hat{i}_{\mathrm{sN}}(k) \\ &= \frac{T_{\mathrm{s}}}{L_{\mathrm{N}}}\{[(\hat{S}_{\mathrm{ab}}(k-1) - S_{\mathrm{ab}}(k-1)]u_{\mathrm{dc}}(k-1)\}. \end{aligned} \tag{4}$$

According to (4), a fault feature variable D that includes the grid current residual is defined as

$$D = \frac{E(k)L_{\mathrm{N}}}{T_{\mathrm{s}}} = (\hat{S}_{\mathrm{ab}}(k-1) - S_{\mathrm{ab}}(k-1))u_{\mathrm{dc}}(k-1). \tag{5}$$

Since the actual total output level $S_{\mathrm{ab}} = S_1 + S_2 + \cdots + S_n$ is defined for the systems in Fig. 1, the fault feature variable $D = \sum_{i=1}^{n}\sum_{j=1}^{4} D_{ij} \in [-2nu_{\mathrm{dc}}, 2nu_{\mathrm{dc}}]$ can be derived by the sum of the respective fault feature variables D_{11} to D_{n4} when the OC switch fault occurs in the respective switches of power cells 1 to n.

For the respective fault feature variables, assuming that the OC switch fault occurs in switches W_{n1} to W_{n4} for the power cell n, then the corresponding signals g_{n1} to g_{n4} are seen as equal to 0. Hence, for the power cell n, based on (1) and (5), the respective fault feature variables D_{n1} to D_{n4} are expressed by:

$$D_{n1} = p_{n1}(1-x)u_{\mathrm{dc}}(k-1) \tag{6a}$$

$$D_{n2} = -p_{n2}xu_{\mathrm{dc}}(k-1) \tag{6b}$$

$$D_{n3} = -p_{n3}xu_{\mathrm{dc}}(k-1) \tag{6c}$$

$$D_{n4} = p_{n4}(1-x)u_{\mathrm{dc}}(k-1). \tag{6d}$$

In order to distinguish the OC switch faults for the CHBMC, a threshold value T_{th} is set as $0.7U_{\mathrm{dc}}^{*}$ by considering mismatches in the grid model parameters R_{N} and L_{N}, random noise, and sampling errors [20]. When D exceeds the threshold value, i.e., $0.7U_{\mathrm{dc}}^{*}$, the OC switch fault occurs in the system. Hence, an OC switch fault condition is satisfied if $D > T_{\mathrm{th}}$ and $x = 0$, or $D < -T_{\mathrm{th}}$ and $x = 1$. The next step is to find out the specific OC switches based on the OC logic judgment.

C. OC Logic Judgment Process

To analyze the condition of the OC switch fault, a carrier-based modulation and the generation process of the switch driving signals for the CHBMC are shown in Fig. 4. In Fig. 4, M_1 and M_2 are calculated within the control loop period of 50 μs, then sent to the enhanced pulsewidth modulation (EPWM) module, and updated either in the maximum or the minimum value of the carriers [27], as shown in the "sampling starts" and the "updated point" of Fig. 4. The distance between two adjacent

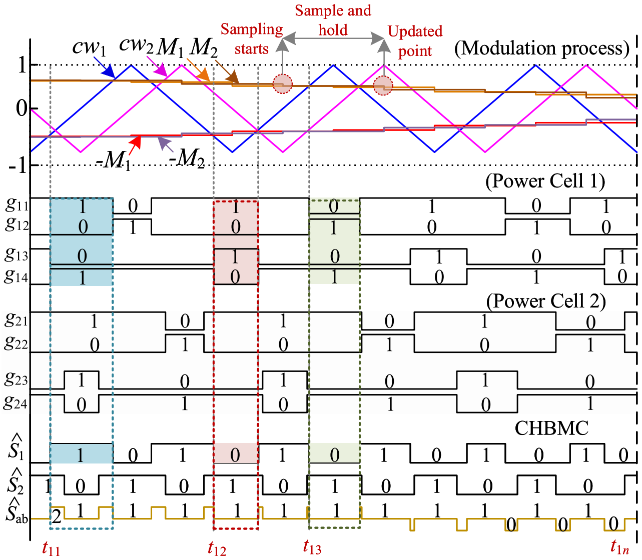


Fig. 4. Carrier-based CPS-PWM process.

updated points is the sample and hold period. The driving signals are generated by the comparison between the cw_1, cw_2 and M_1, M_2. The values of $\hat{S}_1$, $\hat{S}_2$, and $\hat{S}_{\text{ab}}$ are alternatively changed from time instant t_{11} to t_{1n}, which is used to discuss the following OC switch fault diagnosis process. For example, when the OC switch fault occurs in W_{11} for the power cell 1, the conditions under $x = 0$, $\hat{S}_1 = 1$, and $\{g_{11}, g_{12}, g_{13}, g_{14}\}$=$\{1,0,0,1\}$ are assumed at t_{11}. In this assumption, based on Fig. 2(b), the grid current flow path will be changed. Accordingly, $\{g_{11}, g_{12}, g_{13}, g_{14}\}$ can be seen as $\{0,0,0,1\}$ to change the actual port level from "1" to "0." Nevertheless, the signal combination $\{p_{11}, p_{12}, p_{13}, p_{14}\}$ is equal to $\{1,0,0,1\}$ at this instant. According to (3) and (4), the grid current residual is generated to yield the fault feature variable D_{11} based on (6a). Accordingly, D_{11} is equal to D. Similarly, when W_{14} is in OC state, D_{14} is generated by the grid current residual. Hence, the conditions when W_{11} and W_{14} are in OC state are identified.

To distinguish the OC state between switches W_{11} and W_{14}, the modulation process shown in Fig. 4 is utilized. When the modulation process moves from t_{11} to t_{12}, the estimated port level $\hat{S}_1$ is equal to 0, and the state of $\{g_{11}, g_{12}, g_{13}, g_{14}\}$ is $\{1,0,1,0\}$. At this point, the actual value of g_{11} is not the same as that of g_{14}, leading to p_{11} being unequal with p_{14}, which helps to distinguish whether switch W_{11} or W_{14} is in an OC state. Furthermore, if an OC fault occurs in switches W_{12} or W_{13}, (6b) and (6c) are used to differentiate the OC fault in switches W_{12} or W_{13} from that in switches W_{11} or W_{14}, as the polarity of the respective fault feature variable D_{12} or D_{13} is different from that of D_{11} or D_{14}. Based on Fig. 3 and the aforementioned discussion for switches W_{11} and W_{14}, the OC states of switches W_{12} and W_{13} in power cell 1 can also be distinguished. Once the OC fault condition is met, the diagnosis process is started using an OC logic judgment and counters, which correspond to each switch in the system. To clarify the diagnosis process, counters c_{im} and c_{ih} are defined to represent the states of switches W_{im} and W_{ih} in power cell i, where $m = 1$ or 4 and $h = 2$ or 3. These counters directly indicate the corresponding OC state of the switch. If the OC switch fault conditions described previously are met, the values of the corresponding counters are changed as per incremented or decremented modes, respectively. The values of c_{im} and c_{ih} are given by the following discussion.

Under the incremented mode:

If $D(k) > T_{\text{th}}$ and $x(k) = 0$, the value of the counter c_{im} at $(k+1)$ instant is increased as

$$c_{im}(k+1) = c_{im}(k) + 1, \text{ if } \{\hat{S}_i(k) = 1 \parallel [\hat{S}_i(k) = 0 \& p_{im}(k) = 1]\}. \tag{7}$$

If $D(k) < -T_{\text{th}}$ and $x(k) = 1$, the counter c_{ih} at $(k+1)$ instant is incremented as

$$c_{ih}(k+1) = c_{ih}(k) + 1, \text{ if } \{\hat{S}_i(k) = -1 \parallel [\hat{S}_i(k) = 0 \& p_{ih}(k) = 1]\} \tag{8}$$

where $c_{im}(k)$, $c_{ih}(k)$, and $c_{im}(k+1)$, $c_{ih}(k+1)$ are defined counters at k and k+1 instants.

Under the decremented mode:

If $D(k) > T_{\text{th}}$, the value of the counter c_{im} at $(k+1)$ instant is decreased as

$$c_{im}(k+1) = c_{im}(k) - 1, \text{ if } \{\hat{S}_i(k) = -1\}. \tag{9}$$

If $D(k) <$-T_{th}, the value of the counter c_{ih} at $(k+1)$ instant is decreased as

$$c_{ih}(k+1) = c_{ih}(k) - 1, \text{ if } \{\hat{S}_i(k) = 1\}. \tag{10}$$

Based on (7)–(10), the subscript of the switch is the same as that of the counter, in which the maximum value represents the OC switch. To identify OC switch faults in CHMBC in real time using the counters, three cases are considered.

Case I—The OC switch fault in a power cell (n = 1): To illustrate the case where an OC switch fault occurs in a power cell, consider an example in which an OC fault occurs in switches W_{11} and W_{13} such that $D(k) > T_{\text{th}}$. Suppose the following conditions are satisfied simultaneously at instant k: $c_{11}(k) = 0$, $c_{13}(k) = 0$, $x = 0$, and the output voltage level $\hat{S}_1(k) = 1$ with $\{p_{11}, p_{12}, p_{13}, p_{14}\}$=$\{1,0,0,1\}$ at t_{11}. Then, using (7), $c_{11}(k+1) = c_{11}(k) + 1 = 1$, $c_{14}(k+1) = c_{14}(k) + 1 = 1$, and $c_{13}(k+1) = 0$ at instant $k+1$. Therefore, at this instant, switches W_{11} and W_{14} are potentially the OC fault switches.

When the instant moves to t_{12}, i.e., $\hat{S}_1(k) = 0$ with $\{p_{11}, p_{12}, p_{13}, p_{14}\}$=$\{1,0,1,0\}$, $c_{11}(k+2) = c_{11}(k+1) + 1 = 2$, and $c_{14}(k+2)$ remains as 1. Therefore, switch W_{11} is identified as the OC fault switch. After diagnosing the OC switch fault in W_{11}, the control feedback signal p_{11} is permanently set as 0, and all the counters are initialized as 0.

Subsequently, when the estimated port level $\hat{S}_1$ is equal to 0 with $\{p_{11}, p_{12}, p_{13}, p_{14}\}$=$\{0,0,1,0\}$, $D(k) <$-T_{th} and $x = 1$, according to (8), $c_{13}(k+1) = c_{13}(k) + 1 = 1$, while other counters remain at 0. Thus, switch W_{13} is also diagnosed as an OC fault switch.

Case II—The OC switch fault in different power cells (n = 2): The same criterion is used to diagnose an OC switch fault in different power cells, i.e., two power cells, similar to the Case I. To clarify, consider another example where OC switch faults occur in W_{11} and W_{21} for power cells 1 and 2, satisfying the conditions $D(k) > T_{\text{th}}$. Assuming that $x = 0$, $\hat{S}_1$ and $\hat{S}_2$ are both equal to 1 with control feedback signals {1,0,0,1}. At time instant k, counters c_{11}, c_{14}, c_{21}, and c_{24} begin counting with $c_{11}(k+1) = c_{11}(k) + 1 = 1, c_{14}(k+1) = c_{14}(k) + 1 = 1,\ c_{21}(k+1) = c_{21}(k) + 1 = 1,$ and $c_{24}(k+1) = c_{24}(k) + 1 = 1$. The remaining counters maintain a value of 0, indicating that W_{11}, W_{14}, W_{21}, and W_{24} are potentially in an OC state.

Suppose that the control feedback signals of $\hat{S}_1$ and $\hat{S}_2$ are changed to {1,0,1,0} and {0,1,1,0} when $D(k) > T_{\text{th}}$ and $x(k) = 0$. Counters $c_{11}(k+2) = c_{11}(k+1) + 1 = 2$, $c_{14}(k+2) = c_{14}(k+1) = 1$, $c_{21}(k+2) = c_{21}(k+1) - 1 = 0$, and $c_{24}(k+2) = c_{24}(k+1) - 1 = 0$ are obtained based on (9) at k+2 instant. The maximum value of c_{11} at this instant identifies that W_{11} is one of the OC fault switches. After diagnosing the OC fault switch in W_{11}, the control feedback signal p_{11} is permanently set to 0, and the values of all counters are reset to 0 within a control loop period, i.e., k+3 instant.

Moreover, during the operation of the system and the modulation process, at k+4 instant, assume that the control feedback signals of $\hat{S}_2$ are changed to {1,0,1,0} and $\hat{S}_1$ keeps {0,0,1,0}. If x remains equal to 0 at k+4 instant, then using (7) and (9), $c_{21}(k+4) = c_{21}(k+3) + 1 = 1$, $c_{11}(k+4) = c_{11}(k+3) - 1 = -1$, and $c_{14}(k+4) = c_{14}(k+3) - 1 = -1$. The values of the other counters remain at 0, indicating the maximum value of c_{21}. Consequently, W_{21} is diagnosed as the OC fault switch. Therefore, the criterion proposed is still applicable for the CHBMC with two power cells (i.e., $n = 2$).

Case III—The OC switch fault in different power cells (n>2): This case explores the suitability of the proposed OC switch fault diagnostic method for CHBMCs with more than two power cells, using a CHBMC with three power cells as an example. Assuming that W_{14} in power cell 1, W_{24} in power cell 2, and W_{32} in power cell 3 are in OC state and setting counters c_{11} to c_{34} to 0. If, at a particular instant k, the conditions $D(k) > T_{\text{th}}$, $x = 0$, and $\hat{S}_1(k) = 0$ with $\{p_{11}, p_{12}, p_{13}, p_{14}\} = \{0, 1, 0, 1\}$, $\hat{S}_2(k) = 0$ with $\{p_{21}, p_{22}, p_{23}, p_{24}\} = \{1, 0, 1, 0\}$, and $\hat{S}_3(k) = -1$ with $\{p_{31}, p_{32}, p_{33}, p_{34}\} = \{0, 1, 1, 0\}$ are all fulfilled, $c_{32}(k+1) = c_{32}(k) = 0$ is obtained, and $c_{14}(k+1) = c_{14}(k) + 1 = 1$ and $c_{21}(k+1) = c_{21}(k) + 1 = 1$ have two bigger values than the rest of the counters based on (7) to (10). According to the criterion, no identification is behaved at this control loop period. The OC switch fault identification is entered into the next control loop period, i.e., k+2 instant.

At k+2 instant, if the control feedback signals of $\hat{S}_1$, $\hat{S}_2$, and $\hat{S}_3$ are modified as: {0,1,0,1}, {0,1,1,0}, and {0,1,1,0}. $c_{14}(k\text{+}2) = c_{14}(k+1) + 1 = 2$ has the maximum value based on (7). $c_{21}(k\text{+}2)$ is equal to $c_{21}(k+1) - 1 = 0$ based on (9). Hence, W_{14} is identified as the first switch to have an OC fault. p_{14} is set to 0 with all counters reset to 0. Following the identification of W_{14} as the first switch with an OC fault, the next step is to change the conditions to $\hat{S}_2(k+3) = 0$ with $\{p_{21}, p_{22}, p_{23}, p_{24}\} = \{0, 1, 0, 1\}$, while assuming $\hat{S}_1(k+3) = -1$ with {0,1,0,0} and $\hat{S}_3(k+3) = -1$ with {0,1,1,0}. With respect to this change, the maximum value of 1 is obtained in counter $c_{24}(k\text{+}3)$. Hence, W_{24} is also identified as having an OC fault. The final switch, W_{32}, can be diagnosed in a similar manner. Therefore, The proposed OC switch fault diagnostic method is shown to be independent of cell number and is suitable for the CHBMC with higher levels and more power cells in practical applications.

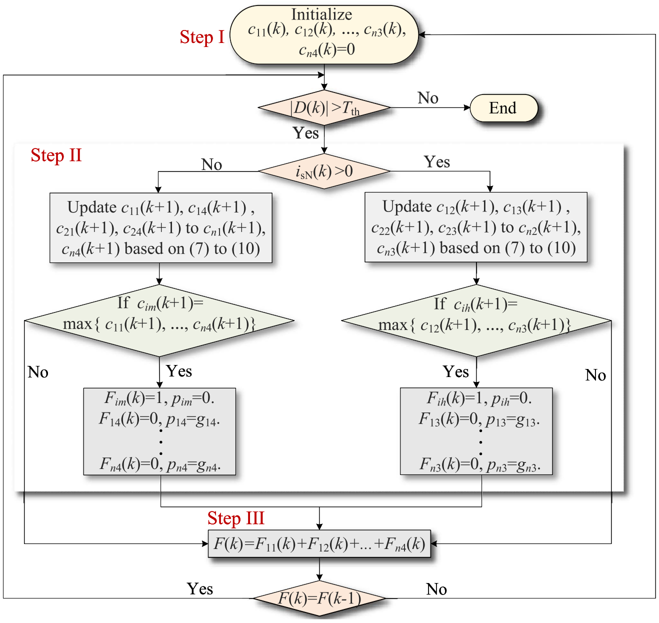


Fig. 5. Flowchart of the proposed method.

In terms of counters c_{11} to c_{n4}, each switch corresponding to a fault is marked using F_{11} to F_{n4}. The total diagnostic mark F is simply the sum of all individual marks. For instance, if c_{11} has the highest value, a mark of 1 is given to F_{11}, and p_{11} is changed to 0. Under the condition of $F(k) \neq F(k-1)$, the proposed method is restarted and all the counters are set as 0.

To summarize, a flowchart of the proposed method is shown in Fig. 5, which includes three steps. In step I, the introduced counters $c_{11}(k)$, $c_{12}(k)$,..., $c_{n4}(k)$ are initialized. Based on the absolute value of $D(k)$, i.e., $|D(k)|$, the proposed counters execute the fault diagnostic process is detailed in Step II, that is: If $|D(k)| > T_{\text{th}}$ and $x = 0$, the counters c_{11}, c_{14}, c_{21}, c_{24} to c_{n1}, c_{n4}, which satisfies the conditions based on (7) to (10), will be updated and start to count. It will be divided into two cases.

1) If there exists a counter whose value is maximum, the corresponding fault mark is set from 0 to 1 for visually identifying the OC switch, in which other fault marks are kept at 0. Accordingly, the control feedback signal is reset as 0 and kept constant. Eventually, the total diagnostic mark $F(k)$ is equal to 1, as shown in Step III. It should be noted that all the counted counters are reset when $F(k)$ is not equal to $F(k-1)$ to restart the new round of counting.
2) If the values of two or more than two counters are maximum to result in $F(k) = F(k-1)$, all the counters will keep counting at the next control period.

For example, if $|D(k)| > T_{\text{th}}$ and $x = 0$ is satisfied at k instant, given that c_{11} gets the maximum value among all the counters based on (7) to (10), the fault mark F_{11} is equal to 1, and other fault marks are kept at zero to identify the switch W_{11} in the OC

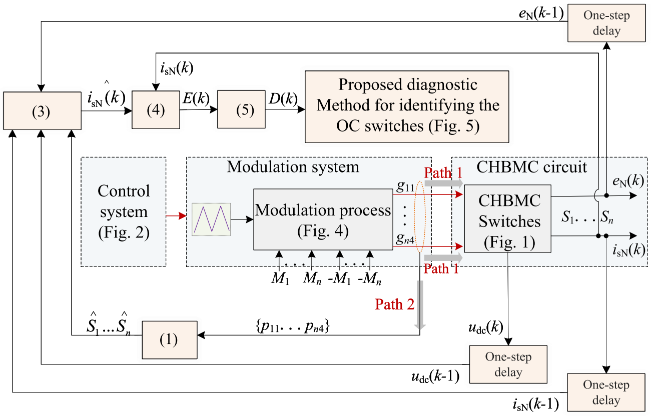


Fig. 6. Overall CHBMC system block diagram.

state. Accordingly, the control feedback signal p_{11} is set as 0 so that the estimated port level $\hat{S}_1$ is equal to the actual port level S_1 based on (1). This process enables $|D(k)|<T_{\text{th}}$ to end the OC fault diagnosis for the switch W_{11}. Eventually, according to Step III, the value of the total fault mark $F(k)$ is equal to F_{11}, i.e., which resets all the counters by the condition: $F(k) \neq F(k-1)$ to have other OC switches identified at the next control period, as shown in Fig. 5. Regarding the case 2) hereinbefore, given that the values of c_{11} and c_{24} get simultaneous maximization, in this case, $F(k)$ is equal to $F(k-1)$. All the fault marks are kept as zero to result that $F(k)$ is equal to 0. Hence, the values of all the counters continuous to count based on the previous values at the next control period. Similar analysis holds for the conditions: $|D(k)|>T_{\text{th}}$ and $x = 1$.

According to Fig. 5, the overall CHBMC system is shown in Fig. 6. The control system block (see Fig. 2) feeds the modulation system block (see Fig. 4) that generates the driving signals $g_{11}...g_{n4}$ to the CHBMC circuit whether the OC switch faults occur or not, and then to output the actual port levels S_1 to S_n. Note that the physical transmission of the driving signals $g_{11}...g_{n4}$ is done through Path 1; however, this path is used to generate a second path, i.e., Path 2, as shown in Fig. 6. In this path, the driving signals $g_{11}...g_{n4}$ are renamed as the control feedback signals $p_{11}...p_{n4}$, respectively, to obtain estimated port levels $\hat{S}_1$ to $\hat{S}_n$ based on (1). Furthermore, the grid current $\hat{i_{\text{sN}}}(k)$ at k instant is estimated according to (3). The actual grid current $i_{\text{sN}}(k)$ is measured at k instants, and then the grid current residual $E(k)$ and the fault feature variable $D(k)$ are obtained, based on (4) and (5), respectively. The fault feature variable D is sent to the proposed method, as shown in Fig. 5, to identify the OC switch fault for the corresponding switch. Accordingly, the control feedback signal corresponding to the OC switch is set to 0 before entering the OC switch fault diagnostic process at the next instant. During this entire process, the modulation process remains independent of the OC switch fault diagnostic process, with the exception that the switch driving signals are fed back into the proposed OC switch fault diagnostic method, as shown in Fig. 6.

According to the aforementioned discussion, the proposed method is applicable for identifying the OC switch fault in a power cell, two power cells, and more than power cells without increasing the computational burden.

III. Verification and Comparative Results

A. Simulation Results

To verify the proposed method, the CHBMC system is simulated in MATLAB/Simulink. The simulation parameters are: $L_{\text{N}} = 3$ mH, $R_{\text{N}} = 0.1\ \Omega$, $U_{\text{dc}}^* = 100$ V, $C_{\text{dc1}} = C_{\text{dc2}} = C_{\text{dc3}} = 2.8$ mF, and $R_{\text{dc1}} = R_{\text{dc2}} = R_{\text{dc3}} = 20\ \Omega/40\ \Omega$. In addition, the control loop period T_s is 50 μs, the switching frequency is 1 kHz, and the grid voltage frequency is 50 Hz.

1) OC Switch Fault Occurring in a Power Cell ($n = 1$) Scenario: Fig. 7(a) simulates the fault diagnostic process when the OC switch fault occurs in W_{11} and W_{13} for a power cell. During a control period, i.e., 50 μs from t_0 to t_1, the value of the counter c_{13} is equal to 1, which is maximum than other counters to activate the fault mark F_{13} as 1. This process helps visually identify W_{13} in the OC state. Accordingly, the control feedback signal p_{13} is set as 0 to remove the current residual generated by W_{13}. Since $F(k) = 1$ is not equal to $F(k-1) = 0$ at t_1, all the counters are reset to enter the new fault diagnostic process at the next instant. After a couple of control periods, at t_2, c_{11} reaches 1, while other counters kept at zero to activate F_{11} equal to 1, which visually shows that W_{11} is in OC state. Subsequently, the control feedback signal p_{11} is set as 0 to reset the fault feature variable D_{11}. The diagnostic result accords with the theory described in Case I in Section II-C.

2) OC Switch Fault Occurring in Two Power Cells ($n = 2$) Scenario: The proposed OC switch fault diagnostic method is executed in the CHBMC with two power cells, as shown in Fig. 7(b). Before t_1, the values of c_{11} and c_{24} start to increase based on (7). At t_1, the values of c_{11} is prompted to be maximum to trigger F_{11} so that the OC state of W_{11} is identified. After several control periods, i.e., at t_{21}, c_{21} get the maximum value among all the counters to trigger F_{21}. Hence, the OC state of W_{21} is identified as well. The diagnostic result accords with the theory described in Case II in Section II-C.

3) OC Switch Fault Occurring in More Than Two Power Cells ($n>2$) Scenario: Fig. 8 depicts how to diagnose the multiple OC switches for the CHBMC with more than two power cells (i.e., $n = 3$). As shown in Fig. 8(a), before t_0, all the counters and fault marks are initialized. At conditions: $|D(k)|>T_{\text{th}}$ and $x = 1$ are satisfied, c_{23} and c_{33} start to count based on (8). c_{33} reaches its maximum value at t_1 to trigger F_{33} at this instant. After this control period, p_{33} is set as 0 and all the counters are initialized again. At t_2, the count condition is satisfied again to enable c_{12} maximum so that F_{12} is triggered and p_{12} is set as 0. Hence, W_{12} and W_{33} are identified as OC states eventually. Similar with Fig. 8(a), when more than two OC switches W_{14}, W_{24}, and W_{32} occur in power cells 1, 2, and 3, as shown in Fig. 8(b) to satisfy the conditions in (7)–(10), W_{14} is firstly identified as OC state at t_1, and the identification of the OC state in W_{24} is closely following. At t_3, F_{32} is triggered since c_{32} gets the maximum value at this instant. The whole process takes approximately 7.45 ms. The diagnostic result accords with the theory described in Case III in Section II-C. Regarding the

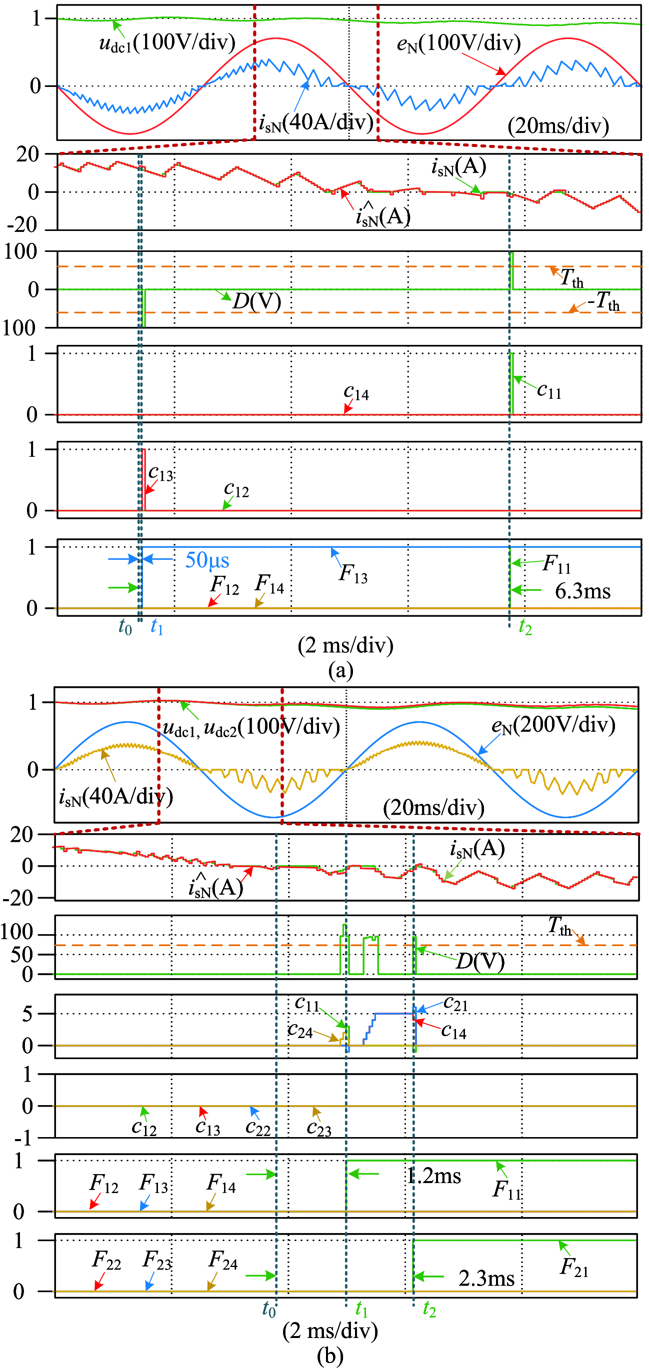


Fig. 7. Simulation results of the OC fault diagnosis of different switches for the CHBMC. In power cell 1: (a) Switches W_{11} and W_{13}. In different power cells: (b) Switches W_{11} and W_{21}.

aforementioned verification results, the proposed method is valid for the CHBMC with higher power cells, which highlights its practical application value.

B. Experimental Results

Fig. 9 shows a scale-down setup used to verify the effectiveness of the proposed method in a power cell and different power cells, respectively. The model parameters are listed on the right-hand side of Fig. 9. The rest of electrical parameters are identical with the simulation parameters.

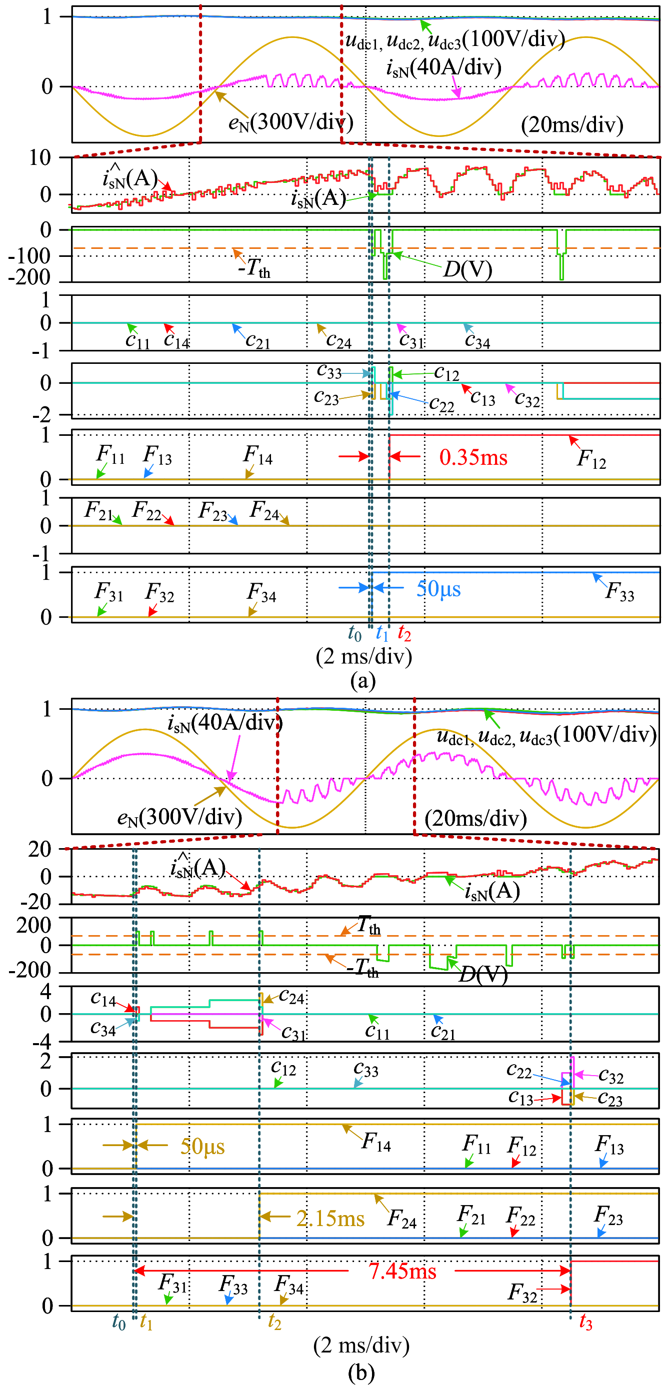
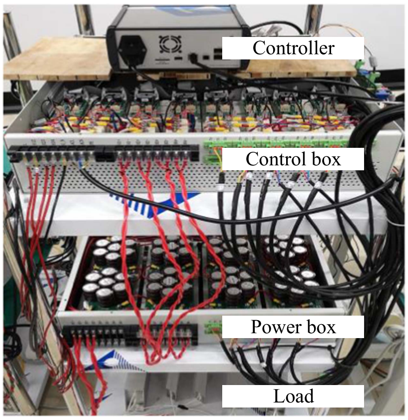


Fig. 8. Simulation results of the OC fault diagnosis of different switches for the CHBMC. In different power cells: (a) Switches W_{12} and W_{33}. In different power cells: (b) Switches W_{14}, W_{24}, and W_{32}.

Fig. 10(a) shows the fault diagnostic process when the OC fault occurs in W_{11} and W_{13} in a power cell. Prior to t_0, the estimated current $\hat{i}_{sN}$ is almost equal to i_{sN}. When the OC fault is triggered, i.e., $F_t = 1$, and the distorted actual current appears at t_0, the counters begin to count based on (8). At t_1 instant, the fault feature variable D is smaller than the negative threshold



(a)

Model:

Digital controller:
RT-Box 1

Control box:
Sampling circuits
Drive circuits
(IGBT devices:
FF75R12RT4)

Power box:
Grid-side inductor
DC-link capacitors
(Load:
DC-link Resistors)

(b)

Fig. 9. Experimental setup and model parameters. (a) Experimental setup. (b) Model parameters.

value, i.e., $-0.7U^*_{\mathrm{dc}}$, and the counter c_{13} is changed to 1. The other counters keep zero. Hence, the OC fault occurs in the corresponding switch W_{13}. The diagnostic mark F_{13} is changed to 1 simultaneously. Subsequently, a step change is enabled in the counter c_{11} and F_{11} to identify the OC fault of W_{11} at t_2 instant within 4.8 ms. Fig. 10(b) shows the OC fault occurs in W_{11} and W_{14} for instance. The counters c_{14} and c_{11} begin to count at t_1 and t_2 instants, respectively. Meanwhile, the diagnostic marks F_{14} and F_{11} increase to 1 to identify the OC switch faults of W_{14} and W_{11} successively.

Furthermore, the fault diagnosis results of the OC fault switches in different power cells are demonstrated in Fig. 11(a) and (b), in which, W_{11} and W_{21}, and W_{12} and W_{23} are shown as OC faulty switches in power cells 1 and 2. The counters c_{11} and c_{21} reach maximum values to enable the fault marks F_{11} and F_{21}, see Fig. 11(a). Similar results are presented in Fig. 11(b) to demonstrate the effectiveness of the proposed method.

Fig. 12 shows the degrees of parameter mismatches, i.e., $(R_{\mathrm{N}}/R_{\mathrm{N0}})$ and $(L_{\mathrm{N}}/L_{\mathrm{N0}})$ versus the per-unit value of $|D|$ under the normal and OC switch fault conditions, where R_{N} and L_{N} indicate the actual resistance and inductance. R_{N0} and L_{N0} are the values in the control system. Based on Fig. 12, from mismatched degrees of ±50% of grid impedance in (3) and under the normal condition, the per-unit values of D are below the per-unit value of T_{th}, i.e., 0.7. Under the OC switch fault condition, the per-unit values of D are larger than 0.7 to identify the OC switch fault, which demonstrates strong robustness of the proposed method against impedance parameters mismatch in the grid model.

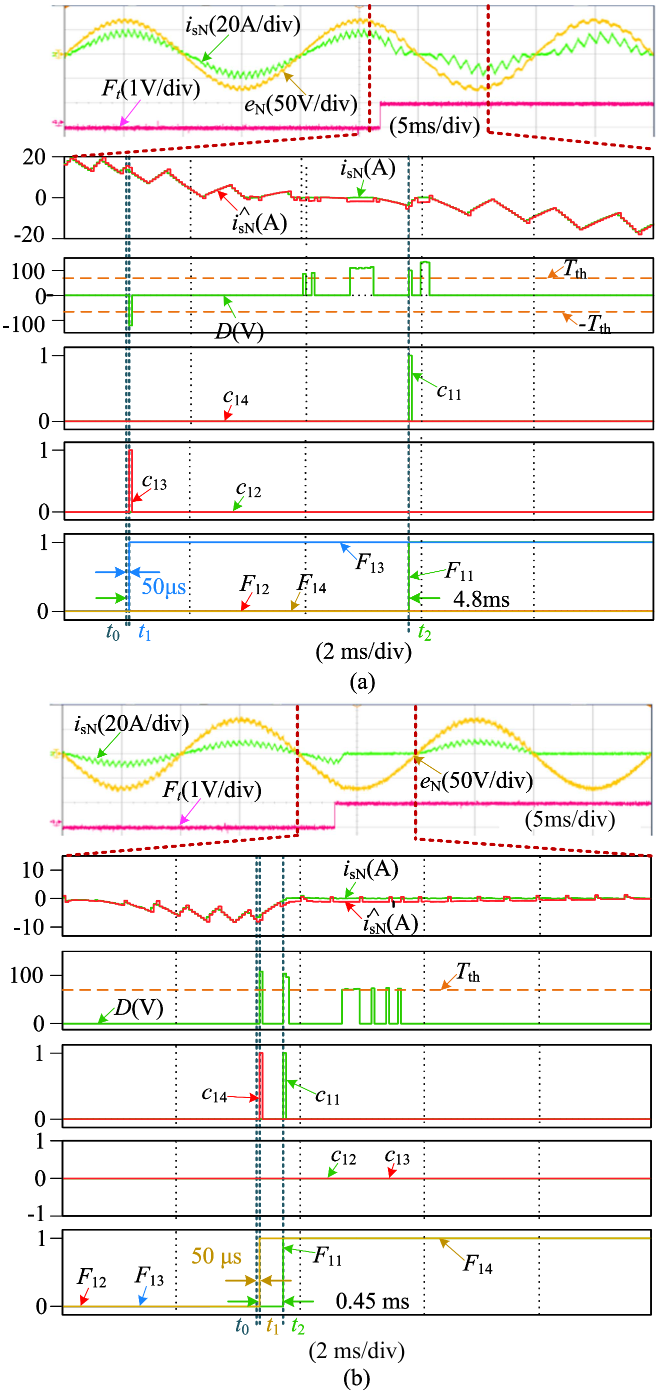
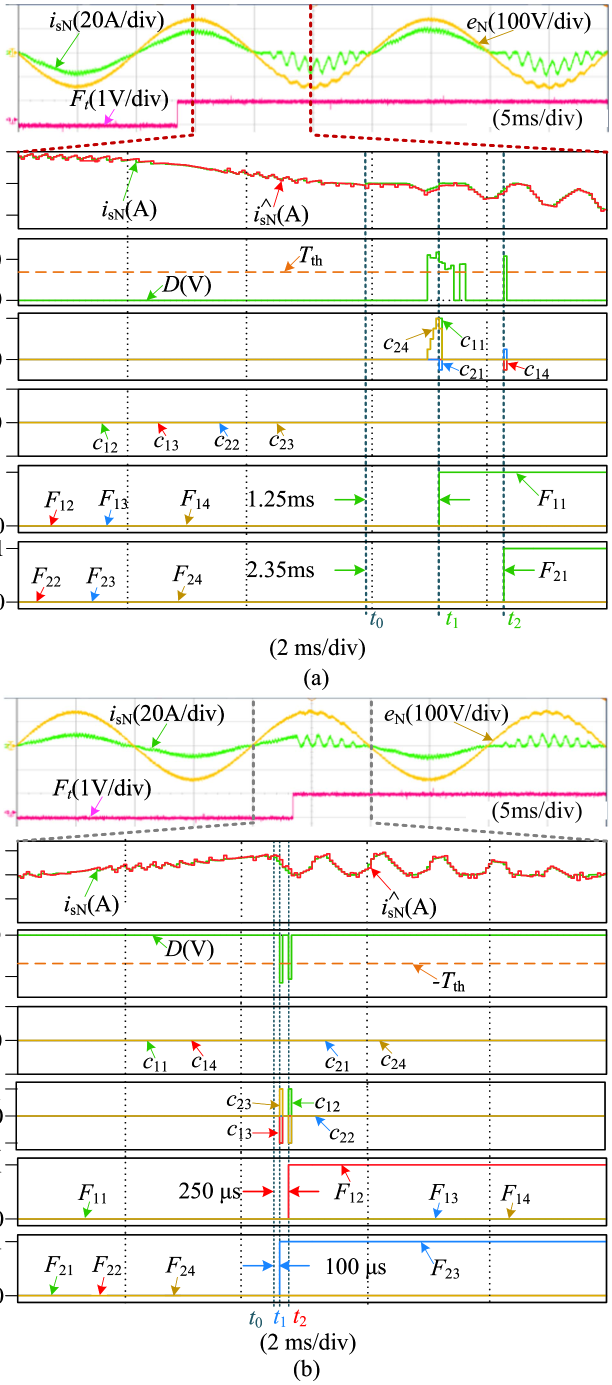


Fig. 10. Experimental results of the OC fault diagnosis of different switches for the CHBMC. In power cell 1: (a) Switches W_{11} and W_{13}, and (b) switches W_{11} and W_{14}.

C. Comprehensive Comparative Results

Fig. 13 depicts the fault diagnostic time versus fault diagnostic scenarios corresponding to the OC switch faults in Figs. 8, 10, and 11. Since the proposed method is level-independent, the OC faults of multiple switches in two power cells and more than two power cells are identified within 8 ms, which highlights the diagnostic speed of the proposed method.

Suppose that W_{11} and W_{21} are in OC state in different power cells for the CHBMC. Without extra sensors, the methods in [20] and [21] have similar diagnostic performance with the proposed method. In order to make a fair comparison, Fig. 14 shows that the methods in [20] and [21], and the proposed method diagnosing the OC switches during a fundamental period are compared by OC switch fault diagnostic time versus fault occurring time.



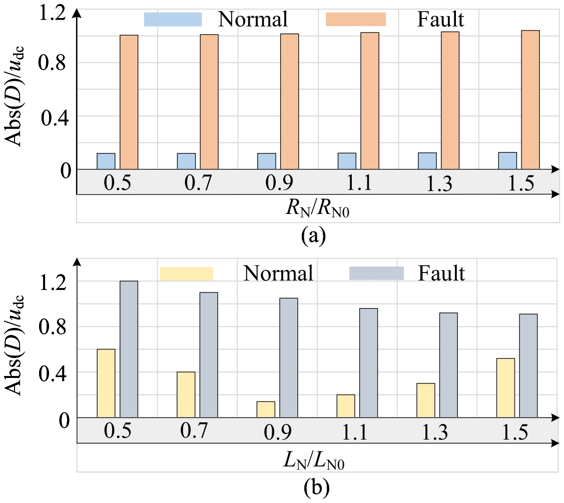
(a)

(b)

Fig. 11. Experimental results of the OC fault diagnosis of different switches for the CHBMC. In different power cells: (a) Switches W_{11} and W_{21}, and (b) switches W_{12} and W_{23}.

According to Fig. 14, the proposed method exhibits the shortest fault diagnostic time than the other two methods.

Comparative results between the proposed method and the state-of-the art methods are given in Table I. For the diagnostic range, the methods in [14], [18], and [22] fail to diagnose multiple OC switch faults. The methods in [16], [20], [21], and [23], and the proposed method succeed in diagnosing multiple OC switch faults within the similar diagnostic time, respectively.



(a)

(b)

Fig. 12. Per-unit value of D effected under different mismatched parameters: (a) R_N/R_{N0} and (b) L_N/L_{N0}.

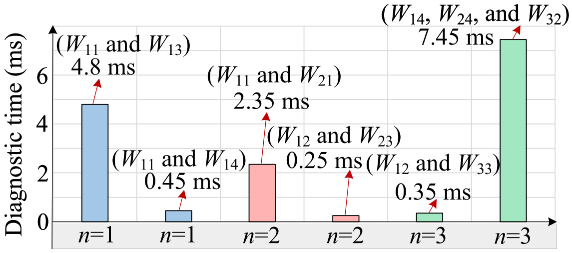


Fig. 13. Diagnostic time under different OC switch faults.

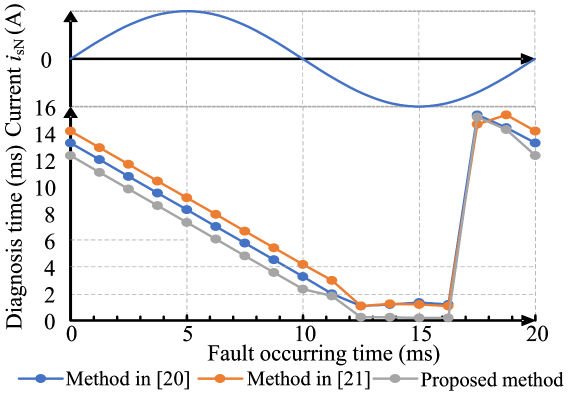


Fig. 14. Diagnostic time versus OC switch fault occurring time.

For complexity, the methods in [14], [18], and [20] require long fault feature extraction time, extra comparisons, and residual detection operations. The method in [22] requires to assume and verify the potential faulty switches, and the method in [23] requires to acquire the switching transient and change the modulation process, which increases the computational burden. In addition, the methods in [16], [22], and [23] require extra sensors and multiple thresholds. Also, the method in [21] needs multiple iterated detection matrices. Compared with the above methods,

TABLE I
COMPARISON RESULTS BETWEEN THE PROPOSED METHOD AND THE STAT-OF-THE-ART METHODS

Methods	Diagnostic range and time	Extra sensors	Algorithm feature
[14]	Single: $<2T_f$	-	(Long fault feature extraction time)
[16]	Single or Multiple: $<(3/4)T_f$	√	(Diagnostic logics with multiple thresholds)
[18]	Single: $<(1/4)T_f$	-	(Comparison of voltage and current residual)
[20]	Single: $<(1/4)T_f$ Multiple: $<(3/4)T_f$	-	(Dual current residuals -based detection)
[21]	Single: $<(1/4)T_f$ Multiple: $<T_f$	-	(Multiple iterated detection matrices)
[22]	Single: $<(1/4)T_f$	√	(Assumption and verification of potential faulty switches)
[23]	Single: $<(1/4)T_f$ Multiple: $<T_f$	√	(Switching transient acquisition and modulation change)
Proposed	Single: $<(1/4)T_f$ Multiple: $<(3/4)T_f$	-	(Simple counter with one threshold)

T_f: Fundamental current cycle. √ and - indicate "Required" and "Not required".

the proposed method exhibits the simplest criterion based on several counters and one threshold.

IV. CONCLUSION

A counter-based OC switch fault diagnostic method for the CHBMC is proposed in this article. A simple yet effective logical criterion to identify the corresponding OC switches demonstrates that the counters can be used to identify the OC switch fault position. The extension of the OC switch fault from one power cell to the rest of power cell is proposed, allowing to tackle multiple OC switch faults in the CHBMC. The proposed method is level-independent, and helps to identify the OC switch faults in a power cell, two power cells, and more than two power cells without increasing the computational burden. Finally, these features and merits have been confirmed by experimental and comparative results.

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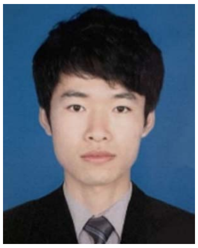

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