# A Compact Single-Phase Cascaded Three-Level AC/DC Converter With Variable DC Bus Voltage and Low CM Noise

Yuanbin He, *Member, IEEE*, Hao Liu, Junjie Zhang, Chenyu Shen, Xiaogao Xie, *Senior Member, IEEE*, and Lijun Hang, *Senior Member, IEEE*

***Abstract*—This article proposes a new topology technology of a two-stage ac/dc converter with variable dc bus voltage control. The technology is a cascaded combination of a new type of single-inductor-based cascaded three-level totem-pole power-factor-correction (PFC) circuit and a three-level *LLC* half-bridge converter. Although the existing variable dc bus voltage control strategy based on a two-level ac/dc converter exhibits better overall efficiency than fixed dc bus control, it faces problems such as high withstand voltage stress of the power semiconductor device and large inductance volt-second product and filter volume. In order to address these issues, a novel cascaded three-level ac/dc converter with 600 V withstand voltage devices and phase-shift modulation technology is proposed. The new single-inductor-based mirror-symmetric cascaded three-level totem-pole PFC can achieve low common-mode electromagnetic interference without relying on impedance balance. As verification of the proof-of-concept, a hardware prototype of a scale-down 1 kW ac/dc converter is developed. The experimental results show that the converter can operate in an ultrawide battery terminal voltage range of 220–420 V, with a peak efficiency of 96.35%, and a power density of 28% higher than the traditional two-level converter.**

***Index Terms*—AC/DC converter, charger, common-mode (CM), variable dc bus voltage.**

## I. Introduction

In terms of electric vehicle charging applications, the two-stage ac/dc converter is mainly composed of a power-factor-correction (PFC) circuit and an isolated dc/dc conversion circuit [1], [2]. The rear stage is usually a Boost-type PFC or a bridgeless totem-pole PFC, and the poststage is an *LLC* converter or a bidirectional *CLLLC* converter. In view of the higher efficiency of bridgeless totem-pole PFC, it has become the mainstream topology of single-phase PFC. Since single-phase bridgeless totem-pole PFC has a boost function, the dc bus voltage is generally regulated at a constant dc bus voltage, 400 V, for applications with an input voltage of 220 Vrms [3]. In this case, due to a wide range of changes in the battery terminal voltage, such as an ultrawide range of changes from 250 to 450 V or even wider, the poststage dc/dc converter needs to change its own voltage gain accordingly to adapt to the battery terminal voltage. This requires the *LLC* converter to be equipped with an ultrawide range of voltage regulation capabilities [4]. Therefore, when designing the parameters of the *LLC* converter, the inductor ratio ($L_m/L_r$) and quality factor (Q) of the resonant tank need to be weighed carefully to meet the needs of wide voltage gain [5]. This will bring two problems. First, in the constant current (CC) or constant power (CP) charging mode, the *LLC* often operates in the range of under-resonance, and the larger reactive current will reduce the power efficiency of the converter; second, when the *LLC* converter performs pulse-frequency-modulation (PFM) operation, an ultrawide change of switching frequency will indirectly increase the volume of the output filter and reduce the power density of the converter.

In view of the problems of the above-mentioned constant dc bus voltage control scheme, since the year of 2014, some scholars have studied variable dc bus voltage control schemes for two-stage ac/dc converters. Variable dc bus voltage control means that the dc bus voltage value is changed through the prestage PFC, thereby alleviating the voltage regulation stress of the poststage *LLC* circuit. According to the range of variable dc bus voltage, it is mainly divided into two types of variable dc bus voltage control strategies:

1) small-range changes in the dc bus voltage (e.g., 400–450 V for single phase) [6], [7], [8], [9];
2) wide-range changes in the dc bus voltage by following the battery terminal voltage (e.g., 500–840 V for single phase) [10], [11], [12], [13], [14], [15], [16].

The former is mainly based on the allowable voltage stress range of a 600 V switching device. Adjust the dc bus voltage in a small range, thereby reducing the voltage regulating stress of the poststage *LLC* circuit. This method has limited help in improving system efficiency and power density [12]. Therefore, scholars pay more attention on the study of the wide-range variable dc bus voltage control strategy. As shown in Fig. 1, the poststage *LLC* converter is basically only regarded as a dc

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The authors are with the Hangzhou Dianzi University, Hangzhou 310018, China (e-mail: yuanbinhe@hdu.edu.cn; 925537059@qq.com; 947041633@qq.com; 1224464067@qq.com; xiexg@hdu.edu.cn; lijunhang.hhy@aliyun.com).

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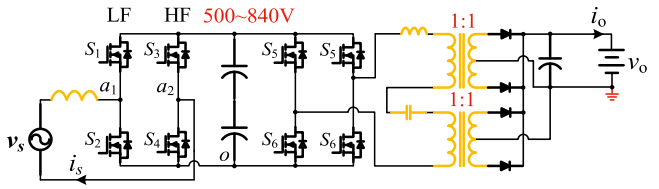


Fig. 1 Traditional single-phase two-stage two-level AC/DC converter with variable DC bus voltage regulation and split transformers.

transformer (DCX) and operates near the switching frequency. Even if the *LLC* converter sometimes needs to suppress the double line-frequency ripple at the battery terminal, it only performs a very small range of PFM operations [11]. The authors in [12] comprehensively analyze and verify the power efficiency of a two-level ac/dc converter with different dc bus voltage levels. The corresponding dc bus voltage control range is recommended to be 500–840 V for the application of the battery terminal voltage 250–450 V. The converter architecture with wide-range variable dc bus voltages has been proven to increase system efficiency by 1%–2%, but it requires dc bus voltage support of up to more than 800 V [12]. Therefore, two-level converters under wide-range variable dc bus voltage control require 1200 V switching devices, which not only increase the cost of switching devices and magnetic devices but also limit the increase in system power density due to the higher inductance volt-second product and larger filter volume.

In order to meet the needs of converters for high efficiency and high power density, multilevel conversion technology has always been favored due to its advantages of low voltage stress and small inductance volt-second product [17], [18], [19]. Recently, the power density of the flying capacitor-based and cascaded multilevel PFC converter has been increased to 1000 W/in$^3$ in the laboratory [18], [19] while achieving a peak efficiency of more than 99%. However, the flying capacitor multilevel circuit needs to precharge (PC) the flying capacitor at startup to ensure the voltage-stress balance of each switching device, which reduces the reliability of the circuit [20]. In contrast, cascaded multilevel topologies are favored because of their higher modularity and expandability. Nevertheless, there is serious common-mode (CM) circulation between the dc buses and conducted electromagnetic interference noise problems in the cascaded multilevel topology [21], [22], [23]. The authors in [21] utilize the mirror-bridge phase-shift modulation and impedance balancing principle to suppress the CM noise of cascaded multilevel PFC circuits, but this depends on the overall balance of the circuit.

This article aims to study a cascaded three-level ac/dc converter based on a variable dc bus voltage structure. To the knowledge of the authors, there has been no research on this topic so far. In this article, a novel two-stage cascaded three-level ac/dc converter with variable dc bus voltage control is proposed. The converter consists of a single-inductor-based cascaded three-level totem-pole PFC and *LLC* DCX. It employs an input series and output parallel architecture. The proposed three-level ac/dc converter has the following advantages.

1) The switching ripple of the input and output currents is eliminated by the phase-shift modulation of the PFC and LLC, thereby reducing the volume of the differential-mode filter.
2) The new type of cascaded three-level PFC circuit can eliminate CM noise and CM circulation without relying on impedance balance.
3) It has high efficiency, high power density, and ultrawide output voltage regulation capability.

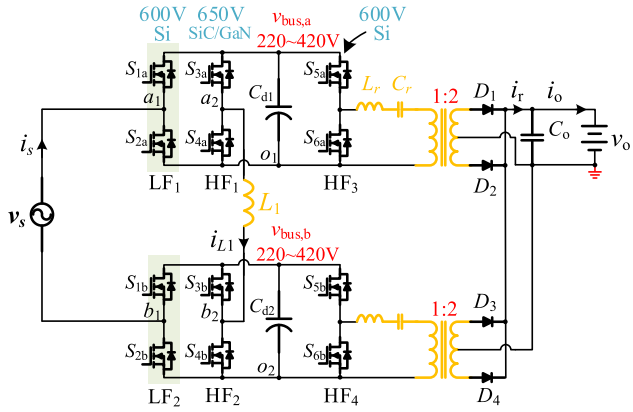


Fig. 2. Proposed single-phase two-stage cascaded three-level AC/DC converter with variable DC bus voltage regulation.

Therefore, the proposed topology meets the needs of high efficiency and high power density for electric vehicle charging applications. Section II will introduce the proposed converter topology, calculate its input and output current ripple, analyze the CM noise suppression ability of the PFC circuit, and present the corresponding variable dc bus voltage control strategy. Section III will compare the differences in main cost, volume, and power loss between the proposed three-level topology and the existing two-level topology. Then, Section IV verifies the advantages of the new topology in the above aspects. Finally, a summary is made in Section V.

## II. Novel Cascaded Three-Level AC/DC Converter

The proposed topology of the two-stage cascaded three-level ac/dc converter based on variable dc bus voltage control is given in Fig. 2. In Fig. 2, the midpoints of the two line-frequency half-bridges ($LF_1$, $LF_2$) on the PFC side are directly connected to both ends of the ac power supply, and the midpoints of the high-frequency half-bridges ($HF_1$, $HF_2$) in the two units are cascaded through one inductor. Silicon (Si) devices of 600 V are used for PFC line-frequency bridge arms, while either Si, silicon carbide (SiC), or gallium nitride (GaN) devices can be used for *LLC* high-frequency bridge arms ($HF_3$, $HF_4$). From an efficiency perspective, SiC and GaN are preferred due to smaller switching losses; conversely, from a cost point of view, Si device is preferred. For PFC high-frequency bridge arms, wide bandgap devices such as SiC or GaN should be chosen. The dc bus voltage tracks the range of changes in the battery terminal voltage, such as 220–420 V, and the turns ratio of the transformers is 1:2. The cascade bridge arms of the new PFC structure perform 180° phase-shift modulation, while the two *LLC* half-bridge converters perform 90° phase-shift modulation.

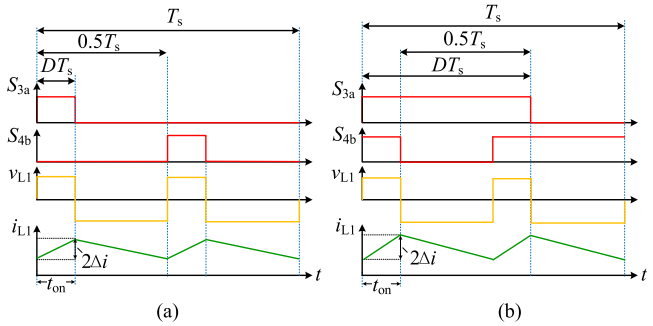


Fig. 3. Key waveforms of three-level PFC. (a) $0 < D \leq 0.5$. (b) $0.5 < D \leq 1$.

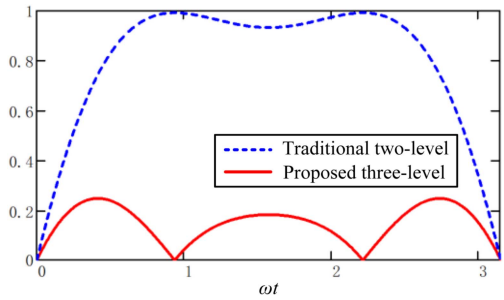


Fig. 4. Normalized inductor current ripple comparison between the proposed three-level PFC and the traditional two-level PFC.

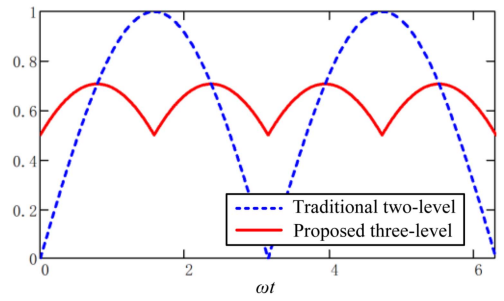


Fig. 5. Normalized rectified output current waveform comparison between the cascaded three-level *LLC* and two-level *LLC*.

### A. *Input and Output Current Ripple Analysis*

According to Kirchhoff's voltage law, the voltage on the PFC inductor $L_1$ of the proposed topology in Fig. 2 is expressed as

$$v_{L1} = v_{a_2a_1} - v_{b_2b_1} + v_s \tag{1}$$

where $v_{a_2a_1}$ and $v_{b_2b_1}$ represent the voltage across $a_2$ and $a_1$ and the voltage across $b_2$ and $b_1$, respectively.

Combining (1) with the switching state, the waveforms of the voltage across the PFC inductor and the inductor current in a switching cycle are plotted in Fig. 3, where $T_s$ is the switching cycle, $D$ means the duty cycle ratio of switches, and $t_{\rm on}$ represents the switch ON time. Taking a positive half-line cycle as an example, $v_{a_2a_1}$ and $v_{b_2b_1}$ during the time interval $t_{\rm on}$ is calculated as

$$v_{a2a1} = v_{a2o1} - v_{a1o1} = 0 \tag{2a}$$

$$v_{b2b1} = v_{b2o2} - v_{b1o2} = \begin{cases} \mathrm{V}_{\rm bus,b} & D \in (0, 0.5) \\ 0, & D \in (0.5, 1) \end{cases}. \tag{2b}$$

To facilitate the calculation of inductance current ripple, assume that both the dc bus voltages of the two cascaded PFCs equal $V_{\rm bus}$. Then, by substituting (2) into (1), the inductance current ripple formula is calculated as

$$\Delta i_{L_1}(\omega t) = \begin{cases} \frac{[v_s(\omega t) - V_{\rm bus}] \cdot D(\omega t) \cdot T_s}{2L_1}, & \text{if } 0 \leq D(\omega t) \leq 0.5 \\ \frac{v_s(\omega t) \cdot [D(\omega t) - 0.5] \cdot T_s}{2L_1}, & \text{if } 0.5 < D(\omega t) \leq 1 \end{cases} \tag{3}$$

where $L_1$ means the PFC inductance, $\omega$ represents the angular line frequency, and

$$\begin{cases} v_s(\omega t) = V_m \cdot |\sin \omega t| \\ D(\omega t) = 1 - \frac{v_s(\omega t)}{2V_{\rm bus}} \end{cases}. \tag{4}$$

Likely, the inductance current ripple formula of the traditional two-level totem-pole PFC can be calculated as

$$\Delta i'_{L_1}(\omega t) = \frac{v_s(\omega t) \cdot D(\omega t) \cdot T_s}{2L_1}. \tag{5}$$

In order to fairly compare the inductor current ripple, the two-level PFC and the cascaded three-level PFC are thought to work at the same voltage boost ratio. Since the cascaded three-level PFC is composed of two two-level PFCs in series, the dc bus voltage of the two-level PFC is twice that of the three-level PFC under the same voltage boost ratio, and the duty-cycle expression in (5) can still be expressed in (4). Thus, the normalized inductance current ripple curve of the proposed cascaded three-level PFC and the traditional two-level PFC with the same inductance is drawn, as shown in Fig. 4. As can be seen from the figure, the inductance current ripple of the cascaded three-level PFC is much smaller than that of the two-level PFC. The maximum inductance current ripple of the cascaded three-level PFC is only one-fifth of the two-level PFC.

In Fig. 2, the two *LLC* half-bridge converters perform 90° phase-shift modulation, and the secondary side of the transformers is connected in parallel through diodes. Assuming that the operating frequency of the *LLC* converter equals the resonant frequency, each rectified output current exhibits a sinusoidal half-wave shape. For the proposed cascaded three-level ac/dc conversion circuit in Fig. 2, the expression of the *LLC* rectified output current is

$$i_r(\omega_r t) = \frac{I_{om}}{2}\left[\sin(\omega_r t) + \sin\left(\omega_r t + \frac{\pi}{2}\right)\right] \tag{6}$$

where $\omega_r$ means the *LLC* resonance angular frequency and $I_{om}$ represents the amplitude of the rectified output current.

Likely, for the traditional two-level ac/dc converter, the rectified output current is

$$i'_r(\omega_r t) = I_{om} \sin(\omega_r t). \tag{7}$$

According to (6) and (7), the normalized *LLC* rectified output current waveform can be plotted, as shown in Fig. 5. Due to the phase-shift modulation technology, the switching ripple of the

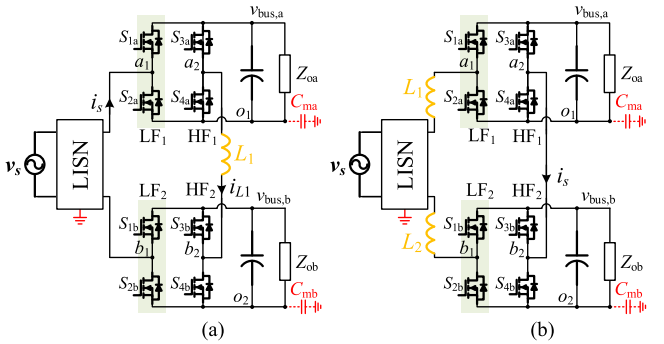


Fig. 6. Simplified PFC circuit with LISN and parasitic capacitance. (a) Proposed single-inductor-based topology. (b) Traditional split-inductor-based topology.

*LLC* rectified output current is much smaller than that of the traditional two-level *LLC*.

Based on the above analysis, the input and output current switching ripple of the new cascaded three-level ac/dc converter based on variable dc bus voltage control is much smaller than that of the traditional two-level ac/dc converter. Therefore, the input and output filtering elements required for the three-level converter are smaller, which is more conducive to improving the power density of the system.

### B. CM Analysis of the Proposed PFC

In order to facilitate the analysis of the CM characteristics of the proposed single-inductor-based cascaded three-level PFC topology, Fig. 2 is simplified to Fig. 6(a). In the figure, the line-impedance stabilization network (LISN) represents the line impedance stabilization network, and $Z_{oa}$ and $Z_{ob}$ represent the equivalent output load impedance, respectively. $C_{ma}$ and $C_{mb}$ mainly include the coupling capacitor between the dc bus and ground, the parasitic capacitor between the primary side and the secondary side of the *LLC* transformer, and an additional Y capacitor practically placed between the negative dc bus terminal and negative output terminal of the dc/dc converter for the alleviation of CM noise [21], [24]. The value of capacitances $C_{ma}$ and $C_{mb}$ could be hundreds of picofarads or even several nanofarads [21]. In contrast, the parasitic capacitance between the midpoints of high-frequency bridge arms and ground is much smaller [25], so it is ignored in Fig. 6.

To facilitate the CM analysis, the line-frequency bridge arms $LF_1$ and $LF_2$ are equivalent to the corresponding line-frequency square wave noise sources $v_{a1o1}$ and $v_{o2b1}$, and the high-frequency bridge arms $HF_1$ and $HF_2$ are equivalent to the corresponding high-frequency square wave noise sources $v_{o1a2}$ and $v_{b2o2}$. Based on that, the CM equivalent circuit of the new single-inductor-based three-level CHB-PFC is drawn, as shown in Fig. 7, where $Z$ is the equivalent impedance of the linear impedance stabilization network. Fig. 7 contains multiple CM noise sources, which are coupled to each other and act on the LISN impedance $Z$. In order to facilitate the analysis of CM noise, the current response of the high-frequency noise sources

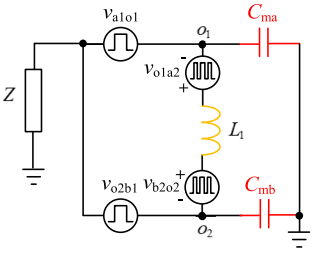


Fig. 7. CM equivalent circuit of the proposed PFC.

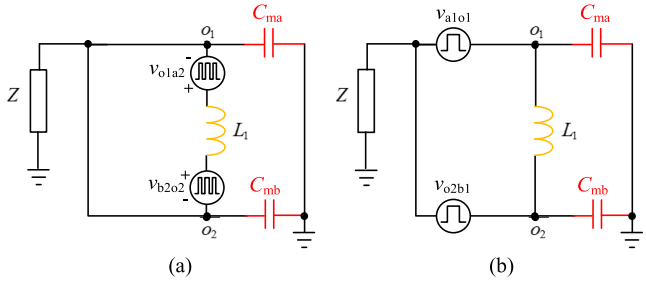


Fig. 8. Decomposed CM equivalent circuit of the proposed PFC. (a) Equivalent circuit for high-frequency noise sources. (b) Equivalent circuit for line-frequency noise sources.

and the line-frequency noise sources is solved separately according to the principle of circuit superposition. The decomposed CM equivalent circuit is shown in Fig. 8. Fig. 8(a) is the CM equivalent circuit corresponding to the high-frequency noise sources. Since $o_1$ and $o_2$ are shorted, the current response of the high-frequency noise sources $v_{o1a2}$ and $v_{b2o2}$ acting on the LISN impedance $Z$ is zero. In Fig. 8(b), the line-frequency noise sources can be expanded into the following Fourier expression:

$$v_{a1o1}(t) = \frac{V_{\text{bus}}}{2} + \frac{2V_{\text{bus}}}{\pi}\sum_{n=1}^{\infty}\frac{\sin(0.5n\pi)}{n}\cos(n\omega t) \tag{8a}$$

$$v_{o2b1}(t) = -\frac{V_{\text{bus}}}{2} + \frac{2V_{\text{bus}}}{\pi}\sum_{n=1}^{\infty}\frac{\sin(0.5n\pi)}{n}\cos(n\omega t) \tag{8b}$$

where $n = 1, 3, 5, \ldots$.

Thus, by using the loop current method, the current response expression of the line-frequency noise source acting on the LISN impedance $Z$ can be derived as

$$i_{\text{cm}}(t) = \sum_{n=1}^{\infty}\gamma_i(\lambda)\sin(n\omega t + \varphi) \tag{9}$$

in which the amplitude of the CM current is

$$|\gamma_i(\lambda)| = \frac{2|\lambda| C_{ma} V_{\text{bus}}\omega}{\pi\sqrt{(2+\lambda)^2 C_{ma}^2 Z^2 n^2\omega^2 + 1}} \tag{10}$$

where $\lambda$ is the deviation rate of parasitic capacitance and $\lambda = \left(\frac{C_{mb}}{C_{ma}} - 1\right)$.

Since the above amplitude in (10) decreases as the frequency increases, we only need to pay attention to the amplitude of the CM current at the lowest odd frequency, such as 150.05 kHz in

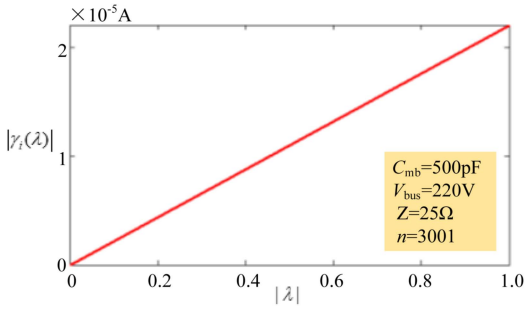


Fig. 9. Relationship curve of the CM current amplitude $|\gamma_i(\lambda)|$ at the frequency of 150.05 kHz relative to the deviation rate λ for the proposed PFC.

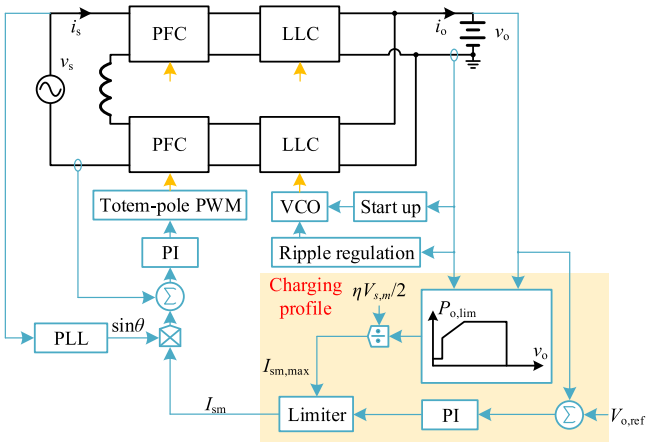


Fig. 10. Schematic diagram of variable DC bus voltage control based on the proposed AC/DC converter.

the CM test frequency range. The relationship curve of the CM current amplitude relative to the deviation rate is plotted in Fig. 9. It is seen that when the parasitic capacitances $C_{ma}$ and $C_{mb}$ are equal, the CM current $i_{\rm cm}$ becomes zero. Even if a significant deviation exists, the response of line-frequency noise sources acting on the LISN is very small. Thus, the proposed single-inductor-based three-level CHB-PFC topology has a strong CM noise suppression ability without relying on impedance balance. Conversely, the traditional split-inductor-based PFC topology as shown in Fig. 6(b) relies on symmetrical PWM modulation and impedance balance to suppress CM interference [22].

### C. Two-Stage Control Strategy

Fig. 10 shows the variable dc bus voltage control scheme proposed in this article, where the poststage *LLC* circuit is mainly responsible for soft start and double line-frequency ripple elimination. The mean switching frequency of *LLC* is set at the resonance frequency. By extracting the double line-frequency ripple information of the output current and using it to adjust the voltage gain of the *LLC* in a small range, the effective suppression of the double line-frequency ripple can be achieved. As for the prestage PFC circuit, it is mainly responsible for battery charging control and power factor adjustment. Among them, the charging control defines the amplitude of PFC input current reference $I_{\rm sm}$ according to the charging profile module. The charging profile includes PC, CC, CP, and constant voltage (CV) charging modes. Based on the charging current requirement of PC, CC, and CP charging modes, calculate the corresponding charging power command ($P_{\rm o,lim}$), thereby indirectly obtaining the PFC input current reference limit ($I_{\rm sm,max}$), which is also the output limit of the battery voltage control.

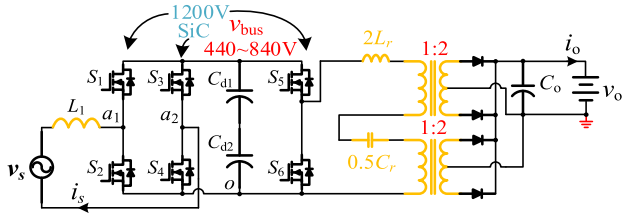


Fig. 11. Traditional two-level AC/DC converter used for comparison.

Since the mean switching frequency of *LLC* equals the resonance frequency, the average voltage gain of the *LLC* circuit remains the same. Thus, the dc bus voltage follows the battery voltage change. The proposed variable dc bus voltage control scheme does not require direct adjustment of the two dc bus voltages. Moreover, since the entire system is an input-in-series and output-in-parallel architecture, there is no need for *LLC* current sharing control.

It should be noted that the bandwidth of the battery voltage loop in CV charging mode should be designed much lower than the PFC current loop to meet the requirements of dual closed-loop regulation, thereby ensuring stable operation. For *LLC* double line-frequency ripple elimination control, since it only affects the adjustment of 100Hz current ripple, it basically does not affect the PFC-stage control. Referring to the design process in [26], full control parameters are designed and tabulated in Table II.

As can be seen from Fig. 10, the proposed ac/dc converter control strategy is simple and easy to implement.

## III. Comparative Studies

This section will compare the proposed three-level converter with the existing two-level converter in terms of cost, volume, and power loss. The poststage dc/dc circuit in the traditional two-level ac/dc converter adopts a half-bridge *LLC* circuit with split transformers, as shown in Fig. 11, where the parameter value of passive elements in the *LLC* circuit part is the same, as in Fig. 2. The operating principle of the poststage *LLC* in Fig. 11 is consistent with the proposed three-level converter, mainly for start-up control and double line-frequency ripple suppression. Therefore, the dc bus voltage varies between 440 and 840 V, and the switching devices used on the primary side of the transformers are all 1200 V SiC MOSFETs in Fig. 11.

Table I lists the comparison of the key parameters of the proposed three-level converter with the existing two-level converter. Prioritizing circuit cost, the switches of *LLC* high-frequency bridge arms of the new topology adopt Si MOSFETs. Fig. 12 shows the comparison results of the corresponding volume and cost. As can be seen from Fig. 12(a), the proposed three-level

TABLE I
KEY PARAMETERS OF THE AC/DC CONVERTERS

| Topology | Name | Symbol | Values |
|---|---|---|---|
| Proposed three-level | Primary-side switches | $LF_1$, $LF_2$ | Si, 600 V, 99 mΩ |
| | | $HF_1$, $HF_2$ | SiC, 650 V, 80 mΩ |
| | | $HF_3$, $HF_4$ | Si, 600 V, 89 mΩ |
| | PFC input inductance | $L_1$ | 600 μH |
| | Output capacitance | $C_o$ | 20 μF |
| Traditional two-level | Primary-side switches | $S_1$~$S_6$ | SiC, 1200 V, 160 mΩ |
| | PFC input inductance | $L_1$ | 2200 μH |
| | Output capacitance | $C_o$ | 200 μF |
| Both topologies | Secondary-side diodes | $D_1$~$D_4$ | SiC, 650 V, 1.35 V |
| | Magnetizing inductance | $L_m$ | 140 μH |
| | Resonant inductance | $L_r$ | 31.5 μH |
| | Resonant capacitance | $C_r$ | 80 nF |
| | DC-link capacitance | $C_{d1}$, $C_{d2}$ | 470 μF |

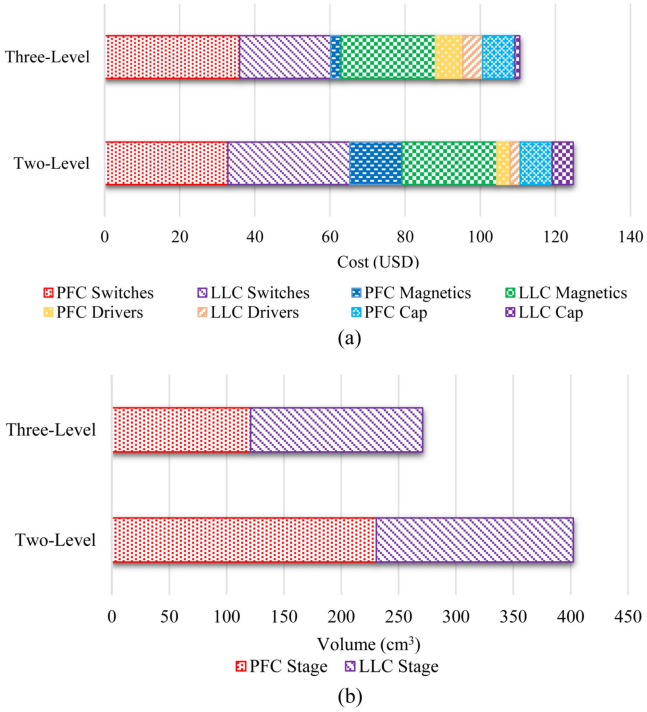


Fig. 12. Comparison of component cost and volume between the proposed three-level topology and the traditional two-level topology. (a) Cost comparison. (b) Volume comparison.

converter is about 10% lower in key costs than the existing two-level converter, which is mainly due to the reduction in the cost of the three-level PFC inductor. In terms of total volume, as shown in Fig. 12(b), due to the use of lower withstand voltage Si devices, smaller PFC inductor, and smaller LLC output-side filter capacitors, the proposed three-level converter reduces the total volume by 30%.

In terms of power loss, the losses of PFC and LLC are evaluated separately. The specific main loss calculation can be found in the Appendix. The loss calculation, especially the loss of switching devices, is based on the premise of thermal stability. According to the thermal management analysis in [9] and [27]

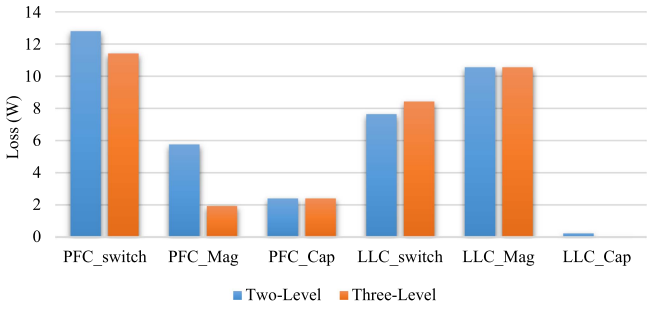


Fig. 13. Loss breakdown of the proposed three-level topology and the conventional two-level topology at $v_o = 320$ V, $P_o = 1$ kW.

TABLE II
KEY PARAMETERS IN THE EXPERIMENTS

| Parameter | Value |
|---|---|
| Rated output power | 1 kW |
| Input voltage | 220 Vrms/50 Hz |
| Output DC voltage | 220–420 V |
| Switching frequency of PFC | 50 kHz |
| Resonant frequency of *LLC* | 100 kHz |
| Turn ratio of the transformers | 1:2.1 |
| PFC inner current loop | PI controller: $K_p = 7$, $T_i = 0.0003$ |
| PFC outer voltage loop | PI controller: $K_p = 0.3$, $T_i = 0.005$ |
| *LLC* ripple regulation loop | PI controller: $K_p = 0.1$, $T_i = 0.005$<br>Bandwidth of Bandpass filter: 20 Hz |

and the evaluated loss of switching devices, in our case study, the heatsink is used to dissipate heat from switches. On this basis, Fig. 13 shows the power loss comparison results of the proposed three-level topology with the existing two-level topology at the output voltage $V_o = 320$ V and full load. As can be seen from the figure, due to the use of lower withstand voltage switching devices and smaller PFC inductors, the proposed cascaded three-level PFC topology loss is significantly smaller than the traditional two-level PFC. On the dc/dc converter side, the main loss difference lies in the loss of the primary-side switching devices and the conduction loss of the output capacitor but the difference between them is small. Therefore, in terms of overall power loss, the proposed three-level topology is smaller than the existing two-level topology.

Based on the above comparative analysis, the proposed three-level ac/dc converter not only can adapt to an ultrawide battery voltage range but can also have a higher efficiency and power density than the existing two-level topology.

## IV. EXPERIMENTAL RESULTS

The top-view prototype photos of the proposed three-level converter and the traditional two-level converter are shown in Fig. 14. From the perspective of power density, the new topology is about 28% higher than the traditional topology, which is consistent with the theoretical evaluation in Section III. The key parameters in the experiments are tabulated in Tables I and II. The system is implemented in digital controller TMS320F28379D with an interrupt frequency of 100 kHz. The input terminal of the converter is connected to the real power grid.

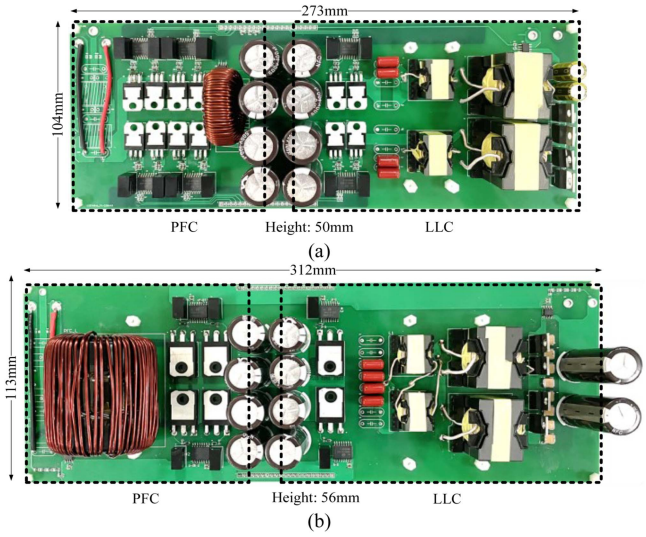


Fig. 14. Top view prototype photos of the ac/dc converter. (a) Proposed three-level converter. (b) Traditional two-level converter.

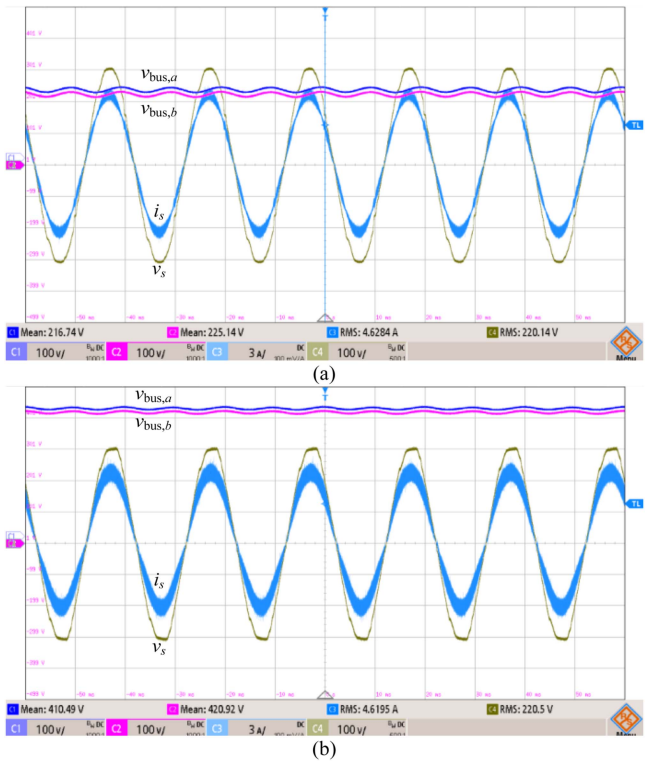


Fig. 15. Waveforms of the proposed three-level PFC at (a) $v_{\rm bus} = 220$ V and (b) $v_{\rm bus} = 420$ V.

## A. Key Waveforms of PFC and LLC

Fig. 15(a) and (b) shows the operating waveforms on the PFC side, including the bus voltage, input voltage, and inductor current. Among them, Fig. 15(a) presents the key waveforms when the bus voltage is 220 V. Since the minimum duty cycle of the converter is less than 0.5, the inductor current exhibits a three-level operating mode. Fig. 15(b) gives the key waveforms

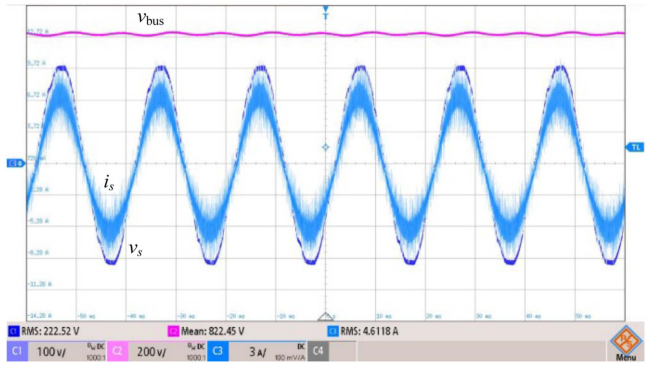


Fig. 16. Waveforms of the traditional two-level PFC at $v_{\rm bus} = 820$ V.

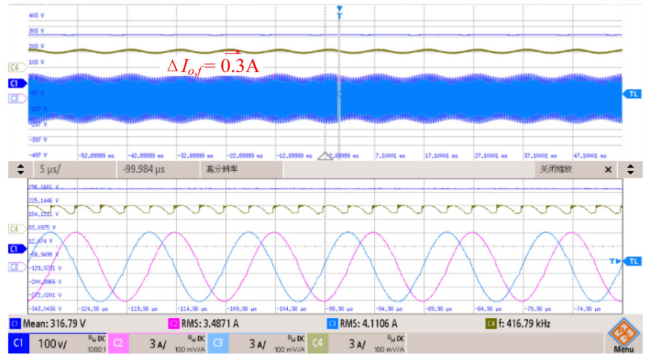


Fig. 17. Waveforms of the three-level LLC at $v_{\rm o} = 320$ V.

when the bus voltage is 420 V. At this time, the minimum duty cycle of the converter is greater than 0.5, and the inductor current exhibits a two-level operating mode. In the figures, the voltage difference between the two busbars is caused by the inconsistent voltage gain of two poststage *LLC* converters due to the deviation in the resonance parameters. In contrast, the inductance volt-second product of the traditional two-level PFC converter is about five times that of a cascaded three-level PFC, so a larger inductance is required to reduce the inductance current ripple. As shown in Fig. 16, with a much larger inductance (i.e., 2200 $\mu$H), the traditional two-level inductor current ripple is comparable with the cascaded three-level with a smaller inductance (i.e., 600 $\mu$H).

The operating waveforms on the *LLC* side are shown in Fig. 17. Due to the double line-frequency ripple suppression strategy adopted as shown in Fig. 10, the double line-frequency ripple of the output current is about 0.3 A, which meets the requirements of the Chinese national standard GB/T 40432-2021 for electric vehicle on-board charger. It is stipulated in the standard that when the output dc current is less than 10 A, the current error should be less than $\pm$0.5 A. The three-level *LLC* converter adopts a 90° phase-shift operation to ensure that the switching ripple of the rectified output current is reduced. As seen from the comparison waveforms in Fig. 18, under the same operating conditions, the switching ripple of the rectified output current of the cascaded three-level *LLC* is much smaller than that of the traditional two-level *LLC*, which is consistent with

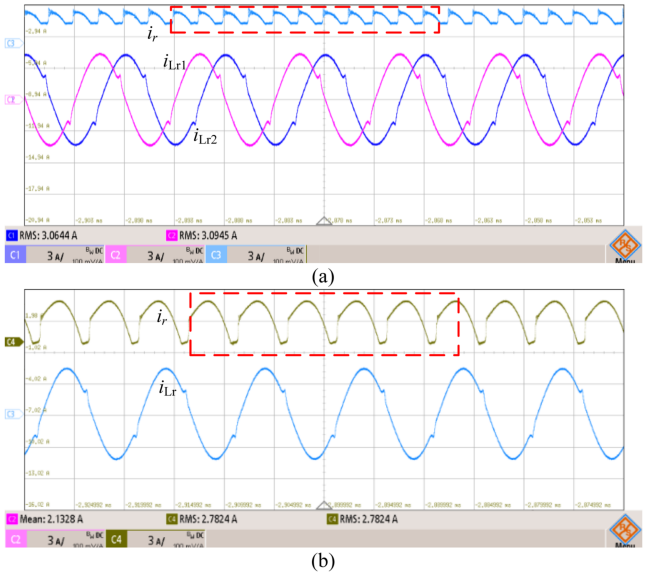


Fig. 18. Current waveforms of (a) three-level *LLC* with 90° phase-shift modulation and (b) traditional two-level *LLC*.

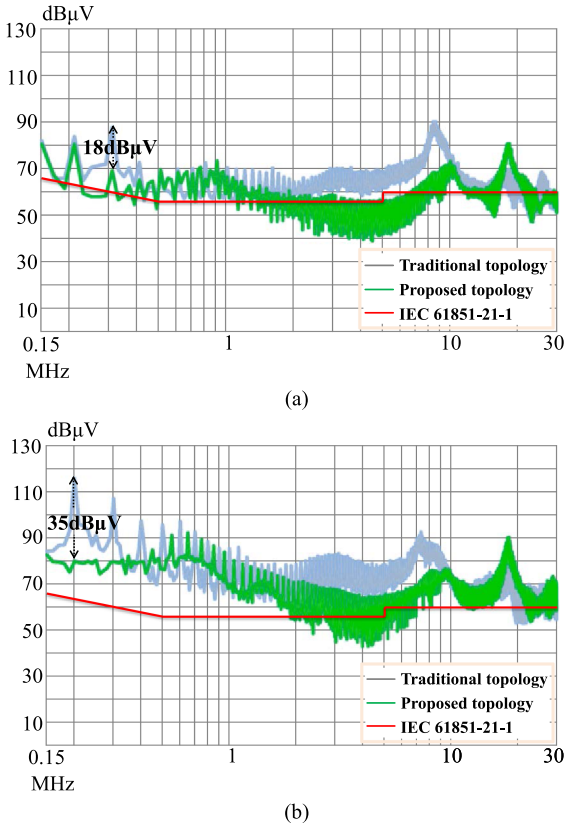


Fig. 19. Comparative CM noise spectrum of the proposed single-inductor-based PFC and the traditional split-inductor-based PFC. (a) With balanced parasitic capacitance. (b) With imbalanced parasitic capacitance.

the theoretical analysis in Section II. In Fig. 18, it can be clearly seen that the rectifier output current contains some oscillations, which are caused by the resonance interaction between the line parasitic inductance and the parasitic capacitance of the secondary rectifier diodes.

### *B. Comparative CM Results of the Cascaded Three-Level PFC*

In order to verify the advantages of the proposed PFC circuit in terms of CM noise suppression, this section compares the CM noise spectrum between the proposed single-inductor-based cascaded three-level PFC and the traditional split-inductor-based cascaded three-level PFC [22].

First, the parasitic capacitance is artificially placed between each dc bus and ground to simulate the parasitic capacitance of the poststage dc/dc converter. Then, the CM noise measurement is carried out on the LISN device, and the spectrum results without the CM filters are shown in Fig. 19, where the electric vehicle on-board charger electromagnetic compatibility requirements in the standards IEC 61851-21-1 or IEC 61000-6-3 are used as a reference line. When both parasitic capacitances of the two busbars are 500 pF, the single-inductor and split-inductor-based PFC circuits exhibit mirror symmetry, as shown in Fig. 19(a). The CM noise of the traditional split-inductor-based topology is comparable with the proposed single-inductor-based topology, which is consistent with the analysis in [21]. When the parasitic capacitance of the two busbars is differentiated, for example, one is 500 pF and the other is 1000 pF, the dominant CM noise amplitude of the proposed topology increases slightly. By contrast, the main CM noise amplitude of the traditional topology significantly increases by 30 dBμV. Moreover, the proposed topology reduces the CM noise amplitude by 35 dBμV compared to the traditional one, as presented in Fig. 19(b). Therefore, the suppression of CM noise by the proposed PFC topology does not depend on impedance balance and needs a smaller CM filter value and size, which is consistent with the theoretical analysis in Section II. Since the design of the CM filter is beyond the scope of this article, the corresponding experimental results with the CM filters are not given.

### *C. Power Efficiency Comparison*

Fig. 20(a) and (b) shows the calculated and measured efficiency curves of the PFC side, *LLC* side, and the entire converter under different output voltage conditions and different load conditions, respectively. Compared with theoretical calculation, the measured efficiency is low to a certain extent, especially on the *LLC* side, which is mainly due to errors in the evaluation of magnetic loss. However, the changing trend of calculated efficiency is consistent with the measured results. For the measured results, the efficiency of the PFC decreases with the increase in the bus voltage because the switching loss and magnetic loss increase. The highest efficiency of the PFC exceeds 98.5% at $v_{\text{bus}} = 220$ V. The maximum full-load efficiency on the *LLC* side appears near the bus voltage of 310 V, and the maximum full-load efficiency is 97.8%. The maximum full-load efficiency of the entire converter is also at the bus voltage of 310 V, and the maximum full-load efficiency is 96.22%. Fig. 20(b) gives the efficiency curve under different loads and $v_o = 320$ V. Among them, the maximum efficiency of the entire converter

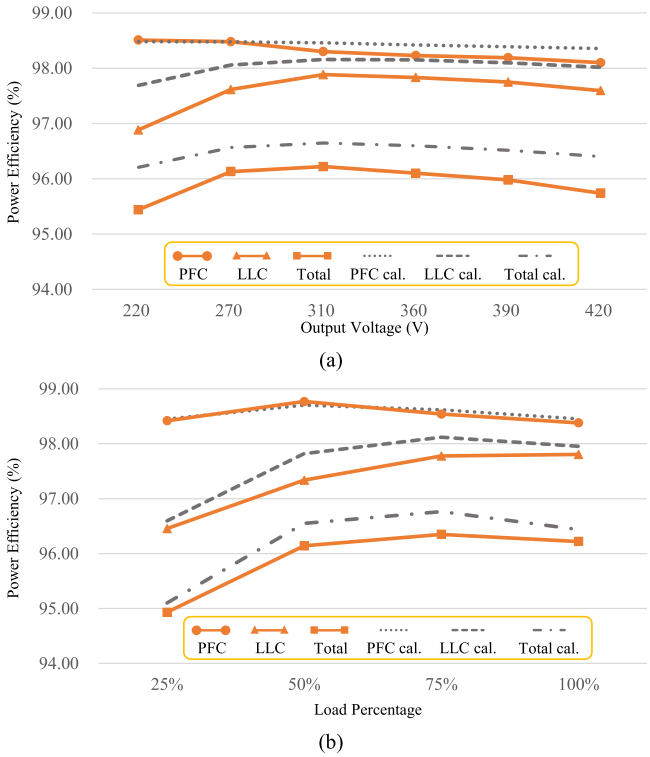


Fig. 20. Calculated and measured efficiency curve (a) under different output voltage and full load and (b) under different loads ($v_o = 320$ V).

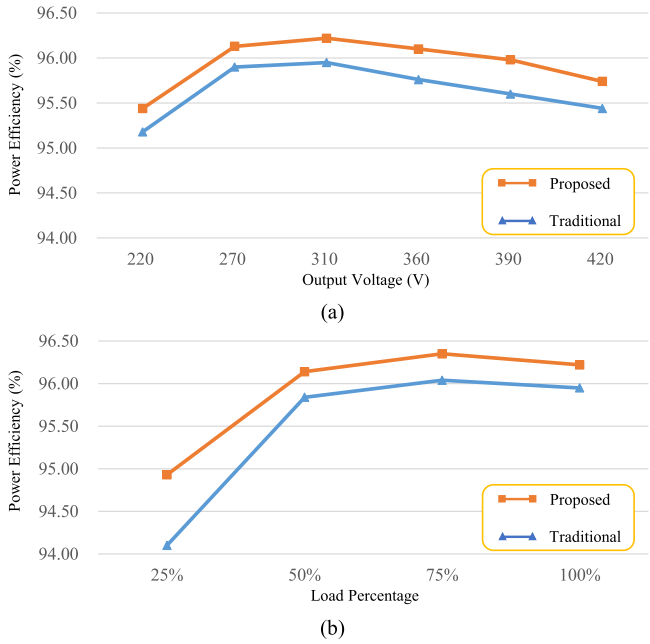


Fig. 21. Comparative efficiency curve between the proposed cascaded three-level topology and the traditional two-level topology. (a) Under different output voltage and full load. (b) Under different loads ($v_o = 320$ V).

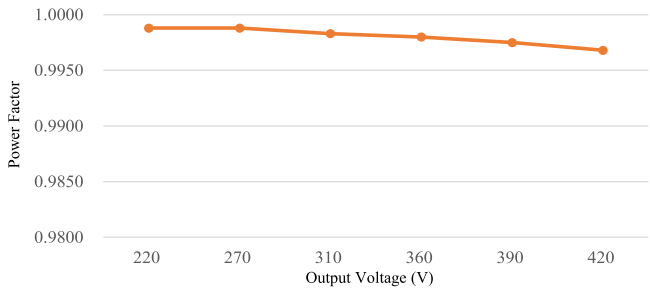


Fig. 22. Power factor under different output voltage.

is 96.35% under 75% load conditions, which meets the design expectations.

As shown in Fig. 21(a), compared with the traditional two-level ac/dc converter based on variable bus voltage regulation, the full-load efficiency of the proposed three-level topology has increased by an average of 0.2%–0.5%. This is mainly due to the reduction of PFC inductor loss. The efficiency comparison curve under different load conditions is shown in Fig. 21(b). As seen from the figure, at light load, the efficiency improvement of the proposed topology is becoming more obvious. For example, at 25% load, it has increased by nearly 1% compared with the traditional topology. This is mainly due to the larger proportion of magnetic loss in the PFC inductor at light load. This power efficiency improvement with voltage and load is effective for both EV charging scenarios and other applications.

Fig. 22 shows the input power factor at different bus voltages. As seen from the figure, the influence of different bus voltages on the input power factor is very small, and the input power factor under different bus voltages is greater than 0.995.

## IV. Conclusion

This article proposes a new type of cascaded three-level on-board charger architecture based on variable bus voltage control to handle an ultrawide battery voltage range. The proposed three-level topology and the traditional two-level topology are evaluated and compared. The results show that using the proposed cascaded three-level structure, it features smaller input and output current ripple, lower primary-side device voltage stress, higher power density, and efficiency. Moreover, compared with the existing split-inductor-based cascaded three-level PFC, the proposed single-inductor-based cascaded three-level PFC has a stronger CM noise suppression capability. A 1-kW experimental prototype is built in the laboratory. It shows that, compared with the traditional two-level topology, the full-load efficiency of the proposed topology increases by 0.2%–0.5%, and the power density increases by 28%. It should be noted that when expanding to more levels ($N$>3), the proposed cascaded PFC can only be expanded with a three-level cell as a unit. In the future, we intend to extend our work to cascaded multilevel ($N$>3) topology to verify the versatility of the proposed variable bus structure.

## Appendix

The main losses at the PFC stage are calculated as follows.

1) Conduction loss and switching loss of power semiconductor devices

Conduction loss:

$$P_{s,\mathrm{con,PFC}} = 2I_{s,\mathrm{rms}}^2 \left(R_{ds,\mathrm{LF}} + R_{ds,\mathrm{HF}}\right).$$

Switching loss:

$$P_{s,\mathrm{sw,PFC}} = \frac{2f_s V_{\mathrm{bus},x}}{T}\ (t_r + t_f) \int_0^T I_{sm} \left|\sin\ \omega t\right| dt$$

where $I_{s,\mathrm{rms}}$ is the RMS value of the input current, $R_{ds,\mathrm{LF}}$ and $R_{ds,\mathrm{HF}}$ are the ON-resistance of switching devices at line- and high-frequency bridges, $f_s$ means the switching frequency, $T$ is the line cycle, and $t_r$ and $t_f$ are the rising and falling times of switching devices.

2) Copper and core loss of PFC inductor

$$P_{\mathrm{ind,PFC}} = I_{s,\mathrm{rms}}^2 R_{w,\mathrm{PFC}} + kV_e \left[\frac{1}{T}\int_0^T \Delta B\left(\omega t\right) dt\right]^a f_s^b$$

where $R_{w,\mathrm{PFC}}$ is the equivalent dc and ac resistance of the copper, $V_e$ is the volume of the magnetic core, the coefficients of the core loss at the second part of the equation right-hand side are the empirical parameters, and $\Delta B$ is calculated as

$$\Delta B\left(\omega t\right) = \begin{cases} \frac{(V_{sm}\left|\sin\ \omega t\right| - V_{\mathrm{bus},x})D}{2N\ f_{\mathrm{sw}} A_e}, & \text{if } 0 \le D \le 0.5 \\ \frac{V_{sm}\left|\sin\ \omega t\right|(D-0.5)}{2N\ f_s A_e}, & \text{otherwise} \end{cases}$$

where $V_{sm}$ is the RMS value of the input voltage, $N$ is turns number of the inductor, and $A_e$ means the section area of the magnetic core.

3) Conduction loss of the bus capacitors

$$P_{Cb,\mathrm{PFC}} = I_{Cb,\mathrm{rms}}^2\ R_{\mathrm{ESR,dc}}$$

where $I_{Cb,\mathrm{rms}}$ is the RMS value of current through bus capacitors, and $R_{\mathrm{ESR,dc}}$ is the equivalent series resistance of bus capacitors.

The main losses at the *LLC* stage are calculated as follows.

1) Conduction loss and switching loss of power semiconductor devices

Conduction loss:

$$P_{s,\mathrm{con},LLC} = 2I_{r,\mathrm{rms}}^2 R_{ds,LLC} + I_o V_f.$$

Switching loss:

$$P_{s,\mathrm{sw},LLC} = 2f_s V_{\mathrm{bus},x} I_M t_f$$

where $I_{r,\mathrm{rms}}$ is the RMS value of the resonance current, $R_{\mathrm{dc},LLC}$ is the ON-resistance of switching devices, $I_o$ means the output current, $V_f$ is the forward voltage of diodes, and $I_M$ is the peak value of magnetic current.

2) Copper and core loss of the resonance inductor and transformer

$$P_{m,LLC} = 2I_{r,\mathrm{rms}}^2 \left(R_{w,r} + R_{w,p}\right) + \left(\frac{1.57}{\sqrt{2}} I_o\right)^2 R_{w,s} + 2\left(V_{e,r} + V_{e,T}\right) P_{VT}$$

where $R_{w,r}$, $R_{w,p}$, and $R_{w,s}$ mean the equivalent dc and ac resistance of the copper, $V_{e,r}$ and $V_{e,T}$ are the volumes of the magnetic cores, and $P_{VT}$ means the core loss per unit volume.

3) Conduction loss of the bus capacitors

$$P_{\mathrm{Co},LLC} = I_{\mathrm{Co,rms}}^2\ R_{\mathrm{ESR},o}$$

where $I_{\mathrm{Co,rms}}$ is the RMS value of current through output capacitors, and $R_{\mathrm{ESR},o}$ is the equivalent series resistance of output capacitors.

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**Yuanbin He** (Member, IEEE) received the Ph.D. degree in electrical engineering from The City University of Hong Kong, Hong Kong, in 2017,

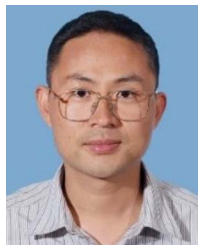
He was a Research Assistant from April to August 2013 and a Postdoctoral Research Fellow from February to July 2017 with The City University of Hong Kong. From 2011 to 2013, he was an Associate Researcher with Nanjing FSP-Powerland Technology, Inc., Nanjing, China, where he was involved in the research and development of dc–dc and dc–ac converters. From February to June 2016, he was a Visiting Scholar with the University of Manitoba, Winnipeg, Canada. Since May 2017, he has been with Hangzhou Dianzi University, Hangzhou, China, where he is currently an Associate Professor with the Department of Electrical Engineering and Automation. His current research areas include renewable energy conversion technology, high-efficiency power conversion, power quality, and smart grid.

**Hao Liu** received the B.E. degree in electrical engineering in 2021 from Hangzhou Dianzi University, Zhejiang, China, where he is currently working toward the M.E. degree with the Department of Automation.

**Junjie Zhang** received the B.E. degree in electrical engineering and the M.E. degree in control engineering from Hangzhou Dianzi University, Hangzhou, China, in 2020 and 2023, respectively.

He is currently involved in the chip industry, mainly researching display power management chips.

**Chenyu Shen** received the B.E. degree in electrical engineering from the NingBo University of Technology, Zhejiang, China, in 2022. He is currently working toward the M.E. degree with the Department of Automation, Hangzhou Dianzi University, Hangzhou, China.



**Xiaogao Xie** (Senior Member, IEEE) was born in Hunan Province, China, in 1975. He received the M.S. and Ph.D. degrees in electrical engineering from Zhejiang University, Hangzhou, China, in 2000 and 2005, respectively.

He was a Postdoctoral Fellow with the College of Electrical Engineering, Zhejiang University, from 2005 to 2007. He is currently a Professor with the School of Automation, Hangzhou Dianzi University, Hangzhou. His research interests include high-efficiency power conversion, LED driving technology, and renewable energy conversion technology.

**Lijun Hang** (Senior Member, IEEE) received the B.S. and Ph.D. degrees in electrical engineering from Zhejiang University, Hangzhou, China, in 2002 and 2008, respectively.

From 2008 to 2011, she was a Postdoctoral Researcher with Zhejiang University. From 2011 to September 2013, she was a Research Assistant Professor with CURENT, University of Tennessee, Knoxville, TN, USA. From 2013 to 2015, she was an Associate Professor with the Department of Electrical Engineering, Shanghai Jiao Tong University, Shanghai, China. Since 2015, she has been a Professor with Hangzhou Dianzi University, Hangzhou, China. She has authored or coauthored more than 150 published technical papers. Her research interests include digital control of power electronics for power converters, bidirectional dc–dc converters for microgrid, and renewable energy systems.