A Bidirectional Three-Level Converter Control With Shared Control Circuit and Single-Point Sensing for Flying Capacitor Balance

Yu-Yu Lin, Yi-Rong Huang, Ching-Jan Chen, *Senior Member, IEEE*, Yuan-Chih Lin, *Student Member, IEEE*, and Tsung-Wei Huang

***Abstract*—This article presents a novel three-level (TL) converter control integrated circuit (IC) with a flying capacitor control loop, an adaptive constant ON-time (ACOT) control, and a shared control circuit in bidirectional operation for the battery charger system. To solve the flying capacitor balance issue in TL converters, the flying capacitor control with single-point sensing (SPS) of switching voltage V_X is proposed to balance the flying capacitor without a complex control and sensing circuit in an IC implementation. The proposed SPS also minimizes the inductor ripple. Besides, both directions (buck mode or boost mode) share the same control circuits except for the compensator to minimize the controller die area. The proposed scheme is realized with a 1.5 MHz switching frequency bidirectional TL converter IC in the TSMC 0.18 μm complementary metal-oxide-semiconductor (CMOS) process. The measurement result verifies that the functions are feasible in both directions, and there are no flying capacitor voltage runaway and mismatch issues. The proposed ACOT design achieves less than 6% switching frequency variation over the load range in boost mode, which is much smaller than conventional ACOT control. The proposed TL buck converter achieves an efficiency of 95.89% at 1-A load. The efficiency of the proposed TL boost converter is up to 96.02% at 0.5-A load.**

***Index Terms*—Adaptive constant ON-time (ACOT) control, bidirectional control, flying capacitor balance, on-the-go (OTG), three-level (TL) converter, virtual inductor current (VIC).**

I. Introduction

A HIGH-EFFICIENCY bidirectional battery charger is becoming popular for mobile devices with universal serial bus (USB) input. As shown in Fig. 1, the battery charger system incorporates a converter with the input from adapters or USB, and the output connects to a battery such as a Li-ion battery [1]. In general conditions, the battery charger operates in buck mode, which means the power flows from the high-side USB or adapters to the low-side batteries. Since the high-side voltage is 5 V or even higher voltage domain, high efficiency and high input voltage converters are required. Recently, the application of a USB on-the-go (OTG) communication system has been widely applied to electronic devices [2]. The OTG means the power flows from batteries to adapters or USB, so the battery acts as a supplier for another device. Therefore, the battery charger requires bidirectional capability and operates in the boost mode for OTG applications.

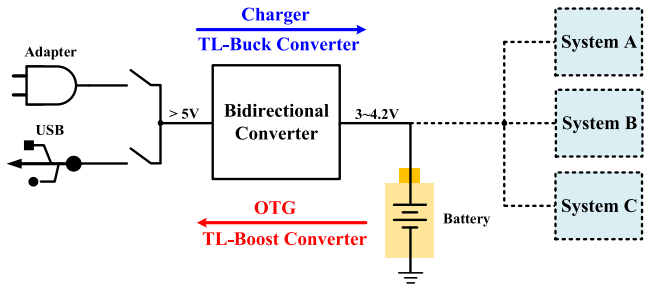

Fig. 1. Battery power system in mobile devices.

Three-level (TL) converters show benefits for high voltage, high frequency, and high-power density applications with reduced switching loss [3], [4], [5], [6], [7], [8]. TL converter topologies and operation waveforms of buck and boost modes at $D_1 < 0.5$ and $D_1 > 0.5$ are shown in Fig. 2. The difference between buck mode and boost mode is the definition of input voltage and output voltage. For buck mode, the input is the high-side voltage V_{High} and the output is the low-side voltage V_{Low}. Oppositely, the boost mode swaps the input and the output in the buck mode. Q_1 and Q_4 operate in a complementary way, the same as Q_2 and Q_3. There are 180° of phase shifts between Q_1 and Q_2. By interleaving the switching signal and balancing flying capacitor voltage at about half of the high-side voltage, each switching frequency of power metal-oxide-semiconductor (MOS) is half of the overall system, and the switching voltage V_x varies from 0 to $V_{\mathrm{High}}/2$ during $D_1 < 0.5$ or from $V_{\mathrm{High}}/2$ to V_{High} during $D_1 > 0.5$. Owing to the balance of the flying capacitor, the smaller amplitude and the doubled switching frequency of switching voltage reduce the voltage across the inductor and make the lower inductor current ripple [6], [7], [8]. Hence, the size of the inductor can be reduced. According to the

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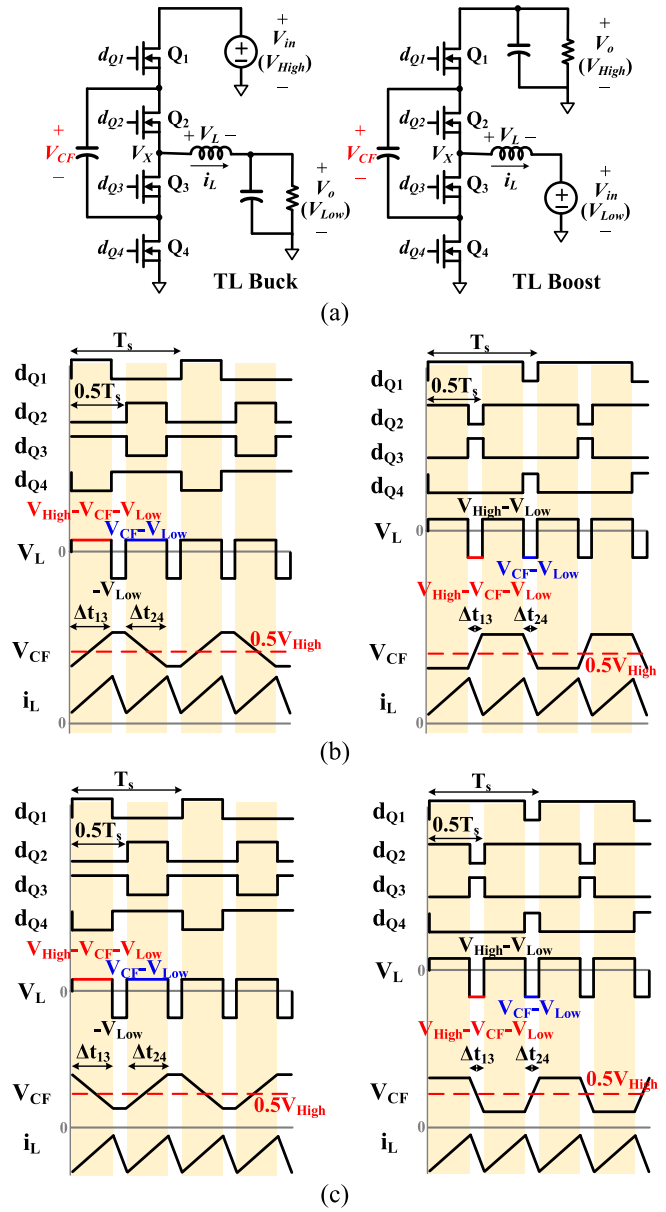


Fig. 2. (a) Topologies of TL converters. (b) Key waveforms of the TL buck converter. (c) Key waveforms of the TL boost converter.

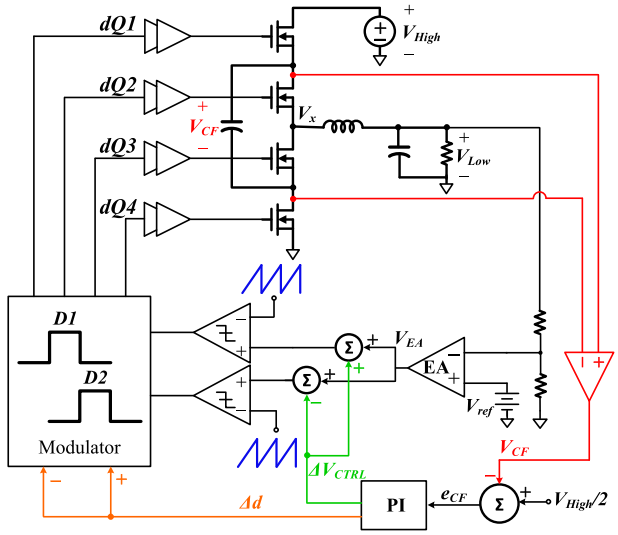


Fig. 3. Conventional flying capacitor control [5], [18], [19], [20], [21].

switching loss proportional to the peak current and the switching voltage, the reduction of the inductor current ripple and the switching stress reduce the switching loss. The reduced voltage stress across devices also allows for the use of low-voltage lateral devices [6], [7], [8], [9], [10]. Consequently, TL converters offer the benefits of reducing switching loss and efficiency drop at a higher frequency. It is obvious that TL converters are suitable for the battery charger application. Nevertheless, it can be seen that most of the advantages mentioned above rely on the balance of the flying capacitor. An unbalanced voltage across the flying capacitor causes a higher inductor ripple and uneven switching voltage, which leads to increased power loss and voltage stress [11], [12], [13], [14]. In fact, flying capacitor unbalance for TL converters happens due to circuit mismatches, such as nonuniform switch resistance and poor delay matching between gate driving signals [15].

Various methods are proposed to achieve flying capacitor balance for TL converters. One method is to achieve the balance with the intrinsic control loop of the system [7], [12], [16], [17], but this method needs a control scheme change such as using valley-current mode with constant ON-time and peak current mode with constant OFF-time for $D_1 < 0.5$ and $D_1 > 0.5$ conditions, respectively [17]. The other method is widely used to achieve the balance by adding an additional balance loop [4], [5], [18], [19], [20], [21]. The conventional flying capacitor control uses two-terminal sensing to maintain V_{CF} equal to half of the high side voltage. It would sense two-terminal voltages across the flying capacitor to obtain the flying capacitor voltage (V_{CF}) and compare it with the half of high side voltage ($V_{\mathrm{High}}/2$). Two conventional methods of flying capacitor control are shown in Fig. 3. The difference between V_{CF} and $V_{\mathrm{High}}/2$ would transfer to ΔV_{CTRL} (the green path) or Δd (the orange path) after the V_{CF} error goes through the proportional-integral (PI) controller. Then, the charging and the discharging times adjust to balance the flying capacitor voltage. However, the sensing method of two terminals requires differential pair circuits to sense V_{CF} and other components such as PI compensators and at least two subtractors, causing a complex circuit design. Furthermore, controlling V_{CF} to $V_{\mathrm{High}}/2$ still suffers from a larger inductor current ripple due to the different turn-ON resistance between Q_1 to Q_4. As shown in Fig. 4, the voltage across the inductor, i.e., V_L, is unbalanced due to different turn-ON resistances between Q_1 to Q_4. Unbalanced V_L voltage induces different slopes as slope_1 and slope_2, which causes a larger inductor current ripple. This problem is similar to the issue of flying capacitor unbalance, which causes a larger inductor current ripple [11], [12], [13], [14], but the larger ripple is caused by different turn-ON resistance instead of flying capacitor unbalance. The detailed analysis of the inductor current ripple will be conducted in Section II.

The adaptive constant ON-time (ACOT) control brings the advantages of high light-load efficiency for TL converter; however,

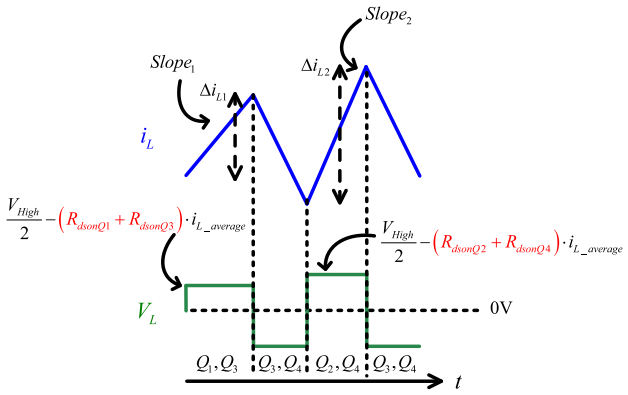


Fig. 4. Inductor current and V_L waveforms with $V_{\mathrm{CF}} = V_{\mathrm{High}}/2$.

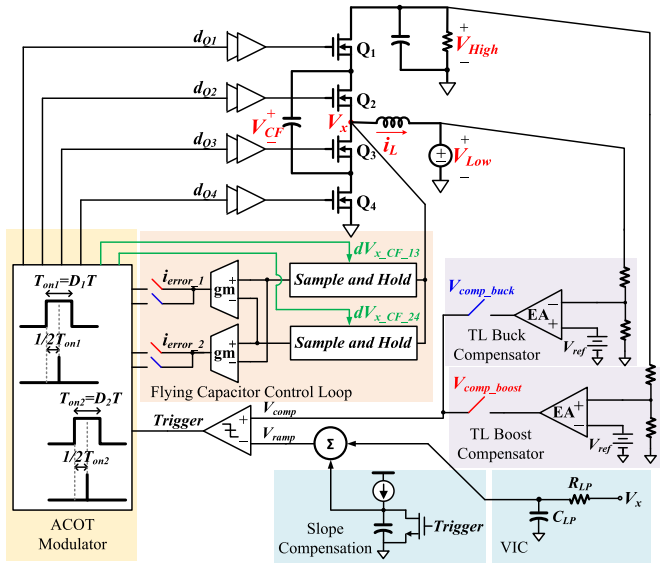


Fig. 5. System architecture of the proposed bidirectional TL converter.

the current approaches suffer from relatively large frequency variation in continuous conduction mode (CCM) at various loading conditions [22], [23], [24], [25], [26]. To alleviate the frequency variation, the conventional ACOT techniques use the input voltage and output voltage information to generate adaptive ON-time to achieve CCM pseudoconstant switching frequency in various V_{High} and V_{Low} in traditional buck converters [24], [25], [26]. However, the performance is still constrained because there is no ability to maintain the switching frequency, which depends on load conditions from practical parasitics. Consequently, the ACOT techniques with the duty cycle or the switching voltage information instead of the input and output voltage information have been applied to cancel the frequency variation well in different load conditions for traditional buck converters [22], [23]. However, the current ACOT techniques for traditional boost converters can only eliminate the factors of input voltage and output voltage, but the load conditions have not been taken into consideration [27], [28].

Integrated circuit (IC) implementation for bidirectional TL converter is preferred for low-voltage mobile applications; however, there is no such implementation in the papers [15], [25], [26], [27], [28]. Although bidirectional TL converter control is presented in papers. However, they are implemented by discrete components [15], digital control [26], [28], or behavior circuits with only simulation [27]. IC implementation can exhibit its advantages for low-voltage mobile applications, such as portable devices, smartphones, and tablets. In these applications, it is a common practice to integrate the power MOS and controller of the IC chip to save volume and cost. If the power converter is realized by digital signal processor (DSP) or field-programmable gate array (FPGA), the driver and power MOS are discrete components, which increases cost and occupies a large area of the printed circuit board (PCB) for portable devices. Since IC implementation saves cost, reduces converter size, and meets commercial application requirements, proposing an IC implementation solution is indispensable.

Besides, the traditional current mode control on bidirectional TL converter adopts double closed-loop control and requires sensing inductor current, which increases controller cost and complexity [25], [26]. The two loops include the voltage outer loop and the current inner loop. In addition, the controller uses separate control loops for buck mode and boost mode. Thus, it increases controller complexity and sense components to realize the bidirectional circuit. On the other hand, traditional voltage mode control on a bidirectional TL converter does not require sensing inductor current. However, the control-to-output transfer function of voltage mode control has LC complex poles, making it difficult to compensate for the voltage loop [15].

Motivated by the above concerns, we propose a bidirectional TL converter control IC with control sharing and area minimizing to improve the complicated bidirectional control and remove the current sensors for modulation. Moreover, the flying capacitor control with single-point sensing (SPS) proposed in Section II avoids complex differential voltage sensing design and reduces the inductor current mismatch by ensuring that the switching voltages are equal during the flying capacitor charging and discharging period. Additionally, ACOT for pseudofixed switching frequency is also proposed in Section II to eliminate frequency variation at different load conditions, especially for the boost mode. The transistor-level simulation and experimental results are presented in Section III. Finally, Section IV concludes this article.

II. Proposed Bidirectional TL Converter With Single-Point Sensing (SPS) for Flying Capacitor Balance

A. System Architecture

Fig. 5 shows the architecture of the proposed bidirectional TL converter with ACOT control and SPS for flying capacitor balance. The proposed converter consists of a TL power stage, TL buck and TL boost compensators, a virtual inductor current (VIC) circuit with slope compensation, a flying capacitor control loop, and an ACOT modulator. The red and blue switches turn ON in boost and buck modes, respectively. It can be seen that most of the control circuits are combined for buck mode and boost mode except the compensator. Thus, the IC area and power

consumption can be reduced. The output voltage is regulated by feedbacking the output voltage through the compensator to generate $V_{\rm comp}$. The other loop, the inner loop, is generated by the VIC with slope compensation for both directions. After comparing $V_{\rm comp}$ and $V_{\rm ramp,}$ which is generated by the VIC circuit with slope compensation, the trigger signal would decide the timing to trigger an ON-time by the proposed ACOT modulator. Finally, the flying capacitor control loop balances the flying capacitor voltage $V_{\rm CF}$ by ensuring that the switching voltages are equal during the charging and discharging period. The proposed control only samples switching voltage V_x at half of $T_{\rm ON}$ timing with the signals $dV_{x\_{\rm CF}\_13}$ and $dV_{x\_{\rm CF}\_24}$ provided by the proposed ACOT modulator. Additionally, the error currents $i_{\rm error1}$ and $i_{\rm error2}$, which are generated by the switching voltage difference between the charging and discharging period, adjust the ON-time directly to avoid the inductor current mismatch caused by the large ripple of error flowing into the outer voltage loop.

B. Flying Capacitor Control With V_x Sensing

This section addresses the flying capacitor stability analysis of the TL converter with COT control in buck and boost modes. Through the analysis, we can obtain the flying capacitor balance mechanism after perturbation and discuss whether buck mode or boost mode needs to add a flying capacitor balance loop under COT control. For the TL converter, the flying capacitor charging or discharging period is during Q_1 and Q_3 ON (Δt_{13}) or Q_2 and Q_4 ON (Δt_{24}) as depicted in Fig. 2. Due to the nature of COT control, Δt_{13} equals Δt_{24}. The definitions of inductor current and inductor voltage are the same for both modes. Therefore, the inductor current in boost mode is less than zero and in phase with buck mode, as depicted in Fig. 2. In steady state, the charge of the flying capacitor is equivalent. The voltage across the inductor during Δt_{13} ($V_{L,13}$) and the voltage across the inductor during Δt_{24} ($V_{L,24}$) are shown as

$$V_{L,13} = V_{\rm High} - V_{\rm CF} - V_{\rm Low} \tag{1}$$

$$V_{L,24} = V_{\rm CF} - V_{\rm Low}. \tag{2}$$

To find out the flying capacitor balance mechanism, we give a perturbation such that the flying capacitor voltage ($V_{\rm CF}$) is larger than half of the high side voltage. That is, the average charging current of the flying capacitor is larger than discharging. The voltage across the inductor is shown as

$$V_{L,13} = V_{\rm High} - (V_{\rm CF} + \Delta V_{\rm CF}) - V_{\rm Low} \tag{3}$$

$$V_{L,24} = (V_{\rm CF} + \Delta V_{\rm CF}) - V_{\rm Low}. \tag{4}$$

For the TL buck converter, the flying capacitor charge during Δt_{13} and discharge during $\Delta t_{24,}$ as shown in Fig. 2, so the slope of inductor current during flying capacitor charging is smaller than discharging. Hence, the larger average inductor current occurs during the flying capacitor discharging period. As a result, the larger discharging current of the flying capacitor forces the flying capacitor to a balanced position. Thus, the TL buck converter with COT control naturally has a negative feedback mechanism. On the other hand, the period of flying capacitor charging and discharging is the opposite for TL boost. The larger inductor current in the charging period causes the flying capacitor to store more charges. The flying capacitor will be continuously increasing and then voltage runaway eventually. This issue will be verified by simulation in Fig. 10. As a result, the TL boost converter with COT control must add a flying capacitor control loop to avoid $V_{\rm CF}$ runaway.

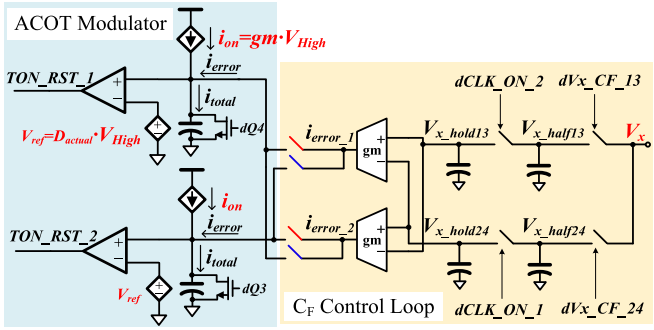


Fig. 6. Structure of the proposed flying capacitor control loop and ON-time modulator.

The flying capacitor control with SPS is proposed in Fig. 6 to overcome the complexity and inductor current mismatch issues. The simpler design with only four sample and hold (S/H) circuits and two operational transconductance amplifiers (OTAs) can achieve flying capacitor control. In addition, the design target is to make sure the average value of V_x is the same during the flying capacitor charging and discharging periods. In steady state, V_x reflects the slope of i_L. The proposed flying capacitor control can minimize the mismatch of inductor current peak values during flying capacitor charging and discharging. Take the operation during $D < 0.5$ in boost mode as an example; we can write V_x in each state as

$$Q_1,\ Q_3 \text{ on}: \quad V_{x,13} = V_O - 2I_L R_{\rm DS} - V_{\rm CF} - I_L R_{\rm mismatch} \tag{5}$$

$$Q_3,\ Q_4 \text{ on}: \quad V_{x,34} = -2I_L R_{\rm DS} \tag{6}$$

$$Q_2,\ Q_4 \text{ on}: \quad V_{x,24} = -2I_L R_{\rm DS} + V_{\rm CF} \tag{7}$$

$$Q_3,\ Q_4 \text{ on}: \quad V_{x,34} = -2I_L R_{\rm DS} \tag{8}$$

where $R_{\rm DS}$ is the mean ON-resistance of four switches, and $R_{\rm mismatch}$ represents the mismatch of the equivalent ON-resistance between charging and discharging paths. Once we control $V_{x,13}$ equals $V_{x,24}$, the flying capacitor voltage would be controlled at the balance value, as given by

$$V_{\rm CF} = \frac{1}{2}\left(V_O - I_L R_{\rm mismatch}\right). \tag{9}$$

It can be derived that during other modes like $D > 0.5$, (9) still holds.

The slight adjustment of the flying capacitor voltage forces the voltage across the inductor during charging and discharging to be equal. Consequently, it is beneficial for flying capacitor control with V_x sensing to minimize inductor ripple. Besides,

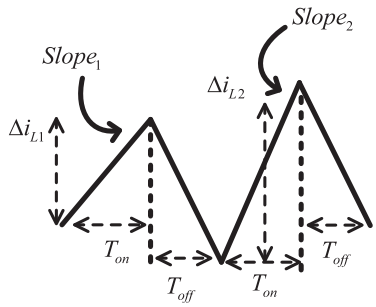


Fig. 7. Different inductor ripple caused by the mismatch of turn-ON resistance.

V_{CF} value is predictable by (9), which can be designed to avoid switch overstress issues.

For the analysis of inductor current ripple mismatch behavior, we use the case of buck mode with duty cycle <0.5 and ON-resistances are different between Q_1 to Q_4 as an example. For buck mode with duty cycle <0.5, the V_x voltage on each state is as

$$\mathrm{Q_1, Q_3ON}: V_{x,13} = V_{\mathrm{in}} - V_{\mathrm{CF}} - I_{L\_\mathrm{ave}}\left(\left(R_{\mathrm{DS\_4}} + \Delta R_{\mathrm{mismatch\_4,1}}\right) + R_{\mathrm{DS\_3}}\right) \quad (10)$$

$$\mathrm{Q_3, Q_4ON}: V_{x,34} = -I_{L\_\mathrm{ave}}\left(R_{\mathrm{DS\_3}} + R_{\mathrm{DS\_4}}\right) \quad (11)$$

$$\mathrm{Q_2, Q_4ON}: V_{x,24} = V_{\mathrm{CF}} - I_{L\_\mathrm{ave}}\left(R_{\mathrm{DS\_3}} + \Delta R_{\mathrm{mismatch\_3,2}} + R_{\mathrm{DS\_4}}\right) \quad (12)$$

$$\mathrm{Q_3, Q_4ON}: V_{x,34} = -I_{L\_\mathrm{ave}}\left(R_{\mathrm{DS\_3}} + R_{\mathrm{DS\_4}}\right) \quad (13)$$

where $\Delta R_{\mathrm{mismatch\_41}} = R_{\mathrm{DS\_1}}$-$R_{\mathrm{DS\_4}}$, and $\Delta R_{\mathrm{mismatch\_32}} = R_{\mathrm{DS\_2}}$-$R_{\mathrm{DS\_3}}$.

As shown in Fig. 7, the mismatch of turn-ON resistance $\Delta R_{\mathrm{mismatch\_41}}$ and $\Delta R_{\mathrm{mismatch\_32}}$ makes the inductor current ripple Δi_{L1} and Δi_{L2} different. Δi_{L1} can be derived as (14). In (14), it can be found the duty cycle D_1 should be derived. By inductor voltage balance, D_1 can be derived as (15). By substituting (15) into (14), Δi_{L1} can be obtained as (16). By the same process, Δi_{L2} can be obtained as (17). From (16) and (17), it can be found that the difference between Δi_{L1} and Δi_{L2} is caused by $\Delta R_{\mathrm{mismatch\_41}}$ and $\Delta R_{\mathrm{mismatch\_32}}$.

$$\Delta i_{L1} = \mathrm{slope_1} \cdot T_{\mathrm{ON}} = \mathrm{slope_1} \cdot \frac{1}{2} D T_s = \frac{V_{\mathrm{in}} - V_{\mathrm{CF}} - I_{L\_\mathrm{ave}}\left(\left(R_{\mathrm{DS\_4}} + \Delta R_{\mathrm{mismatch\_4,1}}\right) + R_{\mathrm{DS\_3}}\right) - V_o}{L} \cdot \frac{1}{2} D T_s \quad (14)$$

$$D = \frac{2\left(V_{\mathrm{out}} + I_L\left(R_{\mathrm{DS\_3}} + R_{\mathrm{DS\_4}}\right)\right)_s}{\left(V_{\mathrm{in}} - I_{L\_\mathrm{ave}}\left(\Delta R_{\mathrm{mismatch\_4,1}} + \Delta R_{\mathrm{mismatch\_3,2}}\right)\right)} \quad (15)$$

$$\Delta i_{L1} = \frac{V_{\mathrm{in}} - V_{\mathrm{CF}} - I_{L\_\mathrm{ave}}\left(R_{\mathrm{DS\_3}} + R_{\mathrm{DS\_4}}\right) - I_{L\_\mathrm{ave}} \cdot \Delta R_{\mathrm{mismatch\_4,1}} - V_o}{L} \cdot \frac{2\left(V_{\mathrm{out}} + I_L\left(R_{\mathrm{DS\_3}} + R_{\mathrm{DS\_4}}\right)\right)_s}{\left(V_{\mathrm{in}} - I_{L\_\mathrm{ave}}\left(\Delta R_{\mathrm{mismatch\_4,1}} + \Delta R_{\mathrm{mismatch\_3,2}}\right)\right)} \cdot \frac{1}{2} T_s \quad (16)$$

$$\Delta i_{L2} = \frac{V_{\mathrm{CF}} - I_{L\_\mathrm{ave}}\left(R_{\mathrm{DS\_3}} + R_{\mathrm{DS\_4}}\right) - I_{L\_\mathrm{ave}} \cdot \Delta R_{\mathrm{mismatch\_3,2}} - V_o}{L} \cdot \frac{2\left(V_{\mathrm{out}} + I_L\left(R_{\mathrm{DS\_3}} + R_{E\_4}\right)\right)_s}{\left(V_{\mathrm{in}} - I_{L\_\mathrm{ave}}\left(\Delta R_{\mathrm{mismatch\_4,1}} + \Delta R_{\mathrm{mismatch\_3,2}}\right)\right)} \cdot \frac{1}{2} T_s. \quad (17)$$

In the conventional flying capacitor control technique, the voltage of the flying capacitor V_{CF} is controlled to $V_{\mathrm{in}}/2$. By substituting $V_{\mathrm{CF}} = V_{\mathrm{in}}/2$ into (16) and (17), the ripple of inductor current based on conventional technique $\Delta i_{L1\_\mathrm{convention}}$ and $\Delta i_{L2\_\mathrm{convention}}$ can be obtained as (18) and (19). From (18) and (19), we know that the conventional technique suffers from the mismatch $\Delta \mathrm{R}_{\mathrm{mismatch\_41}}$ and $\Delta \mathrm{R}_{\mathrm{mismatch\_32}}$.

$$\Delta i_{L1\_\mathrm{convention}} = \frac{\frac{V_{\mathrm{in}}}{2} - I_{L\_\mathrm{ave}}\left(R_{\mathrm{DS\_3}} + R_{\mathrm{DS\_4}}\right) - I_{L\_\mathrm{ave}} \cdot \Delta R_{\mathrm{mismatch\_4,1}} - V_o}{L} \cdot \frac{2\left(V_{\mathrm{out}} + I_L\left(R_{\mathrm{DS\_3}} + R_{\mathrm{DS\_4}}\right)\right)_s}{\left(V_{\mathrm{in}} - I_{L\_\mathrm{ave}}\left(\Delta R_{\mathrm{mismatch\_4,1}} + \Delta R_{\mathrm{mismatch\_3,2}}\right)\right)} \cdot \frac{1}{2} T_s \quad (18)$$

$$\Delta i_{L2\_\mathrm{convention}} = \frac{\frac{V_{\mathrm{in}}}{2} - I_{L\_\mathrm{ave}}\left(R_{\mathrm{DS\_3}} + R_{\mathrm{DS\_4}}\right) - I_{L\_\mathrm{ave}} \cdot \Delta R_{\mathrm{mismatch\_3,2}} - V_o}{L} \cdot \frac{2\left(V_{\mathrm{out}} + I_L\left(R_{\mathrm{DS\_3}} + R_{\mathrm{DS\_4}}\right)\right)_s}{\left(V_{\mathrm{in}} - I_{L\_\mathrm{ave}}\left(\Delta R_{\mathrm{mismatch\_4,1}} + \Delta R_{\mathrm{mismatch\_3,2}}\right)\right)} \cdot \frac{1}{2} T_s. \quad (19)$$

In the proposed flying capacitor balance technique, the V_{CF} is controlled to the voltage as (20). By substituting (20) into (16) and (17), the ripple of inductor current based on the proposed technique can be obtained as (21) and(22). From (21) and (22), it can be found that the mismatches $\Delta \mathrm{R}_{\mathrm{mismatch\_41}}$ and $\Delta \mathrm{R}_{\mathrm{mismatch\_32}}$ are averaged. Therefore, the inductor current ripples $\Delta i_{L1\_\mathrm{proposed}}$ and $\Delta i_{L2\_\mathrm{proposed}}$ can be smaller than conventional control $\Delta i_{L1\_\mathrm{convention}}$ and $\Delta i_{L2\_\mathrm{convention}}$, respectively.

$$V_{\mathrm{CF}} = \frac{1}{2}\left(V_{\mathrm{in}} - I_{L\_\mathrm{ave}}\left(\Delta R_{\mathrm{mismatch\_4,1}} + \Delta R_{\mathrm{mismatch\_3,2}}\right)\right) \quad (20)$$

$$\Delta i_{L1\_\mathrm{proposed}} = \frac{\frac{V_{\mathrm{in}}}{2} - I_{L\_\mathrm{ave}}\left(R_{\mathrm{DS\_3}} + R_{\mathrm{DS\_4}}\right) - I_L\left(\frac{\Delta R_{\mathrm{mismatch\_4,1}} + \Delta R_{\mathrm{mismatch\_3,2}}}{2}\right) - V_o}{L} \cdot \frac{2\left(V_{\mathrm{out}} + I_L\left(R_{\mathrm{DS\_3}} + R_{\mathrm{DS\_4}}\right)\right)_s}{\left(V_{\mathrm{in}} - I_{L\_\mathrm{ave}}\left(\Delta R_{\mathrm{mismatch\_4,1}} + \Delta R_{\mathrm{mismatch\_3,2}}\right)\right)} \cdot \frac{1}{2} T_s \quad (21)$$

$$\Delta i_{L2\_\mathrm{proposed}} = \frac{\frac{V_{\mathrm{in}}}{2} - I_{L\_\mathrm{ave}}\left(R_{\mathrm{DS\_3}} + R_{\mathrm{DS\_4}}\right) - I_{L\_\mathrm{ave}}\left(\frac{\Delta R_{\mathrm{mismatch\_4,1}} + \Delta R_{\mathrm{mismatch\_3,2}}}{2}\right) - V_o}{L} \cdot \frac{2\left(V_{\mathrm{out}} + I_L\left(R_{\mathrm{DS\_3}} + R_{\mathrm{DS\_4}}\right)\right)_s}{\left(V_{\mathrm{in}} - I_{L\_\mathrm{ave}}\left(\Delta R_{\mathrm{mismatch\_4,1}} + \Delta R_{\mathrm{mismatch\_3,2}}\right)\right)} \cdot \frac{1}{2} T_s. \quad (22)$$

For example, $R_{ds\_1} = 30\,\mathrm{m\Omega}$, $R_{ds\_2} = 15\,\mathrm{m\Omega}$, $R_{ds\_3} = 10\,\mathrm{m\Omega}$, $R_{ds\_4} = 10\,\mathrm{m\Omega}$, $V_{\mathrm{in}} = 5$ V, $V_o = 2$ V, $L = 470$ nH, $T_s = 1.33\ \mu$s (750 kHz), and $I_{L\_\mathrm{ave}} = I_o = 6$ A. $\Delta i_{L1\_\mathrm{convention}}$ and $\Delta i_{L2\_\mathrm{convention}}$ are 0.818 A and 0.888 A by (18) and (19), respectively. $\Delta i_{L1\_\mathrm{proposed}}$ and $\Delta i_{L2\_\mathrm{proposed}}$ are 0.853 A and 0.853 mA by (21) and (22), respectively. It can be found that the proposed control has a smaller inductor current ripple ($\Delta i_{L1\_\mathrm{proposed}} = \Delta i_{L2\_\mathrm{proposed}} = 0.853$ A) than the convention technique ($\Delta i_{L2\_\mathrm{convention}} = 0.888$ A). The ripple factor ($\Delta i_L / i_{L\_\mathrm{ave}}$) of the proposed technique is 0.142, and the conventional is 0.148. The proposed control improves the 4% ripple factor of the convention technique.

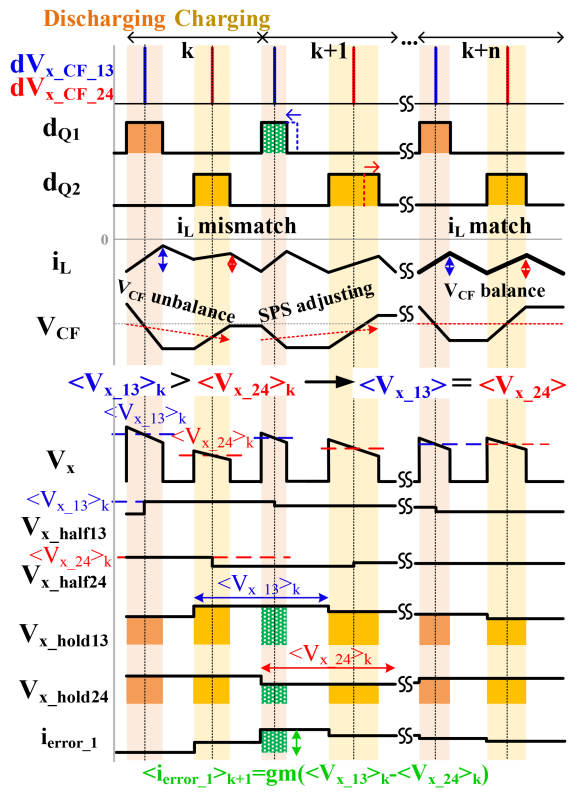


Fig. 8. Operation of the proposed flying capacitor control loop.

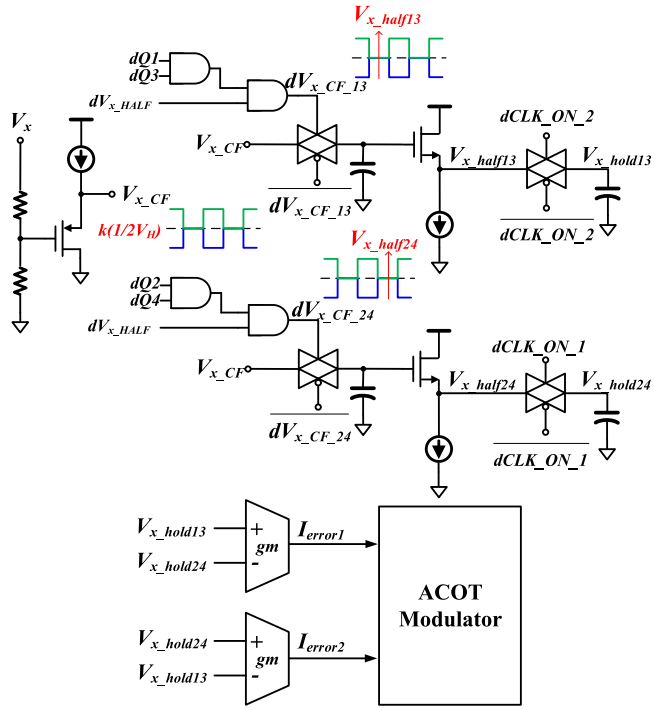


Fig. 9. Implementation of the proposed flying capacitor control loop.

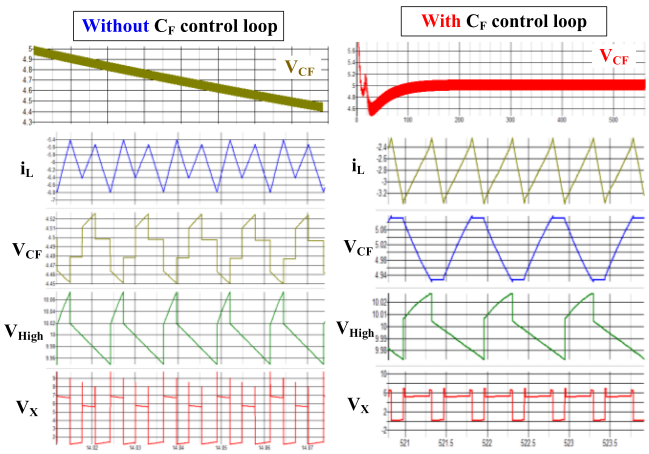


Fig. 10. SIMPLIS simulation waveforms of boost mode about with and without flying capacitor control loop.

The operation of the flying capacitor control loop is shown in Fig. 8. The V_x sensing method is introduced, which senses V_x at half of ON-time to represent the average value of switching node voltage. The signal *dVx*_CF_13 or *dVx*_CF_24 is generated from the ACOT modulator sensing the *k*th cycle's average *Vx* during flying capacitor discharging or charging. It would be sensed in the first S/H circuit as V_{x_half13} or V_{x_half24}.

After the *dCLK_ON* signal is triggered, which represents the ON instant of another power switch, the sensed value is stored in V_{x_hold13} or V_{x_hold24}. At that time, the error voltage between flying capacitor charging and discharging transfer into current, i.e., $i_{error,}$ drawing into or out of the ON-time generator through transconductance amplifiers (gm). The transconductance of the gm circuit is designed to have enough regulation accuracy for the flying capacitor control loop. The ON-time slightly changes in an opposite way and makes V_x at the same position during flying capacitor charging and discharging. Eventually, the flying capacitor avoids voltage runaway, and the inductor current ripple can be minimized. The reason for using two S/Hs is that when the first S/H is sensing $V_{x,13}$ of the $(k+1)$th cycle, and the second S/H can simultaneously compare the previous two V_x, which are $V_{x,13}$ and $V_{x,13}$ of the *k*th cycle and adjust the length of ON-time at the same time.

Fig. 9 shows the implementation of the flying capacitor control loop. The first consideration is the discharging path as the voltage on the capacitor of S/H is higher than the sampled switching voltage. Therefore, source followers are introduced before the voltage flows through the set of S/H. In addition, the p-type source follower separates V_x and $V_{x\_CF.}$ The n-type source followers are put after the sampled capacitor to separate the circuit and cancel the voltage deviation due to source followers.

To verify the proposed SPS technique, the SIMPLIS simulations of the TL boost converter without and with a flying capacitor control loop are depicted in Fig. 10. Switch Q_1 to Q_4 are ideal switches with ON-resistance of 22.2 mΩ, 18.9 mΩ, 12.4 mΩ, and 12.7 mΩ, respectively. The dc resistance of the inductor is the value of 21 mΩ. The closed loops include the inner loop with VIC, the flying capacitor control loop, and the outer voltage loop. Voltage runaway and the inductor ripple mismatch without a flying capacitor control loop in simulation occurs. The waveforms show that the switching voltage is unequal during the

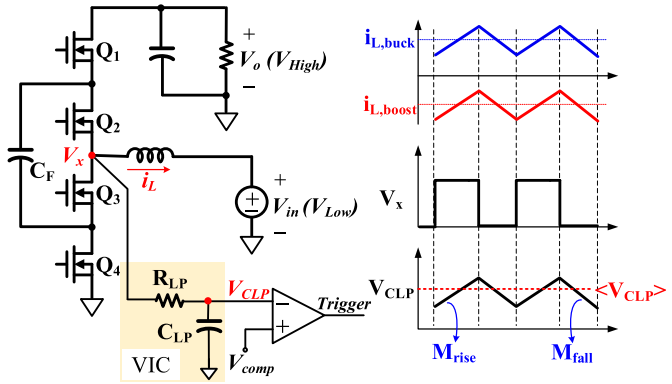


Fig. 11. Circuit diagram and time waveform of the VIC circuit.

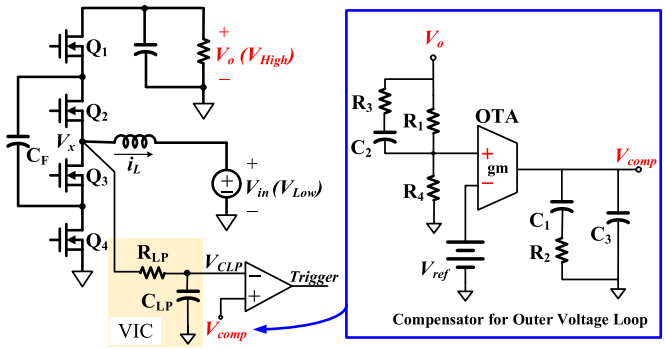


Fig. 12. Implementation of compensation in TL boost converter.

charging and discharging periods. After adding the proposed technique, the flying capacitor voltage and the inductor current ripple are calibrated well.

C. Bidirectional Control Circuit

A VIC circuit is introduced for the inner loop and shared for both directions to reduce area as much as possible, apart from the flying capacitor control loop. As shown in Fig. 11, considering to sense the same direction of the inductor current, the inductor current of boost mode is in phase with TL buck but has a reversed dc level, that is, $i_{L,\mathrm{boost}}$ is negative. To solve the negative value issue in boost mode and consider a common sensing method for both directions, a VIC circuit is proposed. By SPS of switching voltage, the pulse-like waveform of V_x flows through a low pass filter composed of R_{LP} and C_{LP}, and then generates the triangle waveform, V_{CLP}, in phase with inductor current. Assume the time constant of low-pass filter τ_{LP} is much larger than the switching period where τ_{LP} represents R_{LP} times C_{LP}. Without considering the effect of ON-resistance, the rising slope M_{rise} and the falling slope M_{fall} of V_x during $D_1 < 0.5$ can be derived as (23) and (24), respectively. It can be seen that VIC slopes in (23) and (24) and the inductor current ripple Δi_L given by (25) are both proportional to the voltage across the inductor, i.e., V_L. So, it is inferred that V_{CLP} and the inductor current are in phase. Thus, the *RC* value can be seen as the sensing gain, and we do not need to match the time constant of this *RC* value with the inductor time constant. Besides, the average of V_{CLP} that can be obtained from (26) is always positive in both directions. Hence, the issue of the negative value of the inductor current in boost mode can be solved. As a result, the VIC technique can work as the current ripple required for the inner loop in both modes.

$$M_{\mathrm{rise}} = \frac{V_{\mathrm{High}} - V_{\mathrm{CF}} - V_{\mathrm{Low}}}{R_{\mathrm{LP}} \cdot C_{\mathrm{LP}}} \tag{23}$$

$$M_{\mathrm{fall}} = \frac{V_{\mathrm{CF}} - V_{\mathrm{Low}}}{R_{\mathrm{LP}} \cdot C_{\mathrm{LP}}} \tag{24}$$

$$\Delta i_{\mathrm{L}} = \frac{V_{\mathrm{L}}}{L} \cdot \Delta t \tag{25}$$

$$< \mathrm{V_{CLP}} > \; = \mathrm{D_1} \cdot V_{\mathrm{High}} - 2 \cdot I_{\mathrm{L}} \cdot R_{\mathrm{DS}} \cong V_{\mathrm{Low}}. \tag{26}$$

The slope compensation of the inner loop and the outer loop polarity need to be taken into consideration for the loop stability. On the one hand, the inner loop would be unstable without slope compensation. The detailed derivation of required slope compensation will be published in another paper owing to the complex derivation. On the other hand, the outer voltage loop polarity needs to be modified in the TL boost converter. Based on the upper bridge control of the proposed control, the ideal duty ratio without considering the ON-resistance of switches and dc resistance of the inductor in boost mode and CCM is derived as follows according to the volt-sec balance in steady state:

$$D_{1,\mathrm{ideal}} = \frac{V_{\mathrm{in,boost}}}{V_{\mathrm{out,boost}}} = \frac{V_{\mathrm{Low}}}{V_{\mathrm{High}}}. \tag{27}$$

Observing the relationship between the output voltage and the ideal duty cycle of Q_1, $D_{1,\mathrm{ideal}}$ must become larger to stabilize the output voltage when the output voltage is higher than the regulation target. To obtain the above relationship, the compensator with OTA is implemented in Fig. 12, which lets the feedback of output voltage flow into the positive input of OTA. As shown in Fig. 4, the feedback of output voltage flows into OTA's negative input for buck mode instead. There is no way to use OPA compensation in this work because only OTA can bring feedback to the positive input terminal of the OTA without affecting the transfer function of the original Type III compensation.

D. ACOT Modulator

The conventional COT modulator is implemented by the fixed current source (i_{ON}) and the fixed reference voltage (V_{ref}). However, the frequency is proportional to the duty cycle as shown in (28) due to the fixed T_{ON}. Thus, the conventional COT topology suffers severe frequency variation at input and output voltage variation which degrades the performance of analog circuits and induces unpredictable electromagnetic interference issues [22], [23]. Consequently, the ACOT control is introduced.

$$f_s = \frac{D}{T_{\mathrm{ON}}}, \text{ where } T_{\mathrm{ON}} = \frac{C_{\mathrm{ON}} \cdot V_{\mathrm{ref}}}{i_{\mathrm{ON}}}. \tag{28}$$

The duty cycle is derived below to design ACOT with pseudoconstant frequency, including the nonideal case such as

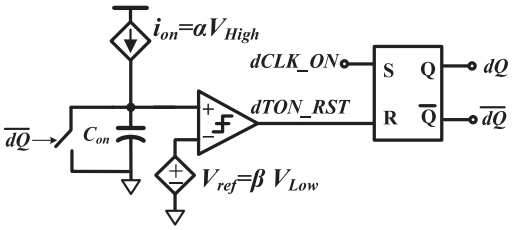


Fig. 13. Conventional structure of ACOT.

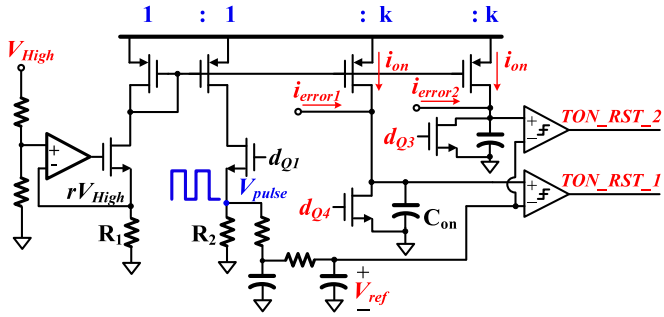


Fig. 14. Implementation of the proposed ACOT modulator.

ON-resistance and inductor dc resistance (DCR). Assume the flying capacitor is balanced. According to the volt-sec balance in steady state, (29), which extends from (27), presents that the actual duty cycle of Q_1 with the nonideal case is derived where $D_{1,\text{ideal}}$ equals V_{Low} divided by V_{High}. Obviously, the parasitic resistances cause voltage drop along with the increase of the inductor current.

$$D_{1,\text{actual}} \cong \frac{V_{\text{Low}} + I_L \cdot (2R_{\text{DS}} + \text{DCR})}{V_{\text{High}}} = D_{1,\text{ideal}} + \Delta D. \tag{29}$$

The conventional ACOT structure in Fig. 13 shows that T_{ON} is proportional to V_{Low} divided by V_{High} such that the switching frequency in the original design ($f_{\text{sw,ideal}}$) shown in (30) maintains constant.

$$f_{\text{sw,ideal}} = \frac{D_{\text{ideal}}}{T_{\text{ON}}} \propto \frac{\left(\frac{V_{\text{Low}}}{V_{\text{High}}}\right)}{\left(\frac{V_{\text{Low}}}{V_{\text{High}}}\right)} = \text{constant}. \tag{30}$$

However, the frequency deviation at load change due to practical parasitic is ignored. To solve this issue, T_{ON} is designed to be proportional to D_{actual} in the buck converter [22]. However, T_{ON} design in the boost converter is complicated due to the ideal duty equal to (V_{High}-V_{Low}) divided by V_{High} as the lower bridge control. The recent designs solve part of the issue by making T_{ON} proportional to (V_{High}-V_{Low}) or (V_{High}-V_{Low}) divided by V_{High} but still have the load effect from nonideal resistances [27], [28].

The proposed ACOT modulator in this article considers the load condition in the boost converter and minimizes frequency variation in both directions. With the upper bridge control of both TL buck and TL boost converters, T_{ON} of proposed ACOT modulator in Fig. 14 is proportional to $D_{1,\text{actual}}$. That is, design i_{ON} to be proportional to V_{High}, and V_{ref} to be proportional to

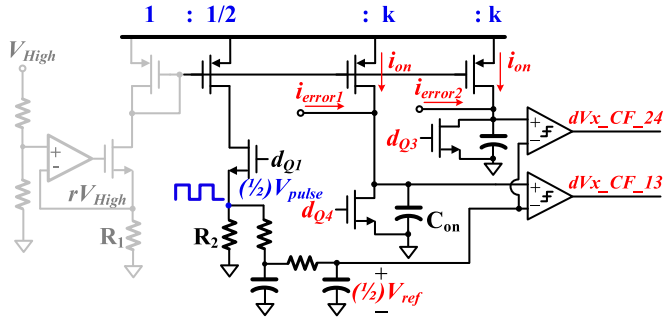


Fig. 15. Implementation of the half-ON-time generator.

($D_{1,\text{actual}} \cdot V_{\text{High}}$) as

$$T_{\text{ON}} \propto \frac{D_{1,\text{actual}} \cdot V_{\text{High}} \cdot C_{\text{ON}}}{gm \cdot V_{\text{High}}} = \frac{C_{\text{ON}}}{gm} \cdot D_{1,\text{actual}}. \tag{31}$$

Then, switching frequency variation is minimized at various input voltage, output voltage, and load, as can be seen from the switching frequency derived as follows:

$$f_{\text{sw,actual}} = \frac{D_{1,\text{actual}}}{T_{\text{ON}}} = \frac{D_{1,\text{actual}} \cdot \text{gm}}{D_{1,\text{actual}} \cdot C_{\text{ON}}} = \text{constant}. \tag{32}$$

The implementation of the proposed ACOT modulator combines i_{ON} and V_{ref} from the same source, i.e., V_{High}, to save the use of elements. i_{ON} can be obtained by simple transconductance, and V_{ref} is generated by the average of V_{pulse}, which equals $D_{1,\text{actual}}$ times V_{High}. To reduce the circuit area and timing mismatch, it is beneficial for two pairs of the clock signal to share the same V_{ref}. Instead of directly utilizing V_{High} to switch V_{pulse}, the benefit of using transconductance with a switch that turns ON along with d_{Q1} to produce V_{pulse} is a reduction of the V_{DS} drop of the switch, which can increase accuracy. The error currents i_{error1} and i_{error2} from the flying capacitor control loop summarize with i_{ON} and transform the ON-time pulse indirectly. Furthermore, the half-ON-time trigger signals *dVx_CF_13* and *dVx_CF_24*, for sensing the average V_x for the flying capacitor control loop, can be merged with the proposed ACOT as well and save the use of elements as depicted in Fig. 15. As long as adding one more set of the pulse generator, we can generate half of V_{pulse} by halving the current source depending on V_{High}.

E. System Simulation

The full transistor-level TL converter design, including flying capacitor control, ACOT modulator, and bidirectional control, is verified by simulation in Spectre under a CMOS 0.18 μm process. The parameters in the simulation are the same as in the experiment. The steady-state waveform is depicted in Fig. 16, where $V_{\text{High}} = 12$ V, $V_{\text{Low}} = 5$ V, and $i_{\text{L}} = 4$ A for both modes. The flying capacitor balance loop works well to maintain the switching voltage equal during charging and discharging periods in both modes. The bidirectional design in the outer loop also performs properly to ensure the feedback acts like the aforementioned design.

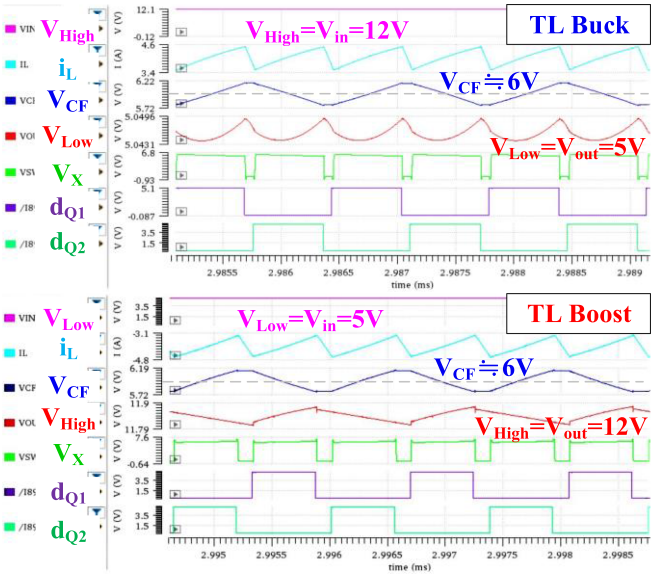


Fig. 16. TL converter full transistor-level simulation in steady-state waveforms.

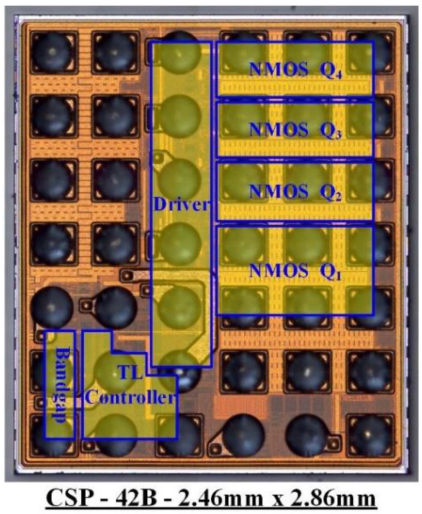


Fig. 17. Chip photograph of the proposed TL converter control IC.

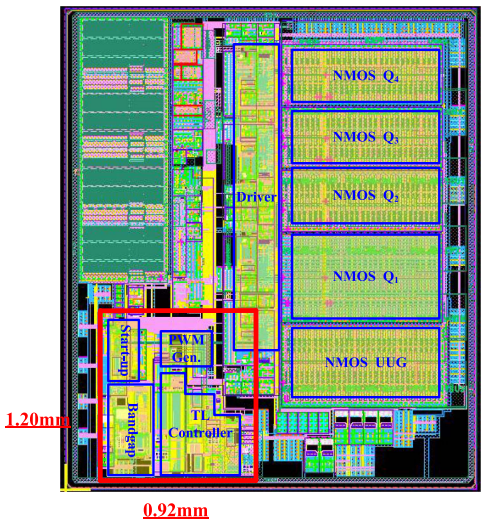


Fig. 18. Layout photograph of the proposed TL converter control IC.

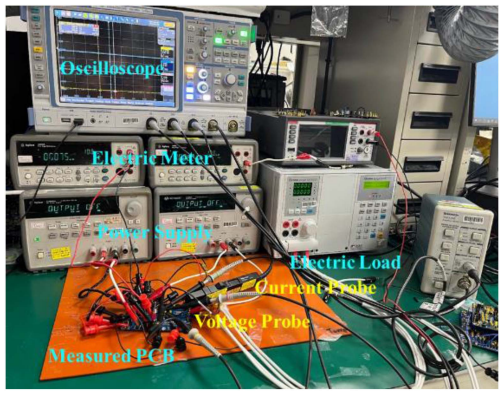
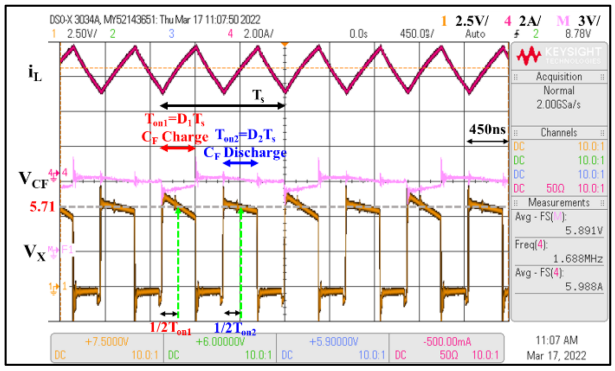


Fig. 19. Measurement environment photograph.

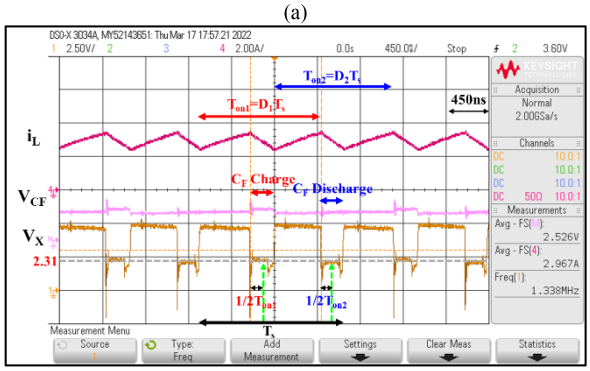
III. Experimental Results

The proposed bidirectional TL converter was fabricated in a CMOS 0.18 μm process and the chip-scale package. This chip occupies around 2.46 mm × 2.86 mm with 42 solder balls, as presented in Fig. 17 . Fig. 18 shows the layout photo of the proposed IC. Except for passive components, the transistor-level ON-chip design includes power switches, bidirectional TL controllers, and other analog circuits. The test conditions and designed parameters are $V_{\rm High}$ = 5–12 V, $V_{\rm Low}$ = 3–5.5 V, per-switch switching frequency = 750 kHz, total switching frequency (switching frequency seen by the inductor) = 1.5 MHz, L = 470 nH, output capacitance $C_{\rm O}$ = 20 μF, flying capacitance is 10 μF, full load of TL buck = 6 A, and full load of TL boost = 2.4 A for the charger application. As a result of TL characteristics, the voltage stress of the first switch Q_1 is chosen with 12 V considering start-up, and others are chosen with 6 V. As presented in Fig. 19, instruments are required in the experiment, such as a power supply for offering the input power, an electric load for providing output load, an oscilloscope with voltage probe and current probe for waveforms tracing, and an electric meter for the voltage or the current measurement.

Figs. 20 and 21 show the measured steady-state waveforms of the proposed bidirectional TL converter under buck mode and boost mode. For buck mode, Fig. 20(a) depicts the case of the duty cycle of Q_1 lower than 0.5, where $V_{\rm High}$ = 12 V, $V_{\rm Low}$ = 3 V, full load = 6 A, and $V_{\rm CF}$ is balanced at 5.891 V, and the duty cycle of Q_1 larger than 0.5 are illustrated in Fig. 20(b), where $V_{\rm High}$ = 5 V, $V_{\rm Low}$ = 4 V, the load = 3 A, and $V_{\rm CF}$ is balanced at 2.526 V. Due to the larger voltage rating of Q_1, the ON-resistance of Q_1 is higher than the others. Thus, as shown in Fig. 20(a), compared to the period of $T_{\rm ON2}$, there is a steeper slope of switching voltage V_x, especially in full load during $T_{\rm ON1}$, where Q_1 and Q_3 turn ON, and the flying capacitor is in the charging period. Additionally, (9) is verified by measured $V_{\rm CF}$ in Fig. 20(a). $R_{\rm DS,Q1}$ to $R_{\rm DS,Q4}$ are provided as follows: 22.2 mΩ, 18.9 mΩ, 12.4 mΩ, and 12.7 mΩ, and $R_{\rm p}$, which represents the PCB parasitic resistance from the IC pin of the high side to the

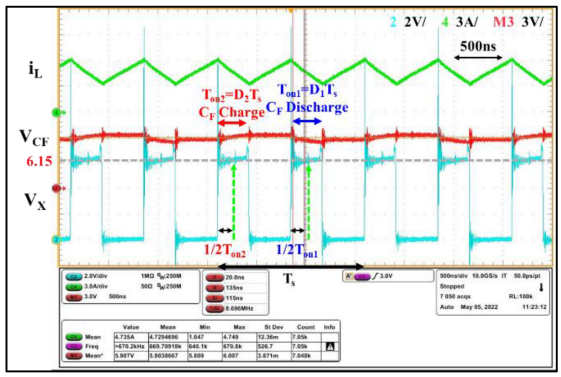


(a)

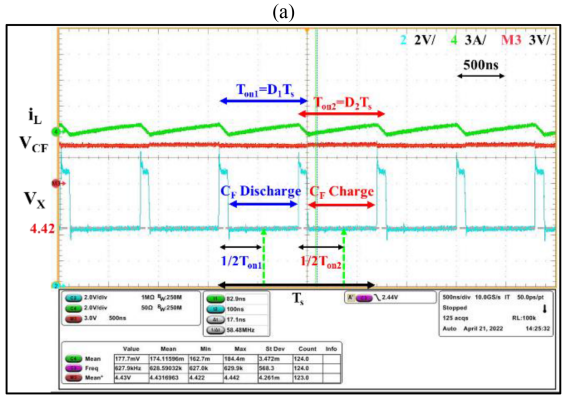


(b)

Fig. 20. Measured steady-state waveforms of TL buck converter. (a) $D_1 < 0.5$. (b) $D_1 > 0.5$.

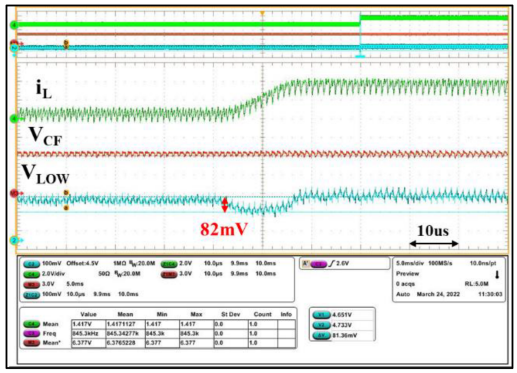


(a)

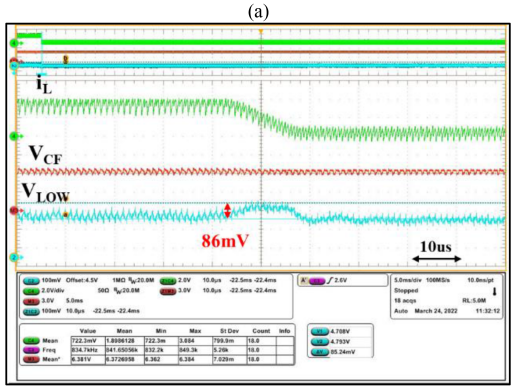


(b)

Fig. 21. Measured steady-state waveforms of TL boost converter. (a) $D_1 < 0.5$. (b) $D_1 > 0.5$.



(a)

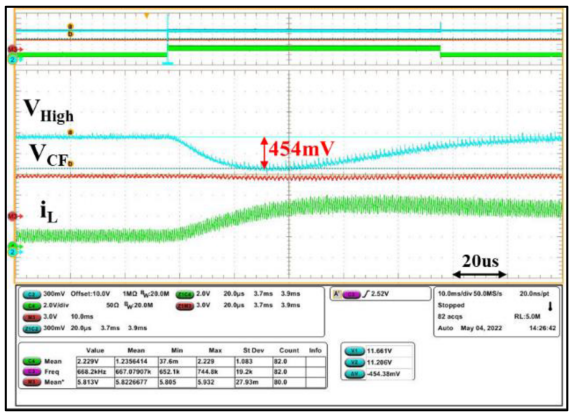


(b)

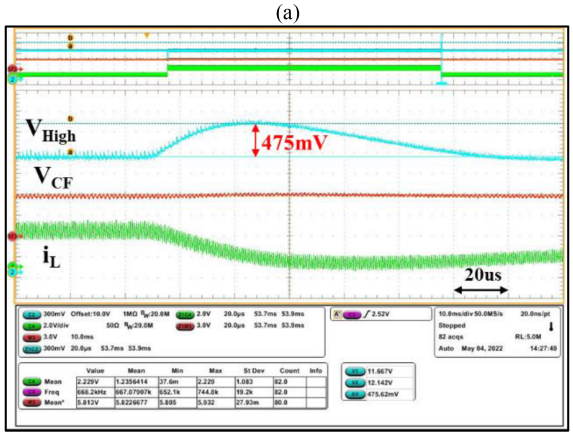
Fig. 22. Measured step-load transient response waveforms of TL buck converter. (a) Step-up of zoom in. (b) Step-down of zoom in.

PCB pin which connects to the supply, is about 6.4 mΩ. The total resistance on the charging path with the parasitic resistance on PCB is about 41 mΩ and the total resistance on the discharging path is about 31.2 mΩ. Therefore, the calculation of V_{CF} with (9) is about 5.8956 V. Compared to the measurement result of 5.891 V, it is almost the same between the calculation and the measurement. Moreover, whether in heavy or light, V_x at half of on time, which represents the average of V_x during charging and discharging periods, can be accurately regulated by the balance control. Hence, the flying capacitor voltage is balanced. Besides, there is no inductor current mismatch in buck mode, as presented in 6. Fig. 21(a) illustrates the case of the duty cycle of Q_1 lower than 0.5 in boost mode, where $V_{\mathrm{Low}} = 3$ V, $V_{\mathrm{High}} = 12$ V, the load = 1 A, and V_{CF} is balanced at 5.907 V, and the duty cycle of Q_1 larger than 0.5 are depicted in Fig. 21(b), where $V_{\mathrm{Low}} = 5$ V, $V_{\mathrm{High}} = 9$ V, the load = 100 mA, and V_{CF} is balanced at 4.43 V. The flying capacitor balance loop works well in boost mode as well. The balanced average V_x values are 6.15 V and 4.42 V in Fig. 21(a) and (b), respectively. Additionally, the steady-state waveforms present the TL switching voltage, where V_x changes from 0 to $V_{\mathrm{High}}/2$ during the duty cycle of Q_1 lower than 0.5 and from $V_{\mathrm{High}}/2$ to V_{High} during the duty cycle of Q_1 larger than 0.5.

The measured step-up and step-down load transient response with the load current slew rate of 250 mA/μs are depicted in Figs. 22 and 23. For the buck mode, the load current step is from 1 to 4A, where $V_{\mathrm{High}} = 12$ V and $V_{\mathrm{Low}} = 5$ V. The load



(a)



(b)

Fig. 23. Measured step-load transient response waveforms of TL boost converter. (a) Step-up of zoom in. (b) Step-down of zoom in.

current step is from 420 mA to 1.2 A, where $V_{\rm High} = 12$ V and $V_{\rm Low} = 4$ V in boost mode. As illustrated in Fig. 22(a) and (b), the undershoot voltage and the overshoot voltage in buck mode are 82 mV and 86 mV, respectively. In addition, the overshoot voltage and the undershoot voltage in boost mode are also presented in Figs. 19(b) and 20(a), respectively. Both the undershoot voltage and the overshoot voltage are over 450 mV.

Measured switching frequencies at various conditions in boost mode for the TL converter are shown in Fig. 24. The maximum frequency variation is only 80 kHz compared to the designed total switching frequency of 1.5 MHz. The percentage of the frequency variation of the proposed ACOT control is less than 6% among the maximum load of 1.25 A. Compared to recent papers' variations which are 13% among the maximum load 0.4 A [28] and 30% among the maximum load 0.7 A [27] in conventional boost converters with ACOT control, the proposed ACOT control achieves a smaller percentage of variation in a wider load range. The proposed ACOT control in the buck converter also cancels the effect of input voltage, output voltage, and output load. The maximum frequency variation is only 75 kHz, which is less than 6% among the maximum load 4 A.

Figs. 25 and 26 show the measured efficiencies of the TL converter in buck mode and boost mode, respectively. The peak efficiency of buck mode is 96.02% at the output load 1 A with $V_{\rm High} = 7$ V, and $V_{\rm Low} = 5.5$ V. The measured efficiency is very

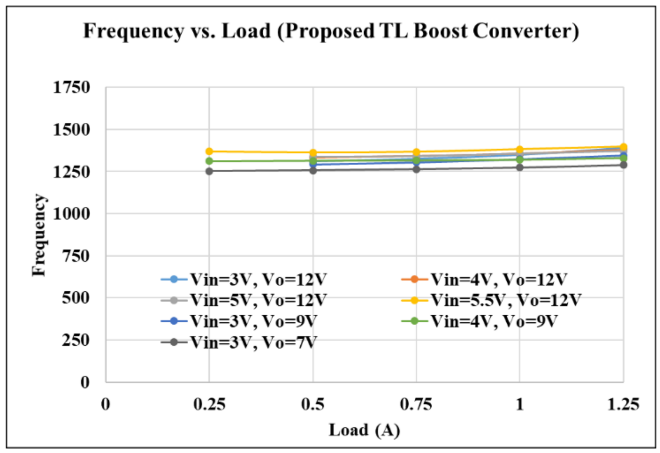


Fig. 24. Measured switching frequency at various conditions in boost mode.

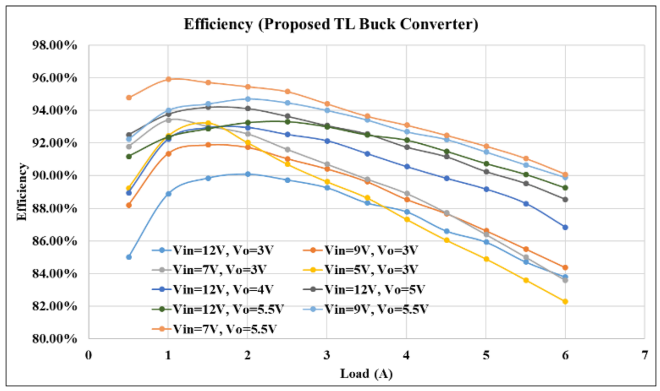


Fig. 25. Measured efficiency for TL buck converter.

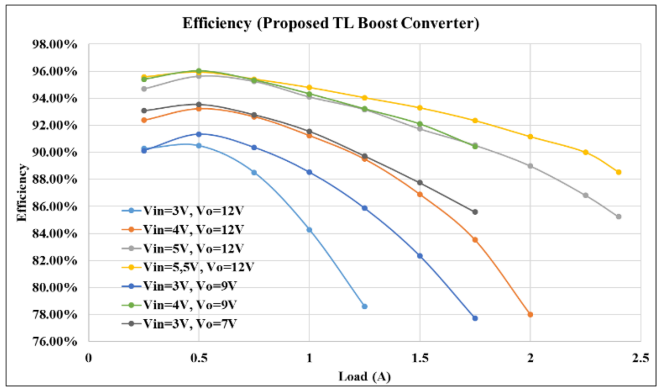


Fig. 26. Measured efficiency for TL boost converter.

close to the calculated result. The peak efficiency of boost mode achieves 96.02% at the output load 0.5 A with $V_{\rm High} = 9$ V and $V_{\rm Low} = 4$ V.

The measurement results are compared with the state-of-the-art TL converters with IC implementation as shown in Table I. It can be noticed that the proposed TL converter is the first paper to propose bidirectional control in TL converters with IC implementation. Compared to other IC implementation papers,

TABLE I
SUMMARY OF PERFORMANCE COMPARISON

	[35] ISCAS'23	[11] TPE'21	[17] JSSC'20	This work
CMOS process	CMOS 180 nm	CMOS 130 nm	CMOS 65 nm	**CMOS 180 nm**
Topology	TL buck	TL buck	TL boost	**Bidirectional TL**
Highside Voltage [V]	6	8	2.4–5	**5–12**
Lowside Voltage [ ]	0.4–5.6	1.8–3.3	0.3~3	**3–5.5**
Peak Output Current [A]	1000 m	550 m	83 m	**TL buck: 7.064 TL boost: 2.666**
Switching freq. [Hz]	2 M	0.8 ~ 1 M	0.5~45 M	**750 k/per switch; 1.5 M/total**
Peak Eff. @V_{High}[V]/V_{Low}[V]	N/A	88.6% @8/3	96.8% @4/3	**96.02% @4/9**
Flying Cap. balance	Loop-Free (V_{in}/2)	Loop-Free (V_{in}/2)	Intrinsic (V_{in}/2)	**Single point (Vx) Sense (V_{in} -$I_L R_{mismatch}$)/2**
Pseudo-fixed frequency COT	No	No	No	**Yes**
Chip area [mm*mm]	No	3.7*4.5	0.53*0.53	**2.46*2.86**

*N/A: Not Applicable

the proposed bidirectional TL converter with the SPS flying capacitor balance method operates at a higher voltage and output current level and achieves higher than 95% of the peak efficiency. Besides, the paper achieves pseudofixed frequency for COT control while others do not implement this technique.

IV. CONCLUSION

This article presents a bidirectional TL converter with an SPS technique for flying capacitor balance and was implemented in a standard CMOS 0.18 μm process. The bidirectional design shares control for the two operation directions to minimize the control circuit area. The flying capacitor control loop with SPS simplifies the balance loop and reduces the inductor current ripple mismatch. The proposed ACOT modulator with upper bridge control in both directions effectively suppresses the frequency variation, especially for boost mode, which is less than 6% within the wider load range of 1.25 A compared to previous works. Undershoot and overshoot voltages of load transient with the slew rate of 250 mA/μs are only 82 mV and 86 mV in a wide load step from 1 A to 4 A in buck mode. The proposed TL buck converter achieves about 95.89% efficiency at 1-A load, where the input voltage is 7 V and the output voltage is 5.5 V. For the proposed TL boost converter, the efficiency is up to 96.02% at 0.5-A load, where the input voltage is 4 V and the output voltage is 9 V. As a result, the measured result verifies the proposed bidirectional TL converter in terms of high efficiency, low switching frequency variation, and bidirectional design feasibility including flying capacitor balance and bidirectional control.

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