Very-High-Frequency Resonant Dual-Channel LED Driver With Capacitive Current Balance and Low Voltage Stress on Diodes

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***Abstract*—By combining the existing very-high-frequency (VHF) dc/dc converter and resonant switched capacitor (SC) techniques, this article proposes a VHF dual-channel light-emitting diode (LED) driver with capacitive current balance. Unlike the conventional capacitive current-balancing LED drivers, the proposed one has higher power density, and no current spike occurred at the switching moment. Due to the problem of higher voltage stress on the diode in resonant operation for the existing VHF LED drivers, the proposed one makes both diodes that are alternately turned ON clamp to each other by extending one more LED channel without adding any resonant components. As a result, the voltage stress on diode can be reduced to the total dc output voltage, which is beneficial for selecting switching components. In addition, the parasitic capacitance of both diodes can be a part of the required capacitor regardless of their inconsistency, which means that they can be absorbed by one discrete capacitor and further promote power density. The analysis and design consideration of the proposed LED driver are studied in detail. With the ON–OFF control strategy, the feasibility and theoretical analysis are experimentally verified with a rated output power of 12 W dual-channel prototype.**

***Index Terms*—Current balance, light-emitting diodes (LEDs), resonance, switched capacitor (SC), very high frequency (VHF).**

I. Introduction

With the advantages of long lifespan, high luminous efficacy, and small size, high-brightness light-emitting diodes (LEDs) are gradually replacing high-intensity discharge, incandescent and fluorescent lamps in various applications, such as residential lighting, automobiles, and backlighting [1], [2], [3]. Due to the limited brightness of a single LED, multiple LEDs usually operate together for the requirement of brightness. In fact, the inherited features of negative temperature coefficient and manufacturing tolerance, as well as nonlinear volt-ampere characteristics, have a substantial impact on whether the brightness of LEDs can be balanced. The simplest solution is to connect all the LEDs in a series manner. However, the sharp increase in output terminal voltage may exceed the safety limit and affect the reliability of the LEDs [4]. To address this problem, it is necessary to use a current-balancing technique on the parallel LED structure to balance their brightness.

So far, the current-balancing technique can be categorized into two types: active and passive methods. The active method is implemented by inserting a switch into each LED string, which can control their current independently [5], [6]. However, it suffers some drawbacks of more active switches, more current sensors, complex drive circuits, and control strategies. Passive methods, such as the inductive and capacitive schemes, are in contrast to active methods and can avoid these problems. For the inductive scheme, the coupled inductors are used to balance current for multiple LED strings, as presented in [7], [8], and [9]. However, the bulky magnetic components not only occupy more space, but also their sensitive coupling coefficient and leakage inductance pose design challenges for current balance.

For the capacitive scheme, it has advantages of high power density and cost effectiveness, which has attracted more and more attention from both academia and industry. Based on the charge balancing principle of capacitors, the ability to balance current is realized by the capacitors' charging current and discharging current flowing through two LED strings, respectively. The power level for the LED drivers mentioned in [10] can be categorized into three groups: high power (>100 W), middle power (25–100 W), and low power (<25 W). Most of these LED drivers are based on half-bridge and full-bridge structures, which are more suitable for high-power applications, such as street lighting and industrial lighting [11], [12]. But for the low- and middle-power applications, it is preferred to use simple structures, such as buck, boost, and buck–boost type. For example, a single-switch LED driver is presented in [13]. In addition to balance the current among LED strings using the switched capacitor (SC), the amounts of charge flowing into and out of the capacitor can also be regulated by adjusting the duty circle of the switch. However, the huge current spike that occurs at the switch-ON moment will shorten the device's lifespan [14]. In [15], the high-efficiency LED driver addresses this problem by using the resonant SCs. Although

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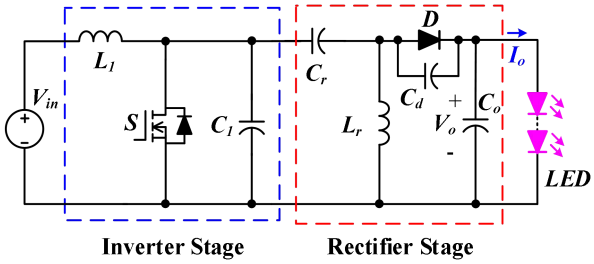


Fig. 1. Conventional VHF LED drive circuit [25].

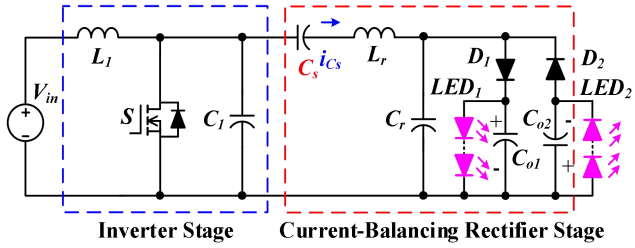


Fig. 2. Proposed VHF dual-channel LED driver.

these structures are simple enough, it is still expected to further promote the power density for low- and middle-power applications.

In recent years, based on zero-voltage-switching (ZVS) and zero-current-switching (ZCS) techniques, the dc–dc power converter operating at very high frequency (VHF, 30–300 MHz) has attracted great attention [16], [17], [18], [19], [20], [21], [22], [23]. Its power density and lifespan are improved, significantly, with the air core inductors and ceramic capacitors in SMD packages [24], [25], [26]. As a LED driver, the SEPIC VHF converter developed in [25] and [26] is the simplest structure, as shown in Fig. 1, which is composed of two switching components and six passive components for feeding a single LED string. Adding another rectifier stage in parallel appears to be a straightforward solution for extending dual-channel LED strings. However, the system will become so complex that its design process is more difficult and more components are required. Besides, due to the resonant operation, the diode is subjected to high reverse voltage stress, especially with more LEDs in series.

In this article, a VHF dual-channel current-balancing LED driver is developed, of which around hundreds of picofarads (pF) SC is used to share the current for both LED strings and takes part in the resonant process to regulated the rated output power. Unlike the conventional capacitive current-balancing LED drivers, the current spike of SC can be effectively suppressed by the resonant operation. Compared to the existing LED driver shown in Fig. 1, the proposed one has the following merits.

1) Reduced voltage stress on diodes to the total dc output voltage.
2) Extending one more LED channel without adding additional resonant components.
3) Parasitic capacitance of both diodes together can be a part of the required resonant capacitance regardless of their inconsistency.

With these advantages, the proposed LED driver is more suitable for low- and middle-power applications. The operating principle and analysis for both inverter stage and rectifier stage are discussed in detail. Combined with simulation verification, the design consideration is also studied. Finally, the experimental results verify the feasibility of the proposed LED driver and correctness of the theoretical analysis.

II. Proposed Dual-Channel LED Drivers

A. Circuit Configuration

As shown in Fig. 2, the proposed LED driver contains a conventional Class E inverter and a current-balancing rectifier. The inverter stage is responsible for generating an approximate half-sinusoidal ac voltage with an inductor L_1, a capacitor C_1, and a switch S. Due to the resonant operation of L_1 and C_1, the switch can operate at ZVS situation to reduce switching loss. Of course, to broaden the output power range, the Class E inverter can also be replaced with the push–pull and series–parallel inverters, as presented in [15] and [16].

Compared to rectifier stage of Fig. 1, the current-balancing rectifier has an additional LED channel with the same number of resonant components. The SC C_s is responsible for balancing the current of both LED strings. Specifically, when the capacitor C_r resonates with L_r and C_s until capacitor's voltage v_{Cr} reaches to v_{Co1}, the capacitor's current i_{Cs} forward flows through L_r-D_1-LED_1 until i_{Cs} decreases to zero naturally. Hence, the diode D_1 is turned OFF and operates in ZCS situation to reduce switching loss. Subsequently, the capacitor C_r continues to resonate with them until v_{Cr} reaches to v_{Co2}, the capacitor's current i_{Cs} reverse flows through LED_2-D_2-L_r until i_{Cs} decreases to zero naturally. Hence, the diode D_2 is turned OFF and operates in ZCS situation. By applying the ampere-second balance through the SC C_s, it can be found that the amounts of charge flowing into and out of the capacitor must be the same during one switching cycle. As a result, both parallel-connected LED strings can share the common average current without the need for additional current sensors and a balanced control strategy.

In addition to the current-balancing capability, the parasitic capacitance of both diodes can be absorbed together by capacitor C_r without considering the inconsistency of parasitic capacitance. In other words, the required capacitance C_r contains the parasitic capacitance of the diodes C_{D1} and C_{D2} and additional discrete capacitance C_{r_disc}, i.e., $C_r = C_{D1} + C_{D2} + C_{r\_\mathrm{disc}}$. As mentioned in [16], when the parasitic capacitance of the diodes is sufficient to provide the required capacitance, the discrete one can be removed. This feature of the proposed current-balancing circuit can further promote the power density and suppress the ringing between C_r and the parasitic inductance of diode package. Different from the existing VHF converters, both diodes that are alternately turned ON can clamp each other to avoid excessive voltage stress caused by the resonant operation, that is, their voltage stresses are both clamped to the total dc output voltages, which can be significantly reduced. This is beneficial for selecting diode and reducing costs. Furthermore, the hundreds of pF SC C_s as part of the resonant tank are always

operated in the resonance process, making the current spike suppressed, and the device's lifespan can be therefore improved.

B. Operating Principle

As analyzed in [17], the inverter stage can be equivalent to a sinusoidal source $v_{\rm sin}$ with a dc component $V_{\rm in}$, i.e.,

$$v_{\rm sin}(t) = V_{\rm in} + V_{\rm AC}\sin(\omega_s t + \varphi) \tag{1}$$

where $V_{\rm AC}$ is the amplitude of fundamental component, whereas ω_s is the angle frequency of $v_{\rm sin}$. Assuming that capacitor's voltage v_{C1} is a half-sinusoidal wave, $V_{\rm AC} = \pi V_{\rm in}/2$ can be obtained by Fourier transform.

To simplify the analysis, other assumptions are made as follows.

1) All the diodes are ideal, i.e., no ON-resistance, parasitic inductance, and capacitance as well as forward voltage drop.
2) All the passive components are also ideal, wherein the capacitor C_{o1} and C_{o2} are so large enough that their voltages can be regarded as constant, i.e., V_{Co1} and V_{Co2}.

Fig. 3 depicts the four operating modes of the proposed LED driver during one switching cycle and its typical waveforms of voltage and current are given in Fig. 4. The specific analysis of each operating modes is described as follow.

Mode I [t_0, t_1]: As shown in Fig. 3(a), all the diodes are turned OFF. The inductor L_r resonates with capacitors C_r and C_s, making the capacitor' voltage v_{Cr} returns to zero and then rises gradually. This mode will continue until capacitor' voltage v_{Cr} reaches to V_{Co1}.

Mode II [t_1, t_2]: As shown in Fig. 3(b), the diode D_1 is turned ON. The inductor L_r resonates with capacitor C_s, making the current i_{Cs} flows though LED_1 string. This mode will continue until the current i_{Cs} drops to 0. Hence, the diode D_1 is turned OFF naturally.

Mode III [t_2, t_3]: As shown in Fig. 3(c), all the diodes are turned OFF. The inductor L_r resonates with capacitors C_r and C_s, making the capacitor' voltage v_{Cr} returns to zero and then drops gradually. This mode will continue until capacitor' voltage v_{Cr} reaches to V_{Co2}.

Mode IV [t_3, t_4]: As shown in Fig. 3(d), the diode D_2 is turned ON. The inductor L_r resonates with capacitor C_s, making the current i_{Cs} flows though LED_2 string. This mode will continue until the current i_{Cs} returns to 0. Hence, the diode D_2 is turned OFF naturally.

C. Analysis of Current-Balancing Rectifier Stage

Based on the principle of ampere-second balance, the charge stored in C_r during mode *I* should be equal to the charge released from C_r during mode *III*, as illustrated in Fig. 4. Therefore, the variation of charge ΔQ_1 and ΔQ_3 can be estimated as

$$\begin{aligned}\Delta Q_1 = &-\Delta Q_3 = C_r\left(V_{Co1} - V_{Co2}\right)\\ &= C_r\left(I_{o1}R_{LED1} - I_{o2}R_{LED2}\right)\end{aligned} \tag{2}$$

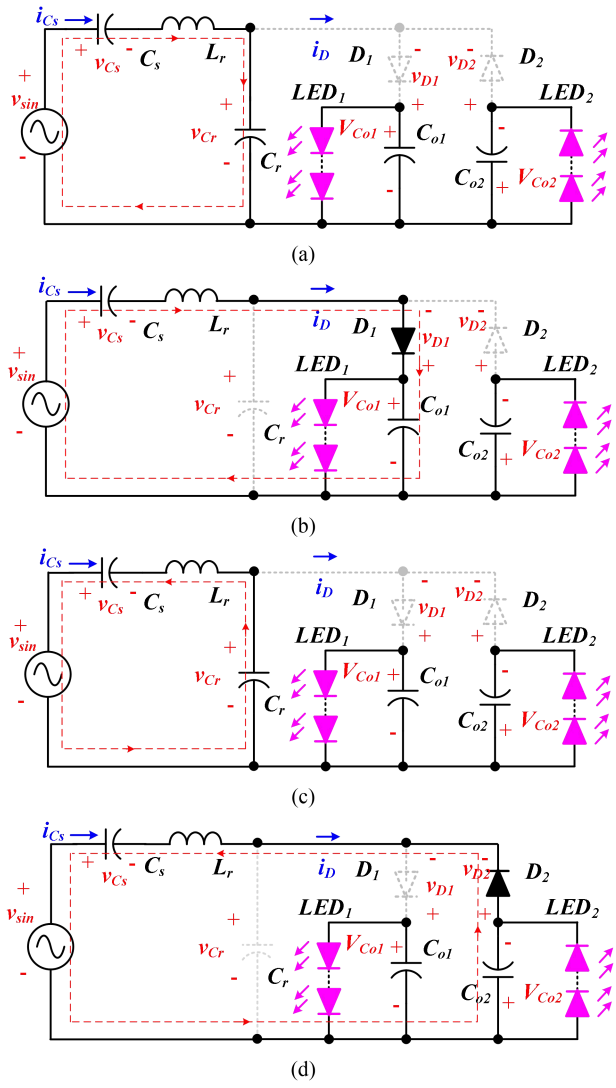


Fig. 3. Operating modes during one switching cycle. (a) Mode *I*. (b) Mode *II*. (c) Mode *III*. (d) Mode *IV*.

where R_{LED1} and R_{LED2} are the equivalent resistance of LED_1 and LED_2, respectively, whereas I_{o1} and I_{o2} are the average output current of LED_1 and LED_2, respectively.

Similarly, the variation of charge ΔQ_2 and ΔQ_4 can also be estimated as

$$\Delta Q_2 = -\Delta Q_4 = I_{o1}T_s = -I_{o2}T_s = \frac{2\pi I_o}{\omega_s} \tag{3}$$

where T_s is the switching cycle and I_o is the absolute value of I_{o1} and I_{o2}.

Due to the symmetry of the operating mode for both positive and negative half cycles, the average voltage of v_{Cr} during one switching cycle can be derived as

$$V_{Cr\_avg} = \frac{V_{Co1} + V_{Co2}}{2} = \frac{I_o\left(R_{LED1} - R_{LED2}\right)}{2}. \tag{4}$$

In addition, the variation of voltage across capacitor C_r can be given by

$$\Delta v_{Cr} = V_{Co1} - V_{Co2} = I_o\left(R_{LED1} + R_{LED2}\right). \tag{5}$$

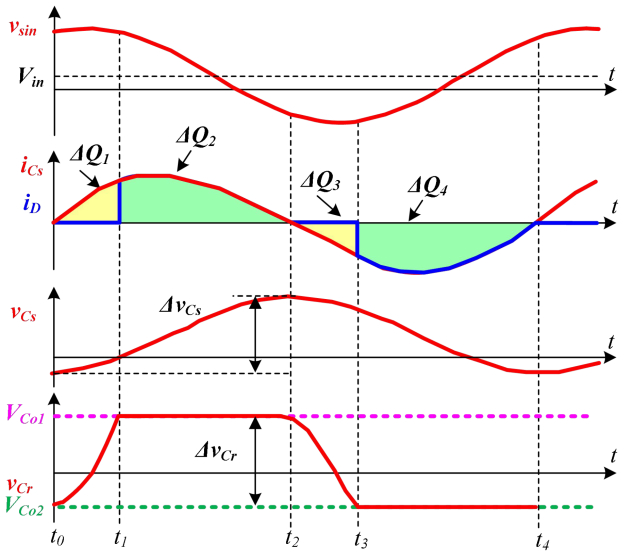


Fig. 4. Typical waveforms of the proposed dual-channel LED driver.

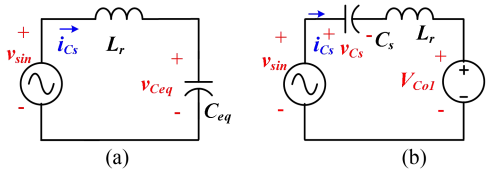


Fig. 5. Equivalent circuits of the rectifier stage for positive half cycles. (a) When D_1 is OFF. (b) When D_1 is ON.

Since the average voltage of inductor L_r is 0 and that of sinusoidal source $v_{\sin}$ is V_{in}, the average voltage of v_{Cs} is derived as

$$V_{Cs\_avg} = V_{\text{in}} - \frac{I_o\left(R_{LED1} + R_{LED2}\right)}{2}. \tag{6}$$

From (2) and (3), the variation of voltage across capacitor C_s can be given by

$$\Delta v_{Cs} = \frac{\Delta Q_1 + \Delta Q_2}{C_s} = \frac{I_o}{C_s}\left[\frac{2\pi}{\omega_s} + C_r\left(R_{LED1} + R_{LED2}\right)\right]. \tag{7}$$

Considering the symmetry of the operating mode for both positive and negative half cycles, the following analysis is based on the circuit during positive half cycle to explore its inherit characteristic.

By referring the operating mode of Fig. 3(a) and (b), Fig. 5 depicts the equivalent circuits when the diode D_1 is ON and OFF, respectively. The duty cycle of diode D_d is defined as the ratio between the diode's ON-time and switching cycle T_s. Therefore, according to Kirchhoff's voltage law, the differential equation during $0 < t < (1\text{-}D_d)T_s$ can be mathematically expressed by

$$L_r C_{eq}\frac{d^2 v_{Ceq}(t)}{dt^2} = V_{in} + V_{AC}\sin\left(\omega_s t + \varphi\right) \tag{8}$$

where $C_{eq} = C_r C_s/(C_r + C_s)$.

The two known initial conditions of (8) are given by

$$\begin{cases} v_{Ceq}(t)\,|_{t=0} = V_{Cs\_avg} - \frac{\Delta v_{Cs}}{2} - I_o R_{LED2} \\ C_{eq}\frac{dv_{Ceq}(t)}{dt}\Big|_{t=0} = i_{Cs\_off}(t)\Big|_{t=0} = 0 \end{cases}. \tag{9}$$

Combining with (8) and (9), the capacitor' voltage $v_{Ceq}(t)$ during $0 < t < (0.5\text{-}D_d)T_s$ can be calculated. In addition, the current $i_{Cs\_off}(t)$ can be further calculated by

$$i_{Cs\_off}(t) = \frac{1}{L_r}\int_0^t V_{in} + V_{AC}\sin\left(\omega_s t + \varphi\right) - v_{Ceq}(t)\,dt. \tag{10}$$

During $(0.5\text{-}D_d)T_s < t < 0.5T_s$, the equivalent circuit is shown in Fig. 5(b). Therefore, its differential equation can be mathematically expressed by

$$L_r C_s\frac{d^2 v_{Cs}(t)}{dt^2} = V_{in} + V_{AC}\sin\left(\omega_s t + \varphi\right) - I_o R_{LED1}. \tag{11}$$

The two known initial conditions of (11) are given by

$$\begin{cases} v_{Cs}(t)\,|_{t=(0.5-D_d)T_s} = v_{Ceq}(t) - I_o R_{LED1} \\ C_s\frac{dv_{Cs}(t)}{dt}|_{t=(0.5-D_d)T_s} = i_{Cs\_off}(t)\Big|_{t=(0.5-D_d)T_s} \end{cases}. \tag{12}$$

Combining with (11) and (12), the capacitor's voltage $v_{Cs}(t)$ can be calculated. The current $i_{Cs\_on}(t)$ can also be calculated by

$$i_{Cs\_on}(t) = \frac{1}{L_r}\int_{\pi(1-2D_d)/\omega_s}^{t} V_{in} + V_{AC}\sin\left(\omega_s t + \varphi\right) - v_{Cs}(t) - I_o R_{LED1}dt + \frac{\pi i_{Cs\_off}}{\omega_s}\left(1-2D_d\right). \tag{13}$$

According to the aforementioned analysis, there are three constraints that should be satisfied, i.e.,

$$\int_0^{\pi(1-2D_d)/\omega_s} i_{Cs\_off}(t)\,dt = C_r I_o\left(R_{LED1} + R_{LED2}\right) \tag{14}$$

$$\int_{\pi(1-2D_d)/\omega_s}^{\pi/\omega_s} i_{Cs\_on}(t)\,dt = \frac{2\pi I_o}{\omega_s} \tag{15}$$

$$i_{Cs\_on}\left(\pi/\omega_s\right) = 0. \tag{16}$$

Substituting $i_{Cs\_off}(t)$ and $i_{Cs\_on}(t)$ into (14)–(16), three nonlinear equations can be obtained. It can be found that there are ten variables V_{in}, ω_s, R_{LED1}, R_{LED2}, D_d, φ, I_o, L_r, C_r, and C_s in total, wherein the external parameters V_{in}, ω_s, R_{LED1}, and R_{LED2} can be initially designed. Then, there are actually only six variables D_d, φ, I_o, L_r, C_r, and C_s remained. If any three of them are known, the remaining variables can be numerically solved in MATLAB by applying these three nonlinear equations.

D. Analysis of Inverter Stage

Fig. 6 shows the schematic of the inverter stage. To facilitate the analysis, the rectifier stage can be approximately equivalent

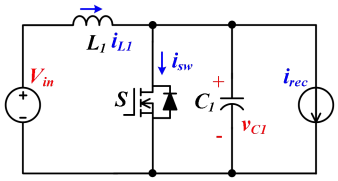


Fig. 6. Schematic of the inverter stage with the rectifier modeled as a current source i_{rec}.

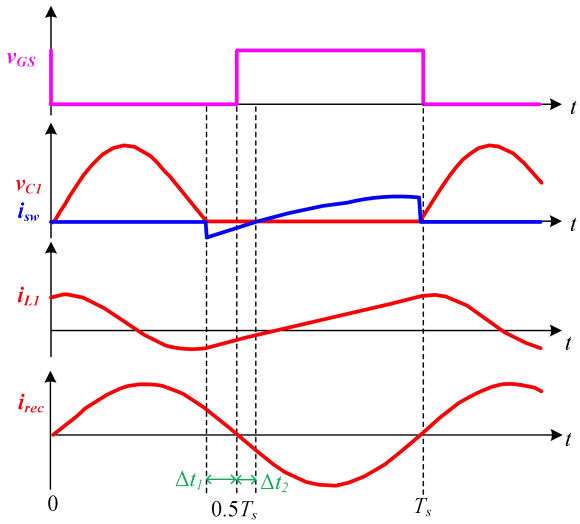


Fig. 7. Typical waveforms of voltage and current for inverter stage.

to a sinusoidal current source i_{rec}, as presented in [27], which can be expressed as

$$i_{rec} = I_{AC} \sin(\omega t) \tag{17}$$

where I_{AC} is the amplitude of current source i_{rec}.

Since the main output power of the LED driver is transmitted by the fundamental components of capacitor' voltage V_{C1}, I_{AC} can be therefore estimated as

$$I_{AC} = \frac{2P_o}{V_{AC}} = \frac{4I_o^2 (R_{LED1} + R_{LED2})}{\pi V_{in}}. \tag{18}$$

For the rectifier stage, the sinusoidal input voltage $v_{\sin}$ and current i_{Cs} should be kept in phase to ensure higher efficiency. As shown in Fig. 7, the capacitor's voltage v_{C1} and the current i_{rec} are therefore kept in phase and equal to 0 at $t = 0$. Typically, the duty cycle of the switch is set to 0.5, but the capacitor' voltage v_{C1} needs to be reduced to 0 before gating signal arrives, making the switch operate at ZVS situation. Besides, the switching current i_{sw} also needs to be kept less than 0 before gating signal arrives, otherwise the capacitor will be charged by the inductor's current i_{L1}, causing additional power loss.

According to the switching state, the equivalent circuits of the inverter stage are depicted in Fig. 8. Then, according to Kirchhoff's current law, the differential equation during $0 < t < (0.5T_s\text{-}\Delta t_1)$ can be mathematically expressed by

$$L_1 C_1 \frac{d^2 i_{L1\_off}(t)}{dt^2} + i_{L1\_off}(t) = I_{AC} \sin(\omega_s t). \tag{19}$$

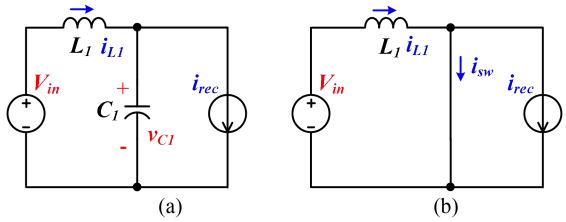


Fig. 8. Equivalent circuits of the inverter stage. (a) When the switch S is turned OFF. (b) When the switch S is turned ON.

The two initial conditions of (19) are given by

$$\begin{cases} i_{L1\_off}(t)|_{t=0} = i_{L1\_off}(0) \\ L_1 \frac{di_{L1\_off}(t)}{dt}\Big|_{t=0} = V_{in} \end{cases} \tag{20}$$

where the initial current $i_{L1\_off}(0)$ is unknown variable.

Combining (19) and (20), the inductor's current $i_{L1\_off}(t)$ can be calculated. In addition, the capacitor' voltage $v_{C1\_off}(t)$ can be further calculated by

$$v_{C1\_off}(t) = \frac{1}{C_1} \int_0^t i_{L1\_off}(t) - I_{AC} \sin(\omega_s t)\, dt. \tag{21}$$

During $(0.5T_s\text{-}\Delta t_1) < t < T_s$, the capacitor's voltage $v_{C1\_on}(t)$ is 0. The inductor' current $i_{L1\_on}(t)$ is given by

$$i_{L1\_on}(t) = i_{L1\_off}(0.5T_s - \Delta t_1) + \frac{V_{in}}{L_1}(t - 0.5T_s + \Delta t_1). \tag{22}$$

According to the aforementioned analysis, there are three constraints that should be satisfied. The first constraint is that the switching current must be equal to 0 at $0.5T_s + \Delta t_2$ to ensure ZVS feature, i.e.,

$$i_{L1\_on}(0.5T_s + \Delta t_2) - I_{AC} \sin(\omega_s (0.5T_s + \Delta t_2)) = 0. \tag{23}$$

The second constraint is that the average voltage of capacitor C_1 must be equal to V_{in}, i.e.,

$$\frac{1}{T_s} \int_0^{0.5T_s - \Delta t_1} v_{C1\_on}(t)\, dt = V_{in}. \tag{24}$$

The third constraint is that the capacitor's voltage must be equal to 0 at $0.5T_s\text{-}\Delta t_1$, i.e.,

$$v_{C1\_off}(0.5T_s - \Delta t_1) = 0. \tag{25}$$

Substituting i_{L1_off}, i_{L1_on}, v_{C1_off}, and v_{C1_on} into these constraints (23)–(25), the three nonlinear equations can be obtained. It can be found that there are eight variables V_{in}, $\omega_s(T_s)$, I_{AC}, Δt_1, Δt_2, $i_{L1}(0)$, L_1, and C_1 in total, wherein the external parameters V_{in}, ω_s, Δt_1, and Δt_2 can be initially designed. Then, there are actually only four variables I_{AC}, $i_{L1}(0)$, L_1, and C_1 remained. If any one of them is known, the remaining variables can be numerically solved in MATLAB by applying these three nonlinear equations.

It should be noted that there may be multiple solutions if only the aforementioned three nonlinear equations are applied. This is because the third constraint does not limit to the first resonant

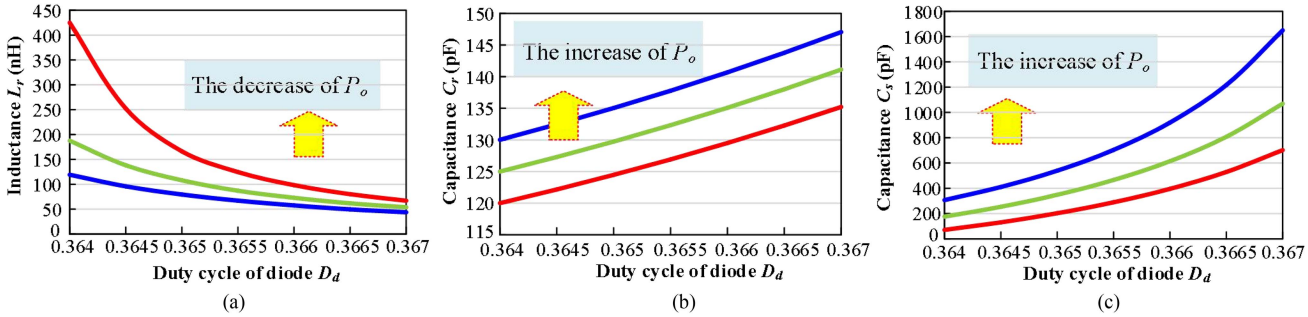


Fig. 9. Curves of capacitances C_r and C_s as well as inductance L_r versus the duty cycle of diode D_d with different output power P_o when $I_o = 0.5$ A. (a) For capacitance C_r. (b) For capacitance C_s. (c) For inductance L_r.

TABLE I
SYSTEM PARAMETERS OF THE RECTIFIER STAGE

Parameter	Value	Parameter	Value
V_{in}	10 V	f_s	30 MHz
P_o	15 W	D_d	0.365
R_{LED2}	40 Ω	R_{LED1}	20 Ω
φ	0	C_{o1}, C_{o2}	10 μF

period. Hence, one additional inequality equation to find the true solution is given by

$$0.5T_s - \Delta t_1 < 2\pi\sqrt{L_1 C_1}. \tag{26}$$

III. DESIGN CONSIDERATION

A. Design Example of Current-Balancing Rectifier Stage

Based on the aforementioned analysis, the following design consideration takes a 15 W, 30 MHz dual-channel LED driver as an example, wherein the input voltage $V_{in} = 10$ V.

For the rectifier stage, the sinusoidal input voltage $v_{\sin}$ and current i_{Cs} should be kept in phase to ensure the higher efficiency so that the phase angle φ must be set to 0. Fig. 9(a) shows the inductance L_r curve for different output power P_o versus the duty cycle of diode D_d. It indicates that the inductance forms an inversely proportional relationship with the duty cycle D_d. Besides, the inductance varies sensitively over a narrow range of duty cycle, especially for the lower P_o. Since too large or small inductance is detrimental to the circuit performance, it is recommended that low-power converter operates in larger D_d, whereas high-power one operates in smaller D_d. Fig. 9(b) and (c) shows the capacitance C_r and C_s curve for different P_o versus D_d, respectively. It can be seen that both of them are proportional to D_d, but the capacitance C_r changes more slowly. Too small capacitance C_r will impose stricter requirement on parasitic capacitance of both diodes, it is recommended to select proper output power and duty cycle to make C_r larger than parasitic capacitance of diodes.

To verify the correctness of the theoretical analysis, a simulation model of current-balancing rectifier stage was built in PSIM9.0. With the parameters, as listed in Table I, the resonant parameters are calculated as $L_r = 79.41$ nH and $C_r = 135.03$ pF as well as $C_s = 539.57$ pF, respectively, from (14)–(16). Fig. 10

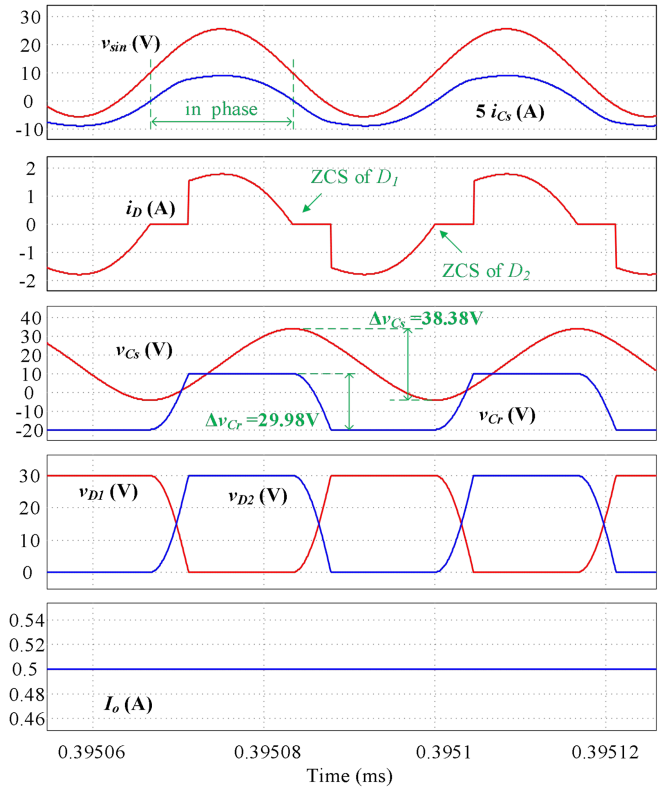


Fig. 10. Simulation waveforms of the current-balancing rectifier stage.

shows the simulation waveforms. It can be seen that the output power $P_o = I_o^2 \times (R_{LED1} + R_{LED2}) = 15$ W and the phase angle $\varphi = 0$ are consistent with those designed in Table I. As the capacitor C_r participates in resonant process, both diodes can achieve ZCS feature. Also, the simulated value of ΔV_{Cs} is close to its theoretical value 38.39 V calculated from (7).

B. Design Example of Inverter Stage

In order to design the inverter stage more clearly, the variables $\Delta t_{1,2}$ are represented as $\Delta\theta_{1,2} = \omega_s \Delta t_{1,2}$. Then, when I_{AC} is set to 1.91 A to match the output power P_o of 15 W calculated from (18), it can be seen from Fig. 11(a) that the calculated capacitance C_1 decreases with the increase of θ_1. Especially with the smaller

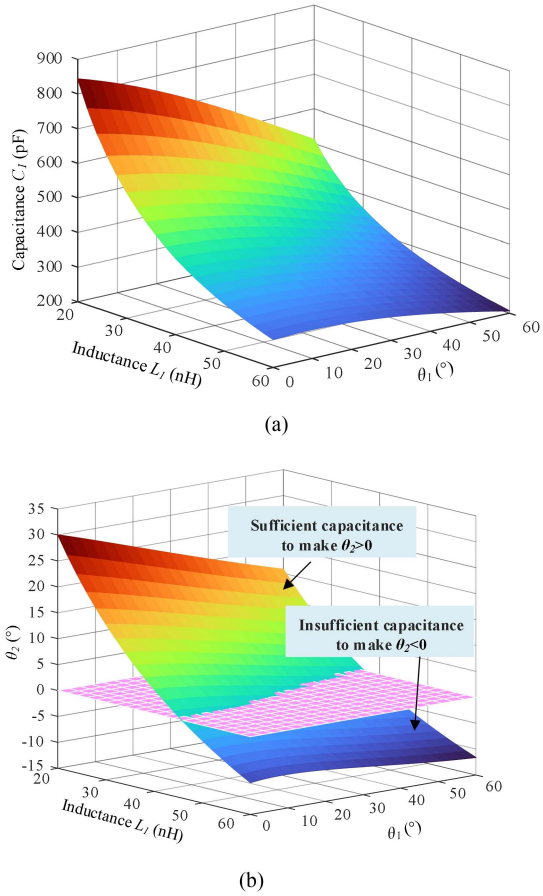


Fig. 11. Relationship of capacitance C_1, the inductance L_1 and $\theta_{1,2}$ when $P_o = 15$ W. (a) Capacitance C_1 versus the inductance L_1 and θ_1. (b) θ_2 versus the inductance L_1 and θ_1.

inductance L_1, the capacitance C_1 will decrease even more. However, in some cases if the calculated capacitance C_1 does not provide enough energy in the reverse conduction process of the switch, a bad phenomenon will occur, which is the capacitor C_1 is charged by the inductor' current before gating signal arrives and then it suddenly discharges at switching moment. Hence, it results in more power losses. Fig. 11(b) shows the relationship of θ_2 versus the inductance L_1 and θ_1. To avoid this bad case, θ_2 should be larger than 0 so that the calculated capacitance C_1 is sufficient to provide energy.

To study the relationship of output power P_o versus the inductance L_1 and θ_1, θ_2 is set to 0 just to ensure sufficient power of capacitor C_1. As shown in Fig. 12, it indicates that the output power is mainly regulated by the inductance. Increasing θ_1 can also slightly reduce the output power, but it will result in more circulating current to reduce efficiency. Hence, it is recommended that θ_1 is set as minimum as possible under the premise of satisfying the ZVS feature of switch.

To verify the correctness of the theoretical analysis, the simulation models of inverter stage for two cases were also built in PSIM9.0, wherein $V_{in} = 10$ V, $f_s = 30$ MHz, and $P_o = 15$ W. With the parameters, as listed in Table II, it can be seen that the capacitor's voltage v_{C1} drops to 0 and then

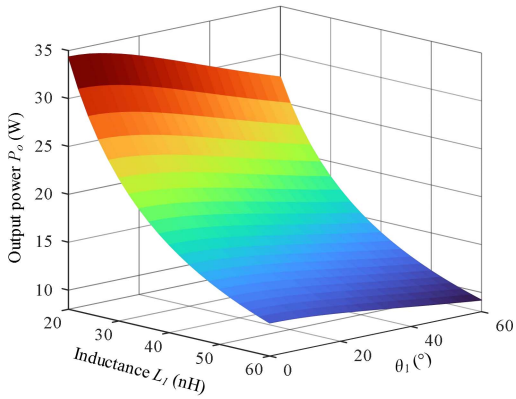


Fig. 12. Relationship of output power P_o versus the inductance L_1 and θ_1 when $\theta_2 = 0$.

TABLE II
SYSTEM PARAMETERS OF THE INVERTER STAGE

Parameter	Normal case	Bad case
θ_1	30°	30°
θ_2	0	-10°
L_1	42.16 nH	60.98 nH
C_1	359.79 pF	264.68 pF

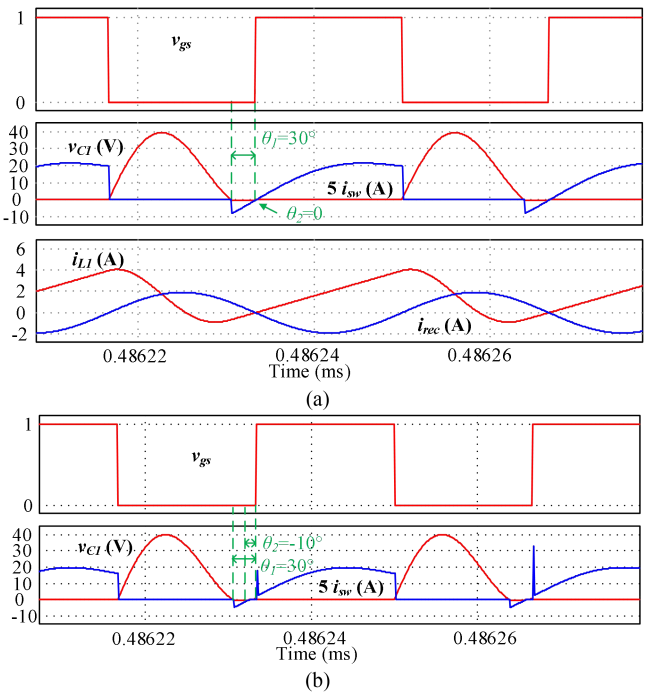


Fig. 13. Simulation waveforms of the inverter stage. (a) In normal case. (b) In bad case.

the switch's current i_{sw} flows through the body diode of switch before gating signal v_{GS} arrives, which achieves ZVS of switch, as shown in Fig. 13(a). To keep θ_1 the same, the inductance L_1 and capacitance C_1 are changed to 60.98 nH and 264.68 pF, respectively. As shown in Fig. 13(b), it can be seen that the capacitor is not enough to provide output power and recharged by the inductor current. Hence, the current spike occurs at the

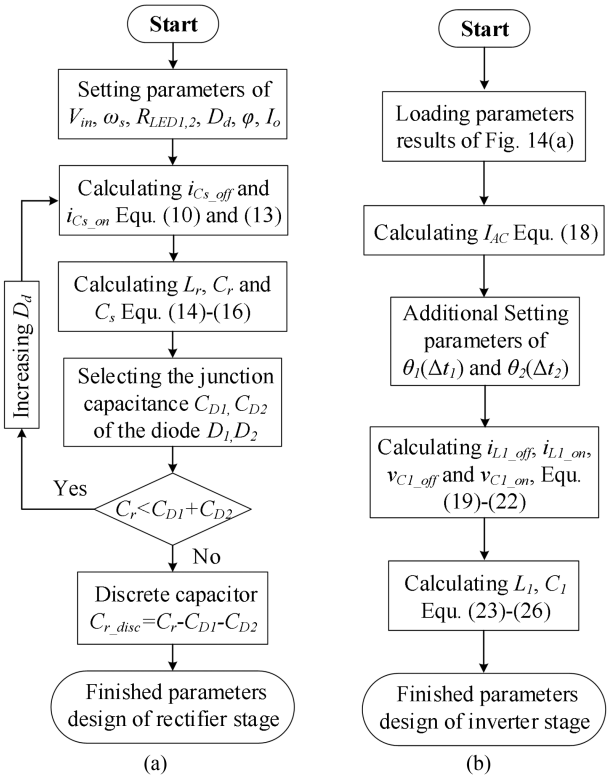


Fig. 14. Flowchart of parameter design. (a) For current-balancing rectifier stage. (b) For inverter stage.

switching moment and results in more power losses, which is corresponding to the aforementioned analysis.

C. Design Procedure

As a result, the design procedures are summarized in Fig. 14, and the detailed description of current-balancing rectifier stage corresponding to Fig. 14(a) is given as follows.

1) According to the design requirement, setting the initial value of V_{in}, ω_s, $R_{LED1,2}$, D_d, φ, and I_o, wherein the phase angle φ should be set to 0 to reduce power loss, whereas $R_{LED1,\ 2}$ and I_o determine the output power P_o.
2) Calculating the functions of SC's current during both diodes turned OFF and one of the diode turned ON from (10) and (13), respectively, i.e., $i_{Cs\_off}(t)$ and $i_{Cs\_on}(t)$.
3) Calculating L_r, C_r, and C_s according to (14)–(16).
4) Determining the diodes' stress according to the output voltage and output current. Then, selecting the proper diode and obtaining their junction capacitance C_{D1} and C_{D2}.
5) Comparing the calculated value C_r with the sum of junction capacitance $C_{D1} + C_{D2}$. If $C_r < C_{D1} + C_{D2}$, it means that too large junction capacitance will shift the phase angle and the power loss will further increase. At this time, the duty cycle of diode D_d should be increased to make larger value of C_r required and then back to step (2).
6) Selecting the additional discrete capacitor $C_{r\_\mathrm{disc}} = C_r - C_{D1} - C_{D2}$.
7) Finally, the circuit parameters L_r, C_r, and C_s can be determined. If the capacitance C_r is only provided by the junction capacitance, the discrete capacitor can be removed. However, the linearity of the junction capacitance should be as good as possible, otherwise there may be some deviations.

TABLE III
CALCULATION BASIS OF THE COMPONENTS PARAMETER

Parameters	Calculation basis
i_{Cs_off}, i_{Cs_on}	(10), (13)
L_r, C_r, C_s	i_{Cs_off}, i_{Cs_on}, (14)–(16)
I_{AC}	(18)
i_{L1_off}, i_{L1_on}, v_{C1_off}, v_{C1_on}	I_{AC}, (19)–(22)
L_1, C_1	i_{L1_off}, i_{L1_on}, v_{C1_off}, v_{C1_on}, (23)–(26)

The detailed description of inverter stage corresponding to Fig. 14(b) is also given as follows.

1) Loading the initial values and calculated values of Fig. 14(a).
2) Calculating I_{AC} from (18).
3) Setting the parameters of $\theta_1(\Delta t_1)$ and $\theta_2(\Delta t_2)$ to ensure ZVS feature of switch.
4) Calculating the functions of $i_{L1\_off}(t)$, $i_{L1\_on}(t)$, $v_{C1\_off}(t)$, and $v_{C1\_on}(t)$ from (19)–(22), wherein $v_{C1\_on}(t)$ is always 0.
5) Calculating L_1 and C_1 from (23)–(26).
6) Finally, the circuit parameters L_1 and C_1 of inverter stage can be determined.

More intuitively, the calculation basis of all the component parameter is summarized in Table III.

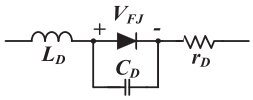
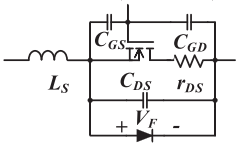
In actual, the circuit waveforms may be slightly different from the independent ones when the rectifier stage and inverter stage are connected with each other. This is because the design process is based on the fundamental assumption. However, the other harmonic components also provide the power. Hence, the output power will be slightly larger than the rated power without considering the power losses, resulting in undesirable phenomenon shown in Fig. 13(b) due to insufficient capacitance C_1. The final procedure of fine tuning parameters needs to be carried out with the help of simulation tools, such as LTSPICE, to fully ensure the ZVS feature of switch.

IV. SIMULATION AND LOSS ANALYSIS

A. Simulation Analysis Considering Parasitic Parameter

The premise of the aforementioned analysis is that all the devices are ideal. However, the actual devices are rich in parasitic parameters, which will affect the external parameter selection and converter performance. The parasitic inductance depends on the package and it is usually less than 1 nH for the small package, such as PowerPAK. The parasitic capacitance is inversely proportional to the reverse voltage of device and it usually varies from tens of pF to hundreds of pF. Hence, the parasitic capacitance should be considered as part of the required resonant capacitance, i.e., ideal required capacitance is the sum of parasitic capacitance and discrete capacitance.

TABLE IV
SPECIFICATION AND COMPONENTS OF THE SIMULATION MODEL

Input voltage V_{in}	10 V
Switching frequency f_s	30 MHz
Discrete capacitor C_1, C_r, C_s, $C_{o1,2}$	440 pF, 35 pF, 760 pF, 10 μF
Discrete inductor L_1, L_r	28 nH, 68 nH
Diode D_1, D_2 (CUS10S40) 	C_D=100 pF (when V_R=0 V) C_D≈15 pF (when V_R=5 V–30 V) V_{FJ}=0.35 V r_D=0.127 Ω L_D=1 nH
MOSFET S (SI7898DP) 	C_{DS}=300 pF (when V_{DS}=0 V) C_{DS}≈100 pF (when V_{DS}=5 V–60 V) V_F=0.75 V r_{DS}=78 mΩ L_S=0.8 nH C_{GS}=500 pF C_{GD}=100 pF
Load R_{LED1}, R_{LED2}	20 Ω, 40 Ω

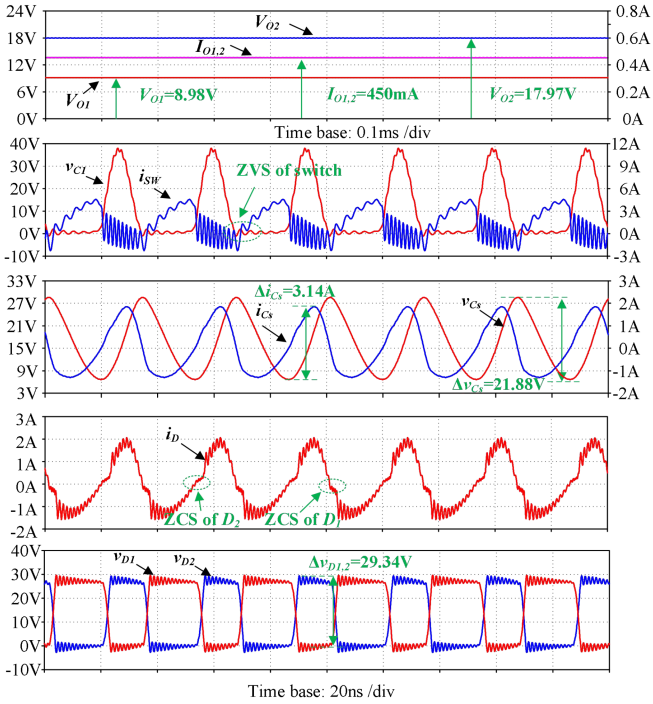


Fig. 15. Simulation waveforms of the proposed LED driver in LTSPICE.

By referring to the circuit configuration of Fig. 2 and using the parameters of Table IV, the simulation model was built in LTSPICE. Each resonant inductor and capacitor were assigned the equivalent series resistance (ESR) of 20 mΩ and 40 mΩ, respectively, to analyze its power loss.

Fig. 15 shows the simulation results of the proposed LED driver with an input power of 14.7 W. It indicates that both output currents can be automatically balanced at 450 mA, and the sum of output voltage is 26.95 V. The simulation efficiency is therefore 82.5%. In addition, since the SC C_s participates in the resonance process, its current spike has been suppressed, effectively. As the parasitic inductor of the device resonates with the capacitor, it can also be seen that the waveforms of switch and diode appear high-frequency ringing. Nevertheless, the ZVS feature of switch and ZCS feature of diodes are still can be ensured due to the low enough parasitic inductance. Moreover, the voltage stresses on diode are clamped to 29.34 V, which is closed to the sum of output voltage. Hence, it is recommended to choose low parasitic inductance package of the device to ensure converter performance.

B. Loss Analysis

The power losses of the proposed LED driver can be approximately categorized into four parts: switch losses, diode losses, inductor losses, and capacitor losses, which are as follows.

1) *Switch losses:* The switch losses mainly consist of driving loss and conduction loss. Specifically, the driving loss of the resonant driving method can be calculated from Guan et al. [25], i.e.,

$$P_{DR} = 2\pi^2 f_s^2 V_{gs}^2 C_{gs}^2 R_g \tag{27}$$

where C_{gs} is the gate-source capacitance of the switch and R_g is the gate resistance.

Due to the ZVS feature of switch, only the conduction loss is taken into consideration. During the forward turn-ON duration, the forward conduction loss of switch can be calculated as

$$P_{S\_CON} = I_{S\_rms}^2 r_{ds} \tag{28}$$

where I_{S_rms} is the root-mean-square (rms) current of switch during forward turn-ON duration.

In addition, the reverse conduction loss of switch also will occur in the process of reverse current flowing through its body diode, which can be estimated by

$$P_{BD\_CON} = V_{F\_BD} I_{F\_BD} \tag{29}$$

where V_{F_BD} and I_{F_BD} are the forward voltage and current of the body diode during the reverse turn-ON duration, respectively.

The total switch losses are the sum of (27), (28), and (29).

2) *Diode losses:* Due to the ZCS feature of diode, the conduction loss of the diode is only considered, which is given by

$$P_D = V_{FJ\_D} I_{D\_avg} + I_{D\_rms}^2 r_D \tag{30}$$

where V_{FJ_D} is the junction forward voltage (excluding parasitic parameters), whereas I_{D_avg} and I_{D_rms} are the average current and rms current of diode, respectively. r_D is the parasitic resistance of the diode.

3) *Inductor losses:* There are two air core inductors employed in the proposed LED driver. Only the copper loss needs to be considered. The copper loss is given by

$$P_L = I_{rms\_L}^2 r_L \tag{31}$$

where I_{rms_L} is the rms current flowing through the winding of inductor and r_L is the parasitic copper resistance.

4) *Capacitor losses:* Due to the ESR of the capacitor, the current flowing into and out of the capacitor will result in power loss. The conduction losses can be calculated by

$$P_C = I_{rms\_C}^2 r_C \tag{32}$$

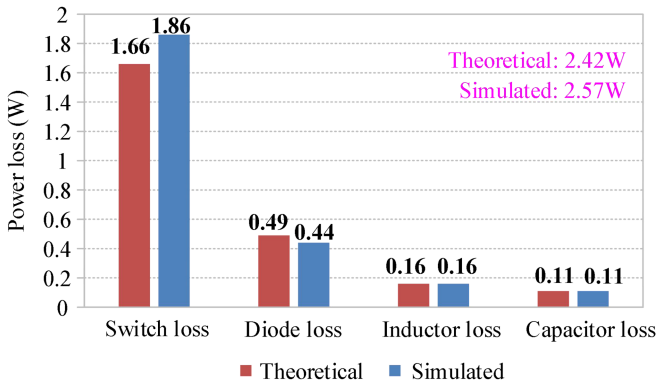


Fig. 16. Power loss distribution for theoretical loss model and simulation model.

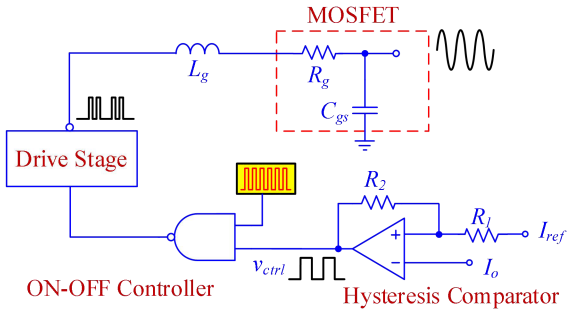


Fig. 17. ON–OFF hysteresis control strategy.

where I_{rms_C} is the rms current flowing through the capacitor and r_C is the ESR of capacitor.

Fig. 16 shows the power losses distribution based on the aforementioned loss models and LTSPICE simulation model. It can be seen that most of the power losses come from the switch, especially the driving loss accounts for about 40% of the switch loss. Therefore, the higher proportion of driving losses makes the overall efficiency only 82.5%. Nevertheless, as the input power increases, the proportion of driving losses will be less. Then, the overall efficiency can continue to rise up to the maximum value. In actual, the efficiency can be further improved with the lower ON-resistance r_{DS} of switch.

V. Experimental Results

To verify the current-balancing capability, the LED_1 channel is connected with the LED load of 9 V/450 mA, whereas LED_2 channel is connected with the LED load of 18 V/450 mA. By referring the circuit configuration of Fig. 2 and ON–OFF hysteresis control strategy of Fig. 17, the experimental bench with a rated input power of 15 W was built, as shown in Fig. 18. Its specification and components are given in Table V.

When the prototype operates at 100% analog dimming, the LED strings' current and voltage are measured, as shown in Fig. 19. It can be seen that both LED strings have almost the same output current. The measured output voltages of LED_1 and LED_2 are 8.75 V and 17.88 V, respectively. In this case, the system maximum efficiency is measured as 79.6%, the output

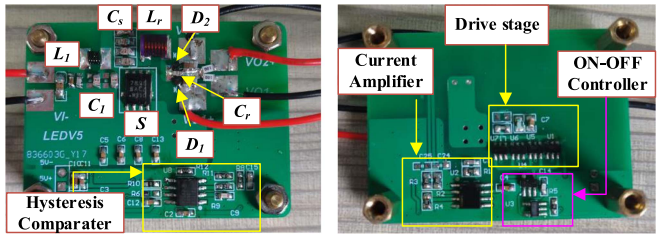


Fig. 18. Experimental bench for the proposed prototype. (a) Top layout. (b) Bottom layout.

TABLE V
Specification and Components of the Proposed VHF Prototype

Input voltage V_{in}	10 V
Switching frequency f_s	30 MHz
Capacitor C_1, C_r, C_s, $C_{o1,2}$	440 pF (discrete), 50 pF (discrete), 760 pF, 10 μF
Inductor L_1, L_r	27 nH (discrete), 58 nH (discrete)
Diode D_1, D_2	CUS10S40
MOSFET S	SI7898DP
Drive circuit	NL27WZ04
ON-OFF controller	LTC6905, NC7SZ00M5X
Hysteresis comparator	TLV3501
Current amplifier	TLV2241

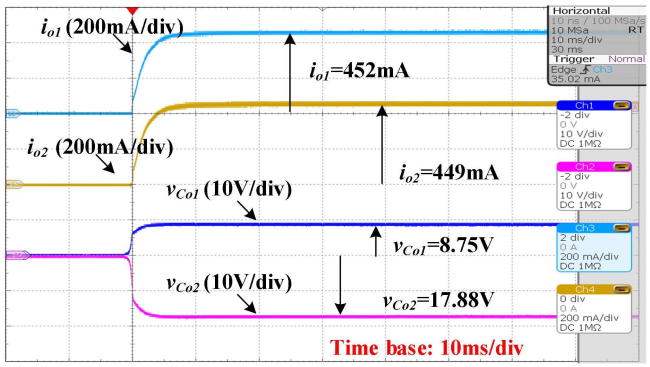


Fig. 19. Measured strings' current and voltage at 100% analog dimming.

power is approximately 12 W, and the total equivalent resistance for LED strings is estimated as 59 Ω.

Fig. 20 shows the experimental waveforms including capacitor's voltage v_{C1}, v_{Cs} and diodes' voltage v_{D1}, v_{D2}. The measured peak-to-peak voltage value Δv_{Cs} of 23.32 V is close to the theoretical value 24.97 V calculated from (7). As both diodes are alternately turned ON and clamped to each other, the voltage stress on diodes is reduced to approximately total output voltage, but it is still slightly larger than output voltage. This is caused by the parasitic inductance of printed circuit board (PCB) layout and passive component deviation. Nevertheless, it demonstrates that the voltage stress on diodes can be reduced effectively, whereas the voltage stress given in [25] is almost three times of output voltage.

When the prototype operates at 65% analog dimming, the measured LED strings' current and voltage are shown in Fig. 21. It can be seen that the output currents of both LED strings can also be regulated to 284 mA by adjusting the control signal $v_{\rm ctrl}$

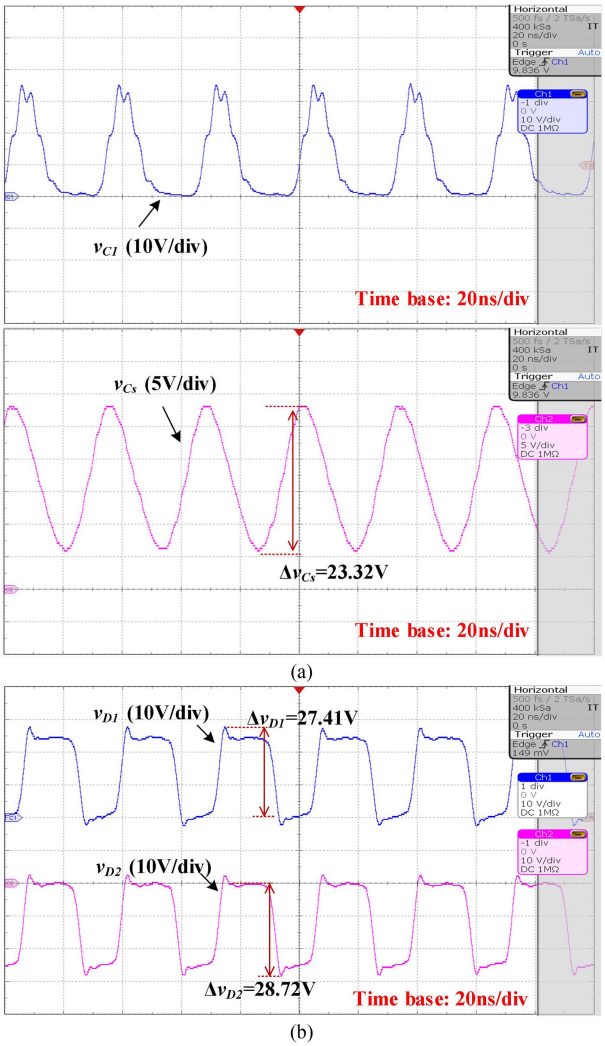


Fig. 20. Measured capacitor's voltage and diodes' voltage. (a) Capacitor's voltages v_{C1} and v_{Cs}. (b) Diodes' voltages v_{D1} and v_{D2}.

simultaneously. In addition, as shown in Fig. 22, it can also be seen that the current ripple is approximately 50 mA. The high-frequency ripple is mainly caused by parasitic resistance of output capacitor, whereas the low-frequency ripple is mainly caused by the hysteresis width.

Fig. 23 shows the dynamic current-balancing performance of the proposed prototype when LED_2 is suddenly short-circuited, it indicates that the output current of LED_1 quickly stabilizes to the reference current. The current recovery time depends mainly on the slew rate of the current amplifier. Nevertheless, it has verified that the proposed prototype can realize partial short-circuit protection without any additional short-protection circuits.

Fig. 24 shows the measured efficiency curve of the proposed prototype when the dimming ratio changes from 10% to 100%. It indicates that the efficiency increases along with the dimming ratio.

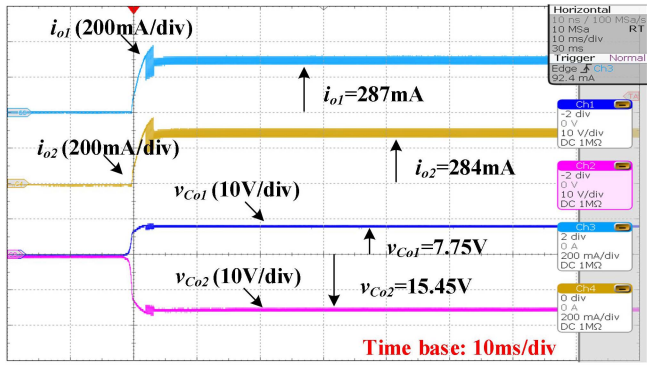


Fig. 21. Measured strings' current and voltage at 65% analog dimming.

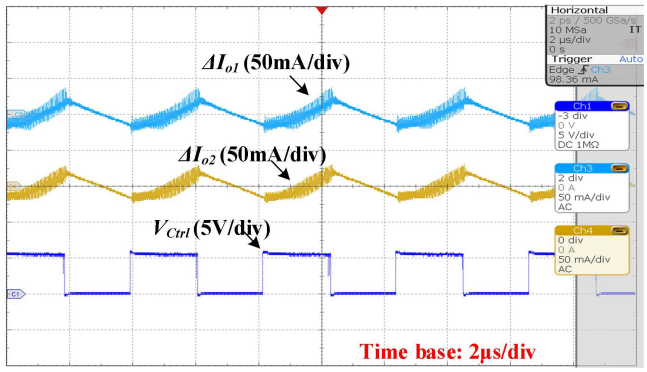


Fig. 22. Control signal v_{ctrl} and ac ripple of LED_1 output current.

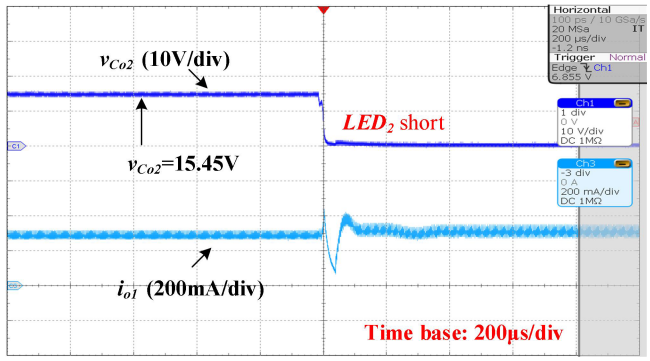


Fig. 23. Dynamic current-balancing waveforms when LED_2 is a suddenly short-circuited.

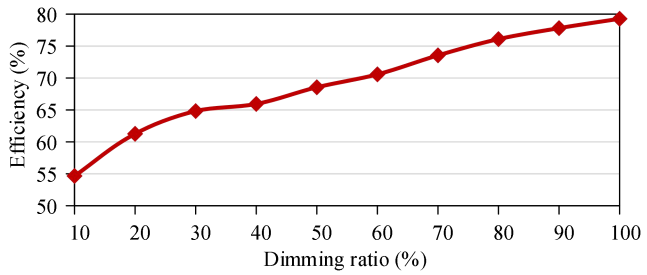


Fig. 24. Measured efficiency of the prototype with varied dimming ratio.

TABLE VI
COMPARISON OF SOME EXISTING CONVERTERS SUITABLE FOR LED APPLICATION

Reference	Switching frequency	Output power	Input/output voltage	Switch/diode number	Inductors/capacitors/ Transformer number	Current-balancing	Diode's stress	Power density	Efficiency (on-resistance of switch)
[11]	65 kHz	16 W	100 V/25 V	4/2	1/1/0	Yes	V_o	N/A	92.6% (9.5 mΩ)
[12]	100 kHz	100 W	400 V/220 V	2/4	1/2/1	Yes	V_o	N/A	96.5% (300 mΩ)
[13]	100 kHz	9 W	12 V/32 V	1/2	1/1/0	Yes	V_o	N/A	92.5% (150 mΩ)
[17]	30 MHz	14 W	15 V/28 V	1/1	2/3/0	No	$3.1V_o$	200 W/in^3	82.5% (36 mΩ)
[19]	30 MHz	50 W	36 V/24 V	2/2	6/6/1	No	$3.5V_o$	50 W/in^3	73.3% (78 mΩ)
[23]	20 MHz	10 W	10 V/5 V	1/1	1/3/1	No	$4V_o$	50 W/in^3	82% (25 mΩ)
[25]	20 MHz	9 W	12 V/5 V	1/1	2/3/0	No	$3V_o$	39 W/in^3	90% (36 mΩ)
Proposed	30 MHz	12 W	10V /26 V	1/2	2/3/0	Yes	V_o	28 W/in^3	79.6% (78 mΩ)

To highlight the merits of the proposed VHF LED driver, a comparative study with the existing VHF converters suitable for LED applications and conventional capacitive current-balancing LED drivers has been carried out, as listed in Table VI. The results show that the conventional capacitive current-balancing LED drivers presented in [11], [12], and [13] have higher efficiency with low switching frequency. However, the bulky inductors and capacitors increase the system size. For the VHF converters, it can be seen that their voltage stress on diode is up to three times the output voltage due to the resonant process, whereas the proposed one is clamped to output voltage. Benefited from the step-up and step-down voltage conversion capability, these existing VHF converters are suitable for LED applications, but they are difficult to extend to one more LED channel with current-balancing capability. In contrast, the proposed LED driver only use one more diode than Zhang et al. [17] and Guan et al. [25] to obtain dual output so that their power density is about the same in theory. Although the power density value shows that the proposed topology is slightly lower, in fact, the PCB space is sufficient, which can be further optimized to increase the power density. All these merits indicate that the proposed VHF topology can be a new LED driver suitable for low- and middle-power applications.

VI. CONCLUSION

In this article, a VHF dual-channel LED driver with capacitive current balance is proposed by using the resonant SC techniques. Unlike the conventional LED driver with capacitive current balance, the proposed one has higher power density and no current spike occurred at switching moments due to its higher switching frequency and resonant operation. Compared to the existing VHF single-channel LED driver, the proposed one is easier to extend one more LED channel without adding any passive components. Furthermore, the diodes' voltage stresses are significantly reduced to the total dc output voltage as both diodes alternately turned ON are clamped to each other. These merits make the proposed LED driver suitable for low- and middle-power applications with strict volume requirements, such as mobile devices. Based on the theoretical analysis and simulation results, the design consideration of the parameters is discussed in detail. Finally, the experimental results with a rated output power of 12 W prototype verify the good performance of the proposed solution.

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