Stray Parameter Extraction Method Based on High-Frequency Oscillation: An Experimental Study With Theoretical and Execution Demo

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***Abstract*—Stray parameter extraction is crucial for the safe operation and stress estimation in power electronics systems. This study proposes a multifaceted stray parameter extraction method based on high-frequency oscillation characteristics of switching transient. Unlike existing methods that rely on waveform amplitude accuracy and channel sampling synchronization, the proposed method requires less precision in these areas. Hence, it is more resilient to signal attenuation and mismatch issues, making it a robust solution. First, the mathematical analysis of the oscillation behavior in the turn-OFF transients is presented. Next, the relationship of the oscillation frequency with the parameters in a second-order and a fourth-order model is analyzed. A novel extraction method and the corresponding design of the extraction kit are then presented. The effectiveness is verified by the extraction application in various components in a high-power converter, including copper and laminated busbars, dc-link capacitors, and semiconductor power modules. The robustness and frequency algorithm were improved and verified by Monte Carlo trials. Both partial and total loop parameter extraction tests validate that the proposed method can accurately obtain values in the order of 10 nH and offers high test precision, simple operation, and low extraction error.**

***Index Terms*—Commutation loop, frequency analysis, high power converter, stray parameter, transient oscillation.**

I. Introduction

ACCURATE extraction and analysis of stray parameters have become critical with the demand for higher power density and faster switching speed in power converters. The presence of stray elements, such as inductances and capacitances, can exacerbate the switching performance and compromise the converter efficiency, electromagnetic interference, and reliability [1], [2], [3], [4], [5]. This issue is particularly important in the context of high-power converters, where the values of stray parameters are higher, and they are distributed across different components in the commutation loop. The electromagnetic behavior during the commutation process is closely related to the stray parameters [6], [7], [8] and dynamic characteristics of the components in the entire circuit. Neglecting the effects of these stray parameters can no longer withstand scrutiny, especially as high-frequency technology advances. Therefore, the extraction and analysis of stray parameters has become a pressing issue [7], [8], [9], [10].

Stray parameters are distributed throughout the commutation loop, including stray inductance of bolts, dc-link capacitors, and power devices as well as the combinations of stray inductance and stray capacitance in connecting components such as busbar. Stray parameter extraction methods can be generally divided into two categories: calculation-based and experimental-based methods. Calculation-based methods use finite element or partial element equivalent circuits to solve Maxwell equations. These methods obtain the values of stray parameters based on accurate 3-D modeling and material characteristics. An Ansys simulation study on the internal inductance of device packaging revealed that size, position, and current path are critical factors in simulation calculations, with the current path and distribution being particularly complex and difficult to determine [11].

Experimental-based methods for the stray parameter extraction can be categorized into steady-state and transient methods. Steady-state methods utilize the impedance characteristic under a steady excitation, while transient methods use the circuit's response to extract the parameter. Among them, steady-state methods mainly use specialized equipment, such as the impedance analyzer and network analyzer for impedance analysis. The interference introduced by the fixture is an important factor affecting measurement accuracy [12], [13]. Moreover, some researchers have used time-domain reflection technology to improve the accuracy of stray parameter extraction in complex circuits [14], [15].

Transient response methods determine stray inductance by analyzing voltage and current slope during switch transients [7]. There are three types: 1) measures di/dt and voltage drop during turn-ON transient; 2) measures di/dt and voltage overshoot during turn-OFF transient; and 3) utilizes oscillation frequency during turn-OFF transient. The parameter estimation accuracy in types 1 and 2 depends on the clarity of the voltage drop steps in the transient waveform and the precision of multichannel voltage and current sampling.

Manuscript received 20 April 2023; revised 19 July 2023; accepted 19 August 2023. Date of publication 28 August 2023; date of current version 23 October 2023. This work was supported in part by the National Natural Science Foundation of China under Grant 52177199 and in part by the Zhejiang Provincial Natural Science Foundation of China under Grant LGG22E070013. Recommended for publication by Associate Editor M. Hartmann. *(Corresponding author: Sideng Hu.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3309402.

Digital Object Identifier 10.1109/TPEL.2023.3309402

Several studies have attempted to analyze and optimize different aspects impacting extraction. It has been pointed out in [16] that when the current probe and oscilloscope rise time cannot meet three times the rise time of the test signal, it will cause a 5% test error. This concern becomes even more serious in the case of wideband gap devices [17], [18]. Zhu et al. [19] utilized a regression algorithm to accurately extract power module stray inductance. Jiang et al. [20] used integral methods to extract busbar stray inductance, which can effectively reduce measurement noise and high-frequency ripple interference. Meanwhile, Li et al. [18] pointed out that the resistance-based channel delay correction method can effectively improve the synchronization performance between the voltage-current sampling channels.

Type 3 in the transient response method benefits in lower requirements for waveform amplitude and channel sampling synchronization. It is based on the inherent correlation between oscillation frequency and stray parameters [7], [21]. The turn-OFF oscillation and DFT analysis are utilized in [21] and [22] for loop stray inductance estimation. Its generality and extension for the extraction in diverse components are still obscure, and corresponding robustness and extraction accuracy are still worthy of further study.

To address the challenges in stray parameter extraction and the limitations of existing methods, this article presents a general stray parameter extraction method based on the high-frequency oscillation characteristics in the poststage, i.e., the oscillation stage of the turn-OFF transient. The objective and contribution of this work can be summarized as follows.

1) Compared with the methods that rely on voltage and current slopes in the preceding stage waveform, i.e., commutation-stage, the featured method has lower requirements for waveform amplitude accuracy and channel sampling synchronization. That benefits in robustness to signal attenuation and misalignment issues.
2) This article not only features a stray parameter extraction method but also provides a detailed theoretical analysis for generality and bias distribution. The improvement through the extraction kit and DFT algorithm is also demonstrated.
3) The effectiveness of the proposed method is verified by its application on various components in a total loop and compared with mathematical equations, finite element calculations, and instrument measurements.
4) The double pulse test carried out on an overall commutation loop shows that the voltage spike calculated based on the sum of obtained stray inductances matches well with the experimental spike results.

II. Mathematical Analysis of High-Frequency Oscillation in Switching Transient

Fig. 1 shows the configuration of a typical commutation circuit with its stray parameters, where S_1 is a switching device, such as MOSFET, and D is a diode.

In Fig. 1(a), the turn-OFF behavior of the switching device S_1 introduces a step excitation into the circuit, and the corresponding circuit model is shown in Fig. 1(b), where $i_{\rm load}$ is the current flow through S_1. When S_1 is turned OFF, the current

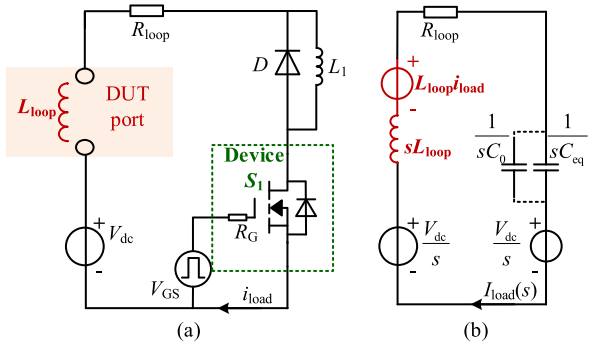

Fig. 1. Basis of circuit commutation analysis. (a) Converter commutation loop. (b) Circuit in oscillation stage.

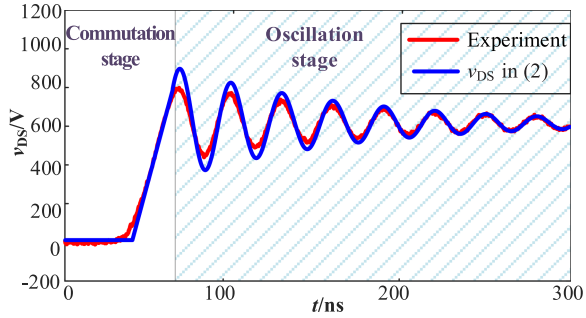

Fig. 2. $v_{\rm DS}$ from experimental test and analytical derivation.

in S_1 detours to diode D, which is a commutation between S_1 and D [23]. After the commutation stage, $v_{\rm DS}$ would rise to $V_{\rm dc}$ and $i_{\rm load}$ would freewheel through diode D. Then the device S_1 is in OFF-state and can be replaced by $C_{\rm eq}$, which is the total equivalent capacitor of the device in the switching process [24]. Thereby, a voltage oscillation process would be generated due to the loop inductance $L_{\rm loop}$ and $C_{\rm eq}$, as shown in Fig. 2.

The analytical expression for the voltage oscillation is shown in (1) and (2). The waveform of $v_{\rm DS}$ acts in an underdamped oscillation with the frequency ω in (3) and an envelope amplitude A in (4). The expression (3) indicates that the ω and attenuation coefficient α are related to the circuit stray parameters. Furthermore, when $\alpha << \omega_{\rm r}$ gets satisfied, the ω can be replaced by $\omega_{\rm r}$ in (5).

$$V_{\rm DS}(s) = \frac{V_{\rm dc}}{s} + \frac{L_{\rm loop} i_{\rm load}}{s^2 L_{\rm loop} C_{\rm eq} + s R_{\rm loop} C_{\rm eq} + 1} \tag{1}$$

$$v_{\rm DS}(t) = V_{\rm dc} + e^{-\alpha t} \frac{i_{\rm load}}{\omega C_{\rm eq}} \sin \omega t \tag{2}$$

$$\omega = \sqrt{\frac{4L_{\rm loop} - {R_{\rm loop}}^2 C_{\rm eq}}{4{L_{\rm loop}}^2 C_{\rm eq}}}, \quad \alpha = \frac{1}{\tau} = \frac{R_{\rm loop}}{2L_{\rm loop}},$$

$$\omega_{\rm r} = \sqrt{\frac{1}{L_{\rm loop} C_{\rm eq}}} \tag{3}$$

$$A = \frac{i_{\rm load}}{\omega C_{\rm eq}} \tag{4}$$

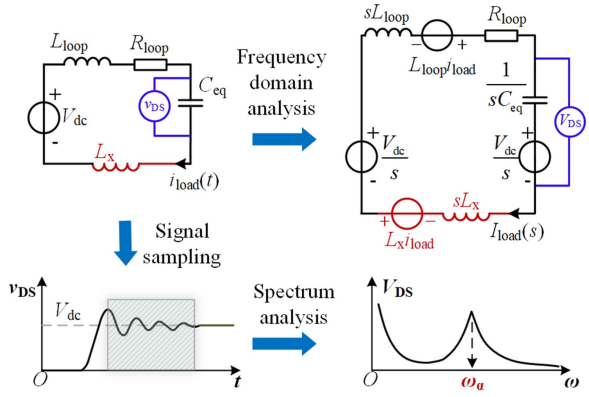

Fig. 3. Modeling and analysis for the oscillation under inductive DUT.

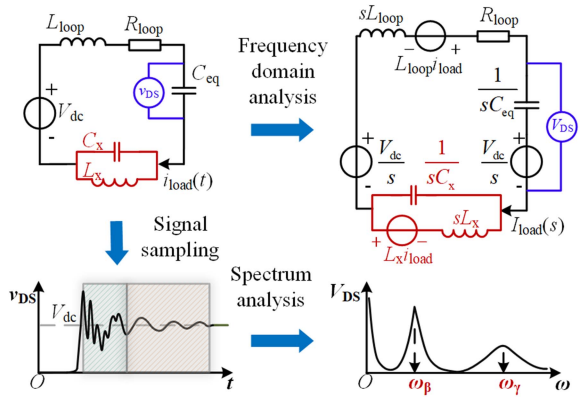

Fig. 4. Modeling and analysis for the oscillation under complex DUT.

$$\omega = \sqrt{\omega_{\mathrm{r}}^2 - \alpha^2} \approx \omega_{\mathrm{r}} = \sqrt{\frac{1}{L_{\mathrm{loop}} C_{\mathrm{eq}}}}. \tag{5}$$

The waveform of v_{DS} from (2) is demonstrated and compared with the experimental test waveforms in Fig. 2.

It can be observed that despite the mismatch in the amplitude, the oscillation frequency of the experimental waveform is very close to the v_{DS} theoretical wave derived from (2). Thereby, the oscillation frequency expression in (5) can be taken to extract the circuit stray parameters.

III. Principle for the Stray Parameter Extraction Method Based on Oscillation

Based on the correlation between the oscillation and the loop stray parameters, a stray parameter extraction method for the power converter is discussed in this section.

A. Extraction Method for the Inductive Component

For components without laminated structures, such as copper busbars and cables [25], the distributed capacitance effects are very limited and can be ignored [26]. Thus, a single inductance model is used to characterize these components.

Fig. 3 shows the component with an inductance value L_{x} connecting to the DUT port. The formed second-order circuit leads to an underdamped oscillation with the characteristic frequency ω_α as follows:

$$\omega_\alpha = \sqrt{\frac{1}{(L_{\mathrm{loop}} + L_{\mathrm{x}}) C_{\mathrm{eq}}}}. \tag{6}$$

The value of C_{eq} and L_{loop} in (6) can be obtained in the kit calibration process. First, short the DUT port, ω_{k1} and ω_{k2} can be triggered by the tests with or without a pretested auxiliary capacitor C_0 in the loop, as shown in Fig. 1(b). ω_{k1} is determined by (5), and ω_{k2} is demonstrated as follows:

$$\omega_{\mathrm{k2}} = \sqrt{\frac{1}{L_{\mathrm{loop}} (C_{\mathrm{eq}} + C_0)}}. \tag{7}$$

Through ω_{k1} and ω_{k2}, L_{loop} and C_{eq} are obtained. After that, the parameter L_{x} can then be calculated according to (6) and the frequency ω_α through v_{DS} spectrum analysis.

During the calibration process, the standard part with a regular shape and known size is used as the short-circuit connector Therefore, the connector's inductance L_{s} can be obtained in advance and is later subtracted from the acquired L_{loop}.

B. Extraction Method for Inductance and Capacitance Coexisting Components

Laminated structures feature in low stray inductance. They are widely adopted in the commutation components [27], [28], [29], [30], such as laminated busbars, power modules like lv-100 [31], and coils with distributed capacitance effects. Fig. 4 shows the coexistence of the stray inductance L_{x} and stray capacitance C_{x}. Oscillation in these applications contains two characteristic frequencies, which is different from that in Fig. 3

$$\begin{cases} \omega_\beta = \left(\dfrac{-\sqrt{K_1^2 - 4K_2} + K_1}{2K_2} \right)^{1/2} \\ \omega_\gamma = \left(\dfrac{\sqrt{K_1^2 - 4K_2} + K_1}{2K_2} \right)^{1/2} \end{cases} \tag{8}$$

where

$$\begin{cases} K_1 = L_{\mathrm{loop}} C_{\mathrm{eq}} + L_{\mathrm{x}} C_{\mathrm{eq}} + L_{\mathrm{x}} C_{\mathrm{x}} \\ K_2 = L_{\mathrm{loop}} C_{\mathrm{eq}} L_{\mathrm{x}} C_{\mathrm{x}} \end{cases}. \tag{9}$$

The angular frequencies ω_β and ω_γ can be obtained through v_{DS} spectrum analysis. Then, the unknown L_{x} and C_{x} can be obtained through (8) and (9).

C. Strategy for the Accuracy Improvement

Equation (8) can be viewed as the general expression of a fourth-order system whose angular frequencies ω_β and ω_γ are determined by the four parameters L_{x}, C_{x}, L_{loop}, and C_{eq}. The accuracy of L_{x} from (8) is affected by the perturbation of the parameters L_{loop} and C_{eq}, as well as C_{x} from the fixture.

As a solution, it is found in the mathematic derivation that if the capacitance paralleled to the DUT port is much larger than C_{eq}, the system oscillation frequencies ω_β and ω_γ would

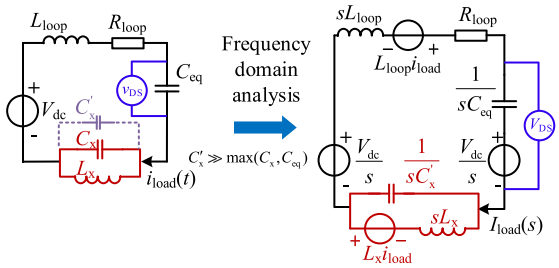

Fig. 5. Analysis of the strategy for accuracy improvement.

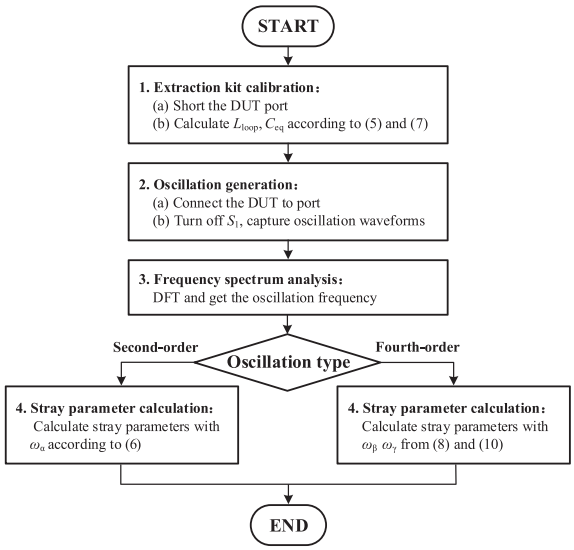

Fig. 6. Flowchart for the proposed extraction method.

depart from each other and are expressed as (10). Then the L_x can be elucidated using only ω_β in (10). As shown in Fig. 5, a capacitor whose value C'_x is much greater than both C_x and C_{eq} is paralleled to the DUT port. That benefits in accuracy improvement for large-size object extraction, such as dc-link capacitors and copper sheets, whose robustness to perturbation L_{loop}, C_{eq}, and C_x get enhanced.

$$\begin{cases} \omega_\beta = \sqrt{\dfrac{1}{L_x C'_x}} \\ \omega_\gamma = \sqrt{\dfrac{1}{L_{loop} C_{eq}}} \end{cases}. \tag{10}$$

D. Overall Implementation Guidance

Based on the high-frequency oscillation characteristics, the parameter extraction steps are summarized, as shown in Fig. 6.

First, calibrate the kit to get the L_{loop} and C_{eq} according to Section III-B. Then, perform the frequency spectrum analysis on the sampled v_{DS} waveform. Finally, calculate the stray inductance and capacitance values based on the frequency value and the oscillation formula.

IV. System Design and Parameter Setting

This section presents the hardware and algorithm design according to the above discussion.

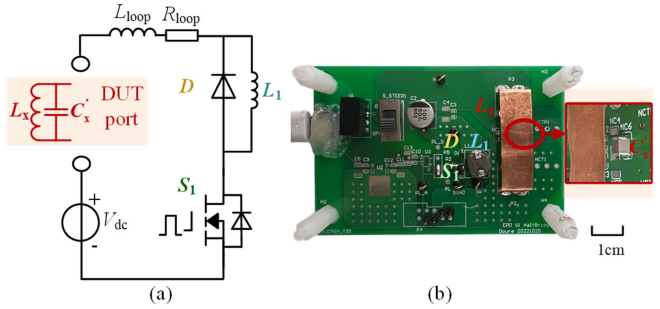

Fig. 7. Demonstration of extraction kit. (a) Extraction kit circuit diagram. (b) Extraction kit hardware.

A. Hardware Design

Fig. 7 shows the extraction kit and its circuit diagram. According to (5), a smaller stray parameter would result in a higher oscillation frequency. Meanwhile, the oscillation decays faster under the larger α in (3). Thereby, the extraction kit aims at extending the extraction range by ensuring an oscillation with an evident waveform amplitude and a wide frequency coverage.

First, with a fixed bus voltage V_{dc}, a more obvious underdamped oscillation process could be generated by increasing the load current [32]. Second, the frequency coverage limitation is mainly caused by the difference between the ideal step excitation and the actual v_{DS}. The maximum frequency f_{max} excited by v_{DS} in the circuit is determined by the time t_f rising from zero to V_{dc} as follows:

$$f_{max} = \frac{1}{t_f}. \tag{11}$$

Taking the v_{DS} in Fig. 11(a) with t_f equals 6.202 ns as an example, the upper limit of the test frequency f_{max} is about 161.24 MHz.

B. Accuracy Analysis Based on Algorithm

For the uncertain target frequency characteristic in Figs. 3 and 4, the noninteger-period sampling might result in frequency spectrum leakage and frequency bias phenomenon [33]. The maximum induced frequency bias δ_ω can reach to half of the frequency resolution $\Delta\omega$, as in (12). That would affect the accuracy based on the conventional DFT, such as in [21]

$$\Delta\omega = \frac{2\pi}{T_{win}} \tag{12}$$

where T_{win} means the window duration in sampling.

Taking a second-order circuit as an example, the inductance extraction bias δ_L is related to the oscillation frequency ω_{real} and the frequency bias δ_ω from DFT in (13) and (14). ω_{cal} means the DFT result and ω_{real} means the true value of oscillation frequency.

$$\frac{\omega_{cal}}{\omega_{real}} = \frac{\omega_{real} + \delta_\omega}{\omega_{real}} = \frac{\frac{1}{\sqrt{(L+\delta_L)C}}}{\frac{1}{\sqrt{LC}}} = \sqrt{\frac{L}{L+\delta_L}} \tag{13}$$

$$\frac{\delta_L}{L} = \left| \left(\frac{\omega_{real}}{\omega_{real} + \delta_\omega} \right)^2 - 1 \right| \approx 2\frac{\delta_\omega}{\omega_{real}}. \tag{14}$$

TABLE I
PARAMETER OF THE MONTE CARLO SIMULATION

Parameter	Value
V_{dc}	600 V
i_{load}	10 A
C_{eq}	330 pF
R_{loop}	0.5 Ω
max(τ)	0.4 μs according to (3)
T_{win}	0.4 μs or 1.2 μs

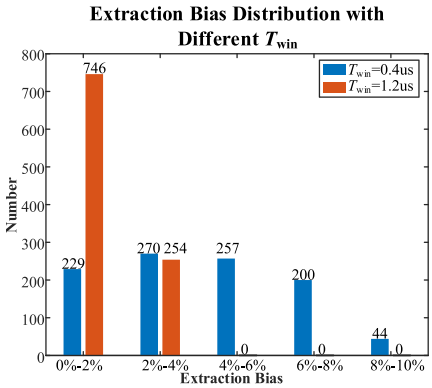

Fig. 8. Monte Carlo simulation results under different T_{win}.

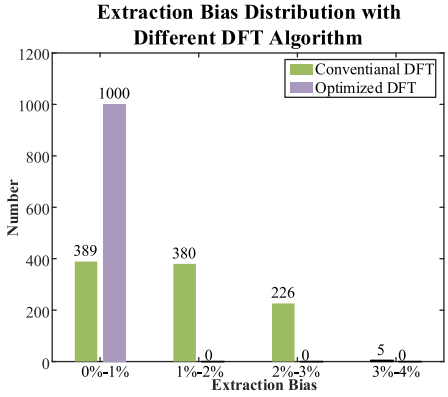

Fig. 9. Monte Carlo simulation for algorithms comparison.

Taking an inductance of 100 nH for instance, the maximum theoretical extraction bias calculated from Table I can be 9% and 3% under T_{win} value in 0.4 μs and 1.2 μs, respectively.

A Monte Carlo simulation is applied on (14) to analyze the extraction bias distribution under different T_{win}. The v_{DS} Monte Carlo trials are generated from (2) with 1000 random inductance values uniformly distributed within 50–100 nH and the corresponding parameters are set as in Table I. Then, DFT is applied on the v_{DS} trials to get ω_{cal}. The distribution of extraction bias obtained from (14) is shown in Fig. 8 .

Monte Carlo simulation results show that the maximum biases are located in 2%–4% and 8%–10% under T_{win} value in 0.4 μs and 1.2 μs, respectively. That matches well with the theoretical value 3% and 9% from (14). Meanwhile, the accuracy improvement is obvious when T_{win} is selected as 3τ.

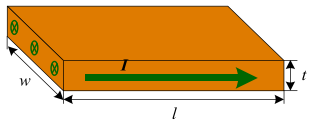

Fig. 10. Structure and size of the copper sheet.

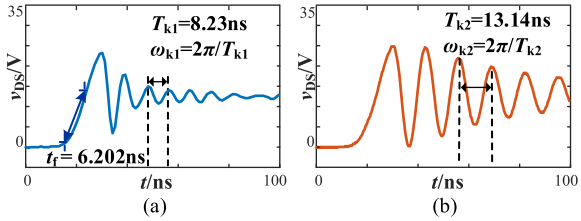

Fig. 11. Calibration for extraction kit. (a) C_0 disconnected. (b) C_0 connected.

Furthermore, methods such as iteration, interpolation [34], window-adding [35], and attenuation oscillation recognition algorithms [36] can also be introduced to improve the accuracy of frequency parameters. A DFT with interpolation is taken to improve the frequency resolution [34]. Fig. 9 shows that the optimized DFT algorithm could provide a more precise extraction result with bias under 1%.

V. APPLICATION EXAMPLES

The effectiveness of the proposed method is verified by its application on a copper sheet, power module, laminated busbar, and dc-link capacitor, as well as an overall commutation test.

A. Inductance Extraction of Copper Sheet With Standard Size

Fig. 10 shows the schematic diagram of the copper sheet element. The parameter to be extracted is the inductance L_x of the copper sheet, which has the following dimensions: thickness $t = 0.2$ mm, width $w = 10$ mm, and length $l = 33$ mm.

1) Effect of the Proposed Method: First, the circuit calibration is conducted as described in Section III-B. Two oscillation frequencies ω_{k1} and ω_{k2} are constructed with auxiliary capacitance C_0, as shown in Fig. 11. The calibration is carried out according to (5) and (7). The C_{eq} and L_{loop} are 63.85 pF and 26.84 nH, respectively.

Then, the copper sheet is connected to the DUT port in parallel with a 22 nF C_x', which is much larger than C_{eq}. The oscillation waveform and the frequency extraction results are shown in Fig. 12 . The L_x results from (9) and (10) are 15.94 nH and 15.99 nH, respectively, which differs less than 0.4%, confirming the rationality of the analysis in Section III-C.

2) Comparison With Other Methods: Table II summarizes the inductance values obtained through three different ways. The theoretical value of the copper sheet inductance was obtained according to (15) [37], [38]. The value of the copper sheet inductance from the Ansys Q3D simulation is also included. Fig. 13 shows the results from impedance analyzer. Due to the impact of the fixture, the average result in three rounds is selected

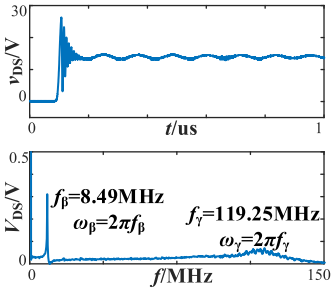

Fig. 12. Test waveforms with copper.

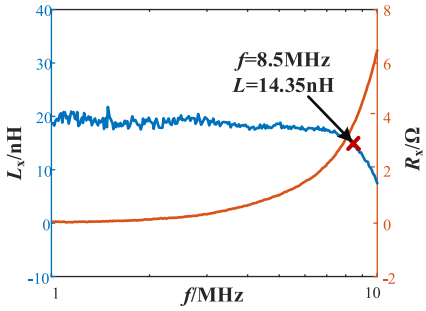

Fig. 13. Results from impedance analyzer (Agilent 4294A).

TABLE II
COMPARISON OF DIFFERENT METHODS

Extraction Method	Result/nH
Proposed Method	15.94
Theoretical Calculation	16.08
Electromagnetic Simulation	15.67
Impedance Analyzer	16.88 (①14.35; ②19.49; ③16.81)

as the measured value.

$$L = 2l\left(\ln\left(\frac{2l}{w+t}\right) + 0.5 + 0.2235\left(\frac{w+t}{l}\right)\right) \times 10^{-7}. \tag{15}$$

It can be seen that the copper sheet inductance values obtained by the first three methods are very close. The results obtained by the impedance analyzer are larger than the previous ones.

B. Power Module Stray Inductance Extraction

Fig. 14 shows the application of the proposed method for extracting the stray inductance inside of a power module. The silicon carbide (SiC) power module shown in Fig. 14(a) owns a half-bridge structure, including upper device T_1 and lower device T_2. Through different terminal connections, the inside stray inductance of the module in each part can be extracted. Through the calibration, we get C_{eq} and L_{loop} as 351.39 pF and 43.68 nH, respectively.

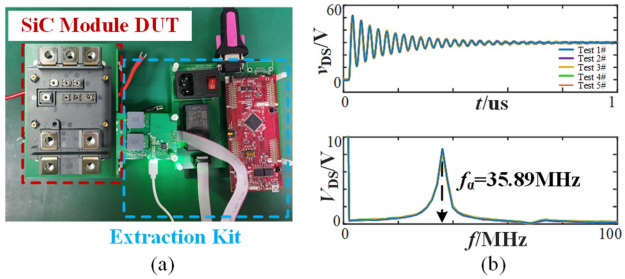

Fig. 14. SiC power module stray inductance extraction. (a) Extraction setup. (b) Extraction waveforms.

TABLE III
POWER MODULE STRAY INDUCTANCE RESULTS

Parameter	Proposed Method	Impedance Analyzer	Relative Error
Upper device T_1	12.29 nH	12.10 nH	1.6%
Lower device T_2	10.31 nH	9.81 nH	3.3%

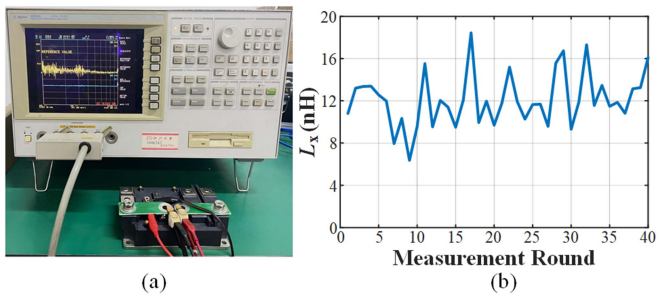

Fig. 15. Power module stray inductance measured by impedance analyzer. (a) Impedance analyzer setup. (b) Measurement result under each round.

Taking the upper device T_1 of the module as the DUT, the five-round results from the proposed method are shown in Fig. 14(b). The stray inductance of both devices (T_1, T_2) can be extracted from (6) and summarized in Table III.

The stray inductance is also measured by the impedance analyzer. The upper device T_1 in Fig. 15(a) is taken as DUT and the inductance from the PCB connector has been considered in the calibration process before each measurement. A 40-round measurement is performed, and the results shown in Fig. 15(b) indicate that the measured inductance is located around 12.10 nH with a 50% fluctuation. The average value is adopted as the result of the impedance analyzer.

The extraction result in Table III shows that the difference between the two methods is around 3%.

C. DC-Link Capacitor Stray Inductance Extraction

Fig. 16 demonstrates the implementation of the proposed method to extract the stray inductance of a dc-link capacitor. To perform the accuracy improvement described in Section III-C, a 10 nF capacitor C_x' is put on the connecting busbar and is in parallel with the dc-link capacitor at the DUT port. The test waveforms obtained under different voltages and currents are shown in Fig. 16(b). The frequency spectrum analysis shows that despite the varying amplitude in each test, the consistent

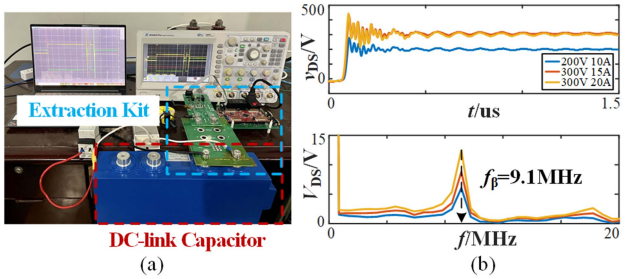

Fig. 16. DC-link capacitor stray inductance extraction. (a) Extraction setup. (b) Extraction waveforms.

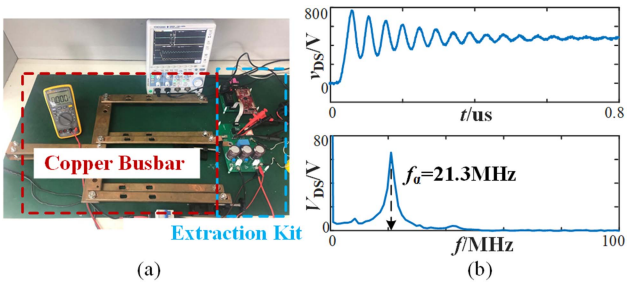

Fig. 17. Copper busbar stray inductance extraction. (a) Extraction setup. (b) Extraction waveforms.

TABLE IV
COPPER BUSBAR STRAY INDUCTANCE RESULTS

Busbar Section	Proposed Method	Impedance Analyzer	Relative Error
Phase A	249 nH	241 nH	3.3%
Phase B	159 nH	164 nH	3.0%
Phase C	201 nH	208 nH	3.3%

oscillation frequency information ensured the test result consistency.

By substituting the obtained ω_β into (10), the calculated stray inductance is found to be 29.94 nH, which is close to the impedance analyzer measurement result of 26.73 nH.

D. Copper Busbar Stray Inductance Extraction

In this section, the oscillation method is applied to extract the stray inductance of the copper busbar. Fig. 17 illustrates the test setup and waveform obtained when a three-phase copper busbar is connected to the DUT port.

The extracted stray inductance of each phase is given in Table IV. Compared with the extracted results of the impedance analyzer, the measurement error is around 3%.

E. Laminated Busbar Stray Parameter Extraction

Fig. 18 shows the application for extracting the stray parameters $C_{\rm lam}$ and $L_{\rm lam}$ of the laminated busbar. Similar to the parameter calculation in Section V-A, two oscillation frequencies ω_β and ω_γ are obtained by DFT. The extraction results from (9) are given in Table V.

Table V presents the comparison between the results obtained from the proposed method and the impedance analyzer. The

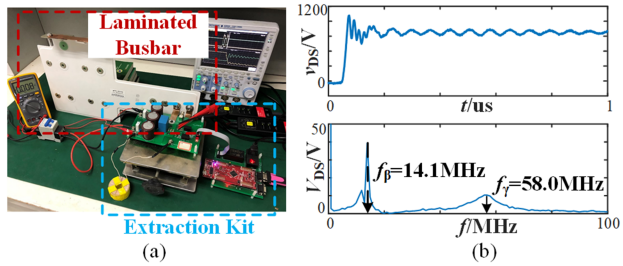

Fig. 18. Laminated busbar stray parameter extraction. (a) Extraction setup. (b) Extraction waveforms.

TABLE V
LAMINATED BUSBAR STRAY PARAMETERS

Parameter	Proposed Method	Impedance Analyzer	Relative Error
$L_{\rm lam}$	43.8 nH	44.4 nH	1.4%
$C_{\rm lam}$	2.76 nF	2.81 nF	1.8%

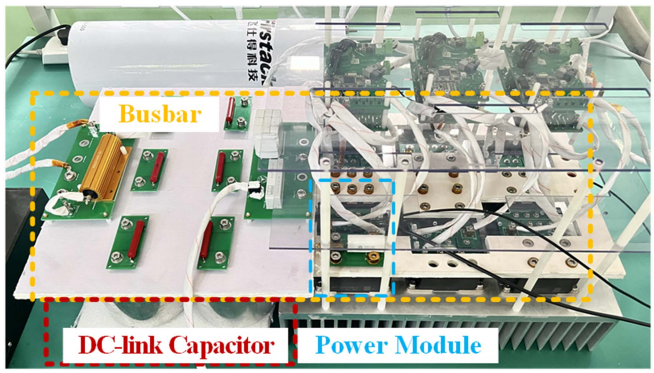

Fig. 19. Overall performance test in a half-bridge commutation process.

TABLE VI
DETAILED COMPONENT STRAY INDUCTANCE IN A COMMUTATION LOOP

DUT	Parameters	Results
Stray inductance in components	$L_{\rm cap}$ in DC-link capacitor	143.2 nH
	$L_{\rm upp}$ in the upper device	12.3 nH
	$L_{\rm bar}$ in busbar	36.8 nH
	$L_{\rm con}$ in terminals	78.6 nH
Total Value	$L_{\rm total}$	270.9 nH

relative difference is within 2%, demonstrating the effectiveness of the proposed method for extracting stray parameters of the laminated busbar that features in the inductance–capacitance coexisting structures.

F. Overall Performance in a Commutation Test

An SiC module double-pulse-test under 2100 V and 220 A is performed in Fig. 19. The commutation loop is composed of a busbar, dc-link capacitor, power semiconductor module, and the module terminal connector. The stray inductance in each component is extracted by the proposed method in advance, as given in Table VI.

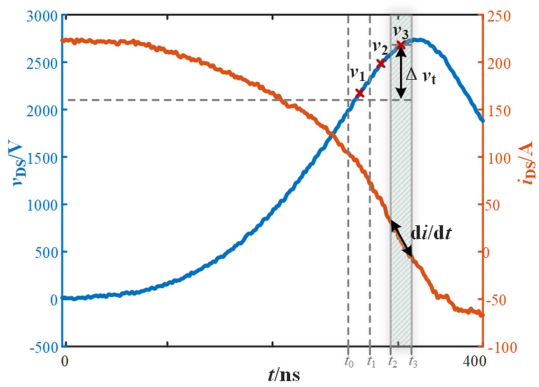

Fig. 20. Waveforms of voltage and current during turn-OFF transient process.

TABLE VII
VOLTAGE SPIKE FROM THE TEST AND ESTIMATION

	t_0–t_1	t_1–t_2	t_2–t_3
Tested di/dt	1.8 A/ns	1.9 A/ns	2.1 A/ns
Tested Δv_t	494.7 V	525.0 V	553.0 V
Estimated Δv_e	476.1 V	541.1 V	574.6 V
relative error	3.8%	3.1%	3.9%

The voltage value in three different sections during the time domain is taken for comparison, as shown in Fig. 20 and Table VII. The estimated Δv_e is calculated according to $\Delta v_e = L_{total} \cdot (\mathrm{d}i/\mathrm{d}t)$. It can be found that the estimated Δv_e in each section is close to the tested Δv_t. This implies that the sum of each component stray inductance obtained by the proposed method matches well with the total value in the commutation loop.

VI. CONCLUSION

This study features a stray parameter extraction method that can extract partial stray parameters in a commutation loop based on high-frequency oscillation characteristics during turn-OFF transients. The proposed method has several advantages over existing methods, including lower requirements for waveform amplitude measurement, channel sampling synchronization, and robustness to signal attenuation and latency. The mathematical derivation of the oscillation process and its frequency-domain analysis provide a reliable foundation for the extraction of stray parameters from second-order and fourth-order circuits. The experimental results demonstrate the effectiveness of the proposed method in extracting stray parameters from various components in the commutation loop of a high-power converter, including copper and laminated busbar, dc-link capacitor, and power semiconductor module. With its high precision, simple operation, and low extraction error, the proposed method can serve as a valuable tool for the optimization of key components in the converter circuit.

REFERENCES

[1] B. Zhang and S. Wang, "A survey of EMI research in power electronics systems with wide-bandgap semiconductor devices," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 626–643, Mar. 2020.

[2] P. Xiang, R. Hao, J. Cai, and X. You, "An active gate driver of SiC MOSFET module based on PCB Rogowski coil for optimizing tradeoff between overshoot and switching loss," *IEEE Trans. Power Electron.*, vol. 38, no. 1, pp. 245–260, Jan. 2023.

[3] M. Tahir, H. Sideng, and H. Xiangning, "Performance improvement strategies for discrete wide bandgap devices: A systematic review," *Front. Energy Res.*, vol. 9, no. 788689, pp. 4691–4699, Nov. 2021.

[4] B. F. Kjærsgaard et al., "Parasitic capacitive couplings in medium voltage power electronic systems: An overview," *IEEE Trans. Power Electron.*, vol. 38, no. 8, pp. 9793–9817, Aug. 2023.

[5] Y. Bai, S. Hu, Z. Yang, M. Tahir, and Y. Zhi, "A selective common mode noise mitigation method using phase-shifted modulation for four-switch buck-boost DC/DC converter," *IEEE Trans. Power Electron.*, vol. 38, no. 6, pp. 7183–7196, Jun. 2023.

[6] Y. Yang, Y. Wu, X. Ding, and P. Zhang, "Online junction temperature estimation method for SiC MOSFETs based on the DC bus voltage undershoot," *IEEE Trans. Power Electron.*, vol. 38, no. 4, pp. 5422–5431, Apr. 2023.

[7] J. Wang, H. S. Chung, and R. T. Li, "Characterization and experimental assessment of the effects of parasitic elements on the MOSFET switching performance," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 573–590, Jan. 2013.

[8] Z. Ma, Y. Pei, L. Wang, Q. Yang, Z. Qi, and G. Zeng, "An accurate analytical model of SiC MOSFETs for switching speed and switching loss calculation in high-voltage pulsed power supplies," *IEEE Trans. Power Electron.*, vol. 38, no. 3, pp. 3281–3297, Mar. 2023.

[9] K. Zhang, M. Cai, M. Yun, L. Song, and D. Yang, "Comparison experiment of parasitic inductance extraction of power module based on ANSYS Q3D software," in *Proc. 18th China Int. Forum Solid State Lighting 7th Int. Forum Wide Bandgap Semicond.*, 2021, pp. 58–60.

[10] F. Palomba et al., "Analysis of the gate driver stray inductance in a Vienna rectifier through parametric electromagnetic simulations," in *Proc. 11th Int. Conf. Integr. Power Electron. Syst.*, 2020, pp. 1–7.

[11] Z. Liu, X. Huang, F. C. Lee, and Q. Li, "Package parasitic inductance extraction and simulation model development for the high-voltage cascode GaN HEMT," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1977–1985, Apr. 2014.

[12] T. Liu, T. T. Y. Wong, and Z. J. Shen, "A new characterization technique for extracting parasitic inductances of SiC power MOSFETs in discrete and module packages based on two-port S-parameters measurement," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9819–9833, Nov. 2018.

[13] "Agilent PN 4294A new technologies for accurate impedance measurement product note," Agilent Technologies. Accessed: Sep. 5, 2023. [Online]. Available: http://bee.mif.pg.gda.pl/ciasteczkowypotwor/HP/Publikacje/5968-4506E.pdf

[14] H. Zhu, A. R. Hefner, and J.-S. Lai, "Characterization of power electronics system interconnect parasitics using time domain reflectometry," *IEEE Trans. Power Electron.*, vol. 14, no. 4, pp. 622–628, Jul. 1999.

[15] Z.-N. Ariga, K. Wada, and T. Shimizu, "TDR measurement method for voltage-dependent capacitance of power devices and components," *IEEE Trans. Power Electron.*, vol. 27, no. 7, pp. 3444–3451, Jul. 2012.

[16] *ABCs of Probes Primer*. Beaverton, OR, USA: Tektronix, 2016.

[17] Y. Li, Y. Gao, Y. Zhang, J. Liu, and C. Nie, "Accurate SiC MOSFET chip extraction based on parasitic parameter impact compensation," *IEEE Trans. Power Electron.*, vol. 38, no. 3, pp. 3201–3212, Mar. 2023.

[18] H. Li, Z. Gao, R. Chen, and F. Wang, "Improved double pulse test for accurate dynamic characterization of medium voltage SiC devices," *IEEE Trans. Power Electron.*, vol. 38, no. 2, pp. 1779–1790, Feb. 2023.

[19] A. Zhu, H. Gao, Y. Xia, H. Luo, W. Li, and X. He, "Adaptive stray inductance extraction algorithm using linear regression for power module with high noise immunity and accuracy," *China Power Supply Soc. Trans. Power Electron. Appl.*, vol. 7, no. 2, pp. 176–185, Jun. 2022.

[20] Y. Jiang et al., "An experimental method for extracting stray inductance of bus bars without high bandwidth current measurement," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2017, pp. 1446–1450.

[21] S. Hu, M. Wang, Z. Liang, and X. He, "A frequency-based stray parameter extraction method based on oscillation in SiC MOSFET dynamics," *IEEE Trans. Power Electron.*, vol. 36, no. 6, pp. 6153–6157, Jun. 2021.

[22] M. Dong, H. Li, S. Yin, Y. Wu, and K. Y. See, "A postprocessing-technique-based switching loss estimation method for GaN devices," *IEEE Trans. Power Electron.*, vol. 36, no. 7, pp. 8253–8266, Jul. 2021.

[23] C. Qian, Z. Wang, G. Xin, and X. Shi, "Datasheet driven switching loss, turn-ON/OFF overvoltage, DI/DT, and DV/DT prediction method for SiC MOSFET," *IEEE Trans. Power Electron.*, vol. 37, no. 8, pp. 9551–9570, Aug. 2022.

[24] X. Li, F. Xiao, Y. Luo, R. Wang, and Z. Shi, "An improved equivalent circuit model of SiC MOSFET and its switching behavior predicting method," *IEEE Trans. Ind. Electron.*, vol. 69, no. 9, pp. 9462–9471, Sep. 2022.
[25] M. Tahir, S. Hu, and Z. Zhu, "Cable stray parameters impact exploration on stability of DC distributed power system," in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, 2022, pp. 1–6.
[26] R. Mirzadarani, H. R. Mohammadi, A. Ketabi, S. R. Motahari, and A. Ghorbani, "Analytical estimation of parasitic capacitances in high-voltage switching transformers," *Inst. Eng. Technol. Power Electron.*, vol. 13, no. 16, pp. 3830–3839, Dec. 2020.
[27] Z. Yuan et al., "Insulation and switching performance optimization for partial-discharge-free laminated busbar in more-electric aircraft applications," *IEEE Trans. Power Electron.*, vol. 37, no. 6, pp. 6831–6843, Jun. 2022.
[28] C. Chen, X. Pei, Y. Chen, and Y. Kang, "Investigation, evaluation, and optimization of stray inductance in laminated busbar," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3679–3693, Jul. 2014.
[29] Y. Meng, Z. Liang, S. Hu, Z. Ma, and X. He, "Unit partition method for the resonance research in the dc-link busbar of back-to-back converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2020, pp. 4178–4181.
[30] Z. Wang, Y. Wu, M. H. Mahmud, Z. Yuan, Y. Zhao, and H. A. Mantooth, "Busbar design and optimization for voltage overshoot mitigation of a silicon carbide high-power three-phase T-type inverter," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 204–214, Jan. 2021.
[31] "Mitsubishi electric to launch LV100-type T-series IGBT module for industrial use," Mitsubishi Electric Corp. Accessed: Sep. 5, 2023. [Online]. Available: https://emea.mitsubishielectric.com/en/news/releases/global/2020/0825-a/pdf/200825-a_3367_en_g.pdf
[32] "Time-domain analysis of discrete systems," in *A Practical Approach to Signals and Systems*. Hoboken, NJ, USA: Wiley, 2008.
[33] W. Sun, H. Jin, B. Hu, A. Chen, H. Zhang, and J. Peng, "Research on high accurate measurement on dual frequency signals," in *Proc. IEEE 15th Int. Conf. Electron. Meas. Instrum.*, 2021, pp. 151–156.
[34] Ç. Candan, "A method for fine resolution frequency estimation from three DFT samples," *IEEE Signal Process. Lett.*, vol. 18, no. 6, pp. 351–354, Jun. 2011.
[35] S. R. Chintakindi, O. V. S. R. Varaprasad, and D. V. S. S. S. Sarma, "Improved Hanning window based interpolated FFT for power harmonic analysis," in *Proc. IEEE Region 10 Conf.*, 2015, pp. 1–5.
[36] S. Singh, "Prony toolbox—file exchange—MATLAB central." Accessed: Sep. 5, 2023. [Online]. Available: https://ww2.mathworks.cn/matlabcentral/fileexchange/3955-prony-toolbox
[37] C. R. Paul, *Inductance: Loop and Partial*. Hoboken, NJ, USA: Wiley, 2011.
[38] A. D. Callegaro et al., "Bus bar design for high-power inverters," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2354–2367, Mar. 2018.

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