Predictive Discontinuous Modulation Strategy With Embedded Inter-Phase Cluster Voltage Control for Cascaded H-Bridge StatComs

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***Abstract*—The discontinuous pulsewidth modulation (DPWM) in cascaded H-bridge (CHB) static compensators (StatComs) is achieved via adding a common mode voltage to the converter voltage references. Hence, in discontinuously operated CHB StatComs, the common mode voltage has two functions, namely, interphase cluster voltage control and clamping a converter voltage. These two functions are conventionally achieved by two independently designed control stages and interferences between them can cause the loss of cluster voltage control during unbalanced grid conditions, since the fundamental frequency common mode voltage for discontinuous operation is significant. To solve this control issue, this article proposes a DPWM strategy with embedded interphase cluster voltage control using a finite control set model predictive control approach. The proposed predictive DPWM outperforms the conventional DPWM in switching loss reduction while preventing the cluster voltages from diverging during unbalanced grid conditions. The effectiveness of the proposed strategy is verified experimentally considering various grid conditions.**

***Index Terms*—Cascaded H-Bridge (CHB), discontinuous pulsewidth modulation (DPWM), model predictive control (MPC), static compensator (StatCom).**

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I. Introduction

DISCONTINUOUS pulsewidth modulation (DPWM) strategies are employed for reducing switching loss, enhancing converter reliability, and improving power quality [1], [2], [3], [4], [5], [6], [7], [8]. DPWM consists of clamping a converter ac-side voltage to its dc-link voltage, preventing switching. Adding a zero-sequence voltage (ZSV) to the converter voltage references represents a common approach in three-phase converters.

DPWM is a commonly used technique in converters with a shared dc-link among the three phases, such as the two-level converter and the neutral-point-clamped converter [9], [10], [11], [12]. It is important to note that in such converters, even if a nonnegligible fundamental component appears in the ZSV for DPWM (occurs under unbalanced grid conditions), the per-phase active powers due to the interaction between the ZSV and the corresponding grid current sum to zero at the dc-link [9], [10], [11], [12]. This characteristic simplifies the implementation of DPWM in these converters. However, in the cascaded H-bridge (CHB) static compensators (StatComs), DPWM implementation is less common, as there is no common dc-link [13], [14], [15], [16]. Instead, the dc-side of each leg is made up of floating capacitors, namely one per submodule (SM), as shown in Fig. 1. In this converter, the phase active powers introduced to each dc-side due to DPWM do not cancel out, and therefore affect the individual capacitor voltages.

In CHB StatComs with a star configuration, DPWM can be achieved by clamping the ac-side voltage of a CHB converter leg to an integer fraction of its corresponding cluster voltage (sum of capacitor voltages within the leg) [17]. The conventional DPWM strategy for CHB StatComs involves two independent control stages for calculating the ZSV [18]. First, a fundamental-frequency ZSV (FFZSV) for interphase cluster voltage control is calculated and added to the current control outputs to form the fundamental-frequency converter voltage references. Then, a logic-based algorithm uses these voltage references and the measured capacitor voltages as input to calculate a piecewise

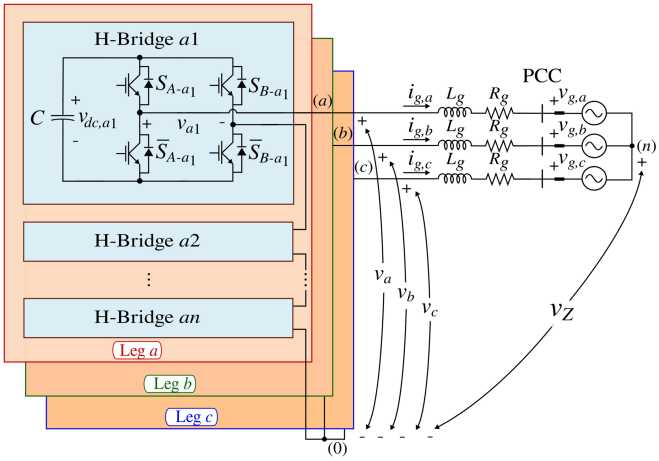

Fig. 1. Circuit diagram of a three-phase CHB power converter with star configuration.

continuous ZSV for discontinuous operation. This conventional strategy works well for balanced grid conditions as the piecewise ZSV for DPWM only consists of triplen harmonics, which do not affect the phase active powers. However, when grid imbalances occur, the logic-based module for DPWM calculates a ZSV with a nonnegligible fundamental-frequency component, which alters the active powers in the phases and tends to cause divergence of the cluster voltages. The two control stages become strongly coupled in this scenario, potentially compromising system stability [19].

To overcome the aforementioned control interactions in the conventional DPWM implementations, a DPWM strategy is proposed in [19]. Despite the fact that the strategy in [19] has a similar hierarchical control scheme as [18], where the unique ZSV is calculated in two stages, it eliminates the fundamental-frequency component in the ZSV for DPWM. However, follow-up research reveals that the performance of the DPWM in [19] is highly related to the phase-angle and frequency of the triangular carrier used to introduce extra switching events to shape the ZSV in a way that decoupling is satisfied [20]. The challenge of finding the optimal carrier renders this DPWM strategy less attractive in practice. Moreover, the DPWM strategy in [19], [20] is highly dependent on the interphase cluster voltage controller.

An advanced DPWM implementation with embedded interphase cluster voltage control is proposed in this article to deal with the aforementioned control issues of the conventional approaches. As previously stated, DPWM can be achieved by clamping the converter ac-side voltage to an integer fraction of the corresponding cluster voltage. As a result, at each time step, there is a finite set of ZSV candidates to achieve DPWM. Accordingly, finite control set model predictive control (FCS-MPC) is used in this article to choose the optimal ZSV that best meets all the control tasks. Specifically, the proposed DPWM predicts, at each sampling step, and for each ZSV candidate, the one-step ahead peak values of the squared cluster voltages in each leg. Then, it chooses a ZSV candidate that minimizes the squared peak regulation error while clamping a leg. Modified second-order generalized integrators (SOGIs) [21] are discretized and included within the proposed prediction model for the purpose of extracting the peak values from the measured squared cluster voltages.

The rest of this article is organized as follows. Sections II and III revisit modeling of the CHB StatComs and the conventional DPWM strategy, respectively. Section IV presents the proposed DPWM strategy based on FCS-MPC. Section V experimentally compares the performance of the conventional DPWM and the proposed DPWM under various grid conditions, verifying the effectiveness of the proposed DPWM. Finally, Section VI concludes this article.

II. Mathematical Model of CHB StatComs

The topology of a three-phase CHB StatCom with star configuration is presented in Fig. 1. As it can be seen, the CHB converter has n H-bridge SMs in each leg, with $j \in \{1, 2, \ldots, n\}$ referring to the SM index within a leg. The dc-side of each SM consists of a floating capacitor C. The converter ac-side positive terminals, i.e., terminals (a), (b), and (c) in Fig. 1, are connected to the point of common coupling (PCC) grid voltages $v_{g,a}$, $v_{g,b}$, and $v_{g,c}$, through filtering inductors (L_g and R_g). The converter ac-side negative terminals are connected forming the neutral of the three-phase converter (0).

The total converter dc-side voltages $v_{dc,x}$ and ac-side voltages v_x in each phase x, with $x \in \{a, b, c\}$ indicating the phase index, are defined as the sum of the n individual voltages, i.e.,

$$v_{dc,x} = \sum_{j=1}^{n} v_{dc,xj} \tag{1}$$

$$v_x = \sum_{j=1}^{n} v_{xj}. \tag{2}$$

Henceforth, $v_{dc,x}$ and v_x are referred as cluster voltage and converter voltage, respectively.

The ac- and dc-side SM voltages, v_{xj} and $v_{dc,xj}$, respectively, are related by the modulating signals as

$$\delta_{xj} = \frac{v_{xj}}{v_{dc,xj}} \tag{3}$$

where, $\delta_{xj} \in [-1, 1]$.

During DPWM, clamping the leg x means that all the n signals δ_{xj} have a value belonging to the discrete set $\{-1, 0, 1\}$, or equivalently, v_{xj} is clamped to $\{-v_{dc,xj}, 0, v_{dc,xj}\}$ according to (3).

The converter voltage v_x can be regarded as the sum of a nonZSV component v'_x and a ZSV component v_Z, i.e.,

$$v_x = v'_x + v_Z \tag{4}$$

where, $(v_a + v_b + v_c)/3 = v_Z$. Note that v'_x satisfies the following relationship:

$$v'_x = L_g \frac{di_{g,x}}{dt} + R_g i_{g,x} + v_{g,x} \tag{5}$$

where, $i_{g,x}$ is the grid current. The grid voltages $v_{g,x}$ are calculated from the measured line-to-line grid voltages $v_{g,ab} = v_{g,a} - v_{g,b}$ and $v_{g,bc} = v_{g,b} - v_{g,c}$, considering $v_{g,a} + v_{g,b} + v_{g,c} = 0$.

Assuming inter-SM capacitor voltage balance, i.e., $v_{dc,xj} = v_{dc,x}/n$ for every j, and negligible converter losses, the following power relationship holds [22]:

$$\frac{1}{2}\frac{C}{n}\frac{dv_{dc,x}^2}{dt} = -\left(v_x' + v_Z\right) i_{g,x}. \tag{6}$$

The abovementioned equation represents the dynamics associated with the capacitor energy, which offers important advantages for the CHB StatCom control and design [22], [23]. Note that the fact that the ZSV v_Z could modify the active power of each phase if it contains a fundamental-frequency component is of great concern, which is addressed by the proposed method in Section IV.

III. Conventional DPWM Background

In this section, the boundaries of the ZSV in CHB StatComs to avoid overmodulation are first explained. Then, the conventional DPWM operating principle, control diagram, and drawbacks, are revisited.

A. ZSV Boundaries

To prevent the injected ZSV v_Z from causing overmodulation in a leg, the following constraint is considered:

$$|v_x| \le v_{dc,x}. \tag{7}$$

Substituting (4) into (7), the maximum and minimum boundaries for v_Z are derived

$$v_{Z,\min} \le v_Z \le v_{Z,\max} \tag{8}$$

where

$$\begin{cases} v_{Z,\max} = \min\left\{v_{dc,a} - v_a', v_{dc,b} - v_b', v_{dc,c} - v_c'\right\} \\ v_{Z,\min} = \max\left\{-v_{dc,a} - v_a', -v_{dc,b} - v_b', -v_{dc,c} - v_c'\right\}. \end{cases} \tag{9}$$

Note that $v_{Z,\max}$ and $v_{Z,\min}$ clamp a converter voltage v_x to its corresponding positive cluster voltage $v_{dc,x}$ and negative cluster voltage $-v_{dc,x}$, respectively.

B. Operating Principle

As previously mentioned, the ZSV v_Z under the conventional DPWM consists of a FFZSV component for interphase cluster voltage control, referred as v_{Zb}, and a ZSV component for DPWM, denoted as v_{Zd}, i.e.,

$$v_Z = v_{Zb} + v_{Zd} \tag{10}$$

each of them calculated by different control modules.

Since v_{Zb} is calculated by an outer control loop, the v_Z boundaries in (9) need to be rewritten in terms of v_{Zd}. Specifically, substituting (10) into (8)

$$v_{Zd,\min} \le v_{Zd} \le v_{Zd,\max} \tag{11}$$

with

$$\begin{cases} v_{Zd,\max} &= v_{Z,\max} - v_{Zb} \\ v_{Zd,\min} &= v_{Z,\min} - v_{Zb}. \end{cases} \tag{12}$$

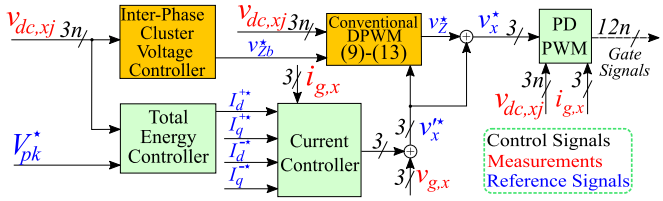

Fig. 2. Control block diagram of a CHB StatCom with conventional DPWM.

The conventional DPWM for CHB StatComs chooses the smallest magnitude of $v_{Zd,\max}$ and $v_{Zd,\min}$ as v_{Zd} [18], i.e.,

$$v_{Zd} = \begin{cases} v_{Zd,\max} & \text{if } |v_{Zd,\max}| \le |v_{Zd,\min}| \\ v_{Zd,\min} & \text{otherwise.} \end{cases} \tag{13}$$

C. Controller Diagram

The hierarchical control approach to implement the conventional DPWM is presented in Fig. 2 [19]. The interphase cluster voltage controller block calculates the FFZSV reference $v_{Zb}^{\star}$ that maintains the cluster voltage control among the legs [24]. The voltage references $v_x'^{\star}$ and $v_{Zb}^{\star}$, together with the measured capacitor voltages $v_{dc,xj}$, are used as inputs to the Conventional DPWM block, which calculates $v_Z^{\star}$ according to (9)–(13). Note that the superscripts $+$ and $-$ denote the positive- and negative-sequence components, and the subscripts d and q stand for the direct and quadrature components, respectively.

D. Drawbacks

Under balanced grid conditions, v_{Zd} mainly consists of triplen harmonics, and therefore, it does not affect phase active powers, i.e.,

$$\frac{1}{T_g}\int_0^{T_g} v_{Zd} i_{g,x} dt = 0 \tag{14}$$

where, T_g is the fundamental-frequency period. However, during grid imbalances, the v_{Zd} calculated by the logic-based algorithm in (13) contains a nonnegligible fundamental-frequency component which violates (14), leading to compromised interphase cluster voltage control. More details on this phenomenon can be found in [19].

Furthermore, in the case of severe grid voltage sags, clamping converter voltage references that are near zero to their respective cluster voltages requires a ZSV with substantial magnitude. This significantly impacts the capacitor voltage dynamics according to (6), and may result in potential stability issues.

IV. Proposed Predictive DPWM

This section presents a peak cluster voltage control strategy based on FCS-MPC for discontinuously operated CHB StatComs. In this section, the finite ZSV control set is first identified. Then, the methodology to predict the one-step ahead peak value of cluster voltages is described. Subsequently, the underlying optimization problem of the proposed DPWM, and the control block diagram are depicted.

A. ZSV Candidates

According to (9), at any control step there are always two possible candidates for v_Z to achieve DPWM, i.e., $v_{Z,\max}$ and $v_{Z,\min}$. However, it is noted that converter voltages are also allowed to be clamped to zero-voltage level in the CHB StatCom [19]. When a converter voltage is clamped to the zero-voltage level, the capacitors of the corresponding leg are bypassed. The required ZSV for clamping a converter voltage to zero-voltage level is denoted as $v_{Z,x0}$, which corresponds to

$$v_{Z,x0} = -v'_x. \tag{15}$$

It should be noted that the additional degrees of freedom provided by using zero-voltage levels alleviates the previously mentioned large-magnitude ZSV-related drawbacks of the conventional DPWM during severe grid voltage sags. Considering the boundaries of v_Z in (8), (15) is rewritten as

$$v_{Z,x0} = \begin{cases} -v'_x & \text{if } v_{Z,\min} \le -v'_x \le v_{Z,\max} \\ \infty & \text{otherwise.} \end{cases} \tag{16}$$

Note that using the zero-voltage level increases the candidates of v_Z for achieving DPWM from two to five

$$v_{Z,h} \in \{v_{Z,\max}, v_{Z,\min}, v_{Z,a0}, v_{Z,b0}, v_{Z,c0}\} \tag{17}$$

where, $h \in \{1, 2, \ldots, 5\}$ is the index used to indicate the different v_Z candidates in (17).

B. Predicted Peak Value of Cluster Voltages

If interphase cluster voltage control functionality is to be embedded within the DPWM algorithm, a prediction model for the cluster voltages is needed. According to (4) and (6), the one-step ahead squared cluster voltage candidates, denoted as, $v^2_{dc,x,h}(k+1)$, for different $v_{Z,h}$ candidates in (17), correspond to

$$v^2_{dc,x,h}(k+1) = v^2_{dc,x}(k) - \frac{2T_s}{C/n} i_{g,x}(k)\left(v'_x(k) + v_{Z,h}(k)\right) \tag{18}$$

where, T_s is the sampling time, and k refers to the sampling step. Note that sampled values $v^2_{dc,x}(k)$, $i_{g,x}(k)$, and $v'_x(k)$ are known within the controller, and $v_{Z,h}(k)$ candidates are readily available according to (9) and (16). Then, predictions $v^2_{dc,x,h}(k+1)$ for each $v_{Z,h}(k)$ candidate in (18) can be calculated.

To simplify the notation in the following developments, the squared cluster voltage $v^2_{dc,x}$ is represented by u_x:

$$u_x = v^2_{dc,x}. \tag{19}$$

Furthermore, for the sake of brevity, given the symmetry among legs, the subscript corresponding to each leg, x, is dropped.

The squared cluster voltages u under DPWM can be approximated as the sum of a twice-fundamental-frequency component, denoted as $\widetilde{u}_{2\omega}$, and a dc-component, denoted as $\overline{u}$, [22], i.e.,

$$u = \widetilde{u}_{2\omega} + \overline{u}. \tag{20}$$

This approximation, where the harmonics in u at frequencies other than the second have been neglected, has shown to work well in the experiment attributed to the cost function defined in the optimization problem [specifically (35) in Section IV-C]. Note that other frequency harmonics in u, for example 4th and 6th harmonics, could have readily been considered by means of using a multiple frequency-decoupled SOGI filters [25].

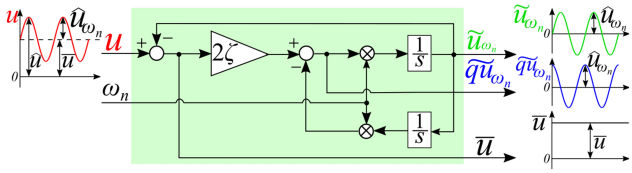

Fig. 3. SOGI filter.

Fig. 3 presents the continuous-time block diagram of a SOGI filter, which is used to obtain the ω_n-frequency harmonic in the input signal u, denoted as $\widetilde{u}_{\omega_n}$, and its quadrature counterpart, denoted as $\widetilde{qu}_{\omega_n}$ [21]. Note that the direct-component $\widetilde{u}_{\omega_n}$ and the quadrature-component $\widetilde{qu}_{\omega_n}$ as well the dc-component $\overline{u}$ have to be extracted in order to obtain the corresponding peak value. The transfer functions from the input signal u to $\widetilde{u}_{\omega_n}$ and $\widetilde{qu}_{\omega_n}$ are given by [21]

$$\frac{\widetilde{u}_{\omega_n}(s)}{u(s)} = \frac{2\zeta\omega_n s}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{21}$$

$$\frac{\widetilde{qu}_{\omega_n}(s)}{u(s)} = \frac{2\zeta s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{22}$$

where, ζ is the SOGI's damping ratio. Note that a small damping ratio between 0.1 and 0.4 is suggested in this study to achieve accurate harmonic extraction performance for peak value prediction and ensure stable operation.

To integrate the SOGI filter within the proposed MPC approach, (21) and (22) are converted to the z-domain via the bilinear approximation [26], i.e.,

$$s = \frac{2}{T_s}\frac{z-1}{z+1} \tag{23}$$

leading to

$$\frac{\widetilde{u}_{\omega n}(z)}{u(z)} = \frac{a_3 - a_3 z^{-2}}{(a_1 + a_3) + a_2 z^{-1} + (a_1 - a_3) z^{-2}} \tag{24}$$

$$\frac{\widetilde{qu}_{\omega n}(z)}{u(z)} = \frac{a_4 - 2a_4 z^{-1} + a_4 z^{-2}}{(a_1 + a_3) + a_2 z^{-1} + (a_1 - a_3) z^{-2}} \tag{25}$$

with coefficients

$$\begin{aligned} a_1 &= \omega_n^2 T_s^2 + 4, \quad & a_2 &= 2\omega_n^2 T_s^2 - 8 \\ a_3 &= 4\zeta\omega_n T_s, & a_4 &= 8\zeta. \end{aligned} \tag{26}$$

According to (24) and (25), the difference equations for calculating the second harmonic in u, its quadrature counterpart, and the dc-component in u, are given by

$$\begin{aligned} \widetilde{u}_{2\omega,h}(k+1) = \frac{1}{(a_1 + a_3)} &\left[a_3 u_h(k+1) - a_3 u(k-1)\right. \\ &\left. - a_2 \widetilde{u}_{2\omega}(k) - (a_1 - a_3)\widetilde{u}_{2\omega}(k-1)\right] \end{aligned} \tag{27}$$

$$\begin{aligned} \widetilde{qu}_{2\omega,h}(k+1) = \frac{1}{(a_1 + a_3)} &\left[a_4 u_h(k+1) - 2a_4 u(k)\right. \\ &+ a_4 u(k-1) - a_2 \widetilde{qu}_{2\omega}(k) \\ &\left. - (a_1 - a_3)\widetilde{qu}_{2\omega}(k-1)\right] \end{aligned} \tag{28}$$

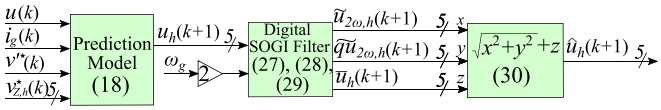

Fig. 4. Proposed discrete-time model for predicting the peak value of the squared cluster voltages.

$$\overline{u}_h\left(k+1\right) = u_h\left(k+1\right) - \widetilde{u}_{2\omega,h}\left(k+1\right) \tag{29}$$

where, $\omega_n = 2\omega_g$, ω_g being the grid angular frequency. Note that the values of u, $\widetilde{u}_{2\omega}$, and $\widetilde{qu}_{2\omega}$ at steps k and $k-1$ in (27) and (28) are memory-stored values from previous control steps, which are calculated based on the optimal v_Z applied.

Consequently, the peak value of u under each ZSV candidate can be readily calculated as

$$\widehat{u}_h\left(k+1\right) = \sqrt{\left(\widetilde{u}_{2\omega,h}\left(k+1\right)\right)^2 + \left(\widetilde{qu}_{2\omega,h}\left(k+1\right)\right)^2} + \overline{u}_h\left(k+1\right). \tag{30}$$

Fig. 4 depicts the procedure for obtaining the peak value predictions in (30).

C. Underlying Optimization Problem

The proposed strategy finds the optimal v_Z that minimizes a cost function J, by evaluating the five candidates $v_{Z,h}$ defined in (17) at each sampling step, i.e.,

$$\begin{aligned} v_Z(k) = \text{arg minimize } & J \\ v_{Z,h} & \\ \text{subject to (17)–(30).} & \end{aligned} \tag{31}$$

The proposed cost function consists of three terms, i.e.,

$$J = J_1 + \alpha_2 J_2 + \alpha_3 J_3 \tag{32}$$

where, α_2 and α_3 are positive weighting factors to tradeoff different control objectives.

Specifically, J_1 is used for balancing the interphase cluster voltage peak values by selecting the optimal ZSV, which minimizes the differences of the three-phase peak value predictions

$$J_1 = \sum_{x=a,b,c}\left(\widehat{u}_{x,h}\left(k+1\right) - \overline{\widehat{u}_{x,h}}\left(k+1\right)\right)^2 \tag{33}$$

in which

$$\overline{\widehat{u}_{x,h}}\left(k+1\right) = \frac{1}{3}\sum_{x=a,b,c}\widehat{u}_{x,h}\left(k+1\right) \tag{34}$$

where, $\widehat{u}_{x,h}(k+1)$ corresponds to the predicted peak values according to (30). Note that $\overline{u}_h(k+1)$ can be used as an alternative option to using $\widehat{u}_{x,h}(k+1)$ in J_1 for interphase capacitor voltage control.

The cost term J_2 is introduced to minimize the harmonics in v_Z by making it track only its fundamental-frequency component

$$J_2 = \left(I^+_{q,pu}\left(v_{Z,h}(k) - v^f_{Z,h}(k)\right)\right)^2 \tag{35}$$

where, $I^+_{q,pu} = I^+_q/I_n$ is the normalized value of I^+_q, with I_n referring to the rated grid current. Variable v^f_Z denotes the fundamental-frequency component of v_Z, which is calculated using a discretized SOGI filter as in (24) and (27), but with $\omega_n = \omega_g$ in this case, i.e.,

$$\begin{aligned} v^f_{Z,h}(k) = \frac{1}{(a_1+a_3)}\big[&a_3 v_{Z,h}(k) - a_3 v_Z\left(k-2\right) \\ &- a_2 v^f_Z\left(k-1\right) - \left(a_1 - a_3\right) v^f_Z\left(k-2\right)\big] \end{aligned} \tag{36}$$

where, v_Z and v^f_Z at steps $k-2$ and $k-1$ are memory-stored values from previous control steps. Note that the values at steps $k-2$ and $k-1$ are not available at the start of the iteration process. However, their effect vanishes in the steady-state due to the stable behavior of the filter transfer function described by (36). The fundamental-frequency component in the ZSV only introduces the second harmonic and the dc-component to the cluster voltages when it interacts with the grid currents, which reinforces the assumption in (20). In addition, according to (6), the harmonic magnitudes in u are proportional to the grid current amplitude, hence the term $I^+_{q,pu}$ is used in (35) to make α_2 less dependent on the operating point. For I^+_q values close to the rated value, harmonics in u become large, and minimization of J_2 gains more priority.

To prevent the index h of applied ZSV candidate from changing at each control step (for instance, when different legs are clamped alternatively at a high frequency), cost term J_3 is added, which is given by

$$J_3 = \left(v_{Z,h}(k) - v_Z\left(k-1\right)\right)^2 \tag{37}$$

where, $v_Z(k-1)$ is the optimal ZSV applied in step $k-1$.

Weighting factors are distributed to J_2 and J_3 since J_1 is the main cost term which guarantees interphase cluster voltage control. The strategy for choosing the values of α_2 and α_3 is as follows. First, α_2 is gradually increased until the cluster voltages exhibit primarily double-grid frequency and interphase cluster voltage control is not compromised. Second, α_3 is increased until the updating rate of the clamped leg and voltage level, represented by h, becomes low and clear.

Note that other control objectives could have been discussed and included in the cost function (30), such as switching loss minimization [27], given the flexibility of the formulation. However, the main contribution of the article is to efficiently embed the interphase cluster voltage control within the DPWM scheme.

D. Controller Diagram

The proposed DPWM implementation scheme is presented in Fig. 5. When compared to the control scheme for the conventional DPWM in Fig. 2, it can be seen that the interphase cluster voltage controller block and the DPWM block are integrated in the MPC-DPWM block. As a result, effective decoupling is achieved. The rest of the control diagram remains the same. Particularly, inter-SM capacitor voltage control is achieved by using a sorting algorithm in conjunction with a phase-disposition PWM scheme [17].

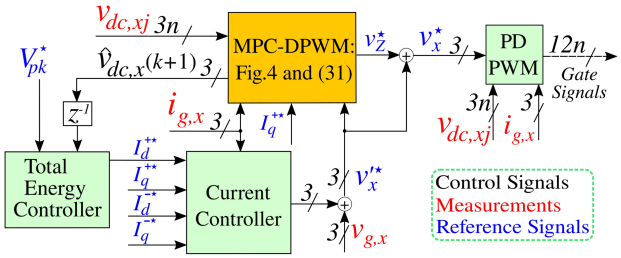

Fig. 5. Control block diagram of a CHB StatCom with the proposed predictive DPWM with embedded interphase cluster voltage control.

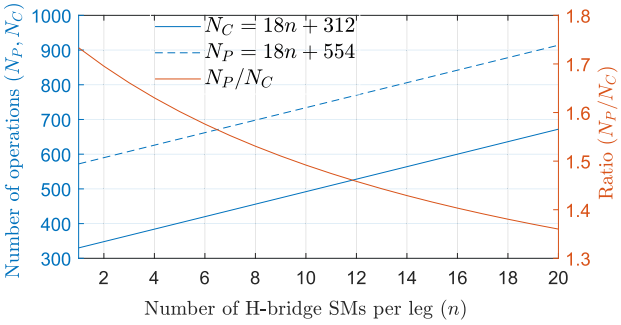

Fig. 6. Number of operations as a function of n, with N_C and N_P referring to the number of operations under the conventional DPWM and the proposed DPWM, respectively.

It is worth mentioning that since predicted peak values of the squared cluster voltages are available within the MPC-DPWM block, they can be readily used by the total energy controller block.

E. Calculation Burden

Fig. 6 assesses the required total number of operations as a function of the number of H-bridge SMs per leg, i.e., n, for both DPWM control schemes shown in Figs. 2 and 5.

As Fig. 6 depicts, the number of mathematical operations for both the conventional DPWM controller and the proposed DPWM controller, denoted as N_C and N_P, respectively, increase linearly with n and at the same rate, while the ratio N_P/N_C approaches 1 as n increases, since $\lim_{n\to\infty} N_P/N_C = 1$. The proposed DPWM has a higher computational burden than the conventional DPWM. This is mainly due to the fact that the proposed method considers three new degrees of freedom regarding the selection of the ZSV, that is, clamping the converter voltages to zero. This added clamping level has shown to be advantageous in grid voltage unbalanced conditions, such as grid voltage sags and faults, and for switching loss reduction [19]. Consequently, the proposed method results in a much better performance in terms of converter loss and capacitor voltage control as discussed in the next section, at the expense of an increased calculation burden compared to the conventional DPWM. However, the increase in calculation burden is not significant and can be readily handled by a standard digital device. The results in Fig. 6 have been corroborated through the use of the "tic toc" MATLAB function in a detailed simulation model with $n = 5$ [28].

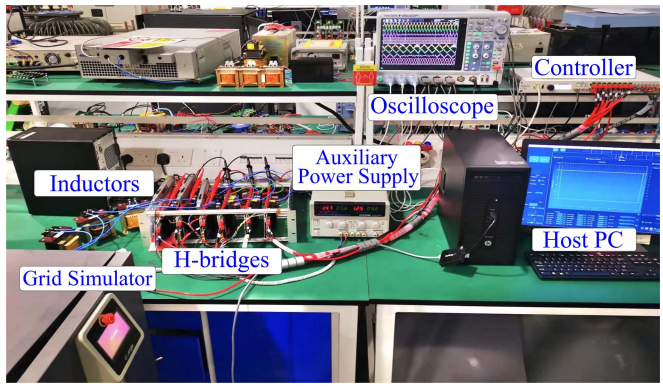

Fig. 7. Experimental setup.

TABLE I
EXPERIMENTAL SYSTEM PARAMETERS

Parameters	Value
PCC grid voltage nominal amplitude, V_{gn}	$100\sqrt{2}$ V
Nominal reactive power, Q_n	2.5 kVAr
Grid angular frequency, ω_g	100π rad/s
Carrier frequency, f_{sw}	9 kHz
Control/sampling frequency, f_s	25 kHz
SMs in each leg, n	2
Peak cluster voltage, V_{pk}	$1.3V_{gn}$
Capacitance per H-bridge, C	1 mF
Filter inductance, L_g	2 mH
SOGI's damping ratio, ζ	0.15
Weighting factor α_2	200
Weighting factor α_3	10

V. EXPERIMENTAL RESULTS

This section experimentally compares the proposed DPWM scheme with the conventional DPWM. The comparison includes waveforms under balanced grid conditions and unbalanced grid conditions. Experimental results are obtained using a CHB StatCom prototype with six IMPERIX PEH2015 H-bridge converters. The PCC grid voltages are provided by a GL&EL 15-kVA CINERGIA grid emulator. A B-Box RCP 3.0 from IMPERIX has been used to implement the controller shown in Figs. 2 and 5. The experimental setup is shown in Fig. 7, and the system parameters are given in Table I.

A. Balanced Grid Condition

1) Current Transition: Fig. 8 presents main CHB StatCom waveforms during a transition from rated capacitive current $I^+_{q,pu} = -1$ to rated inductive current $I^+_{q,pu} = 1$ under balanced grid condition. Specifically, Fig. 8 presents, from top to bottom, individual capacitor voltages (six traces), grid currents, modulating signals in phase a, and ZSV. Fig. 8(a) depicts waveforms in the conventional DPWM, whereas Fig. 8(b) depicts them in the proposed predictive DPWM. As it can be observed, both the proposed DPWM and the conventional DPWM present fast transient performance. The individual capacitor voltages under both modulation schemes are well balanced and their peak values are well regulated, as predicted and the waveforms corroborate. Note that the proposed DPWM presents similar low-frequency capacitor voltage ripples as the convention DPWM, which

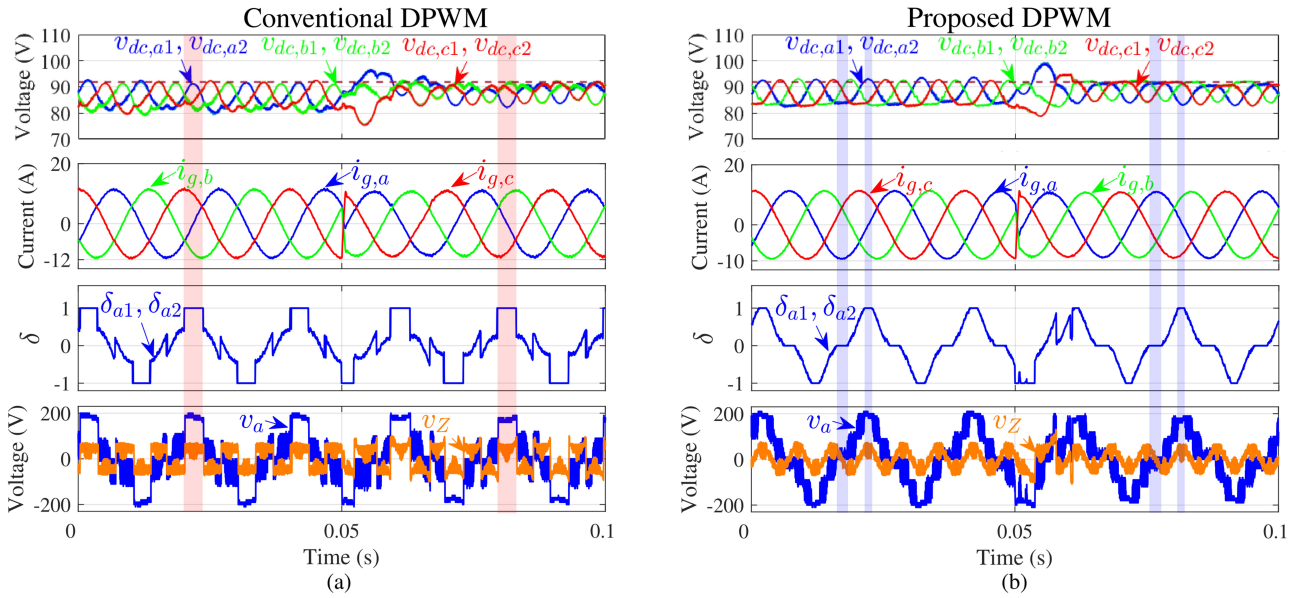

Fig. 8. Transition from 1 p.u. capacitive current to 1 p.u. inductive current at $t = 0.05$ s under balanced grid condition. (a) Conventional DPWM and (b) proposed DPWM.

are smaller than when the continuous pulsewidth modulation (CPWM) is applied, as it was shown in [19].

It is important to highlight the differences between the two modulation schemes in terms of modulating signals, which reflect the clamping behavior of the two DPWM strategies. As it can be observed, δ_{a1} and δ_{a2} are clamped either to 1 or -1 under the conventional DPWM. It is worth noting that these clamping intervals are located near zero-crossing grid current, as indicated by the red shadows in Fig. 8(a), which is not optimal in terms of switching loss minimization. On the other hand, δ_{a1} and δ_{a2} are allowed to be clamped to zero under the proposed DPWM when the corresponding grid current is near its peak value, as highlighted with blue shadows in Fig. 8(b), which is optimal in terms of switching loss reduction because the leg stops switching when the corresponding current is large. The total clamping time of each leg under both DPWM strategies is 1/3 of the fundamental due to balanced grid conditions. However, their different clamping patterns result in different switching loss, as discussed in the following section.

As it can be observed, under balanced grid conditions, v_Z under both DPWM strategies are mainly triplen harmonics, which do not affect interphase cluster voltage control.

2) Switching Loss: The switching loss reduction effect at rated capacitive and inductive current is presented in Fig. 9. The switching loss of the classic CPWM strategy at each operating point is used as the base value for calculating the percent reduction. As it can be observed, the conventional DPWM provides approximately 15% switching loss reduction for both inductive and capacitive operation, while the proposed DPWM renders 30% reduction. The proposed DPWM was expected to have a lower switching loss profile due to its ability to avoid switching legs with high absolute values of current. Note that the fact of clamping converter voltages to zero during peak grid current not only brings lower switching loss, but can also reduce capacitor

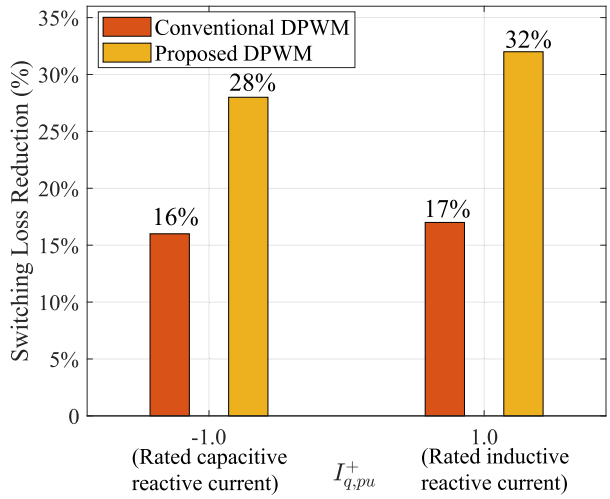

Fig. 9. Switching loss reduction with respect to CPWM under the proposed DPWM and the conventional DPWM.

power loss. This is because the dc-side capacitors are bypassed when the converter voltages are clamped to zero.

B. Unbalanced Grid Conditions

1) Asymmetrical Grid Voltages: Fig. 10 presents the main converter waveforms under the conventional DPWM and the proposed DPWM when the grid voltages $v_{g,a}$ and $v_{g,b}$ drop to zero (grid fault condition). The StatCom is being asked to provide full capacitive current throughout the entire test. As it is shown in Fig. 10(a), the applied ZSV v_Z under the conventional DPWM has a large magnitude during the grid fault because it is used to clamp the converter voltage references close to zero to their respective cluster voltages. The v_Z with large magnitude significantly distorts capacitor voltages, as it is shown in the second subplot of the figure. The bottom subplots depict

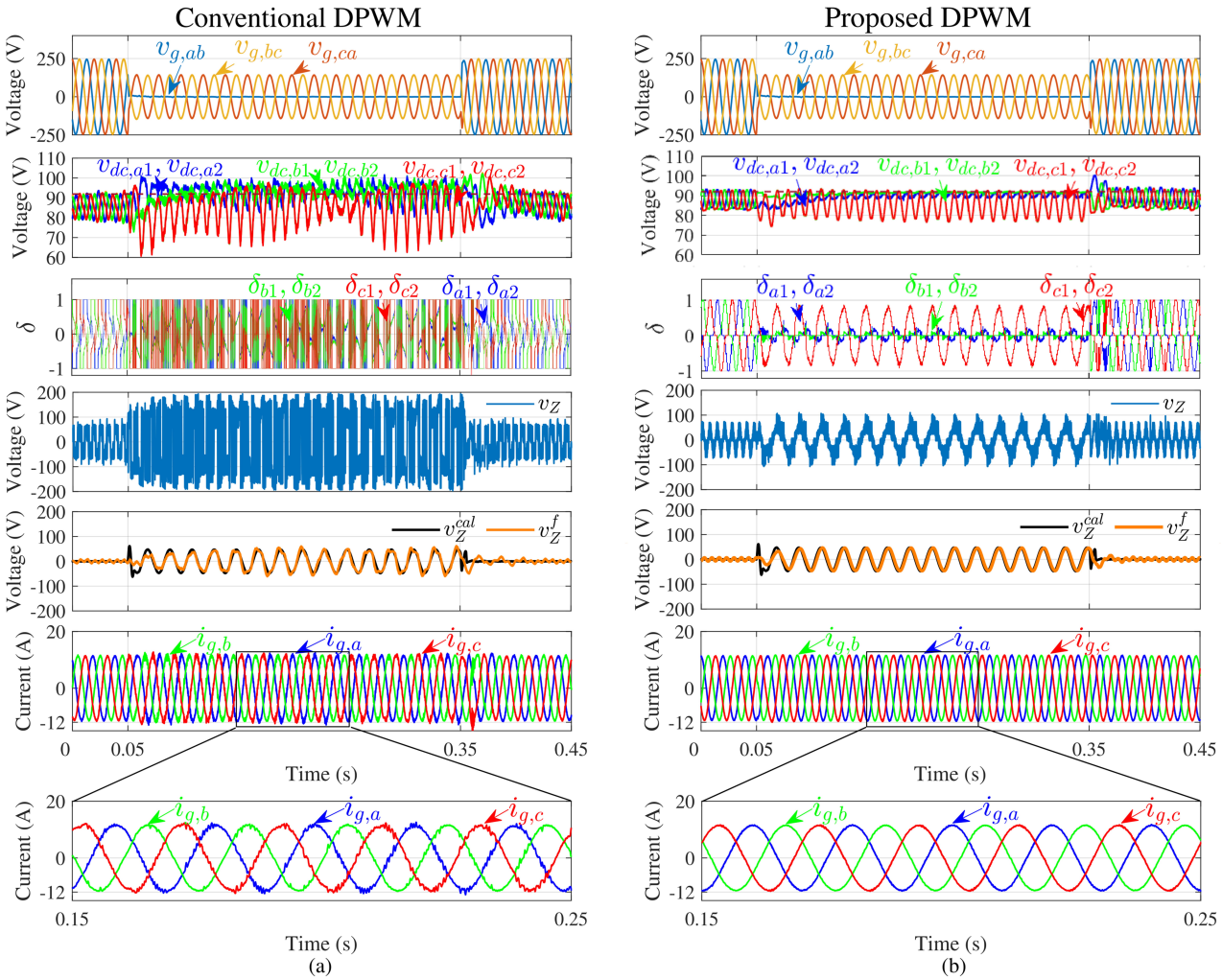

Fig. 10. Grid voltages on phases a and b drop to zero from $t = 0.05$ s to $t = 0.35$ s when the StatCom is providing full capacitive current. (a) Conventional DPWM and (b) proposed DPWM.

the waveforms of the fundamental-frequency component in the ZSV, i.e., v_Z^f, [dynamically calculated via the SOGI filter in (36)], and the analytical FFZSV for interphase cluster voltage control calculated as in [24], and denoted as v_Z^{cal}. Note that v_Z^{cal} is shown only for the sake of illustration and is not used in the proposed controller. As it can be observed, the filtered ZSV v_Z^f does not track accurately the analytical solution v_Z^{cal} due to the coupling between interphase cluster voltage control and DPWM. Consequently, the conventional DPWM yields a disturbed behavior when the grid fault occurs, where the capacitor voltages are not properly controlled and the grid currents become distorted. Differently, as it can be observed from Fig. 10(b), the capacitor voltages under the proposed DPWM are well regulated, and the grid currents are balanced and sinusoidal during the grid fault. As the modulating signals illustrate, legs a and b are being consecutively clamped to the zero during the fault, which requires minimum ZSV, hence not distorting and deviating the capacitor voltages. In addition, v_Z^f tracks v_Z^{cal} with great accuracy, thus validating the effectiveness of the proposed interphase cluster voltage control.

Note that the study in Fig. 10 provides valuable insights to understand the behavior of the StatCom under extreme grid conditions, such as faults, which can be helpful to design appropriate protection schemes and develop control strategies to ensure safe and reliable operation of the system. Moreover, it serves as a benchmark for studying grid voltage sags where the grid voltage drops are in the range $[10\%,\ 90\%]$ according to IEEE standard 1159–2019. In a manner similar to the effectiveness of the proposed DPWM in handling the grid fault, the proposed method is well suited to manage grid voltage swells as well.

2) Asymmetrical Grid Currents: Fig. 11 shows the main CHB StatCom waveforms for the proposed DPWM strategy during a transition from balanced grid currents ($I_{q,pu}^{+} = -1$, $I_{d,pu}^{-} = 0$, $I_{q,pu}^{-} = 0$) to unbalanced grid currents ($I_{q,pu}^{+} = -1$, $I_{d,pu}^{-} = -0.1$, $I_{q,pu}^{-} = 0.1$) at $t = 0.05$ s when the PCC grid voltages are nominal. This corresponds to an imbalance degree of $I^{-}/I^{+} \times 100\% = 14.14\%$, where I^{-} is the amplitude of the negative-sequence current and I^{+} is the amplitude of the positive-sequence current. As it is shown in the bottom plot of Fig. 11, this unbalanced grid condition requires a nonzero FFZSV for interphase cluster voltage control [24], with an amplitude of approximately 15% of the nominal grid voltage. Note that larger I^{-} could cause overmodulation due to the

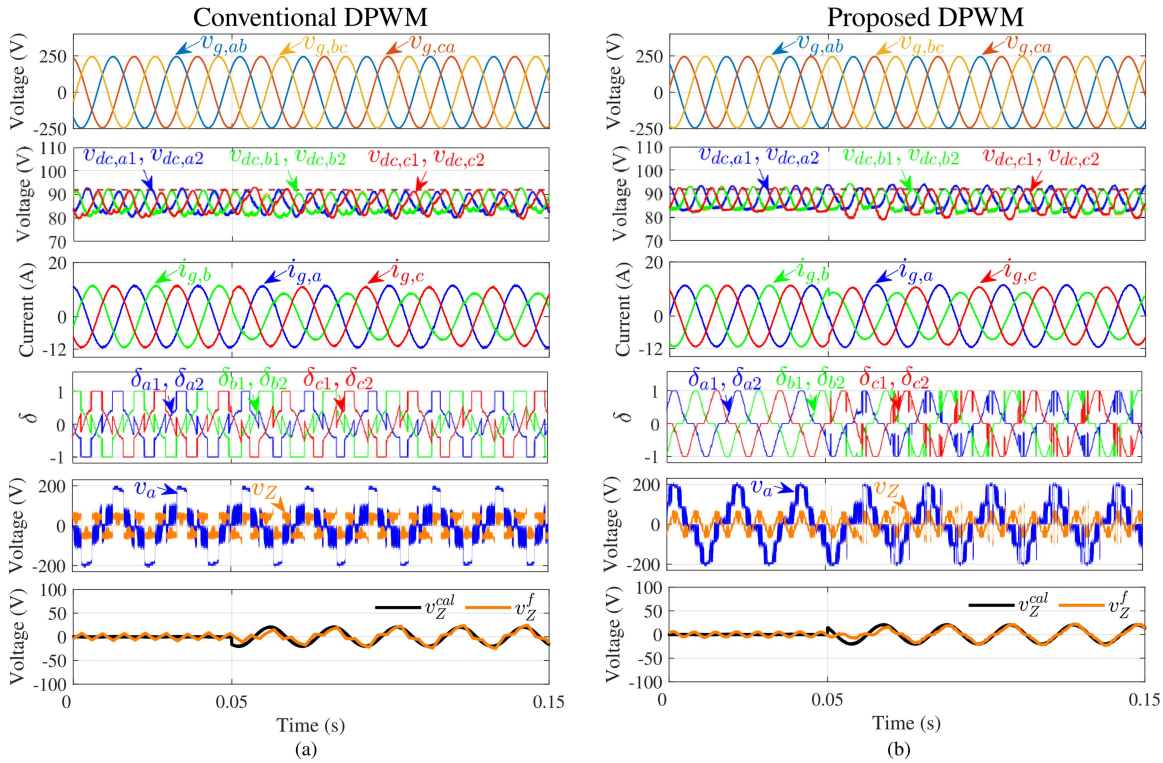

Fig. 11. Transition from balanced grid currents to unbalanced grid currents (with degree of imbalance $I^-/I^+ \times 100\% = 14.14\%$) at $t = 0.05$ s. (a) Conventional DPWM and (b) proposed DPWM.

limited capacity of CHB StatComs in star configuration to deal with unbalanced grid currents [24]. As it can be observed in the second and third row of Fig. 11, capacitor voltage and grid current transients are fast under both DPWM strategies. Moreover, the fourth row in Fig. 11 illustrates the modulating signals during unbalanced grid currents, which are rather similar to the balanced condition. This is because the studied case only adds a 15% FFZSV to the converter voltage references, without a negative-sequence component, such as in Section V-B1, which does not result in a considerable imbalance in the converter voltage references. Consequently, the nonzero active power introduced by the conventional DPWM is easily compensated by the interphase cluster voltage controller.

VI. Conclusion

An FCS-MPC-based DPWM strategy for CHB StatComs has been proposed in this article. The proposed DPWM embeds interphase cluster voltage control, thus it decouples the DPWM implementation and the cluster voltage control. Furthermore, the proposed DPWM control adequately deals with imbalances in the grid. Experimental results validate the ability of the proposed DPWM in handling various grid conditions, including abrupt grid fault. Furthermore, the proposed DPWM strategy reduces switching loss by 30% compared to the classic CPWM, corresponding to a 100% improvement over the conventional DPWM.

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