Effects of Nonlinear Junction Capacitance of Rectifiers on Performance of High Voltage Power Supplies

Sihui Zhou, Qianhong Chen, *Member, IEEE*, Bin Zhang, Jingwen Gao, Chi K. Tse, *Fellow, IEEE*, and Ligang Xu

***Abstract*—Silicon carbide diodes are commonly used in high voltage (HV) power supply rectifiers due to their ability to operate at high frequencies and compact size. This article presents a thorough analysis of how the diode's junction capacitance affects the performance of an HV power supply that includes an *LCL*/P resonant network-based converter and a voltage multiplier. By taking into account the voltage change across the diode due to resonance and voltage buildup, the equivalent junction capacitance of the diode is derived using charge equivalence, which leads to an equivalent circuit of the converter. The analysis shows that the diode's junction capacitance can result in multiple operating points, which can affect the HV power supply's voltage gain and controllability. To ensure a unique operating point and meet design specifications, a parameter design method is proposed. The proposed method is validated through simulation and experimental results from a prototype with a 21–35 V input/3.4–4.4 kV output operating at 450 kHz.**

***Index Terms*—Diode's junction capacitance, high voltage (HV) power supply, multiple operating points, silicon carbide (SiC) diode.**

I. Introduction

HIGH voltage (HV) power supplies can be applied to ionize gases, with applications covering a variety of fields such as electrostatic precipitators [1], plasma generators [2], igniters [3], [4], etc.

Insulation plays a critical role in HV power supplies. Traditionally, two methods have been employed to tackle this issue: introducing an insulating medium [5], [6], [7] or increasing clearance [7]. However, contactless transformers [26] have emerged as a preferred solution due to their significant advantages in isolation and insulation. Besides insulation, achieving HV gain is also crucial for HV power supplies. Typically, transformers with a large turns-ratio are utilized to accomplish this objective. Nevertheless, a large turns-ratio leads to increased parasitic capacitance, winding resistance, and volume. To address these challenges, the combined use of transformers, resonant tanks, and voltage multipliers has become the mainstream design approach for HV power supplies, as given in Table I. HV power supplies require a special feature known as short circuit discharging operation [10], [11], [26]. To limit the energy released during the discharging process, interrupting the converter through a fuzzy logic control scheme [11] and increasing the impedance of the resonant tank through a frequency regulating strategy [26] have been proposed. However, achieving timely sensing and response remains a technical challenge that has yet to be resolved [11], [26]. In contrast, resonant tanks that behave like a current source can offer a compact and reliable solution during the discharging process due to their inherent current limiting capability [12], [13], [14], [15], [16], [17], [18], [19], [20]. Two commonly used circuits for converting a voltage source into a current source are the *LCL* resonant tank [12], [13], [14], [15] and the P resonant tank [17], as shown in Fig. 1.

Low-power HV power supplies require miniaturization, which has led to an increase in their operating frequency to several hundreds of kHz and MHz ranges [21], [22], [23], [24], [25], [26]. Consequently, silicon carbide (SiC) diodes are employed in rectifiers [23], [24], [25], [26]. However, the parasitic capacitance of the SiC diode cannot be ignored under high frequency and HV working conditions. Previous research [23] has

TABLE I
Implementations of a HV Power Supply

Ref.	V_{in} (V)	V_o (kV)	Voltage gain	Turns-ratio	Resonant tank	Voltage multiplier
Thummala et al. [8]	24	2.5	104.17	16:375	\	\
Martin-Ramos et al. [6]	400	150	375	12:1584	LCC	\
Singh et al. [9]	120	2	16.67	1:4	LLC	half-wave CW voltage multiplier
He et al. [22]	160	40	250	10:150	SP	full-wave CW voltage multiplier
Gao et al. [26]	60	3.87	64.5	1:4.38	S/P	half-wave CW voltage multiplier

Manuscript received 24 April 2023; revised 14 June 2023 and 4 August 2023; accepted 25 August 2023. Date of publication 1 September 2023; date of current version 23 October 2023. This work was supported by the National Natural Science Foundation of China under Grant 52277185. Recommended for publication by Associate Editor S. Golestan. *(Corresponding author: Qianhong Chen.)*

Sihui Zhou, Qianhong Chen, Bin Zhang, Jingwen Gao, and Ligang Xu are with the Aero-Power Sci-Tech Center, Nanjing University of Aeronautics and Astronautics, Nanjing 210016, China (e-mail: zsh_2051@nuaa.edu.cn; chenqh@nuaa.edu.cn; 1987bin@nuaa.edu.cn; gjw0315@163.com; xlg324@163.com).

Chi K. Tse is with the Department of Electrical Engineering, City University of Hong Kong Hong Kong, China (e-mail: cktse@ieee.org).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3311191.

Digital Object Identifier 10.1109/TPEL.2023.3311191

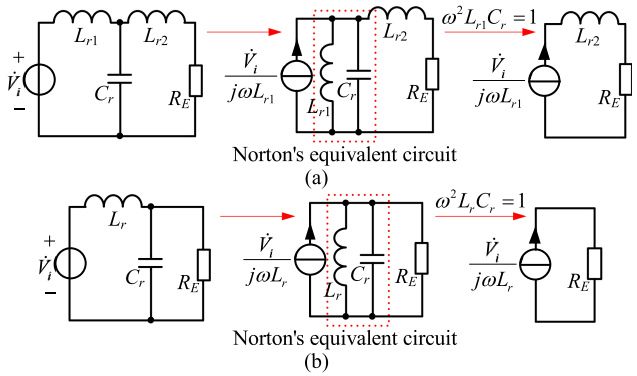

Fig. 1. Resonant tanks as current sources. (a) Norton's equivalent of LCL tank. (b) Norton's equivalent of P tank.

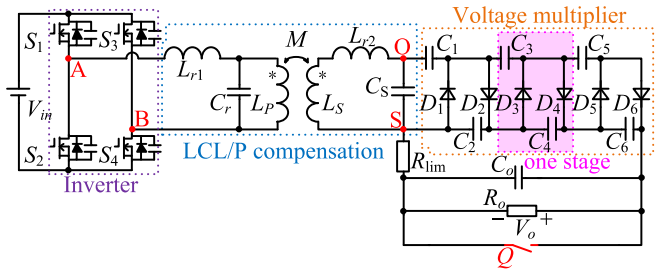

Fig. 2. Proposed topology of HV power supply.

demonstrated that the parasitic junction capacitance between the diode interconnection node and the common line causes voltage imbalance between series SiC diodes. Also, it has been found [25] that the charging and discharging currents of the diode's junction capacitance play a significant role under conditions of high frequency, HV, and low forward current in making the input impedance of the rectifier capacitive. It has been shown [26] that the capacitive input impedance of a voltage multiplier can reduce the voltage gain of an HV power supply, assuming constant junction capacitance. Previous studies [26], [27], [28] have considered the impact of junction capacitance on the voltage gain of an HV power supply, assuming a fixed junction capacitance. However, the junction capacitance changes nonlinearly with voltage variation across the diode due to resonance or voltage buildup. By fitting the *C–V* characteristic curve in the datasheet, a nonlinear model of the junction capacitance can be derived. Accuracy of curve fitting has been verified for both Si diodes [32], [33], [34], [35], [36] and SiC diodes [37], [38]. However, a nonlinear model has only been used to simulate device switching behavior and has not been applied to study its effects on converter performance. Furthermore, the *C–V* characteristics of SiC diodes differ significantly from those of Si diodes. Research has shown [39] that the junction capacitance of SiC diodes is ten times larger than that of Si diodes with the same voltage rating. Therefore, for an HV power supply, the impact of the nonlinear junction capacitance of SiC diodes on voltage gain, operating point, and stability is highly relevant in practice.

Recent research on high-frequency high-voltage power supplies has primarily concentrated on high-power applications ranging from several kilowatts to tens of kilowatts, where the rectifier diode's junction capacitance is assumed to be fixed [28], [29], [30], [31]. While HV products such as Teslaman, Spellman, MORNSUN, and XP Power exist, only MORNSUN and XP Power provide low-power HV power supplies that operate below 100 kHz and use Si diodes. To date, no reports have addressed the challenges posed by the nonlinear junction capacitance of SiC diodes.

The purpose of this article is to analyze the impact of the diode's junction capacitance on the voltage gain, input impedance and the operating point of a HV power supply.

This rest of this article is organized as follows. In Section II, the equivalent junction capacitance of the diode is derived based on charge equivalence, considering the varying voltage across the diode due to resonance and the varying output voltage. The equivalent circuit of the converter is then derived. From the analysis of the input impedance and voltage gain given in Section III, the existence of multiple operating points and its effect on the voltage gain and controllability of a HV power supply are revealed. In Section IV, conditions of the existence of a unique operating point are identified, based on which a parameter design method is derived to ensure a unique operating point that realizes HV gain and soft switching. A 21–35 V input/3.4–4.4 kV output prototype is constructed for experimental verification, as reported in Section V. Finally, Section VI concludes this article.

The major contributions of this article are as follows.

1) An accurate model of the nonlinear junction capacitance based on charge equivalence is proposed, with consideration of the varying voltage across the diode due to resonance and voltage buildup.
2) The nonlinear junction capacitance of the SiC diode has been shown to cause multiple operating points in HV power supplies, which would affect the voltage gain, impedance, and stability of the power supply.
3) A parameter design method is proposed for eliminating multiple operating points in HV power supplies.

II. Equivalent Circuit of HV Power Supply

The equivalent junction capacitance of the diode will be derived in this section, taking into consideration the voltage variation across the diode due to resonance and varying output voltage. Then, the operating modes of the voltage multiplier and the equivalent circuit of the converter will be discussed.

A. Circuit Description

Fig. 2 shows the adopted topology of the HV power supply, which is composed of a full-bridge inverter, an *LCL/P* compensated contactless transformer, and a three-stage half-wave CW voltage multiplier. The contactless transformer has a primary winding inductance L_P, secondary winding inductance L_S, and mutual inductance M. The load consists of a resistance R_o and a capacitance C_o connected in parallel. Resistance R_{lim} limits the current during short-circuit discharging operation. Output

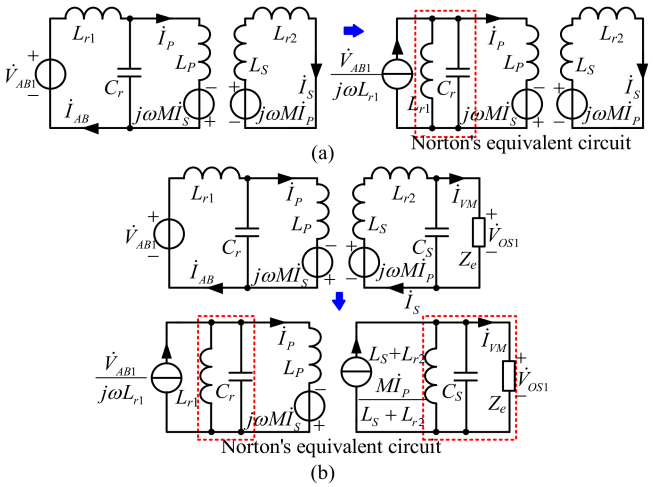

Fig. 3. Equivalent circuits of LCL/P resonant tank in (a) discharging state and (b) charging state.

voltage regulation is achieved by varying the input voltage V_{in} through a non-isolated converter.

Using the fundamental harmonic approximation [16], [17], [18], [19], [20], the equivalent circuits of the *LCL/P* resonant tank in different operating states are shown in Fig. 3, where Z_e represents the equivalent input impedance of the voltage multiplier. To achieve a load-independent current i_P, L_{r1} and C_r are in full resonance, which gives

$$\left|\dot{I}_P\right| = \left|\frac{\dot{V}_{AB1}}{j\omega L_{r1}}\right| = \left|\frac{\frac{2\sqrt{2}}{\pi}V_{\text{in}}}{j\omega L_{r1}}\right|. \tag{1}$$

According to Fig. 3, the voltage gain and impedance characteristics of the *LCL/P* resonant tank in different operating states are derived, as given in Table II. It can be seen from Table II that the magnitudes of Z_{in} and Z_S are bounded in the discharging state. Due to constant i_P, tank currents i_{AB} and i_S are inherently limited, which is desirable for practical applications.

From Table II, the value of Z_e affects the voltage gain and the impedances of the *LCL/P* resonant tank in the charging state. Under high frequency and HV operation, Z_e is capacitive due to the presence of the junction capacitance of the diode in the voltage multiplier. It is necessary to further analyze the impedance characteristics of the voltage multiplier in order to obtain a numerical model of Z_e.

B. Analysis of the Rectifier

Considering the nonlinear junction capacitance of the diode, a three-stage half-wave CW voltage multiplier is illustrated in Fig. 4, where input current i_{VM} is sinusoidal due to resonance, i.e.,

$$i_{VM} = I_m \sin(\omega t). \tag{2}$$

There are four operating modes in a switching cycle. The corresponding equivalent circuits and key waveforms are shown in Fig. 5. The following assumptions are made in our analysis.

TABLE II
CHARACTERISTICS OF *LCL/P* RESONANT TANK

	State	Expression
Voltage gain $G_{vr}=\left\|\frac{\dot{V}_{OS1}}{\dot{V}_{AB1}}\right\|$	Discharging state	0
	Charging state	$\frac{M}{L_{r1}}\left\|\frac{1}{1+j\omega(L_S+L_{r2})(j\omega C_S+\frac{1}{Z_e})}\right\|$
Secondary impedance $Z_S=\frac{j\omega M\dot{I}_P}{\dot{I}_S}$	Discharging state	$j\omega(L_S+L_{r2})$
	Charging state	$j\omega(L_S+L_{r2})+\frac{1}{j\omega C_S+\frac{1}{Z_e}}$
Reflected impedance $Z_f=\frac{-j\omega M\dot{I}_S}{\dot{I}_P}$	Discharging state	$(\omega M)^2/j\omega(L_S+L_{r2})$
	Charging state	$\frac{(\omega M)^2}{j\omega(L_S+L_{r2})+\frac{1}{j\omega C_S+\frac{1}{Z_e}}}$
Input impedance $Z_{in}=\frac{\dot{V}_{AB1}}{\dot{I}_{AB}}$	Discharging state	$j\omega L_{r1}+\frac{1}{j\omega C_r}\|(j\omega L_P+\frac{(\omega M)^2}{j\omega(L_S+L_{r2})})$
	Charging state	$j\omega L_{r1}+\frac{1}{j\omega C_r}\|(j\omega L_P+Z_{f(\text{charging state})})$

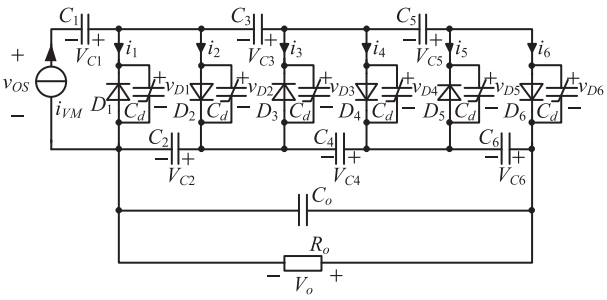

Fig. 4. Three-stage half-wave CW voltage multiplier considering the junction capacitance of the diode.

1) D_1–D_6, C_1–C_6, and C_o are ideal.
2) C_1–C_6 and C_o are large enough to be treated as voltage sources with $V_{C1}=V_o/6$, $V_{C2}=V_{C3}=V_{C4}=V_{C5}=V_{C6}=V_o/3$, and $V_{Co}=V_o$.
3) Junction capacitances of D_1–D_6 are identical and denoted as C_d.

1) Mode 1 [0, t_1] [see Fig. 5(a)]: At $t=0$, D_1–D_6 are OFF, and reverse voltages v_{D1}, v_{D3}, and v_{D5} begin to increase from 0 while $-v_{D2}$, $-v_{D4}$, and $-v_{D6}$ start decreasing. By Kirchhoff's voltage law, v_{D1}–v_{D6} satisfy

$$(-1)^i v_{Di-1}-(-1)^i v_{Di}=V_{Ci}=\frac{V_o}{3}, i=2,3,\ldots,6. \tag{3}$$

If C_d is fixed, the relationship between junction capacitance currents i_1 to i_6 can be easily obtained by taking the derivative of (3) and multiplying both sides by C_d, i.e.,

$$i_1=i_2=i_3=i_4=i_5=i_6=\frac{i_{VM}}{6}=\frac{I_m}{6}\sin(\omega t). \tag{4}$$

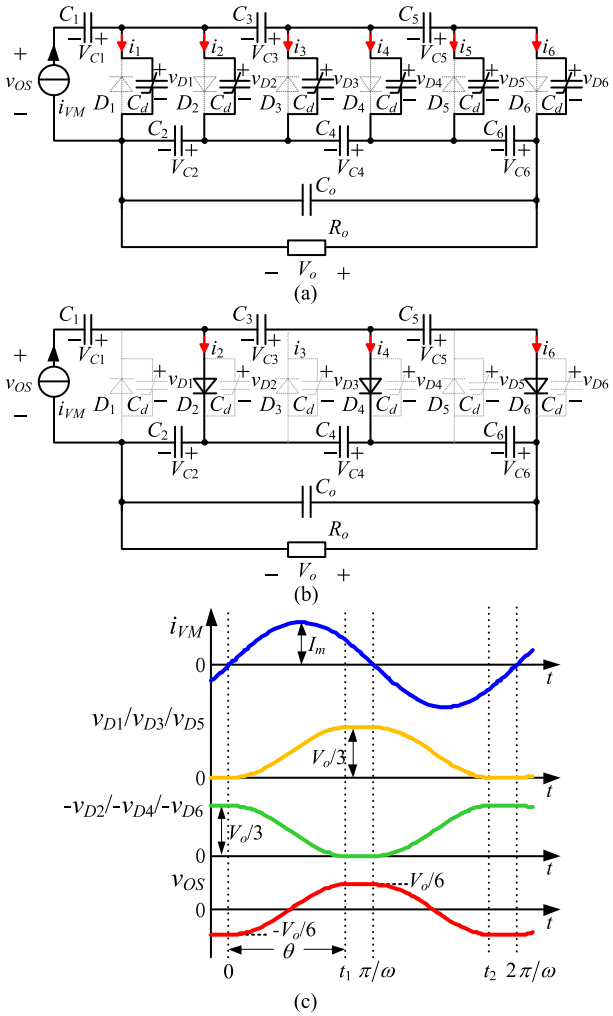

Fig. 5. Equivalent circuits and waveforms of the 3-stage half-wave CW voltage multiplier at different operating modes. (a) Mode 1: $[0, t_1]$. (b) Mode 2: $[t_1, \pi/\omega]$. (c) Key waveforms.

However, C_d varies nonlinearly due to resonance. To obtain the relationship of i_1–i_6, we model C_d as follows.

According to previous results [32], [33], [34], [35], [36], [37], [38], the expression of junction capacitance C_j with reverse voltage v_r across the diode can be written as

$$C_j = \frac{C_{j0}}{(1+\frac{v_r}{V_{bi}})^m} \tag{5}$$

where C_{j0} is the capacitance at $v_r = 0$, V_{bi} is the built-in potential, and m is the grading coefficient and typically ranges from 0 to 1. The accuracy of (5) is validated in Fig. 6, where the C–V characteristics of different diodes have been well fitted over a wide voltage range. Fig. 6 shows that the C_j value of the SiC diode varies from tens of pF to hundreds of pF, which reaches the order of magnitude of the resonant capacitance in high-frequency operation. However, the C_j value of the Si diode ranges from 2 ∼ 3 pF to around 10 pF. In addition, for the SiC diode, the corresponding v_r that C_j changes nonlinearly ranges from 1 V to 1 kV, which is 10 times larger than that of the Si

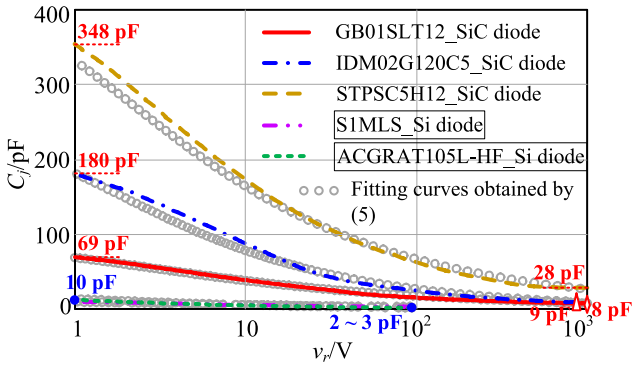

Fig. 6. C_j–v_r curves of several same voltage-rated HV SiC diodes and HV Si diodes.

diode. Therefore, the study of the nonlinear junction capacitance of the SiC diode is necessary for HV power supplies.

To derive the equivalent junction capacitance C_d [40], we introduce the variable charge q of C_j, i.e.,

$$C_d = \frac{q(V_{RE})}{V_{RE}} = \frac{\int_0^{V_{RE}} C_j(v_r)dv_r}{V_{RE}} = \frac{3C_{j0}V_{bi}}{V_o(1-m)}\left[\left(1+\frac{V_o}{3V_{bi}}\right)^{1-m}-1\right] \tag{6}$$

where V_{RE} is the maximum reverse-bias voltage across the diode. Here, $V_{RE} = V_o/3$. When k diodes are connected in series to share V_{RE}, we have

$$C_d = \frac{1}{k}\frac{q(\frac{V_o}{3k})}{\frac{V_o}{3k}} = \frac{3C_{j0}V_{bi}}{V_o(1-m)}\left[\left(1+\frac{V_o}{3kV_{bi}}\right)^{1-m}-1\right]. \tag{7}$$

In a switching period, V_o remains nearly constant. Thus, C_d can be regarded as fixed and (4) is still valid for relating i_1–i_6. Then, v_{D1}–v_{D6} are given by

$$v_{D1} = v_{D3} = v_{D5} = \frac{1}{C_d}\int_0^t \frac{i_{VM}}{6}(\tau)d\tau = \frac{I_m}{6\omega C_d}(1-\cos(\omega t)) \tag{8}$$

$$v_{D2} = v_{D4} = v_{D6} = \frac{I_m}{6\omega C_d}(1-\cos(\omega t)) - \frac{V_o}{3}. \tag{9}$$

From Kirchhoff's voltage law, the input voltage v_{os} of the half-wave CW voltage multiplier is found as

$$v_{OS} = -V_{C1} + v_{D1} = -\frac{V_o}{6} + \frac{I_m}{6\omega C_d}(1-\cos(\omega t)). \tag{10}$$

At t_1, v_{D1}, v_{D3}, and v_{D5} rises to $V_o/3$, and $-v_{D2}$, $-v_{D4}$, and $-v_{D6}$ drops to 0. The electrical angle θ corresponding to the interval of mode 1 is

$$\theta = \omega t_1 = \arccos\left(1-\frac{2\omega C_d V_o}{I_m}\right). \tag{11}$$

2) Mode 2 [t_1, π/ω] [see Fig. 5(b)]: D_2, D_4, and D_6 conduct, and v_{D1}, v_{D3}, and v_{D5} are clamped at $V_o/3$. Thus, v_{OS} is given by

$$v_{OS} = -V_{C1} + V_{C2} = \frac{V_o}{6}. \tag{12}$$

At $t = \pi/\omega$, $-v_{D2}$, $-v_{D4}$ and $-v_{D6}$ start increasing from 0, and v_{D1}, v_{D3} and v_{D5} begins to drop, starting the second half cycle $[\pi/\omega, 2\pi/\omega]$, which is similar to the first half cycle $[0, \pi/\omega]$. According to (10) and (12), v_{OS} in modes 3 and 4 is given by

$$v_{OS} = \frac{V_o}{6} - \frac{I_m}{6\omega C_d}(1+\cos(\omega t)) \quad \left(\frac{\pi}{\omega} \le t \le t_2\right) \tag{13}$$

$$v_{OS} = -\frac{V_o}{6} \quad \left(t_2 \le t \le \frac{2\pi}{\omega}\right) \tag{14}$$

where $t_2 = t_1 + \pi/\omega$.

C. Equivalent Circuit

For small power HV igniters, the load in the charging state is light (usually tens of MΩ), making modes 1 and 3 dominant in a switching cycle. Hence, v_{OS} is mainly determined by (10) and (13), i.e., $v_{OS} \approx v_{OS1} = V_{OS1\_\max}\sin(\omega t+\varphi)$, where v_{OS1} is the fundamental component of v_{OS}, $V_{OS1\_\max}$ represents the amplitude of v_{OS1}, and φ stands for the phase angle of v_{OS1}. Moreover, $V_{OS1\_\max}$ and φ satisfy

$$\begin{cases} V_{OS1\_\max} = \frac{V_o}{f_{vm}(\theta)} = \frac{V_o}{\frac{3\pi(1-\cos\theta)}{\sqrt{\sin^4\theta+(\theta-\frac{1}{2}\sin 2\theta)^2}}} \\ \tan\varphi = \frac{\frac{1}{2}\sin 2\theta - \theta}{\sin^2\theta} \end{cases}. \tag{15}$$

Combining (2) and (15), Z_e can be obtained as

$$Z_e = \frac{\dot{V}_{OS1}}{\dot{I}_{VM}} = \frac{1}{j\omega C_e + \frac{1}{R_e}} \tag{16}$$

where

$$R_e = \frac{V_{OS1\_\max}}{I_m\cos\varphi} = \frac{\sin^4\theta + \left(\frac{1}{2}\sin 2\theta - \theta\right)^2}{6\pi C_d\omega\sin^2\theta} \tag{17}$$

$$C_e = \frac{I_m\sin\varphi}{\omega V_{OS1\_\max}} = \frac{6\pi\left(\theta - \frac{1}{2}\sin 2\theta\right)}{\sin^4\theta + \left(\theta - \frac{1}{2}\sin 2\theta\right)^2}C_d. \tag{18}$$

Ignoring the loss in the half-wave CW voltage multiplier, the input power provided by v_{OS1} and i_{VM} is equal to the output power. Then, I_m and R_e can be expressed as

$$I_m = \frac{V_o^2/R_o}{\frac{1}{2}V_{OS1\_\max}\cos\varphi} = \frac{6\pi}{1+\cos\theta}\frac{V_o}{R_o} \tag{19}$$

$$R_e = \frac{V_{OS1\_\max}^2}{2V_o^2}R_o = \frac{R_o}{2f_{vm}^2(\theta)}. \tag{20}$$

Substituting (19) into (11), θ can be calculated as

$$\theta = \arccos\left(1 - \frac{2\omega C_d}{\omega C_d + \frac{3\pi}{R_o}}\right). \tag{21}$$

From (21), we see that in high-power applications, a heavy load would make θ approach 0. This means that the voltage across the diode follows a square waveform during a switching cycle. Thus, the junction capacitance corresponding to a certain V_o can be regarded as fixed. However, in this article, the proposed high-voltage power supply is designed for low-power ignition. Considering the light load in the charging state and high-frequency operation, θ varies over a small range near π,

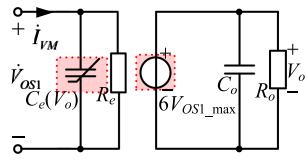

Fig. 7. Equivalent circuit of the 3-stage HWCW voltage multiplier.

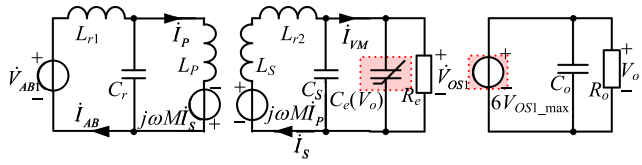

Fig. 8. Equivalent circuit of the proposed HV power supply in charging state.

with voltage across the diode varying in the quasi-resonant mode. Hence, the nonlinear change of the junction capacitance cannot be ignored. Then, (15), (18), and (20) are rewritten as

$$V_{OS1\_\max} \approx V_o/6 \tag{22}$$

$$C_e \approx 6C_d = \frac{18C_{j0}V_{bi}}{V_o(1-m)}\left[\left(1+\frac{V_o}{3kV_{bi}}\right)^{1-m} - 1\right] \tag{23}$$

$$R_e \approx \frac{R_o}{72}. \tag{24}$$

The rating of the diode limits the maximum value of V_o. Hence, C_e is in the range of $[C_{\min}, C_{\max}]$ from (23). Extending to the n-stage half-wave CW voltage multiplier, R_e and C_e are given as follows:

$$\begin{cases} R_e = R_o/8n^2 \\ C_e = 2nC_d = \frac{2n^2C_{j0}V_{bi}}{V_o(1-m)}\left[\left(1+\frac{V_o}{nkV_{bi}}\right)^{1-m} - 1\right] \end{cases}. \tag{25}$$

With the derived C_e and R_e, an equivalent circuit of the three-stage half-wave CW voltage multiplier can be obtained, as shown in Fig. 7. Combining with Fig. 3(b), an equivalent circuit of the proposed converter in charging state can be derived, as shown in Fig. 8.

III. Impact of Junction Capacitances on the Performance of High-Frequency HV Power Supply

From Fig. 8, the change of V_o affects the value of C_e, which further affects the voltage gain and V_o. Thus, a complex coupling relationship between C_e and V_o exists. In this section, we will discuss the impact of the junction capacitance on the performance of the HV power supply, revealing the existence of multiple operating points and its effect on the voltage gain and controllability of the converter.

A. Input Impedance

Substituting (23) and (24) into the expression of Z_{in} of the charging state in Table II, the imaginary part of it is given as

$$\begin{cases} \mathrm{Im}(Z_{in}) = \frac{\omega L_{r1} - \omega L_P - \mathrm{Im}(Z_f(V_o))}{\omega^2 C_r^2 |Z_f(V_o)|^2 + (\omega^2 L_P C_r - 1)^2} \\ \mathrm{Im}(Z_f(V_o)) = \frac{-\omega M^2 Y(V_o)}{\sqrt{X(V_o)^2 + Y(V_o)^2}} \\ X(V_o) = \frac{1}{\omega^2 R_e (C_S + C_e(V_o))^2 + \frac{1}{R_e}} \\ Y(V_o) = \omega(L_S + L_{r2}) - \frac{\omega(C_S + C_e(V_o))}{\omega^2 (C_S + C_e(V_o))^2 + \frac{1}{R_e^2}} \end{cases}. \quad (26)$$

To achieve soft switching of the inverter, Z_{in} is expected to be inductive, i.e.,

$$\omega L_r - \omega L_P - \mathrm{Im}(Z_f(V_o)) > 0. \quad (27)$$

The partial derivative of $\mathrm{Im}(Z_f)$ with respect to V_o is given as

$$\frac{\partial \mathrm{Im}(Z_f)}{\partial V_o} = \frac{1 - 2\omega^2 (L_S + L_{r2})(C_S + C_e)}{\Lambda(C_e)} \cdot \frac{dC_e}{dV_o} \quad (28)$$

where $\Lambda(C_e)$ is given in Appendix A, along with a detailed proof of $\Lambda(C_e) > 0$ and $dC_e/dV_o < 0$. We define $\omega^2(L_S+L_{r2})(C_S+C_e(V_o))$ as $\mathrm{F}(C_e(V_o))$. Combining $dC_e/dV_o < 0$ with (28), we have $\partial \mathrm{Im}(Z_f)/\partial V_o > 0$when $\mathrm{F}(C_e(V_o)) > 0.5$, $\partial \mathrm{Im}(Z_f)/\partial V_o < 0$when $\mathrm{F}(C_e(V_o)) < 0.5$, and $\partial \mathrm{Im}(Z_f)/\partial V_o = 0$ when $\mathrm{F}(C_e(V_o)) = 0.5$. Since $dC_e/dV_o < 0$, $\mathrm{F}(C_e(V_o))$ strictly decreases with V_o. Therefore, $\mathrm{F}(C_e(V_o)) = 0.5$ corresponds to the maximum point for $\mathrm{Im}(Z_f)$, which is the worst case for satisfying (27).

B. Voltage Gain

According to the equivalent circuit shown in the Fig. 8 and G_{vr} of the charging state given in Table II, the voltage gain G_v is given as

$$G_v = \frac{V_o}{V_{\mathrm{in}}} = \frac{V_o}{\left|\dot{V}_{OS1}\right|} \frac{\left|\dot{V}_{OS1}\right|}{\left|\dot{V}_{AB}\right|} \frac{\left|\dot{V}_{AB}\right|}{V_{\mathrm{in}}} = \frac{\frac{24}{\pi} \frac{M}{L_{r1}} R_e}{\left|R_e[1 - \omega^2 (L_S + L_{r2})(C_S + C_e)] + j\omega(L_S + L_{r2})\right|}. \quad (29)$$

As outlined in Section II, the capacitance of C_e approaches the magnitude of C_S during high-frequency operation and displays several times more variation. Equation (29) suggests that even a small shift in C_e from $10C_S$ to C_S can result in a minimum of 400% variation in G_v. Therefore, it is imperative to account for the nonlinear capacitance effect when designing practical circuits. In the next section, we will delve into the influence of nonlinear junction capacitance on voltage gain.

From (29), V_o can be found as

$$V_o = G_v(C_e) V_{\mathrm{in}} = F_1(C_e, V_{\mathrm{in}}). \quad (30)$$

From (23), we get

$$V_o = 3kV_{\mathrm{bi}} \left\{ \left[\frac{(1-m)kC_e}{6C_{j0}} \right]^{\frac{1}{-m}} - 1 \right\} = F_2(C_e). \quad (31)$$

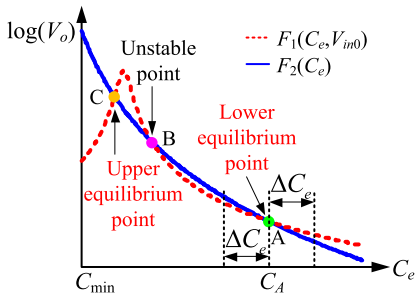

Fig. 9. Multiple operating points caused by diode junction capacitance. V_{in0} = 34 V, M = 15.88 μH, L_S = 246.06 μH, L_{r1} = 20 μH, L_{r2} = 2 mH, C_S = 25 pF, k = 2, n = 3, m = 0.4533, C_{j0} = 84.22 pF, V_{bi} = 0.964 V, and f = 450 kHz.

Combining (29), (30) and (31), the operating point can be found. For analytical simplicity, we adopt a graphic method here. According to (30) and (31), we can plot two curves of $\log(V_o)$ versus C_e, as shown in Fig. 9.

Denoting (30) as $F_1(C_e, V_{\mathrm{in}})$ and (31) as $F_2(C_e)$, we can see that $F_1(C_e, V_{\mathrm{in}})$ is a unimodal function of C_e and $F_2(C_e)$ is a strictly decreasing function of C_e, as shown in Fig. 9. Hence, $F_1(C_e, V_{\mathrm{in}})$ and $F_2(C_e)$ may have multiple intersection points, implying the existence of multiple operating points. However, due to the adoption of Si diode, low output voltage, low operating frequency, and/or high output power, multiple operating points may not be observed.

To analyze the stability of each operating point, small disturbance around the operating point is applied. Taking point A in Fig. 9 as an example, if C_e changes from C_A to $C_A + \Delta C_e$, $F_1(C_e, V_{\mathrm{in0}})$ and $F_2(C_e)$ change to $F_1(C_A + \Delta C_e, V_{\mathrm{in0}})$ and $F_2(C_A + \Delta C_e)$, respectively. If $\Delta C_e > 0$, $F_1(C_A + \Delta C_e, V_{\mathrm{in0}}) > F_2(C_A + \Delta C_e)$, due to $\partial F_1(C_e, V_{\mathrm{in0}})/\partial C_e > dF_2(C_e)/dC_e$ at point A. We know that $F_1(C_e, V_{\mathrm{in}})$ represents the voltage gain and $F_2(C_e)$ describes the relationship between V_o and the physical value of C_e. As seen from Fig. 9, the value of C_e corresponding to the V_o determined by $F_1(C_A + \Delta C_e, V_{\mathrm{in0}})$ is smaller than $C_A + \Delta C_e$. Thus, the operating point returns to point A. Thus, point A is stable. Likewise, we can easily infer that point B is unstable, having $\partial F_1(C_e, V_{\mathrm{in0}})/\partial C_e < dF_2(C_e)/dC_e$, and point C is stable, since $\partial F_1(C_e, V_{\mathrm{in0}})/\partial C_e > dF_2(C_e)/dC_e$. Thus, the criterion for a stable operating point is

$$\left.\frac{\partial F_1(C_e, V_{\mathrm{in}})}{\partial C_e}\right|_{C_e = C_0} > \left.\frac{dF_2(C_e)}{dC_e}\right|_{C_e = C_0} \quad (32)$$

where C_0 denotes the C_e value of the operating point.

The stable operating point is the equilibrium point. As shown in Fig. 9, there are two equilibrium points: points A and C. In the following, we will discuss the impact of multiple equilibrium points.

We start the discussion from the case of voltage buildup. From (23), $C_e = C_{\max}$ when $V_o = 0$ V. Since $F_1(C_{\max}, V_{\mathrm{in}}) > 0$ V and $F_2(C_{\max}) = 0$ V, V_o can be boosted to one of the equilibrium points. According to (23), C_e decreases strictly with V_o. Hence, the lower equilibrium point A will be achieved first, as shown in Fig. 9. Also, V_o will be determined by point A, resulting in the actual V_o being much lower than the desired

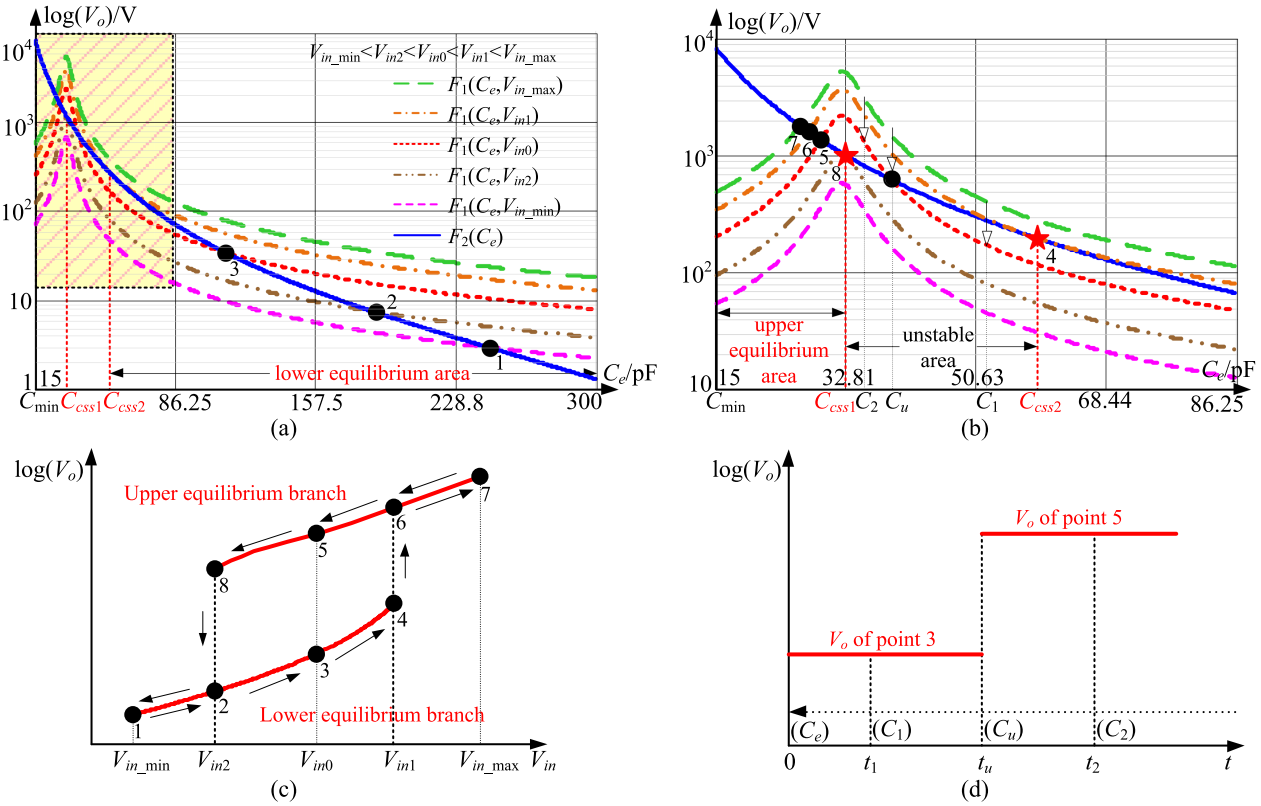

Fig. 10. Operating areas and responses of V_o to $V_{\rm in}$ variation at $M = 15.88$ μH, $L_S = 246.06$ μH, $L_{r1} = 20$ μH, $L_{r2} = 2$ mH, $C_S = 25$ pF, $k = 2$, $n = 3$, $m = 0.4533$, $C_{j0} = 84.22$ pF, $V_{bi} = 0.964$ V, $f = 450$ kHz, $V_{\rm in\_min} = 10$ V, $V_{\rm in2} = 15.5$ V, $V_{\rm in0} = 28$ V, $V_{\rm in1} = 42$ V, and $V_{\rm in\_max} = 55$ V. (a) Operating points under for values of $V_{\rm in}$. (b) enlarged view of the yellow shaded area in (a). (c) Hysteresis response of V_o to $V_{\rm in}$ variation in the steady state. (d) Dynamic response of V_o to different step changes of $V_{\rm in}$ from $V_{\rm in\_max}$ to $V_{\rm in0}$ during voltage buildup.

value. Obviously, the existence of multiple operating points limits the actual voltage gain.

As mentioned in Section II-A, $V_{\rm in}$ usually varies within a certain range $[V_{\rm in\_min}, V_{\rm in\_max}]$ to tightly control V_o. The variation of V_{in} corresponds to a set of curves of $F_1(C_e, V_{\rm in})$, as shown in Fig. 10(a), while $F_2(C_e)$ is fixed. To facilitate illustration, we give a partial enlarged view in Fig. 10(b), where are two special operating points are found, namely, $(C_{css1}, V_{\rm in1})$ and $(C_{css2}, V_{\rm in2})$, which are tangent points of $F_1(C_e, V_{\rm in})$ and $F_2(C_e)$. Here, $(C_{css1}, V_{\rm in1})$ and $(C_{css2}, V_{\rm in2})$ satisfy

$$\begin{cases} F_1(C_e, V_{\rm in}) - F_2(C_e) = 0 \\ \frac{\partial F_1(C_e, V_{\rm in})}{\partial C_e} - \frac{dF_2(C_e)}{dC_e} = 0 \end{cases}. \tag{33}$$

Defining $H(C_e, V_{\rm in}) = F_1(C_e, V_{\rm in}) - F_2(C_e)$ and combining (33) with Fig. 10(a), we can obtain

$$\begin{cases} \frac{\partial H(C_e, V_{\rm in})}{\partial C_e} > 0, \text{when} C_e \in [C_{\min}, C_{css1}] \cup [C_{css2}, C_{\max}] \\ \frac{\partial H(C_e, V_{\rm in})}{\partial C_e} < 0, \text{when} C_{css1} < C_e < C_{css2} \end{cases}. \tag{34}$$

According to above analysis, the operating region can be divided into three areas: upper equilibrium area ($C_{\min} < C_{VM2} < C_{css1}$), lower equilibrium area ($C_{css2} < C_{VM2} < C_{\max}$), and unstable area ($C_{css1} < C_{VM2} < C_{css2}$), as shown in Fig. 10(a) and (b).

In Fig. 10(a) and (b), when $V_{\rm in\_min} < V_{\rm in} < V_{\rm in2}$, there is a lower equilibrium point. When $V_{\rm in2} < V_{\rm in} < V_{\rm in1}$, there are three operating points located in three operating areas. When $V_{\rm in1} < V_{\rm in} < V_{\rm in\_max}$, there is an upper equilibrium point. The existence of multiple operating points within the range of $V_{\rm in}$ variation may cause different responses of V_o to $V_{\rm in}$, which deserves in-depth discussion.

C. Discussion on the Response of V_o to V_{in}

After $V_{\rm in}$ changes, if $H(C_e, V_{\rm in}) = F_1(C_e, V_{\rm in}) - F_2(C_e) > 0$, V_o rises and C_e decreases. Otherwise, V_o decreases and C_e increases. The first equilibrium point in the change direction of C_e determines V_o. As a result, the response of V_o exhibits hysteretic characteristics when V_{in} changes between $V_{\rm in\_min}$ and $V_{\rm in\_max}$.

As seen from Fig. 10(a) and (b), V_o varies along points 1, 2, 3, 4, 6 and 7 when V_{in} increases from $V_{\rm in\_min}$ to $V_{\rm in\_max}$, and jumps from point 4 to point 6, where point 4 is the tangent point $(C_{css2}, V_{\rm in2})$ and is critically stable. Similarly, V_o varies along points 7, 6, 5, 8, 2 and 1 when V_{in} decreases from $V_{\rm in\_max}$ to $V_{\rm in\_min}$, and jumps from point 8 to point 2, where point 8 is the tangent point $(C_{css1}, V_{\rm in1})$ and is critically stable. Thus, a hysteresis characteristic exists in V_{in} and V_o, as illustrated in Fig. 10(c), giving rise to switching of V_o between the upper and lower equilibrium points.

The above discussion shows the response of V_o to V_{in} variation in the steady state. The dynamic response of V_o to a step change of V_{in} during voltage buildup will be quite different. Specifically, V_o starts building up at $t = 0$ when $V_{\text{in}} = V_{\text{in\_max}}$ and $C_e = C_{\max}$. Assuming that V_{in} has a step change from $V_{\text{in\_max}}$ to V_{in0} at $t = t_1$, the corresponding C_e at t_1 is C_1. Since $H(C_1, V_{\text{in0}}) < 0$, as shown in Fig. 10(b), C_e increases and V_o is determined by the first equilibrium point (point 3) along the changing direction of C_e. However, if V_{in} has a step change from $V_{\text{in\_max}}$ to V_{in0} at $t = t_2$ ($t_1 < t_2$), the corresponding C_e at t_2 is C_2. For $H(C_2, V_{\text{in0}}) > 0$ from Fig. 10(b), C_e decreases and the first equilibrium point (point 5) determines V_o. Obviously, the output voltage varies with the step changes, as shown in Fig. 10(d).

D. Conditions for a Unique Operating Point

As discussed above, the existence of multiple operating points affects not only the voltage gain, but also the controllability. It is necessary to analyze the conditions for the existence of a unique operating point.

According to (30), $F_1(C_e, V_{\text{in}})$ is strictly increasing with V_{in}. Since $H(C_e, V_{\text{in}}) = F_1(C_e, V_{\text{in}})$-$F_2(C_e)$, $H(C_e, V_{\text{in}})$ also strictly increases with V_{in}. According to (34), $H(C_e, V_{\text{in}})$ increases strictly within ranges $[C_{\min}, C_{ss1}]$ and $[C_{ss2}, C_{\max}]$ of C_e, and decreases monotonically with the range (C_{ss1}, C_{ss2}) of C_e. Based on Existence Theorem of Zero Points, the converter has a unique operating point when one of the following conditions is satisfied:

$$\begin{cases} H(C_{css1}, V_{\text{in\_max}}) < 0 \\ H(C_{css2}, V_{\text{in\_max}}) < 0 \end{cases} \tag{35}$$

or

$$\begin{cases} H(C_{\min}, V_{\text{in\_max}}) < 0 \\ H(C_{css1}, V_{\text{in\_min}}) > 0 \\ H(C_{css2}, V_{\text{in\_min}}) > 0 \end{cases}. \tag{36}$$

If (35) is met, the unique operating point is the lower equilibrium point; otherwise the unique operating point is the upper equilibrium point. The upper equilibrium point is preferred for its HV gain.

Furthermore, C_{css1} and C_{css2} are two tangent points of $F_1(C_e, V_{\text{in}})$ and $F_2(C_e)$, i.e., extreme points of $H(C_e, V_{\text{in}})$. According to the numerical analysis of the first and second partial derivatives of $H(C_e, V_{\text{in}})$ with respect to C_e, expressions of C_{css1} and C_{css2} are rearranged as

$$C_{css1} \approx C_{peak} = \frac{1}{\omega^2(L_S + L_{r2})} - C_S. \tag{37}$$

$$\begin{cases} C_{css2} = \beta + C_{\text{peak}} \\ \beta^2(\beta + C_{\text{peak}})^{-\frac{1}{m}-1} - \frac{24MV_{in}m\left(\frac{k(1-m)}{2nC_{j0}}\right)^{\frac{1}{m}}}{\pi L_{r1}\omega^2(L_S+L_{r2})nkV_{bi}} = 0 \end{cases} \tag{38}$$

where C_{peak} corresponds to the peak voltage gain. Table III gives validation of the expressions of C_{css1} and C_{css2}.

Substituting $C_{\min}$, C_{css1} and C_{css2} into (36), three constraints on the circuit parameters for achieving a unique operating point can be obtained.

TABLE III
NUMERICAL AND ANALYTICAL SOLUTIONS OF C_{css1} AND C_{CSS_2}

Parameters[1]		Numerical solutions[2]	Analytical solutions[3]
Compensation parameters Input Voltage V_{in}	L_{r1} = 13.28 μH, L_{r2} = 1616 μH, C_S = 22 pF 21 V	C_{css1} = 45.44 pF, C_{css2} = 57.18 pF	C_{css1} = 45.18 pF, C_{css2} = 57.88 pF
Compensation parameters Input Voltage V_{in}	L_{r1} = 9.93 μH, L_{r2} = 1304 μH, C_S = 32.65 pF 21 V	C_{css1} = 48.18 pF, C_{css2} = 73.46 pF	C_{css1} = 48.05 pF, C_{css2} = 74.06 pF
Compensation parameters Input Voltage V_{in}	L_{r1} = 11.27 μH, L_{r2} = 2600 μH, C_S = 0 pF 28 V	C_{css1} = 44.24 pF, C_{css2} = 55.32 pF	C_{css1} = 43.95 pF, C_{css2} = 56.05 pF
Compensation parameters Input Voltage V_{in}	L_{r1} = 18 μH, L_{r2} = 1050 μH, C_S = 54 pF 35 V	C_{css1} = 42.70 pF, C_{css2} = 60.09 pF	C_{css1} = 42.51 pF, C_{css2} = 61.54 pF

[1]Parameters of the contactless transformer are given in Table VI. The operating frequency is set at 450 kHz.
[2]Numerical solutions of C_{css1} and C_{css2} are calculated by Mathcad.
[3]Analytical solutions of C_{css1} and C_{css2} are calculated by (37) and (38).

TABLE IV
DESIGN SPECIFICATIONS

Parameters	Value	Parameters	Value
Input voltage	21~35 V	Output voltage	3.4–4.4 kV
Operating frequency f	450 kHz	Load	R_o = 10 MΩ C_o = 0.52 μF

TABLE V
PARAMETERS OF THE GB01SLT12-214 DIODE

m	V_{bi}	C_{j0}	V_{RRM}
0.346	0.964 V	88.264 pF	1200 V

TABLE VI
PARAMETERS OF THE CONTACTLESS TRANSFORMER

Parameters	Value	Parameters	Value
Self-inductances	L_P = 9.42 μH L_S = 246.06 μH	Parasitic resistances	R_P = 0.327 Ω R_S = 5.05 Ω
Mutual inductance	M = 15.88 μH	Turns-ratio	14:102
Primary Winding	28*AWG 41	Secondary Winding	14*AWG 41

IV. DESIGN EXAMPLE

In this section, a design example is given to illustrate the proposed parameter design method for ensuring a unique operating point, HV gain, and soft switching.

A. Design Specifications

Design specifications are given in Table IV. Since $P_o = {V_o}^2/R_o$, the output power is 1.156 ∼ 1.936 W, as per Table IV. We adopt GeneSiC GB01SLT12-214 diode, whose parameters are given in Table V. To ensure sufficient voltage margin, we use two GB01SLT12-214 diodes in series in the voltage multiplier. Parameters of the contactless transformer are given in Table VI. Detailed design procedure is illustrated in Fig. 11.

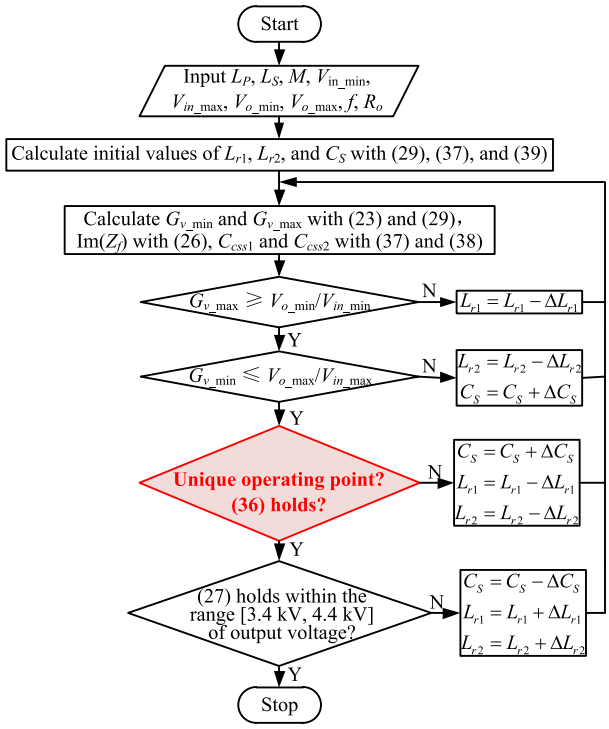

Fig. 11. Parameter design flowchart of the HV power supply with a unique operating point, HV gain, and soft switching.

B. Design Procedure

The values of compensation parameters L_{r1}, $L_{r2,}$ and C_S are designed to achieve HV gain, existence of a unique operating point, and soft switching, simultaneously.

In our design, the range of the voltage gain is determined by the required ignition energy. Our design is used for diesel engine ignition, which needs 3 ~ 5 J ignition energy. The ignition energy is stored on the output capacitor C_o. According to $E = 0.5C_oV_o^2$ and the range of the output voltage given in Table IV, the given C_o is 0.52 μF in order to generate the 3 ~ 5 J ignition energy. Since the voltage range of the front-end converter is from 21 to 35 V, and the output voltage is correspondingly from 3.4 to 4.4 kV, and hence the range of the required voltage gain is 126 to 162.

To achieve a voltage gain ranging from 126 (defined as $G_{v\_\min}$) to 162 (defined as $G_{v\_\max}$), the peak voltage gain G_{v_peak} determined by L_{r1}, $L_{r2,}$ and C_S should be greater than 162. By substituting (24), (37), $f = 450$ kHz, $R_o = 10$ MΩ, and $M = 15.88$ μH into (29), the maximum value of the product of L_{r1} and $(L_S + L_{r2})$ can be calculated as 3.679e^{-8} H^2.

Besides, to achieve an HV gain, C_e corresponding to the required output voltages should be near C_{peak}, where C_{peak} corresponds to the G_{v_peak}. According to (23), values of C_e corresponding to 3.4 kV and 4.4 kV output are 43.94 and 40.28 pF, respectively. Here, C_{peak} is designed to be 1 ~ 1.2 times of C_e corresponding to the required output voltage range, i.e., in the range of 43.94 to 48.34 pF.

According to (22)–(24), we can obtain an expression for the current through the secondary coil of the contactless transformer. As can be seen from (39), the value of C_S will affect $|\dot{I}_S|$. By limiting $|\dot{I}_S|$ to below 0.14 A, thus fitting the output voltage range of 3.4 to 4.4 kV, the maximum value of C_S is 55.17 pF. Combining the range [43.94, 48.34] pF of C_{peak} and the range [0, 55.17] pF of C_S, the design range of L_{r2} is [962.4, 2600] μH

$$\left|\dot{I}_S\right| = \left|[j\omega(C_S + C_e) + \frac{1}{R_e}]\dot{V}_{OS1}\right|$$
$$= \left|\left[j\omega\left(C_S + \frac{18C_{j0}V_{bi}}{V_o(1-m)}\left[\left(1 + \frac{V_o}{3kV_{bi}}\right)^{1-m} - 1\right]\right) + \frac{72}{R_o}\right]\frac{V_o}{6\sqrt{2}}\right|. \quad (39)$$

According to (1), the value of L_{r1} will affect $|\dot{I}_P|$. By limiting the value of $|\dot{I}_P|$ to be less than 2 A, the minimum value of L_{r1} is calculated as 5.57 μH. Combining the maximum value of $L_{r1}(L_S + L_{r2})$ and the minimum value of L_{r2}, the maximum value of L_{r1} is 30.44 μH.

Then, based on the design constraints of a unique operating point (36) and soft switching (27), the values of L_{r1}, $L_{r2,}$ and C_S can be obtained by simulation or numerical methods, such as exhaustive method and genetic algorithm.

Fig. 11 shows an iterative calculation method for L_{r1}, L_{r2} and C_S. First, we set the initial values of L_{r1}, L_{r2} and C_S to be $L_{r1} = 30.44$ μH, $L_{r2} = 2600$ μH and $C_S = 0$ pF, respectively. Using (23) and (29), the maximum and minimum voltage gain $G_{v\_\max}$, $G_{v\_\min}$ can be calculated, where C_e corresponds to $V_{o\_\min} =$ 3.4 kV and $V_{o\_\max} = 4.4$ kV, respectively. Using (26), Im(Z_f) corresponding to different output voltages can be calculated. Using (37) and (38), C_{css1} and C_{css2} can be calculated. Then, by comparing $G_{v\_\min}$ with 126 and $G_{v\_\max}$ with 162, verifying the conditions of unique operating point (36) and soft switching (27), the values of L_{r1}, L_{r2} and C_S can be determined, as shown in Table VII. We use a 22 pF C0G capacitor and a 39 pF C0G capacitor connected in parallel and a 68 pF C0G capacitor in series, to get the calculated value 32.65 pF of C_S.

To facilitate the comparison, we also give the results from conventional parameter design, as given in Table VIII, which only considers HV gain and soft switching. To maximize the voltage gain, the conventional parameter design focuses on

TABLE VII
COMPENSATION PARAMETERS OF THE PROPOSED DESIGN METHOD

Parameters	Calculated	Measured
L_{r1}	9.93 μH	10.70 μH
C_r	11.4 nF	11.4 nF
L_{r2}	1304 μH	1320 μH
C_S	32.65 pF	32.16 pF

TABLE VIII
SPECIFICATIONS AND COMPENSATION PARAMETERS OF CONVENTIONAL DESIGN METHOD

Parameters		Value
Specifications	Input voltage	23 ~ 34 V
	Output voltage	3.4 ~ 4.4 kV
	Operating frequency	450 kHz
	Load	R_o=10 MΩ C_o=0.52 μF
Compensation parameters		L_{r1} = 13.28 μH, C_r = 9.4 nF L_{r2} = 1616 μH, C_S = 22 pF
Transformer parameters		Same as Table VI

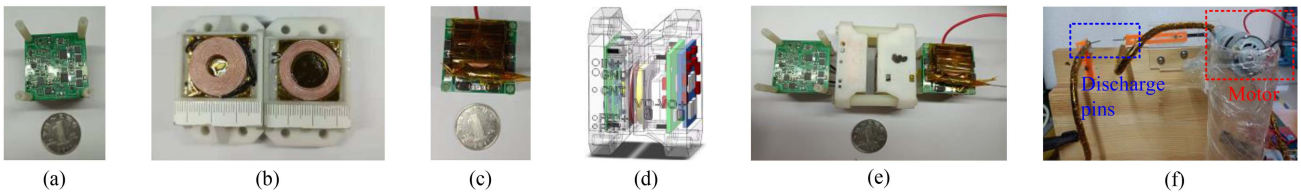

Fig. 12. Photographs of prototype. (a) Primary PCB including the inverter and the primary *LCL* compensation. (b) Contactless transformer. (c) Secondary PCB including the three-stage half-wave CW voltage multiplier and secondary P. (d) Assembly of the prototype. (e) Prototype. (f) Ignition device.

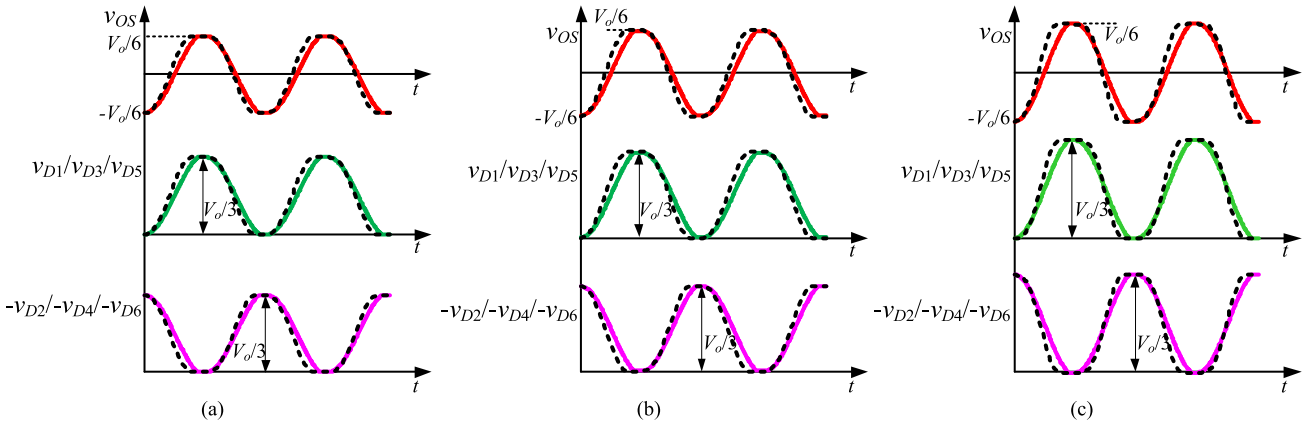

Fig. 13. Key waveforms of the three-stage half-wave CW voltage multiplier obtained by theoretical calculation and LTspice simulation at (a) $V_o = 3.5$ kV (SiC diode GB01SLT12-214), (b) $V_o = 4$ kV (SiC diode GB01SLT12-214), and (c) $V_o = 4.5$ kV (SiC diode IDM02G120C5), where theoretical waveforms are illustrated by solid lines and simulated waveforms are illustrated by dashed lines. Voltage reference directions are shown in Fig. 4.

TABLE IX
PARAMETERS OF THE IDM02G120C5 DIODE

m	V_{bi}	C_{j0}	V_{RRM}
0.478	0.865 V	262.88 pF	1200 V

TABLE X
POWER COMPONENTS IN THE PROTOTYPE CONVERTER

Components	Parts	
MOSFETs S_1 - S_4 in the inverter	Infineon BSZ44010NS3G	
Contactless transformer	Material	DMEGC DMR95
Inductor L_{r1}	Material	DMEGC DMR51
	Winding	15-strands AWG 41
Inductor L_{r2}	Material	DMEGC DMR51
	Winding	10-strands AWG 41
Capacitors C_r, C_S	TDK C0G SMD MLCC series	

setting the operating point as close to the peak voltage gain as possible. This can be easily seen from the value of C_{peak}, where C_{peak} of the conventional parameter deign is 45.18 pF and C_{peak} of the proposed parameter deign is 48.05 pF. We find that parameters designed in this way usually do not guarantee a unique operating point.

V. EXPERIMENTAL RESULTS

To validate the theoretical analysis, two prototypes with compensation parameters given in Tables VII and VIII, respectively, have been built, tested and compared. Two prototypes have different compensation parameters, and are otherwise identical. Fig. 12 shows the photos of the prototype. Details of the power components in two prototypes are listed in Table X.

A. Verification of the Impedance Model

We choose prototype #1 (with compensation parameters given in Table VII) as an example to verify the input impedance model of the half-wave CW voltage multiplier.

First, we validate the proposed junction capacitance model expressed as given in (7). According to (19), substituting parameters of the chosen SiC diode GB01SLT12-214 and IDM02G120C5 given in Tables V and IX into (6) to (10), respectively, the waveforms of v_{D1} to v_{D6} and v_{OS} at different output voltages can be found, as illustrated in Fig. 13 with solid lines. Using parameters given in Tables V and IX to set the junction capacitances of the diodes in Ltspice, the waveforms of v_{D1} to v_{D6} and v_{OS} at different output voltages can be found, as shown by the dashed lines in Fig. 13. It can be seen that the calculated and simulated waveforms are highly consistent, verifying the correctness of the proposed model of the junction capacitance and its effectiveness for representing different diode types. Such consistency can be attributed to the due consideration of the reverse voltage change caused by resonance and voltage buildup in the junction capacitance modeling.

Next, we verify the input impedance model of the half-wave CW voltage multiplier expressed as given in (22) to (24). We measure the input voltage v_{OS} of the half-wave CW voltage multiplier using the SI-9002 differential probe. To reduce the impact of the probe on the input impedance of the half-wave

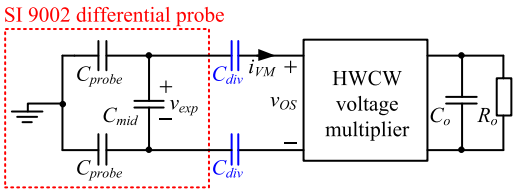

Fig. 14. Test circuit of the input voltage v_{OS} of the CW voltage multiplier.

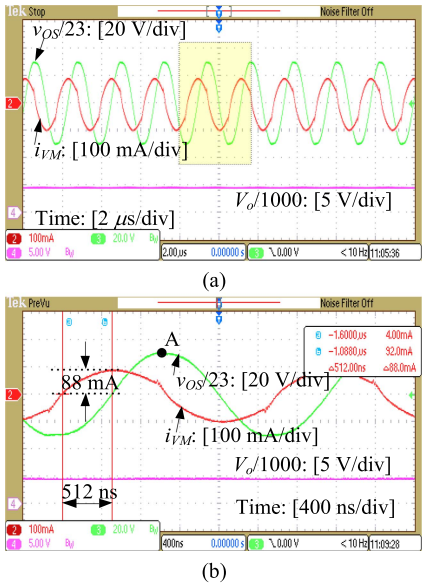

Fig. 15. Waveforms of the half-wave CW voltage multiplier when V_o= 4.45 kV. (a) Input current i_{VM} and input voltage v_{OS}. (b) Enlarged view of the yellow shaded area in (a).

TABLE XI
CALCULATED AND MEASURED VALUES OF THE INPUT VOLTAGE AND INPUT CURRENT OF THE HALF-WAVE CW VOLTAGE MULTIPLIER

	Measured Value[1]	Calculated Value
V_{OS1_max}	699 V	742 V
I_m	88 mA	84 mA
φ	82.9°	86.4°

[1]The measured value of V_{OS1_max} corresponds to 23 times the voltage of point A in Fig. 15(b).

CW voltage multiplier, we connect two 1 pF C0G capacitors (denoted as $C_{\rm div}$) in series at the test nodes, as shown in Fig. 14, where $C_{\rm probe}$ is the capacitance of each probe and is the sum of 5.5 pF from a single probe and 5.5 pF from the probe-to-board adapter, and $C_{\rm mid}$ is a 6 pF capacitor between the two probes of SI-9002. So, the actual v_{OS} is about 23 ((0.5 × 11 + 6)/(0.5 × 1)) times the measured value.

The experimental waveforms of the input voltage v_{OS} and the input current i_{VM} of the half-wave CW voltage multiplier are shown in Fig. 15, where V_o = 4.45 kV. In the figure, v_{OS} lags i_{VM}, implying that the input impedance is capacitive. The calculated values of v_{OS} and i_{VM} from (22)–(24) and the measured values are given in Table XI for comparison. It can be seen that the calculated and measured values are almost identical, which verifies the accuracy of the input impedance model of the half-wave CW voltage multiplier.

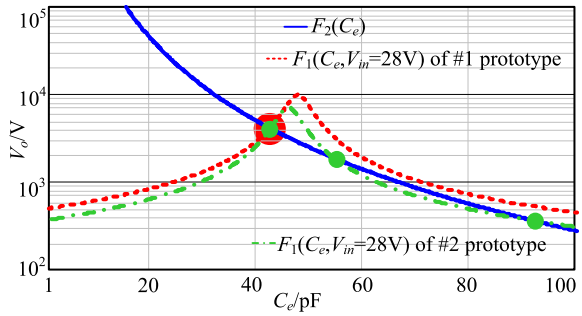

Fig. 16. Operating points of #1 prototype (unique operating point, the red line) and #2 prototype (multiple operating points, the green line) under $V_{\rm in}$ = 28 V.

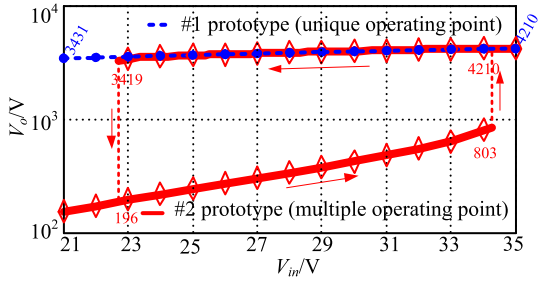

Fig. 17. Curves of V_o versus $V_{\rm in}$ of two prototypes, where the red line and the blue line correspond to #2 prototype (multiple operating points) and #1 prototype (unique operating point), respectively.

B. Verification of Multiple Operating Points

To reveal the existence of multiple operating points and its impact on the voltage gain and controllability of the converter, two prototypes are compared under openloop control.

The operating points of prototypes #1 and #2 for $V_{\rm in}$ = 28 V are shown in Fig. 16. We see that prototype #1 has a unique operating point, and prototype #2 has multiple operating points.

The measured curves of V_o versus $V_{\rm in}$ of the two prototypes are plotted in Fig. 17. Obviously, prototype #2 has multiple operating points, whereas prototype #1 has a unique operating point. As can be seen from Fig. 17, the hysteresis characteristic in V_{in} and V_o for prototype #2 limits the maximum output voltage to 803 V, when its front-end converter is closed-loop regulated in the voltage range of 23 to 34 V. This demonstrates that multiple operating points limit the voltage gain. However, the output voltage of prototype #1 changes from 3.41 to 4.21 kV when V_{in} varies from 21 to 35 V due to the front-end converter.

The experimental waveforms of the dynamic responses of V_o to different step changes of $V_{\rm in}$ during voltage buildup are shown in Figs. 18 and 19. In Fig. 18, different step changes of $V_{\rm in}$ make the output voltage of prototype #2 different: one is 338 V and the other is 3.87 kV. This shows that the existence of multiple operating points will cause severe deviation of the operating point in the occurrence of large disturbance of $V_{\rm in}$ during the voltage buildup. However, regardless of the variation of $V_{\rm in}$, the output voltage of prototype #1 is always 3840 V, as shown in Fig. 19.

Fig. 18. Open-loop dynamic response of V_o to different step change of $V_{\rm in}$ of #2 prototype with compensation parameters in Table VIII. (a) $V_{\rm in}$ is set from 35 V to 28 V when V_o=0.8 kV. (b) $V_{\rm in}$ is set from 35 to 28 V when V_o=2.56 kV.

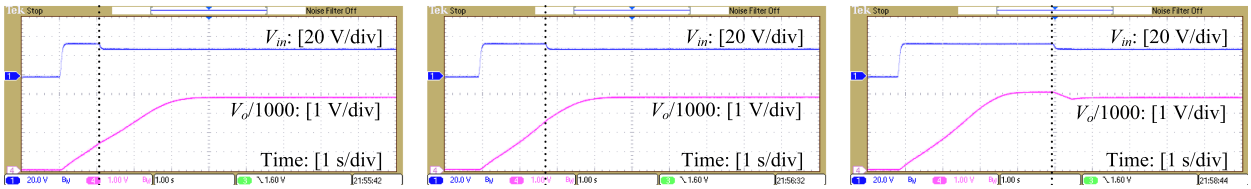

Fig. 19. Open-loop dynamic response of V_o to different step change of $V_{\rm in}$ of #1 prototype with compensation parameters in Table VII. (a) $V_{\rm in}$ is set from 35 V to 28 V when V_o=1.5 kV. (b) $V_{\rm in}$ is set from 35 to 28 V when V_o=2.5 kV. (c) $V_{\rm in}$ is set from 35 V to 28 V when V_o=4.2 kV.

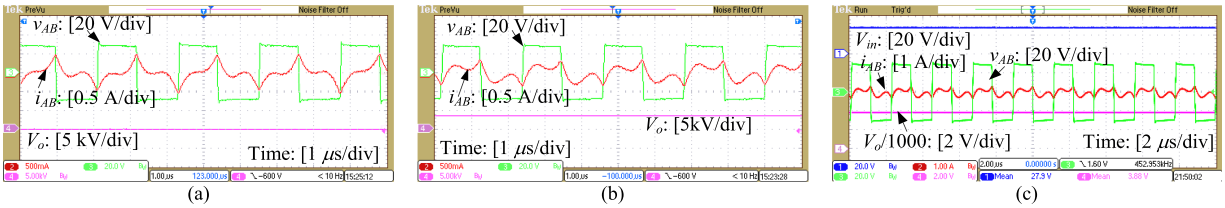

Fig. 20. Waveforms of the output voltage v_{AB} and output current i_{AB} of the inverter at (a) $V_o = 0$ V, (b) $V_o = 3.5$ kV, and (c) $V_o = 3.88$ kV.

C. Experimental Results

The above experiments have demonstrated that prototype #1 has a unique operating point. Next, we focus on the voltage gain and soft switching of prototype #1.

According to Fig. 17, the output voltage of prototype #1 is from 3.43 to 4.21 kV, achieving the desired HV gain. Fig. 20 shows the experimental waveforms of the output current i_{AB} and output voltage v_{AB} of the inverter under different output voltages. As can be seen from Fig. 20, i_{AB} always lags v_{AB}, which realizes soft switching. Moreover, it can be seen from Fig. 20(a) and (b) that the input impedance angle at C_e ($V_o = 0$ V) = 264.79 pF is almost three times that at C_e ($V_o = 3.5$ kV) = 43.52 pF, demonstrating the significant impact of the nonlinear junction capacitance on the impedance.

VI. Conclusion

In this article, a quantitative model of the nonlinear junction capacitance in a high-voltage power supply has been derived and the phenomenon of multiple operating points caused by the presence of the junction capacitance has been analyzed for the first time. By combining an *LCL/P* resonant tank and a half-wave CW voltage multiplier, an input impedance model of the half-wave CW voltage multiplier has been proposed, leading to a simple equivalent circuit for the converter. Characteristics of the converter have been analyzed in detail. Specifically, a hysteresis characteristic of the input and output voltages has been identified. Severe deviation of the operating point caused by multiple operating points, and the conditions for a unique operating point has been studied, clarifying the practical constraints for parameter design. Theoretical and experimental results both demonstrate the accuracy of the proposed input impedance model, the impact of multiple operating points, and the effectiveness of proposed parameter design method for ensuring a unique operating point. The analysis method presented in this article can also be applied to the study of general high-voltage power supplies using resonant tanks and rectifiers.

Appendix A: Input Impedance

The $\Lambda(C_e)$ in (28) is given as follows:

$$\Lambda(C_e) = \frac{\omega^2 M^2 R_e^4}{\left[R_e^2\left(\frac{\alpha\gamma}{R_e} - 1\right)^2 + \alpha^2\right]^{\frac{3}{2}} [\gamma^2 + 1]^{\frac{3}{2}}} \tag{40}$$

where $\alpha = \omega(L_S + L_{r2})$, $\gamma = \omega R_e(C_S + C_e)$. Obviously, $\Lambda(C_e) > 0$. According to (25), dC_e/dV_o can be obtained as

$$\frac{dC_e}{dV_o} = \frac{2nC_{j0}\left\{nkV_{bi}\left[\left(\frac{V_o}{nkV_{bi}}+1\right)^m - 1\right] - mV_o\right\}}{k(1-m)V_o^2\left(\frac{V_o}{nkV_{bi}}+1\right)^m} = \frac{2nC_{j0}f(V_o)}{k(1-m)V_o^2\left(\frac{V_o}{nkV_{bi}}+1\right)^m} \quad (41)$$

where $\frac{df(V_o)}{dV_o} = m(\frac{V_o}{nkV_{bi}}+1)^{m-1} - m$. Due to m < 1, $[1 + V_o/(nkV_{bi})]^{m-1} < 1$, $df(V_o)/dV_o < 0$, $f(V_o) < f(0) = -mV_o < 0$, and then $dC_e/dV_o < 0$.

REFERENCES

[1] S. Fan, Y. Yuan, P. Jia, Z. Chen, and H. Li, "Design and analysis of high voltage power supply for industrial electrostatic precipitators," in *Proc. Int. Power Electron. Conf.*, 2018, pp. 3040–3045.

[2] P. Krupski, H. D. Stryczewska, and G. Komarzyniec, "The push-pull plasma power supply - a combining technique for increased stability," in *Proc. IEEE Pulsed Power Plasma Sci* ., 2019, pp. 1–4.

[3] C. A. Willkens, S. R. Axelson, L. S. Bateman, and D. D. Croucher, "High-voltage miniature igniter development," *IEEE Trans. Ind. Appl.*, vol. 32, no. 5, pp. 1027–1030, Sep./Oct. 1996.

[4] B. Kang and K.-S. Low, "High-voltage pulsed power supply for the igniter circuit of a pulsed plasma thruster," in *Proc. IEEE Int. Conf. Power Electron. Drive Syst* ., 2017, pp. 945–949.

[5] Saijun Mao, Tao Wu, Xi Lu, J. Popovic, and J. A. Ferreira, "High frequency high voltage power conversion with silicon carbide power semiconductor devices," in *Proc. Electron. Syst.-Integr. Technol. Conf.*, 2016, pp. 1–5.

[6] J. A. Martin-Ramos, A. M. Pernia, J. Diaz, F. Nuno, and J. A. Martinez, "Power supply for a high-voltage application," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 16081619, Jul. 2008.

[7] Z. Zheng, L. Bai, T. Jin, G. Li, C. Pei, and Y. Oi, "Study on insulation design of high power high frequency high voltage transformer," in *Proc. IEEE Conf. Energy Internet Energy Syst. Integr.*, 2018, pp. 1–5.

[8] P. Thummala, H. Schneider, Z. Ouyang, Z. Zhang, and M. A. E. Andersen, "Estimation of transformer parameters and loss analysis for high voltage capacitor charging application," in *Proc. IEEE ECCE-Asia*, 2013, pp. 704–710.

[9] A. K. Singh, P. Das, and S. K. Panda, "Analysis and design of SQR-based high-voltage LLC resonant dc-dc converter," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4466–4481, Jun. 2017.

[10] B. S. Nathan and V. Ramanarayanan, "Analysis, simulation and design of series resonant converter for high voltage applications," in *Proc. IEEE Int. Conf. Ind. Technol* ., 2000, pp. 688–693.

[11] N. Grass and T. Fischer, "High voltage power supply and control technologies for electrostatic precipitators in biomass applications," in *Proc. IEEE Ind. Appl. Soc. Annu. Meeting*, 2014, pp. 1–4.

[12] C. Xia, R. Chen, Y. Liu, G. Chen, and X. Wu, "LCL/LCC resonant topology of WPT system for constant current, stable frequency and high-quality power transmission," in *Proc. IEEE PELS Workshop Emerg. Technol., Wireless Power Transfer*, 2016, pp. 110–113.

[13] J. T. Boys and G. A. Covic, "The inductive power transfer story at the University of Auckland," *IEEE Circuits Syst. Mag.*, vol. 15, no. 2, pp. 6–27, Apr.-Jun. 2015.

[14] U. K. Madawala and D. J. Thrimawithana, "Current sourced bi-directional inductive power transfer system," *IET Power Electron.*, vol. 4, no. 4, pp. 471–480, Apr. 2011.

[15] M. L. G. Kissin, C. Huang, G. A. Covic, and J. T. Boys, "Detection of the tuned point of a fixed-frequency LCL resonant power supply," *IEEE Trans. Power Electron.*, vol. 24, no. 4, pp. 1140–1143, Apr. 2009.

[16] W. Zhang and C. C. Mi, "Compensation topologies of high-power wireless power transfer systems," *IEEE Trans. Veh. Technol.*, vol. 65, no. 6, pp. 4768–4778, Jun. 2016.

[17] X. Qu, H. Han, S. Wong, C. K. Tse, and W. Chen, "Hybrid IPT topologies with constant current or constant voltage output for battery charging applications," *IEEE Trans. Power Electron.*, vol. 30, no. 11, pp. 6329–6337, Nov. 2015.

[18] J. Hou, Q. Chen, S. -C. Wong, X. Ren, and X. Ruan, "Output current characterization of parallel-series/series compensated resonant converter for contactless power transfer," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2015, pp. 1625–1629.

[19] X. Qu, W. Zhang, S. Wong, and C. K. Tse, "Design of a current-source-output inductive power transfer led lighting system," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 3, no. 1, pp. 306–314, Mar. 2015.

[20] W. Zhang, S. -C. Wong, C. K. Tse, and Q. Chen, "Load-independent duality of current and voltage outputs of a series- or parallel-compensated inductive power transfer converter with optimized efficiency," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 3, no. 1, pp. 137–146, Mar. 2015.

[21] S. Park, L. Gu, and J. Rivas-Davila, "60 V-to-35 kV input-parallel output-series dc-dc converter using multi-level class-DE rectifiers," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2018, pp. 2235–2241.

[22] Y. He, M. Woolston, and D. Perreault, "Design and implementation of a lightweight high-voltage power converter for electro-aerodynamic propulsion," in *Proc. IEEE 18th Workshop Control Model. Power Electron.*, 2017, pp. 1–9.

[23] Y. He and D. J. Perreault, "Diode evaluation and series diode balancing for high-voltage high-frequency power converters," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 6301–6314, Jun. 2020.

[24] S. Mao, J. Popović, and J. A. Ferreira, "Diode reverse recovery process and reduction of a half-wave series Cockcroft-Walton voltage multiplier for high-frequency high-voltage generator applications," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1492–1499, Feb. 2019.

[25] T. Funaki, T. Kimoto, and T. Hikihara, "Evaluation of high frequency switching capability of SiC Schottky barrier diode, based on junction capacitance model," *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2602–2611, Sep. 2008.

[26] J. Gao, Q. Chen, X. Ren, Z. Zhang, H. Shi, and H. Ran, "Design and analysis of the S/P compensated contactless converter for high voltage ignition," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2018, pp. 1080–1085.

[27] S. Mao, C. Li, W. Li, J. Popović, S. Schröder, and J. A. Ferreira, "Unified equivalent steady-state circuit model and comprehensive design of the LCC resonant converter for HV generation architectures," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7531–7544, Sep. 2018.

[28] S. Mao, P. Jelena, and J. A. Ferreira, "Analysis of the transformer modularization for high frequency isolated high voltage generator with the silicon carbide devices," in *Proc. 22nd Eur. Conf. Power Electron. Appl.*, 2020, pp. 1–8.

[29] S. Mao, Z. Yao, D. Zhu, J. Popovic, and J. A. Ferreira, "A high frequency 110kV output-voltage, 8kW output-power high voltage generator with silicon carbide power semiconductor devices," in *Proc. 21st Eur. Conf. Power Electron. Appl.*, 2019, pp. 1–5.

[30] S. Mao, Z. Yao, D. Zhu, J. Popovic, and J. A. Ferreira, "A 300kHz 4kW 140kVDC output voltage power supply with modular high voltage generation architecture and planar transformer," in *Proc. 21st Eur. Conf. Power Electron. Appl.*, 2019, pp. 1–5.

[31] Y. He and D. J. Perreault, "Lightweight high-voltage power converters for electroaerodynamic propulsion," *IEEE J. Emerg. Sel. Topics Ind. Electron.*, vol. 2, no. 4, pp. 453–463, Oct. 2021.

[32] H. Sekiya, T. Watanabe, T. Suetsugu, and M. K. Kazimierczuk, "Analysis and design of class DE amplifier with nonlinear shunt capacitances," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 10, pp. 2362–2371, Oct. 2009.

[33] H. Sekiya, N. Sagawa, and M. K. Kazimierczuk, "Analysis of class DE amplifier with nonlinear shunt capacitances at any grading coefficient for high Q and 25% duty ratio," *IEEE Trans. Power Electron.*, vol. 25, no. 4, pp. 924–932, Apr. 2010.

[34] F. Zhao et al., "A nonlinear rectifying diode model for low and high power levels in microwave regime," *IEEE Microw. Wireless Compon. Lett.*, vol. 32, no. 5, pp. 456–459, May 2022.

[35] R. Trevisoli, H. P. d. Paz, V. S. d. Silva, R. T. Doria, I. R. S. Casella, and C. E. Capovilla, "Modeling Schottky diode rectifiers considering the reverse conduction for RF wireless power transfer," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 69, no. 3, pp. 1732–1736, Mar. 2022.

[36] S.-P. Gao, W. Hu, H. Zhang, and Y. Guo, "Millimeter-wave rectifiers using proprietary Schottky diodes: Diode modeling and rectifier analysis," in *Proc. Wireless Power Week*, 2022, pp. 180–184.

[37] S. Ahmed, H. A. Mantooth, R. Singh, and M. Mudholkar, "Characterization and modeling of SiC junction barrier Schottky diode for circuit simulation," in *Proc. IEEE 14th Workshop Control Model. Power Electron.*, 2013, pp. 1–5.

[38] Y. Xia and X. Tao, "A precise model of power SiC schottky barrier diodes for circuit simulation," in *Proc. IEEE 4th Int. Elect. Energy Conf.*, 2021, pp. 1–6.
[39] T. Duong et al., "Comparison of 4.5 kV SiC JBS and Si PiN diodes for 4.5 kV Si IGBT anti-parallel diode applications," in *Proc. 26th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2011, pp. 1057–1063.
[40] C. Marxgut, F. Krismer, D. Bortis, and J. W. Kolar, "Ultraflat interleaved triangular current mode (TCM) single-phase PFC rectifier," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 873–882, Feb. 2014.

Sihui Zhou received the B.S. degree in electrical engineering in 2020 from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, where she is currently working toward the Ph.D. degree in electrical engineering with the Nanjing University of Aeronautics and Astronautics.

Her research interests include integrated-magnetics, contactless resonant converters, and wireless charging system.

Qianhong Chen (Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 1995, 1998, and 2001, respectively.

She is currently a Professor with the Department of Electrical Engineering, NUAA. She has authored or coauthored more than 70 papers in international journals and conferences. Her research interests include application of integrated-magnetics, wireless power transfer, high power density power converters.

Bin Zhang received the B.S. degree in electrical engineering from Hebei University of Engineering, Handan, China, in 2010, the M.S. degree in electrical engineering from Lanzhou University of Technology, Lanzhou, China, in 2014, and the Ph.D. degree in electrical engineering from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2022.

His research interests include contactless resonant converters and wireless charging system.

Jingwen Gao received the B.S. and M.S. degrees in electrical engineering from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2017 and 2020, respectively.

Her research interests include contactless resonant converters and wireless charging system.

Chi K. Tse (Fellow, IEEE) received the B.Eng. (Hons.) and Ph.D. degrees in electrical engineering from the University of Melbourne, Melbourne, VIC, Australia, in 1987 and 1991, respectively.

He is currently an Associate Vice-President (Innovation) and a Chair Professor of Electrical Engineering with the City University of Hong Kong, Hong Kong. His research interests include power electronics, nonlinear systems, and complex network applications.

Dr. Tse was the recipient of a number of research and invention prizes including the IEEE CASS Charles A. Desoer Technical Achievement Award in 2022 and a few Best Paper Prizes from IEEE and other journals, as well as a Grand Prize and Gold Medal in Silicon Valley International Invention Festival 2019. He has been appointed to honorary professorship and distinguished fellowship by a few Australian, Canadian, and Chinese universities, including the Chang Jiang Scholar Chair Professor with the Huazhong University of Science and Technology, Wuhan, China, the Honorary Professor of the University of Melbourne, and the Distinguished Professor-at-Large with the University of Western Australia, Perth, WA, Australia. He also served as a Panel Member of the Hong Kong Research Grants Council, and a Member of several professional and government committees. In 2005, 2010, and 2018, he was selected as an IEEE Distinguished Lecturer. In 2006, he chaired the Technical Committee on Nonlinear Circuits and Systems of the IEEE Circuits and Systems Society. He was an Editor-in-Chief for IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: EXPRESS BRIEFS, from 2016 to 2019 and IEEE CIRCUITS AND SYSTEMS MAGAZINE, from 2013 to 2016. He was an Associate Editor for a few other IEEE journals. He was on the Editorial Board of IEEE Proceedings from 2021 to 2022. He has been an Editor-in-Chief for IEICE Nonlinear Theory and Applications since 2013. He has served on a number of IEEE committees including the IEEE Fellow Committee and the IEEE Awards Committee and chaired the Steering Committee for IEEE Transactions on Network Science and Engineering.

Ligang Xu received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2003, 2009, and 2022, respectively.

His current research interests include contactless resonant converters and wireless power transfer system.