Direct Duty Cycle Control-Based Power Allocation Strategy for Single-Stage Multiport Inverter in Islanded Microgrid

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***Abstract*—Single-stage multiport inverter offers direct power flow from the dc side to the ac side and has the advantages of compact size and low costs. However, due to its unbalanced dc-link voltages and coupled power features, it is challenging to realize desirable output current and flexible dc-port power allocation simultaneously. To address the above issues, this article proposes a direct duty cycle control-based power allocation strategy. The duty cycles can be solved based on the mathematical models of the single-stage multiport inverter via two stages. In the first stage, three duty cycles can be obtained by small hexagon selection according to the location of the reference voltage vector. In the second stage, the rest duty cycles are determined by solving the reference voltage vector synthesis and dc-port power tracking equations. Not only the output voltage/current quality is guaranteed, but also flexible dc-side power allocation can be realized under the unbalanced dc-link voltages. In addition, the proposed power allocation strategy has the advantages of simple concepts and fast dynamic response due to duty cycles being directly generated. Finally, the effectiveness of the proposed power allocation strategy is verified by islanded microgrid experimental tests.**

***Index Terms*—Duty cycle control, islanded microgrid, power allocation, single-stage multiport inverter.**

I. Introduction

MICROGRID plays an important role in realizing high penetration of distributed generations, which can operate in grid-connected mode to exchange power with the utility grid, or in islanded mode to support local loads [1], [2]. Microgrid integrated with renewable energy sources (RESs) and energy storage sources (ESSs) is becoming more and more common in the distributed power system paradigm [3]. For instance, the photovoltaic (PV)–ESS hybrid system-based microgrid has achieved vigorous development in recent decades [4], [5]. In the microgrid, the power electronic converter is the key device interfacing RESs and ESSs, which performs power conversions required for the interconnections. Numerous power electronic converter topologies have been studied for the microgrid with hybrid energy systems [6].

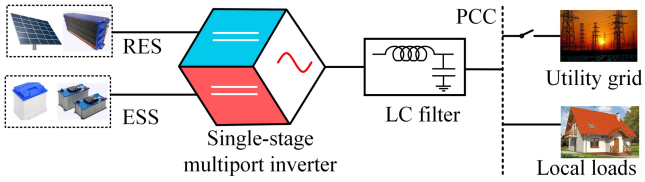

Fig. 1. Configurations of the single-stage multiport inverter-based microgrid applications.

With the fast development of power electronic converter topologies, the single-stage multiport inverter has drawn attention as it can reduce installation costs and power losses [7], [8]. This inverter offers multiple dc ports that can interlink various RESs and ESSs to the ac grid. The single-stage multiport inverter indicates the power electronic converter that provides direct power flow from the dc side to the ac side, i.e., one-stage power flow. Compared with the conventional two-stage configurations, the front-end dc/dc converters are removed in the single-stage configuration [9], [10]. Fig. 1 shows configurations of the single-stage multiport inverter-based microgrid applications. The RES and ESS directly connect to the ac microgrid via the single-stage multiport inverter.

Single-stage multiport inverters can be classified into neutral-point-clamped (NPC) form, modular multilevel form, cascaded-H-bridge form, and switched-capacitor form [11]. It has been clarified that NPC form inverter has the advantages of low cost, small power loss, and low component stress compared with others [11]. Moreover, the NPC form single-stage multiport inverter can be easily realized by connecting the dc source to the midpoint [12], [13]. As a result, the NPC form single-stage multiport inverter has been widely used. Fig. 2 shows the NPC form single-stage multiport inverter: (a) NPC form, (b) T-type

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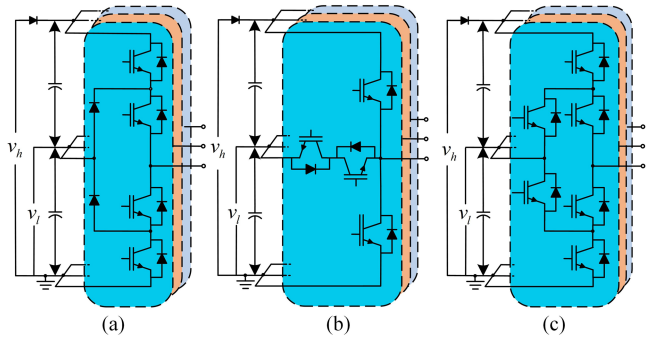

Fig. 2. NPC form single-stage multiport inverter. (a) NPC form. (b) T-NPC form. (c) ANPC form.

neutral-point-clamped (T-NPC) form, and (c) active neutral-point-clamped (ANPC) form. Two independent dc sources were directly connected to the ac side by the NPC form single-stage multiport inverter in [14] and [15]. The T-NPC form single-stage multiport inverter was adopted in [16] and [17], and the ANPC form single-stage multiport inverter has been proposed to connect two different level dc voltages in [18]. The NPC form single-stage multiport inverter can be realized by modifying the conventional three-level NPC inverter. The inherent difference is that the single-stage multiport inverter integrates two different dc sources. In general, the dc port voltages are unbalanced due to the intermittent RES and variable ESS. The control target of the single-stage multiport inverter is not to balance the neutral point voltage but to realize desirable power allocation between RES and ESS. However, the inherent nonlinearities of the single-stage multiport inverter, i.e., unbalanced dc-link voltages and coupled power paths, make it challenging to achieve desirable output voltage/current and flexible power allocation simultaneously.

To address the challenges in the single-stage multiport inverter, some modified modulation strategies have been studied. The modulation strategies for the single-stage multiport inverter can be classified into carrier-based (CB) pulsewidth modulation (PWM) [19], [20] and space-vector (SV) PWM [21], [22], [23], [24], [25]. The CBPWM strategies regulate the dc-side power and synthesize reference voltage vectors by injecting a proper zero-sequence component into the modulation signals [19], [20]. However, modifying the carrier waves under the asymmetrical dc-link voltages is a time-consuming work. The SVPWM strategies distribute the dc-side power in the reference voltage vector synthesis process via regulating the redundant voltage vectors, i.e., small vectors in [21], [22], [23], and [24] and zero vectors in [25]. However, the implementation processes of the SVPWM strategies are complicated due to the inevitable steps: the selection of the three nearest vectors, the calculation of vector dwell time, and the duty cycle calculation for switches. In the case of the asymmetrical dc-link voltages, the amount of SVPWM computation increases tremendously.

As for the control strategies for the single-stage multiport inverter, some previous studies provide effective solutions for desired dc-port power allocation. The space vector modulation (SVM)-based control strategies have been widely used [22], [23], [24], [25], [26]. The PI controller is used to generate the adjustable parameter of redundant vectors [22], [23], [24], [25]. To realize precise power tracking and improve dynamic response, the SVM-based deadbeat control has been proposed in [26]. However, the implementation of the SVM-based strategies is complicated due to the inevitable modulation process. With a general control scheme, dc-port power can be controlled independently with good quality grid current [27]. However, the dynamic model and control system diagrams are complex. Flexible dc-port power allocation and desirable current performance are obtained by the model predictive control in [28]. However, the weighting factor design in the multivariable-based cost function is complicated. The comparison of the power allocation strategies for the single-stage multiport inverter is given in Table I. In summary, the existing control strategies for single-stage multiport inverters show high design complexity. This calls for a simplified power allocation strategy for the single-stage multiport inverter.

To solve the aforementioned problems in the modulation and control strategies, this article proposes a direct duty cycle control-based power allocation strategy for the single-stage multiport inverter. The output voltage vector and dc-side power models about duty cycles are established first. Then, the duty cycles for the single-stage multiport inverter are solved via two stages. According to the location of the reference voltage vector, three duty cycles are determined by the small hexagon selection in the first stage. By solving the reference voltage vector synthesis and dc-port power tracking equations, the rest duty cycles are obtained in the second stage. As a result, beneficial output voltage/current on the ac side and flexible power allocation on the dc side can be realized simultaneously, even in the case of unbalanced dc-link voltages. Complex processes in modulation and control strategies can be avoided due to duty cycles being directly generated. The effectiveness of the proposed strategy is verified by the islanded microgrid experimental tests.

The rest of this article is organized as follows. The topology and mathematical models of the single-stage multiport inverter are illustrated in Section II. Section III provides the proposed direct duty cycle control-based power allocation strategy. The experimental tests are conducted in Section IV. Finally, Section V concludes this article.

II. Topology and Mathematical Models of Single-Stage Multiport Inverter

This section first introduces the topology of a single-stage multiport inverter. Then, the mathematical models for the single-stage multiport inverter are presented.

A. Topology of the Single-Stage Multiport Inverter

The circuit of the NPC form single-stage multiport inverter is depicted in Fig. 3, where v_h and v_l are the dc-side input voltages. The dc source connected to the high-voltage port is considered unidirectional, for instance, the PV unit. The dc source connected to the low-voltage port is considered bidirectional, for instance, battery ESS. i_h and i_l represent the high-voltage port input current and low-voltage port input current, respectively.

TABLE I
COMPARISON OF THE POWER ALLOCATION STRATEGIES FOR SINGLE-STAGE MULTIPORT INVERTER

REF	Method	Multi-objective control	Complexity	Dynamic response
[22]–[25]	SVM-based PI control	NO	Middle	Slow
[26]	SVM-based deadbeat control	NO	Middle	Fast
[27]	General control	YES	High	Slow
[28]	FCS-MPC	YES	High	Middle
-	Proposed	YES	Low	Fast

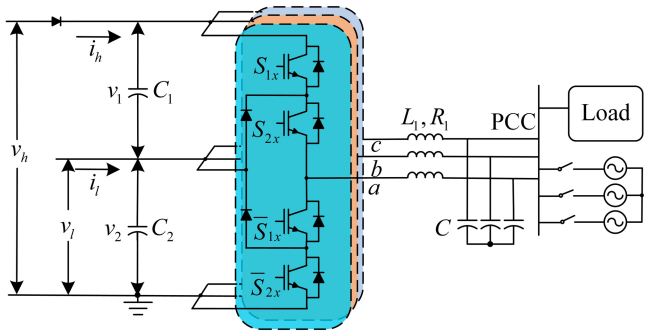

Fig. 3. Circuit structure of the NPC form single-stage multiport inverter.

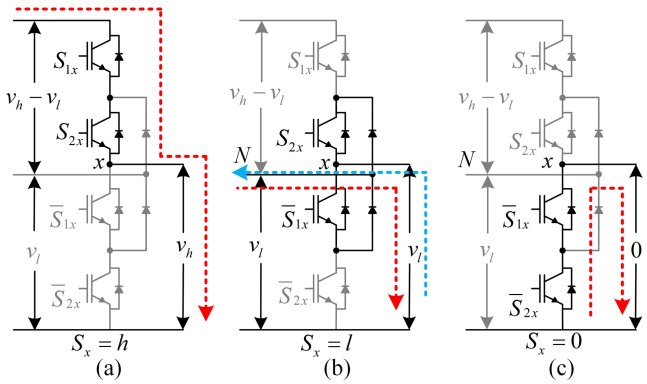

Fig. 4. Switching states and current paths in phase x. (a) $S_x = h$, the high-voltage port supports the ac side. (b) $S_x = l$, the low-voltage port releases/absorbs power to/from the ac side. (c) $S_x = 0$, fly-wheel mode.

The dc-link upper capacitor C_1 and lower capacitor C_2 are assumed to be equal, i.e., $C_1 = C_2$. Then, the dc-link top capacitor voltage can be represented as $v_1 = v_h - v_l$, and the dc-link bottom capacitor voltage can be represented as $v_2 = v_l$. The single-stage multiport inverter connects to a point of common coupling via an *LC* filter.

In this study, the NPC inverter topology is adopted. Each leg of the inverter has four active switches, i.e., S_{1x}, S_{2x}, $\bar{S}_{1x}$, and $\bar{S}_{2x} (x = a, b, c)$. Three different switching states S_x can be obtained as follows:

$$\begin{cases} S_x = h & S_{1x} = 1, S_{2x} = 1 \\ S_x = l & S_{1x} = 0, S_{2x} = 1 \\ S_x = 0 & S_{1x} = 0, S_{2x} = 0. \end{cases} \tag{1}$$

Fig. 4 shows the switching states and current paths in phase x. (a) $S_x = h$, the high-voltage port supports the ac side. (b) $S_x = l$, the low-voltage port releases/absorbs power to/from the ac side. (c) $S_x = 0$, fly-wheel mode. The output voltages are v_h, v_l, and 0, respectively. The switching states and their corresponding output voltages are given in Table II.

TABLE II
SWITCHING STATES AND OUTPUT VOLTAGES OF THE SINGLE-STAGE MULTIPORT INVERTER

$S_{1x}S_{2x}\bar{S}_{1x}\bar{S}_{2x}$	Switching state S_x	Output voltage
1100	h	v_h
0110	l	v_l
0011	0	0

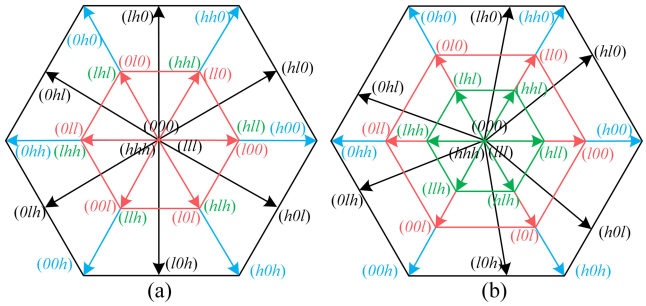

Fig. 5. Space vector diagram of the single-stage multiport inverter. (a) $v_1 = v_2$. (b) $v_1 < v_2$.

Fig. 5 shows the space vector diagram of the single-stage multiport inverter: (a) $v_1 = v_2$ and (b) $v_1 < v_2$. The space vector diagram in Fig. 5(a) is the same as that of a conventional three-level NPC converter. Fig. 5(b) gives the unevenly distributed space vector diagram in the case of the unbalanced dc-link voltages. Synthesizing the reference vectors by uneven space vectors in conventional modulation is a complex task. In this study, synthesizing the reference vectors is realized by directly solving the duty cycles of the single-stage multiport inverter. Based on the proposed solution, complicated calculations of trigonometric functions can be avoided.

B. Mathematical Models for the Single-Stage Multiport Inverter

The output voltage vector and dc-side power mathematical models for the single-stage multiport inverter are established. To simplify the expression, the duty cycles for S_{1x} and S_{2x} are defined as d_{1x} and d_{2x} to establish the mathematical models. There are six duty cycles for the single-stage multiport inverter in total. Controlling the inverter is essential to solve these duty cycles.

The output phase voltage v_{xN} in phase x generated by the single-stage multiport inverter can be expressed as follows:

$$v_{xN} = d_{1x} v_h + (d_{2x} - d_{1x}) v_l. \tag{2}$$

The output voltage vector V_{out} of the single-stage multiport inverter can be calculated as follows:

$$V_{\text{out}} = \frac{2}{3}\left(v_{aN} + \alpha v_{bN} + \alpha^2 v_{cN}\right) \tag{3}$$

where $\alpha = e^{j2\pi/3}$. Then, the mathematical models of grid-side voltage/current can be expressed as follows:

$$\begin{cases} u_g = V_{\text{out}} - L_1 \frac{di_1}{dt} - R_1 i_1 \\ i_g = i_1 - C \frac{du_g}{dt} \end{cases} \tag{4}$$

where u_g/i_g means the grid-side voltage/current, L_1/R_1 indicates the inductance/resistance of the *LC* filter, i_1 is the inverter-side current, and C means the capacitance of the *LC* filter. To ensure beneficial output voltage/current, a cascaded PI controller would be adopted to regulate this second-order system in the following text.

In the $\alpha\beta$ stationary frame, (3) can be rewritten as follows:

$$\begin{cases} V_{\text{out}\alpha} = \frac{2}{3}(v_{aN} - \frac{1}{2}v_{bN} - \frac{1}{2}v_{cN}) \\ V_{\text{out}\beta} = \frac{2}{3}(\frac{\sqrt{3}}{2}v_{bN} - \frac{\sqrt{3}}{2}v_{cN}). \end{cases} \tag{5}$$

According to the current paths in Fig. 4, the dc-side output power model can be written as follows:

$$\begin{cases} P_h = v_h i_h = v_h \sum_{x=a,b,c}(d_{1x} i_x) \\ P_l = v_l i_l = v_l \sum_{x=a,b,c}[(d_{2x} - d_{1x}) i_x] \end{cases} \tag{6}$$

where $i_x (x = a, b, c)$ is the grid-side current and P_h and P_l are the output power of high-voltage and low-voltage dc ports, respectively. Then, the power equation for the single-stage multiport inverter-based microgrid system can be expressed as follows:

$$P_h + P_l = P_{ac} = 3V_g I_g \tag{7}$$

where P_{ac} is the grid-side power, V_g/I_g means the root-mean-square value of the grid-side voltage/current. Hence, flexible dc-side power allocation can be realized by regulating P_h in the case of P_{ac} remains constant.

Based on the aforementioned mathematical models, the optimal duty cycles for realizing reference voltage vector synthesis and dc-side power tracking can be solved. The detailed duty cycle control-based power allocation strategy will be discussed in Section III.

III. Proposed Direct Duty Cycle Control-Based Power Allocation Strategy

The proposed direct duty cycle control-based power allocation strategy is shown in Fig. 6. The single-stage multiport inverter-based microgrid operates in islanded microgrid mode. On the ac side, the traditional cascaded PI control is used to output the reference voltage vector u_g^* [29]. The inputs to the controller are the rated grid voltage and grid frequency. Beneficial grid-side voltage/current would be obtained via the well-known cascaded PI control. On the dc side, the high-voltage port reference output power P_h^* can be obtained from the hybrid ESS power management strategy [30], [31], for instance, filtration-based technique.

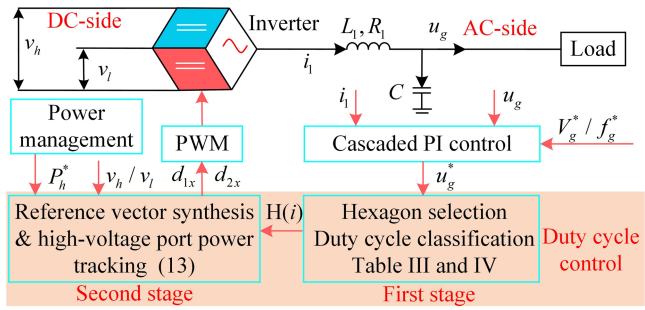

Fig. 6. Direct duty cycle control-based power allocation strategy.

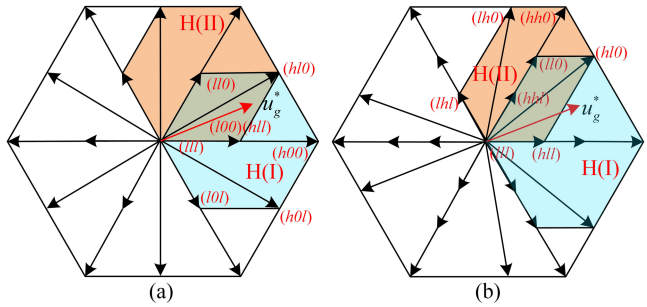

Fig. 7. Hexagon divisions of the single-stage multiport inverter. (a) Hexagon H(I) and hexagon H(II) in the case of $v_1 = v_2$. (b) Hexagon H(I) and hexagon H(II) in the case of $v_1 < v_2$.

As discussed in Section II, the gating signals for the single-stage multiport inverter are six duty cycles. However, the conventional modulation and control solutions for solving these duty cycles are complicated. In this study, these duty cycles are obtained via two stages. In the first stage, the reference voltage vector u_g^* is adopted for the small hexagon selection. Then, duty cycle classification is conducted based on the location of the reference voltage vector. As a result, three duty cycles can be achieved directly in the first stage. To obtain the other three duty cycles, the reference vector synthesis and high-voltage port power tracking equations are solved. Then, beneficial output current and flexible dc-side power allocation can be realized simultaneously.

A. Hexagon Selection and Duty Cycle Classification

The single-stage multiport inverter is first divided into six small hexagons in this study, i.e., H(i), i=I,II,III,IV,V,VI. Fig. 7 shows the hexagon divisions of the single-stage multiport inverter. (a) hexagon H(I) and hexagon H(II) in the case of $v_1 = v_2$. (b) hexagon H(I) and hexagon H(II) in the case of $v_1 < v_2$. The hexagon divisions can be realized based on the location of the reference voltage vector u_g^*. Fig. 7 only shows the hexagon H(I) and hexagon H(II), and the rest hexagons are not shown. It can be concluded from Fig. 7 that the hexagon area is the same in the case of $v_1 = v_2$. On the other hand, the hexagon area is not equal in the case of unbalanced dc-link voltages.

The medium-voltage vectors of the single-stage multiport inverter are adopted for hexagon selection. Table III gives the medium-voltage vectors and switching states of the single-stage

TABLE III
MEDIUM-VOLTAGE VECTORS AND SWITCHING STATES OF THE SINGLE-STAGE MULTIPORT INVERTER

Vector	Switching state	Vector	Switching state
V_{m1}	$(hl0)$	V_{m4}	$(0lh)$
V_{m2}	$(lh0)$	V_{m5}	$(l0h)$
V_{m3}	$(0hl)$	V_{m6}	$(h0l)$

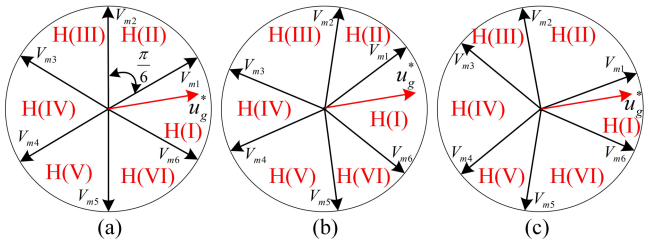

Fig. 8. Results of the hexagon selection with variable dc-link voltages. (a) $v_1 = v_2$. (b) $v_1 < v_2$. (c) $v_1 > v_2$.

TABLE IV
SWITCHING STATES AND DUTY CYCLE CLASSIFICATION IN THE DIFFERENT HEXAGON

Hexagon H	Switching states (duty cycles)		
	Phase a	Phase b	Phase c
I	$h, l(d_{2a}=1)$	$l, 0(d_{1b}=0)$	$l, 0(d_{1c}=0)$
II	$h, l(d_{2a}=1)$	$h, l(d_{2b}=1)$	$l, 0(d_{1c}=0)$
III	$l, 0(d_{1a}=0)$	$h, l(d_{2b}=1)$	$l, 0(d_{1c}=0)$
IV	$l, 0(d_{1a}=0)$	$h, l(d_{2b}=1)$	$h, l(d_{2c}=1)$
V	$l, 0(d_{1a}=0)$	$l, 0(d_{1b}=0)$	$h, l(d_{2c}=1)$
VI	$h, l(d_{2a}=1)$	$l, 0(d_{1b}=0)$	$h, l(d_{2c}=1)$

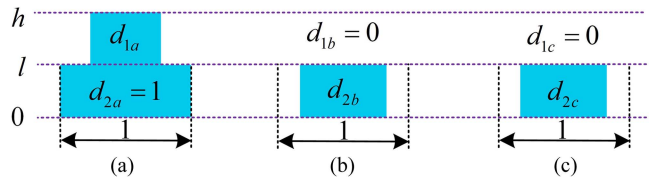

Fig. 9. Duty cycles in hexagon H(I). (a) Phase a. (b) Phase b. (c) Phase c.

multiport inverter. Then, the hexagon selection can be conducted as follows:

$$\mathrm{H}(i) = \begin{cases} \mathrm{I} & \angle\varphi(V_{m6}) < \angle\varphi(u_g^*) \le \angle\varphi(V_{m1}) \\ \mathrm{II} & \angle\varphi(V_{m1}) < \angle\varphi(u_g^*) \le \angle\varphi(V_{m2}) \\ \mathrm{III} & \angle\varphi(V_{m2}) < \angle\varphi(u_g^*) \le \angle\varphi(V_{m3}) \\ \mathrm{IV} & \angle\varphi(V_{m3}) < \angle\varphi(u_g^*) \le \angle\varphi(V_{m4}) \\ \mathrm{V} & \angle\varphi(V_{m4}) < \angle\varphi(u_g^*) \le \angle\varphi(V_{m5}) \\ \mathrm{VI} & \angle\varphi(V_{m5}) < \angle\varphi(u_g^*) \le \angle\varphi(V_{m6}) \end{cases} \tag{8}$$

where $\angle\varphi(u_g^*)$ is the phase angle of reference voltage vector and $\angle\varphi(V_{my})(y = 1, 2, 3, 4, 5, 6)$ indicates the phase angle of medium-voltage vector. Fig. 8 illustrates the results of the hexagon selection with variable dc-link voltages: (a) $v_1 = v_2$, (b) $v_1 < v_2$, (c) $v_1 > v_2$. In the case of $v_1 = v_2$, the angle of each hexagon is $\frac{\pi}{6}$ due to the medium-voltage vector being evenly distributed. In the case of $v_1 < v_2$, the range of H(I)/H(III)/H(V) is wider than that of H(II)/H(IV)/H(VI) whereas the range of H(II)/H(IV)/H(VI) is wider than that of H(I)/H(III)/H(V) under $v_1 > v_2$.

Fig. 7(a) and (b) also show the switching states in hexagon H(I) and hexagon H(II). There are eight candidate switching states in each hexagon. To optimize the switching action and reduce switching losses, the redundant small vectors are selected as $(l0l/ll0)$ and (hll/lhl) in hexagon H(I) and hexagon H(II), respectively. Similarly, the zero vector is selected as (lll). It can be concluded that there are only two switching states in phase $x(x = a, b, c)$ in each hexagon. For example, the phase a switching states in hexagon H(I) are h and l. Then, the duty cycle $d_{2a} = 1$ should be satisfied in hexagon H(I). In summary, the switching states and duty cycles classifications in different hexagons are given in Table IV. As a result, three duty cycles can be achieved via hexagon selection.

B. Duty Cycle Calculation Based on Reference Vector Synthesis and High-Voltage Port Power Tracking

As for the calculation of the other three duty cycles, the mathematical models of the single-stage multiport inverter are adopted. The rest duty cycles can be determined by solving the reference voltage vector synthesis and high-voltage power tracking equations.

Taking hexagon H(I) as an example, Fig. 9 gives the duty cycles in hexagon H(I): (a) phase a, (b) phase b, and (c) phase c. After the hexagon selection, three duty cycles can be obtained in hexagon H(I) as follows:

$$\begin{cases} d_{2a} = 1 \\ d_{1b} = 0 \\ d_{1c} = 0. \end{cases} \tag{9}$$

In hexagon H(I), the control target is to solve d_{1a}, d_{2b}, and d_{2c}. The reference voltage vector synthesis equation can be represented as follows:

$$\frac{2}{3}\left(v_{aN} + \alpha v_{bN} + \alpha^2 v_{cN}\right) = u_g^*. \tag{10}$$

Based on Fig. 9, v_{aN}, v_{bN}, and v_{cN} in hexagon H(I) can be calculated as follows:

$$\begin{cases} d_{1a}v_h + (d_{2a} - d_{1a})v_l = v_{aN} \\ d_{2b}v_l = v_{bN} \\ d_{2c}v_l = v_{cN}. \end{cases} \tag{11}$$

The dc-side power allocation can be realized by regulating the high-voltage port output power P_h^* in the case of ac-side power is a constant value. The high-voltage port output power P_h^* can be described as follows:

$$(d_{1a}i_a + d_{1b}i_b + d_{1c}i_c)v_h = P_h^*. \tag{12}$$

In hexagon H(I), the reference vector synthesis and high-voltage port power tracking equations about the duty cycles can be expressed as follows:

$$\begin{cases} \frac{2}{3}(d_{1a}v_h + (d_{2a} - d_{1a})v_l - \frac{1}{2}d_{2b}v_l - \frac{1}{2}d_{2c}v_l) = u_{g\alpha}^* \\ \frac{2}{3}(\frac{\sqrt{3}}{2}d_{2b}v_l - \frac{\sqrt{3}}{2}d_{2c}v_l) = u_{g\beta}^* \\ d_{1a}i_a + d_{1b}i_b + d_{1c}i_c = P_h^*/v_h \end{cases} \tag{13}$$

where $u_{g\alpha}^*/u_{g\beta}^*$ is the reference voltage vector in the $\alpha\beta$ frame. Then, the other three duty cycles d_{1a}, d_{2b}, and d_{2c} can be solved from (13). To avoid (12) having no solution, the range of P_h^*

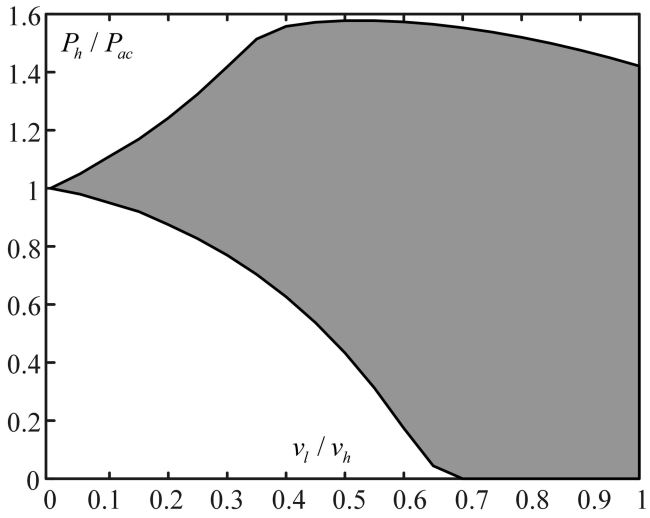

Fig. 10. Power ratio P_h/P_{ac} versus different dc-port voltage ratio v_l/v_h.

should be considered. Fig. 10 shows the power ratio P_h/P_{ac} versus different dc-port voltage ratio v_l/v_h. The relationship between P_h/P_{ac} and v_l/v_h is determined by the redundant small vectors in each hexagon. For example, the positive/negative small vector $S_x = l00/hll$ in hexagon H(I). The redundant small vectors have opposite current paths of the low-voltage port, i.e., $i_l > 0$ when $S_x = l00$ is used, and $i_l < 0$ when $S_x = hll$ is used. For a fixed v_l/v_h, the minimum value of P_h/P_{ac} indicates the negative small vector $S_x = hll$ is discarded whereas the positive small vector $S_x = l00$ is used. In this condition, the high-voltage port and low-voltage port support the ac grid together. The maximum value of P_h/P_{ac} indicates the positive small vector $S_x = l00$ is discarded whereas, the negative small vector $S_x = hll$ is used. In this case, the high-voltage port not only supports ac grid but also charges to the low-voltage port. The range of P_h/P_{ac} is also related to the dc-port voltage ratio v_l/v_h. It can be concluded from Fig. 10 that the range of P_h/P_{ac} increases with the increase of v_l/v_h. The reason is that the freedom of degree provided by redundant small vectors has been increased with the increase of v_l/v_h. To achieve a wider power range, the dc-port voltage ratio v_l/v_h should be set larger. It can be concluded that the high-voltage dc port is unidirectional. Considering that $P_h + P_l = P_{\text{ac}}$ should be satisfied, the low-voltage dc port is bidirectional. Hence, the proposed solution is suitable for the RES–ESS hybrid system. The high-voltage dc port can be adopted to connect RES, for instance, the PV unit. The flexible charging/discharging operation cases of ESS can be realized by the low-voltage dc port.

C. Duty Cycle Calculation Flowchart

It can be concluded from Fig. 7 that there is an overlap between the odd hexagon and even hexagon. For example, there is an overlap between hexagon H(I) and hexagon H(II) under $\angle\varphi(u_g^*) \in [0, \angle\varphi(V_{m1})]$. If the duty cycle solution is out of switching constraints, the overlap can be adopted as redundancy. The flowchart of the duty cycle calculation under $\angle\varphi(u_g^*) \in [0, \angle\varphi(V_{m1})]$ is given in Fig. 11. The overlap between hexagon H(I) and hexagon H(II) is considered as an example to illustrate the duty cycle calculation process. The domain of $d_{jx}(j = 1, 2)$ should be $d_{jx} \in [0, 1]$. As shown in Fig. 11, if there is no solution in hexagon H(I), duty cycle calculation can be conducted in hexagon H(II) due to P_h^* being preset in the controllable range according to Fig. 10.

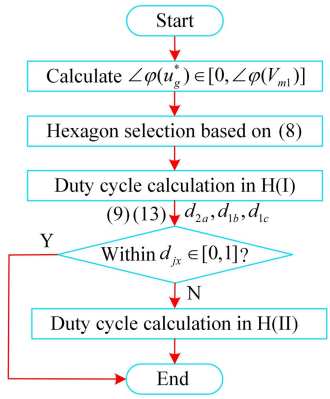

Fig. 11. Flowchart of the duty cycle calculation under $\angle\varphi(u_g^*) \in [0, \angle\varphi(V_{m1})]$.

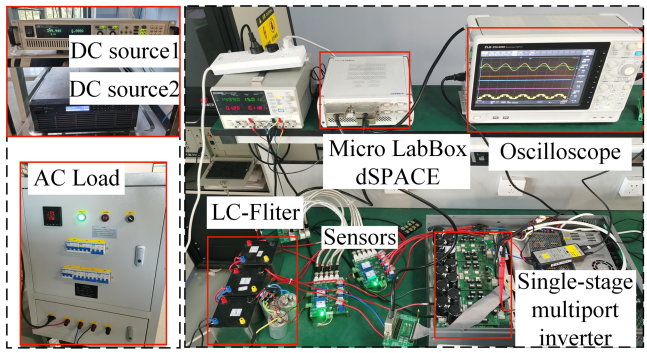

Fig. 12. Experimental test plant.

IV. Experimental Results

The effectiveness of the proposed strategy is evaluated through the experimental results. A down-scaled experimental plant is established to verify the proposed strategy, which is depicted in Fig. 12. To accomplish the proposed algorithm, the dSPACE MicroLabBox DS1202 controller is adopted. The sampling time/frequency is set as T_s=100 μs/f_s=10 kHz. The single-stage multiport inverter was implemented by insulated-gate bipolar transistors. The dc-side input voltages are generated by two programmable dc sources. Where the low-voltage port dc source is bidirectional. An eight-channel oscilloscope is adopted to display experimental variables. The main experimental parameters are listed in Table V.

The following experimental tests are conducted in islanded microgrid mode, including the steady-state tests under variable port voltages, dynamic tests of variable power, and comparison tests with conventional strategies.

TABLE V
PARAMETERS OF THE TEST SYSTEM

Low voltage	v_l=160-240V
High voltage	v_h=400V
DC-side capacitance	$C_1 = C_2$=4920μF
LC-Filter inductance	L_1/R_1=3mH/0.4Ω
LC-Filter capacitance	C=15μF
Sampling time/frequency	T_s=100μs/f_s=10kHz
Rated grid voltage	V_g^*=110V
Rated grid frequency	f_g^*=50Hz
Rated grid active power	P_{ac}^*=1kW
Rated grid reactive power	Q_{ac}^*=0var

A. Steady-State Tests

The steady-state tests under variable port voltages are carried out to verify the effectiveness of the proposed strategy. The variable port voltages can be generated by two programmable dc sources. The high voltage is set as $v_h = 400$ V. Three different port voltage conditions are considered in the steady-state tests, i.e., $v_1 = v_2$, $v_1 < v_2$, and $v_1 > v_2$. The results of hexagon selection and duty cycle calculation, power allocation results under the balanced/unbalanced port voltages, and grid-side current quality analysis are given as follows:

1) Results of Hexagon Selection and Duty Cycle Calculation With Different Port Voltages: Fig. 13 illustrates the steady performance with different port voltages: (a) $v_2 = 200$ V ($v_1 = v_2$), (b) $v_2 = 240$ V ($v_1 < v_2$), and (c) $v_2 = 160$ V ($v_1 > v_2$). From top to bottom: waveform is hexagon H(i), grid-side voltage u_{ga}, u_{gb}, u_{gc}, duty cycle d_{1a}, d_{2a}, and phase voltage v_{aN}. As shown in Fig. 13(a), the same hexagon range is achieved. In Fig. 13(b), the range of H(I)/H(III)/H(V) is wider than that of H(II)/H(IV)/H(VI). The range of H(II)/H(IV)/H(VI) is wider than that of H(I)/H(III)/H(V) in Fig. 13(c). The results of hexagon selection are consistent with the theoretical analysis in Section III. The differences in duty cycle and phase voltage are caused by the different port voltages. Although the port voltages are different in these conditions, beneficial grid-side voltage can be obtained. Hence, the proposed strategy is effective for different port voltages. Desirable hexagon selection and duty cycle calculation can be conducted.

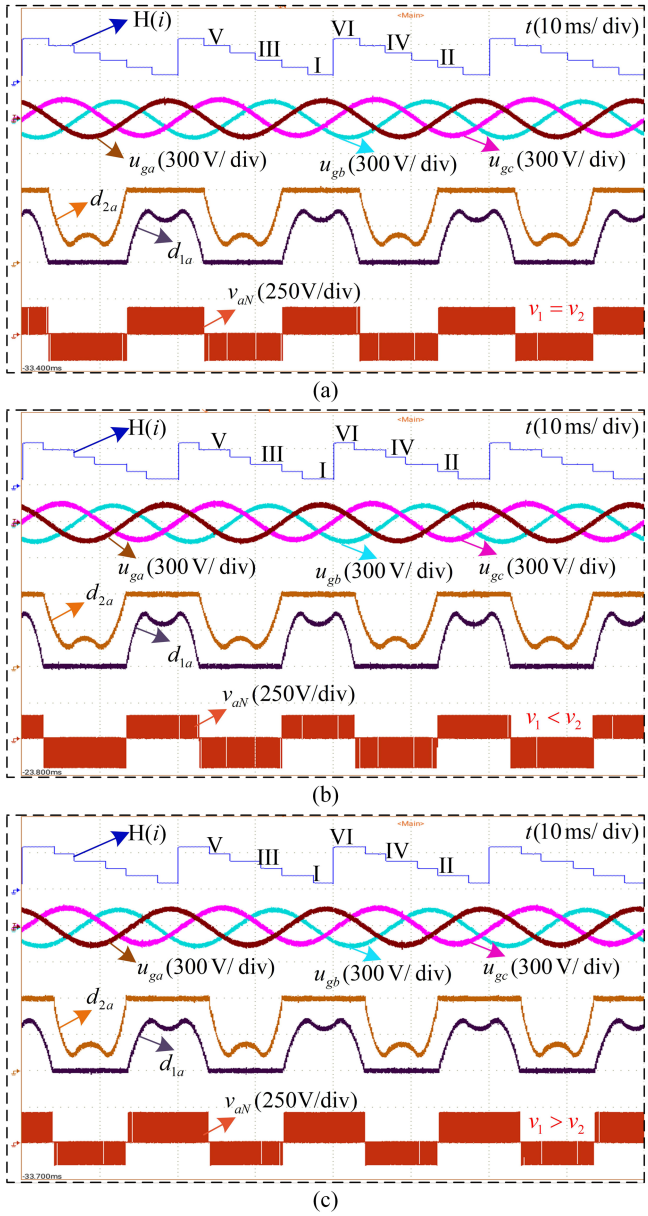

Fig. 13. Steady-state performance with different port voltages. (a) $v_2 = 200$ V ($v_1 = v_2$). (b) $v_2 = 240$ V ($v_1 < v_2$). (c) $v_2 = 160$ V ($v_1 > v_2$). From top to bottom: waveform is hexagon H(i), grid-side voltage u_{ga}, u_{gb}, u_{gc}, duty cycle d_{1a}, d_{2a}, and phase voltage v_{aN}.

2) Power Allocation Results Under Balanced Port Voltages: Power allocation results under balanced port voltages are carried out to verify the proposed power allocation strategy. Fig. 14 shows power allocation results under balanced port voltages: (a) $P_h = 1$ kW ($P_h = P_{ac}$), (b) $P_h = 0.8$ kW ($P_h < P_{ac}$), and (c) $P_h = 1.2$ kW ($P_h > P_{\rm ac}$). From top to bottom: waveform is grid-side voltage $u_{\rm ga}$, grid-side current $i_{\rm ga}$, grid active power $P_{\rm ac}$, grid reactive power $Q_{\rm ac}$, high-voltage port output power P_h, low-voltage port output power P_l, and line-to-line voltage $v_{\rm ba}$. The reference grid active/reactive power is set as a constant, i.e., $P_{\rm ac} = 1$kW, $Q_{\rm ac}$=0 var. Three different power allocation conditions can be realized by regulating the high-voltage port reference output power P_h^*. The high-voltage port can support the ac side alone in Fig. 14(a), i.e., $P_h = P_{\rm ac}$ and $P_l = 0$. This condition can be considered as the conventional three-level NPC inverter with zero neutral currents. The low-voltage port is adopted to release power when $P_h < P_{\rm ac}$, and absorb the excess power when $P_h > P_{\rm ac}$. In addition, it can be concluded from Fig. 14 that grid-side voltage/current and line-to-line voltage are well-tracked in the case of different power allocation conditions. Therefore, the proposed strategy can realize flexible power allocation under balanced port voltages.

3) Power Allocation Results Under Unbalanced Port Voltages: Fig. 15 shows power allocation results under unbalanced port voltages: (a) $v_2 = 240$ V ($v_1 < v_2$) and (b) $v_2 = 160$ V ($v_1 > v_2$). The asymmetrical phase-to-phase voltage $v_{\rm ba}$ is caused by the unbalanced port voltages. In these tests, the reference grid active/reactive power is set as a constant, and the high-voltage port reference output power is set as $P_h^* = 1$ kW. Although the port voltages are unbalanced, the ac/dc-side power

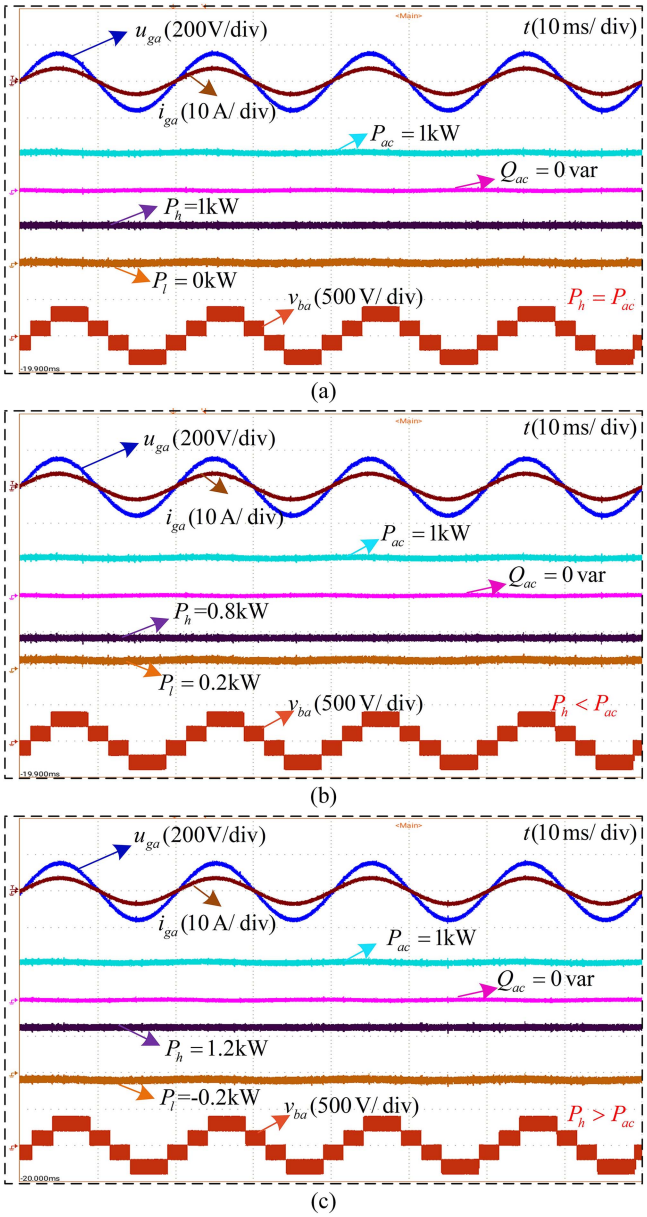

Fig. 14. Power allocation results under balanced port voltages. (a) $P_h = 1$kW ($P_h = P_{ac}$). (b) $P_h = 0.8$kW ($P_h < P_{ac}$). (c) $P_h = 1.2$kW ($P_h > P_{ac}$). From top to bottom: waveform is grid-side voltage u_{ga}, grid-side current i_{ga}, grid active power P_{ac}, grid reactive power Q_{ac}, high-voltage port output power P_h, low-voltage port output power P_l, and line-to-line voltage v_{ba}.

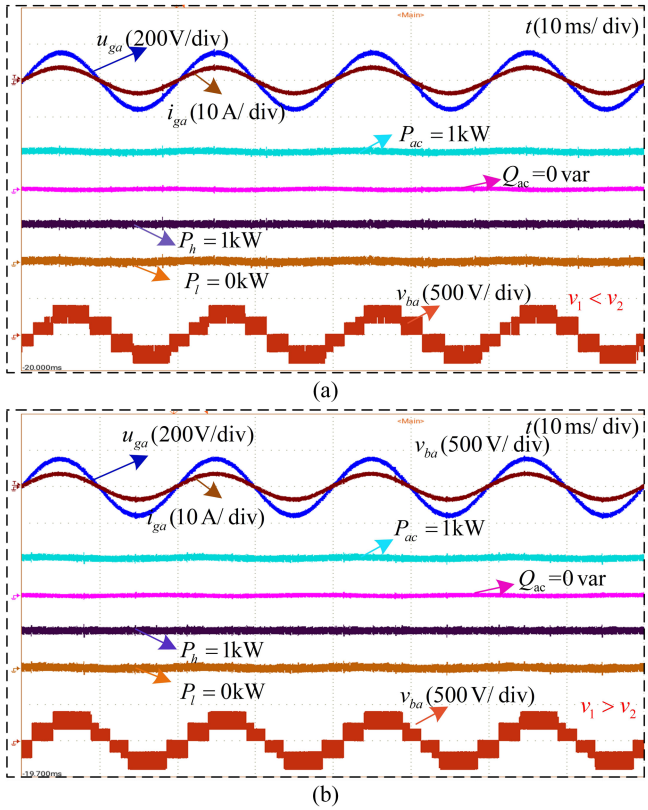

Fig. 15. Power allocation results under unbalanced port voltages. (a) $v_2 = 240$V ($v_1 < v_2$). (b) $v_2 = 160$V ($v_1 > v_2$).

can be controlled as desired. Moreover, the desired grid-side voltage/current is ensured. Hence, the proposed power allocation strategy is effective for unbalanced port voltages.

4) Grid-Side Current Quality Analysis: The quality of the grid-side current should be evaluated. Fig. 16 gives the grid-side current fast Fourier transform (FFT) results under different port voltages: (a) $v_2 = 200$ V ($v_1 = v_2$) and (b) $v_2 = 240$ V ($v_1 < v_2$). The current data were acquired from the oscilloscope and analyzed in MATLAB. From top to bottom: waveform is grid-side current i_{ga} and its spectrum. The total harmonic distortion (THD) is also given. It can be noted that the quality of grid-side current under different port voltages is quite similar, i.e., THD = 2.53% in Fig. 16(a) and THD = 2.55% in Fig. 16(b). Therefore, the proposed strategy could provide beneficial output current at various port voltage scenarios.

B. Dynamic Performance

To verify the dynamic performance of the proposed strategy, the dynamic tests of variable high-voltage port output power and grid power are conducted. In these tests, the results include grid-side voltage/current v_{ga}/i_{ga}, dc-side power P_h/P_l, line-to-line voltage v_{ba}, and dc-side current i_h/i_l.

1) Variable High-Voltage Port Output Power Tests Under Constant Grid Power: Fig. 17 shows the results of the high-voltage port output power step-up/step-down tests under constant grid active power with $v_2 = 240$ V ($v_1 < v_2$): (a) from 0.6 to 1.2 kW and (b) from 1.2 to 0.6 kW. The tests are adopted to simulate variable RES power generation under constant grid power. As shown in Fig. 17, the grid-side voltage/current v_{ga}/i_{ga} and grid active/reactive power P_{ac}/Q_{ac} track the reference value precisely even around the step change. When the high-voltage port power P_h changes, the low-voltage port power P_l changes instantaneously. The dc-side power has a fast response due to the duty cycle being directly generated. The stable line-to-line voltage v_{ba} indicates that the dc-side voltages remain constant, and the variation trend of dc-side current is the same as that of dc-side power.

2) Variable Grid Power Tests Under Constant High-Voltage Port Output Power: Fig. 18 shows the results of the grid power

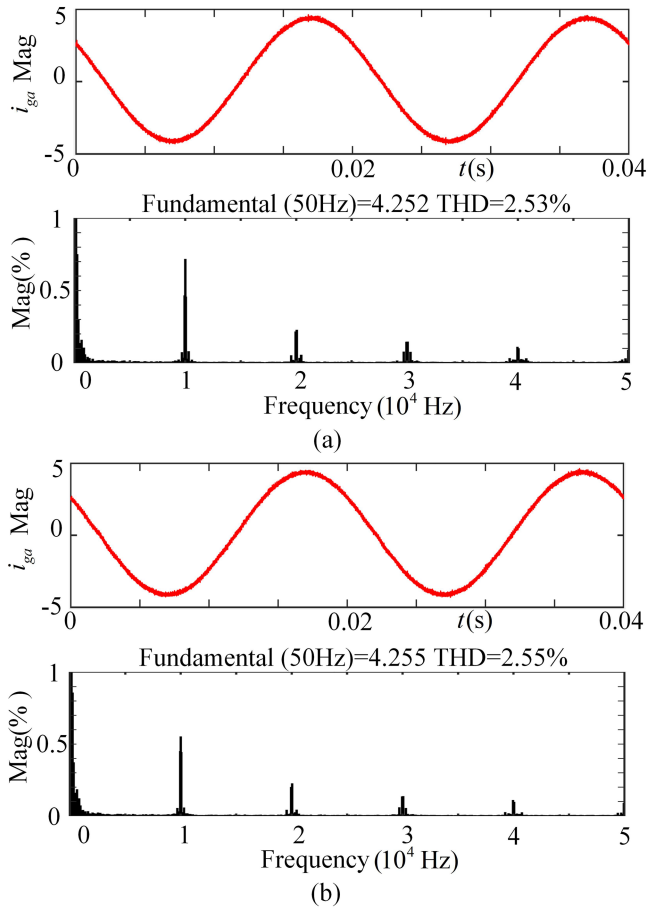

Fig. 16. Grid-side current FFT results under different port voltages. (a) $v_2 = 200$ V ($v_1 = v_2$). (b) $v_2 = 240$ V ($v_1 < v_2$). From top to bottom: waveform is grid-side current i_{ga} and its spectrum.

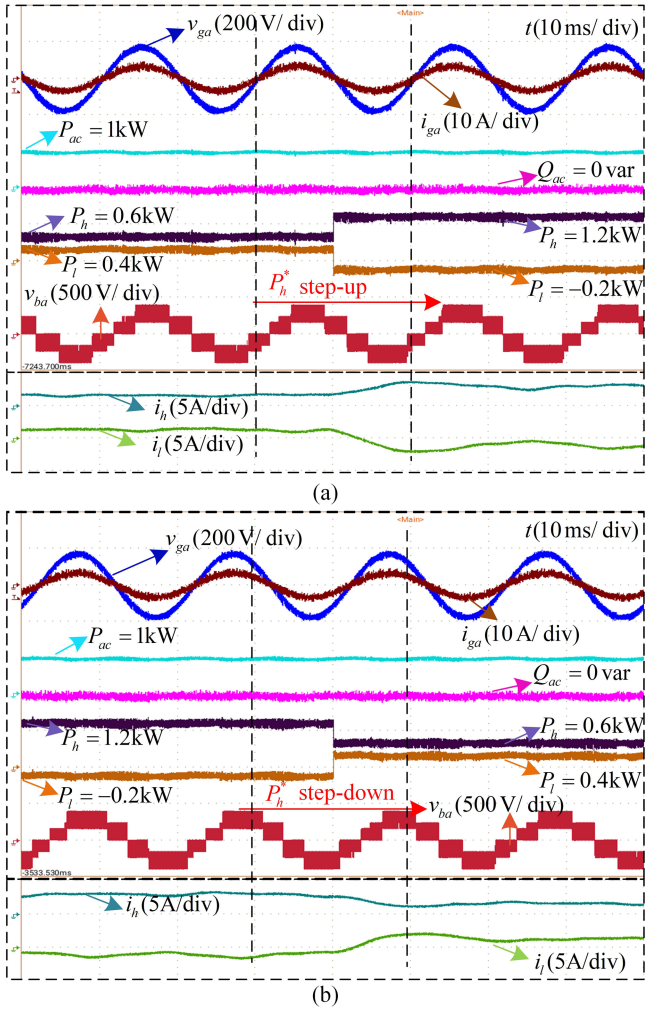

Fig. 17. Results of the high-voltage port output power step-up/step-down tests under constant grid power with $v_2 = 240$ V ($v_1 < v_2$). (a) From 0.6 to 1.2 kW. (b) From 1.2 to 0.6 kW.

step-up/step-down tests under constant high-voltage port output power with $v_2 = 240$V ($v_1 < v_2$): (a) from 0.6 to 1.2 kW and (b) from 1.2 to 0.6 kW. When the load changes suddenly, the high-voltage port power P_h is regulated as a constant value ($P_h =$ 1kW), and the low-voltage port is used to release or absorb the superfluous power. The tests are adopted to simulate variable grid power demand under constant RES power generation. As shown in Fig. 18(a), when grid power P_{ac} changes from 0.6 to 1 kW, the low-voltage port is adopted to release power to the grid, i.e., P_l changes from -0.4 to 0.2 kW. When grid power P_{ac} changes from 1.2 to 0.6 kW in Fig. 18(b), the low-voltage port is used to absorb the excess power, i.e., P_l changes from 0.2 to -0.4 kW. As for the voltage and current response, ac-side voltage v_{ga} remain stable and has small distortion around the step change. The ac-side current i_{ga} changes rapidly with the grid power change. The line-to-line voltage v_{ba} indicates that the dc-side voltages remain stable. Due to the high-voltage port power P_h being regulated as a constant value, the high-voltage port current i_h remains stable with small distortion around the step change. The variation trend of i_l is the same as that of P_l.

Figs. 17 and 18 suggest that the proposed direct duty cycle-based power allocation strategy has a fast and smooth dynamic performance.

C. Comparison Tests With Conventional SVM-Based Control Strategies

To verify the simplification of the proposed strategy, the comparison tests between the conventional SVM-based control strategies in [25] and [26] are carried out. The SVM-based PI control is used in [25], and the SVM-based deadbeat control is studied in [26]. The implementation time of different control strategies is discussed first. Then, the dynamic response performance comparison is given.

1) Implementation Time Comparison: To evaluate the computational burden of the proposed strategy, the implementation time of the conventional SVM-based strategies [25], [26] and the proposed strategy was measured by using the dSPACE profiler. The implementation time of different control strategies is shown in Fig. 19. Each method includes the same time of A/D conversion and others. Due to the modulation process being

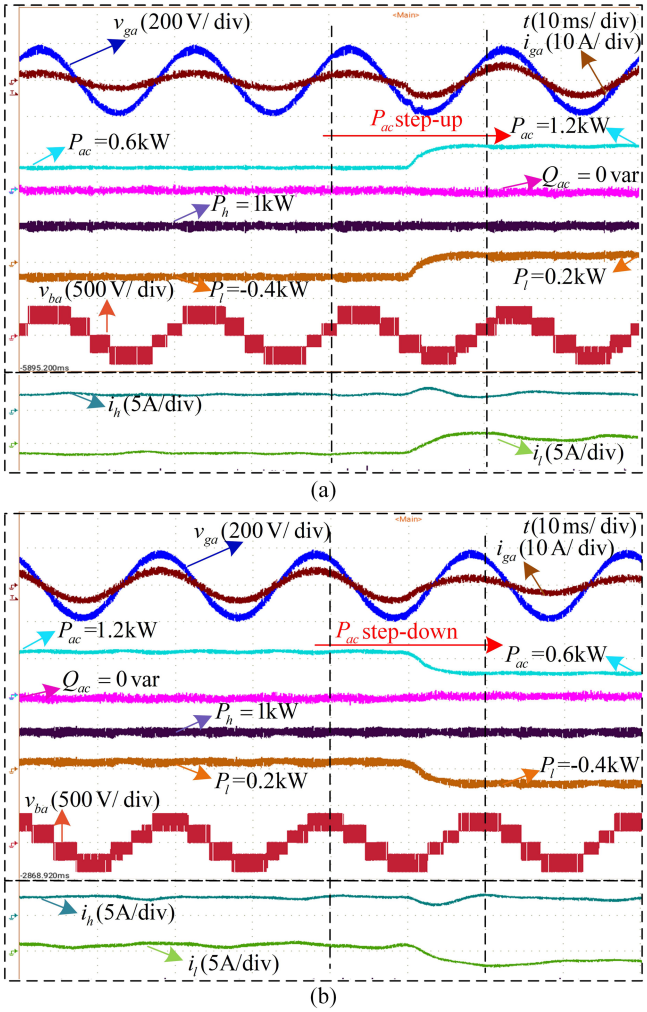

Fig. 18. Results of the grid power step-up/step-down tests under constant high-voltage port output power with $v_2 = 240$ V ($v_1 < v_2$). (a) From 0.6 to 1.2 kW. (b) From 1.2 to 0.6 kW.

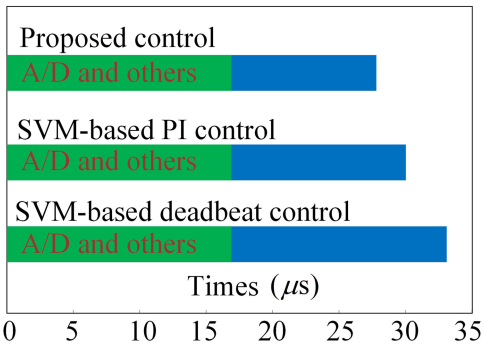

Fig. 19. Implementation time of different control strategies.

unavoidable, the implementation time of SVM-based control strategies is longer than that of the proposed strategy. The longest implementation time of the SVM-based deadbeat control strategy is caused by the complicated power calculation. The proposed strategy has the shortest implementation time i.e., shows the smallest computational burden among these three

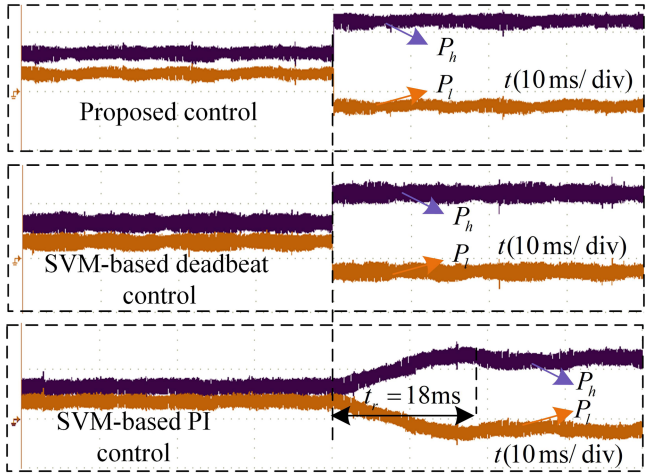

Fig. 20. Dynamic results of dc-side power under P_h changes from 0.6 to 1.2 kW using different control strategies.

strategies. Hence, the proposed strategy could simplify the calculation effectively.

2) Dynamic Response Comparison: To highlight the fast dynamic response of the proposed strategy, the comparison tests with conventional SVM-based control strategies [25], [26] under variable P_h are conducted. Fig. 20 shows the dc-side power under P_h changes from 0.6 to 1.2 kW using different control strategies. The proposed strategy and SVM-based deadbeat control strategy achieve fast dynamic performance due to these methods directly allocating the dc-port power. However, the dc-port power allocation is realized by indirect feedback control in the SVM-based PI method. The transient time of SVM-based PI control is around 18 ms, which is the longest among these strategies.

In summary, the proposed strategy shows less implementation time and faster dynamic response than that of conventional strategies. Simplification in the control implementation can be realized by the proposed strategy.

V. Conclusion

This article proposes a direct duty cycle control-based power allocation strategy for the single-stage multiport inverter. Based on the mathematical models of the single-stage multiport inverter, the reference voltage synthesis and dc-side power tracking can be easily realized by directly controlling the duty cycles without any complicated modulation/control process. The proposed power allocation strategy has the following advantages: 1) the proposed strategy is effective for variable dc-link voltages and power demand; 2) the fast and smooth dynamic response was intact; and 3) beneficial grid-side current together with flexible power allocation can be obtained. Furthermore, experimental evaluations of the islanded microgrid validated the superiority of the proposed power allocation strategy. A single-stage multiport inverter with the proposed power allocation strategy offers a high-efficiency solution for the islanded microgrid.

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