Determination and Implementation of SiC MOSFETs Zero Turn-OFF Loss Transition Considering No Miller Plateau

Shijie Song, *Graduate Student Member, IEEE*, Han Peng, *Senior Member, IEEE*, Xinbo Chen, *Student Member, IEEE*, Qing Xin, and Yong Kang, *Fellow, IEEE*

***Abstract*—Realizing zero turn-OFF loss (ZTL) of SiC MOSFETs in zero voltage switching (ZVS) power converters will further break the limitation of the switching frequency and push for higher power density. However, quantitative models analyzing ZTL phenomenon were not revealed in state-of-arts and the assumptions of switching transients under ZTL were not correct. Current ZTL implementations either have limited application range or sacrificed transition speed. To overcome these limitations, this article proposes an improved determination criterion considering no Miller plateau for an accurate prediction of ZTL and its boundary based on the Miller's theorem. A more accurate multicurve parameter extraction approach is presented combining the C-V curve with the gate charge and transfer characteristic curves for parameters extraction under dynamic switching transients, further improving the ZTL determination accuracy. For ZTL implementation, a novel approach of coadjustment of gate and channel current based on the gate charge compensation is first proposed, with advantages of wide adaptive range and high d*v*/d*t*. Experiments show the quantitative determination of the ZTL boundary has prediction error of less than 9.5%. It is also verified that the proposed ZTL implementation can reduce the turn-OFF loss up to 81% with only 20% increasement in the drain-source voltage rising time at ZTL boundary transition. The proposed implementation is also capable to adjust d*v*/d*t* based on demand with adjustment error less than 7.2%.**

***Index Terms*—Gate charge compensation, no Miller plateau, quantitative model, SiC MOSFETs, zero turn-OFF loss (ZTL).**

I. Introduction

THE newly emerging wide-bandgap semiconductors represented by silicon carbide (SiC) and gallium nitride (GaN) are attractive due to its low resistance and high switching speed, which greatly prompts power converters toward high efficiency and high power density [1]. The realization of the high power density requires high switching frequency to shrink the volume of the converter, which makes switching loss more serious. The turn-ON loss of power devices can be significantly eliminated by the soft switching techniques, such as zero voltage switching (ZVS) [2], [3]. However, the turn-OFF loss is still quite crucial under high power and heavy-load applications. As shown in Fig. 1(a), the turn-OFF loss is approaching turn-ON loss when load current reaches to 100 A of SiC C3M0015065K [4]. Under ZVS turn-ON applications, the turn-OFF loss will be the main loss contributor in the power conversions with zero voltage switching, such as phase-shifted full-bridge converter widely used in on-board chargers for electric vehicles and communication power supplies. Switching frequency will be determined by the turn-OFF loss. Shown in Fig. 1(b), the switching frequency will drop to 100 kHz at 80 A load current under a specified maximum power dissipation. The turn-OFF loss can be the main loss contributor, which will also determine the size of the heat sink, as shown in Fig. 2(a). Therefore, the turn-OFF loss plays a critical role in further breaking through switching frequency limit and improve the power density.

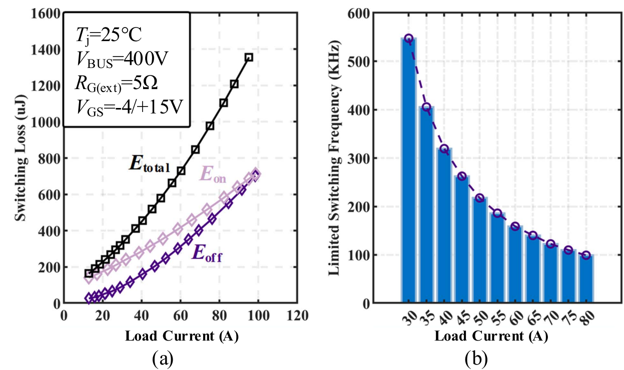


Fig. 1. (a) Clamped inductive switching loss under different loads for Wolfspeed SiC device: C3M0015065K. (b) Upper limit of switching frequency under different loads calculated from C3M0015065K's datasheet under maximum power dissipation of 50 W.

The actual turn-OFF loss should only consider the current flowing through the channel of the power transistor. Due to the existence of the junction capacitance, the drain current i_d is divided into i_{oss} flowing into the junction capacitance and the channel current i_{ch} [5], [6], [7], as shown in Fig. 2(b). Li et al. [8], [9] revealed that zero turn-OFF loss (ZTL) of SiC

Manuscript received 9 January 2023; revised 20 May 2023; accepted 16 July 2023. Date of publication 27 July 2023; date of current version 23 October 2023. This work was supported by the National Natural Science Foundation of China under Grant 52277178 and Grant 52007077. Recommended for publication by Associate Editor J. Popovic-Gerber. *(Corresponding author: Han Peng.)*

The authors are with the State Key Laboratory of Advanced Electromagnetic Technology, School of Electrical and Electronic Engineering, Huazhong University of Science and Technology, Wuhan 430074, China (e-mail: songsj@hust.edu.cn; pengh@hust.edu.cn; xb_chen@hust.edu.cn; qingxin@hust.edu.cn; ykang@hust.edu.cn).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3299387.

Digital Object Identifier 10.1109/TPEL.2023.3299387

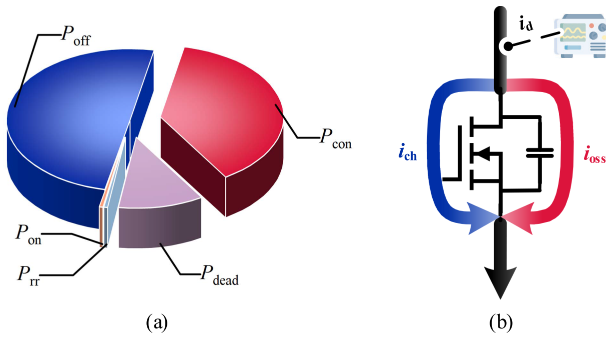


Fig. 2. (a) Loss breakdown under soft turn-ON of SiC device C3M0015065K at the bus voltage of 400 V, load current of 20 A, and switching frequency of 500 kHz and (b) actual current distribution during the turn-OFF process.

MOSFET is achieved at nearly zero i_{ch} and can be achieved by increasing switching speed. A qualitative criterion of ZTL was further proposed in [10] and [11] that ZTL happens at i_{ch} dropping to zero before the end of the drain-source voltage rising. However, no theoretical analysis of ZTL was given, which was not convenient for practical design. Authors in [12] and [13] presented an analytical expression to determine the ZTL current range under the assumption of constant gate voltage v_{gs} at Miller plateau during drain-source voltage v_{ds} rising. However, when power transistors work under ZTL, v_{gs} needs to drop quickly from the Miller voltage V_{mil} to the threshold voltage V_{th}, letting i_{ch} return to zero in advance to v_{ds} rising to bus voltage V_{BUS} [14]. Therefore, there is no Miller plateau under ZTL. As Miller plateau significantly affects the switching transient, large errors of ZTL determining will be induced by adopting models considering constant Miller plateau.

Furthermore, the analytical solutions for determining ZTL require the accurate extraction of power device parameters. State-of-art works relied on the I-V (transfer characteristic) curve and C-V curve from devices' datasheet to obtain the key parameters such as stray capacitance and transfer characteristic [15], [16]. However, the I-V and C-V curves are not accurate to extract the parameters of power devices under high v_{ds} in the dynamic switching transient due to the differences in testing conditions. For example, although the nonlinear parasitic capacitances of the power device were taken into account [17], [18], the predicted switching waveforms were also significantly different from the experiment in current and voltage transition intervals. Authors in [18], [19], and [20] further discussed that the short channel effect and drain-induced barrier lowering (DIBL) cause the transfer characteristic to change with v_{ds} during the current transition interval, resulting in a prediction error of 77.6% on the channel current. Due to the existence of dynamic Miller charge [21], the Miller capacitance (C_{gd}) changes greatly during the switching transient, which cannot be directly extracted from the C-V curve. Although transfer characteristic [22], [23] and dynamic Miller charge [21], [24] can be obtained under repeated experiments, huge time and labor are required, which is not practical of engineering practices.

For the above limitations, this article proposes an improved analytical solution to determine ZTL transition considering no Miller plateau. Combining the C-V curve with the gate charge and transfer characteristic curves, a more accurate method extracting devices' parasitic capacitors and transfer characteristic during the dynamic switching transient is established. Moreover, according to the accurate analytical ZTL model, a novel ZTL implementation approach based on the gate charge compensation is proposed, which can meet both high turn-OFF speed and ultralow loss. The main contributions of this article can be summarized as follows.

1) ZTL is realized with channel current falling to zero before the finish of the drain-source voltage transition. Therefore, no Miller plateau region is under ZTL. A new and more accurate ZTL determination criterion considering no Miller plateau is first proposed in this article. It is carried out by relating the gate-source voltage, drain-source voltage, and their transition speeds at the turn-OFF transient based on the Miller's theorem. The boundary point of ZTL is analyzed to be the optimum condition for both low turn-OFF loss and high turn-OFF speed.
2) To solve the problem of the inconsistency in testing conditions between datasheets and actual switching transients, this article proposes to use C-V curve together with gate charge and transfer characteristic curves to form a more accurate approach to extract device's parasitic capacitors and transfer function. It furthers improve the accuracy of ZTL determination.
3) State-of-art ZTL implementations based on gate driving speed acceleration [9] have limited adjustment range, while the channel current adjustment approach [11] has to sacrifice voltage rising speed in device turning OFF. Thus, this article innovatively suggests a gate charge compensation approach for ZTL realization. Both ZTL and adjustable turn-OFF speed have been simultaneously achieved.
4) The proposed quantitative model of ZTL is verified with prediction error of less than 9.5%. The gate driver with gate current compensated is verified to achieve the ZTL boundary point successfully, which reduces the turn-OFF loss by 81%. Compared with channel-current adjustment at same turn-OFF energy reduction, the proposed approach achieves 52.6% reduction in v_{ds} rising time. $\mathrm{d}v_{ds}/\mathrm{d}t$ can also be adjusted by demand and the adjustment error is less than 7.2%.

The rest of the article is organized as follows: an improved analytical solution to determine ZTL of SiC MOSFETs with no Miller plateau is proposed in Section II, which also includes a more accurate method for parameter extraction during the dynamic switching process. Section III presents the novel gate charge compensation approach to realize ZTL turn-OFF while maintaining similar drain-source voltage rising speed. Prototype and experimental verifications are presented in Section IV, followed by conclusions drawn in Section V.

II. ZTL Determining Considering No Miller Plateau

The purposes of this section are to derive an analytical model for ZTL determining with no Miller plateau. A more

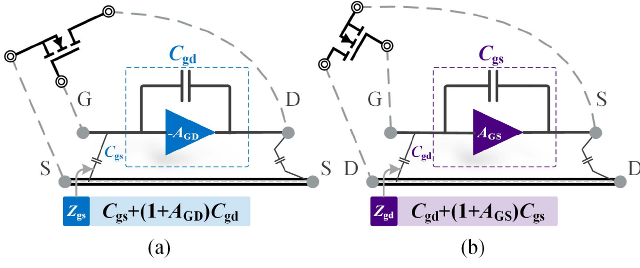


Fig. 3. Miller's theorem on power transistors. (a) Looking from the gate-source side. (b) Looking from the gate-drain side.

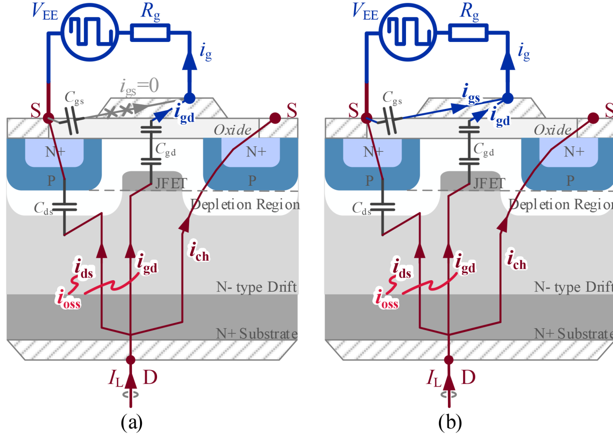


Fig. 4. Gate driver and power loop current distributions during SiC MOSFETs turn-OFF process. (a) With Miller plateau. (b) With no Miller plateau.

accurate approach for device parameters extraction based upon the datasheets for high voltage and current dynamic switching will also be revealed.

A. *ZTL Determining With No Miller Plateau*

The ZTL determination without Miller plateau is established using the mechanism of Miller effect during the turn-OFF process [25]. Considering the Miller's theorem on the gate-source side, as shown in Fig. 3(a), the equivalent capacitance of C_{gd} added to the gate-source side will be expanded to $(1 + A_{GD})C_{gd}$, as

$$
\begin{aligned}
i_g &= C_{gs}\frac{dv_{gs}}{dt} + C_{gd}\left(\frac{dv_{gs}}{dt} - \frac{dv_{ds}}{dt}\right) \\
&= \left(C_{gs} + \left(1 + A_{GD}\right)C_{gd}\right)\frac{dv_{gs}}{dt} \qquad (1)
\end{aligned}
$$

where the drain-source voltage rising speed (dv_{ds}/dt) and the gate-source voltage dropping speed (dv_{gs}/dt) have opposite signs, and A_{GD} represents the ratio of the absolute values of dv_{ds}/dt over dv_{gs}/dt. In conventional switching model with Miller plateau, A_{GD} is usually considered to be greatly large and v_{gs} is unchanged at Miller plateau during v_{ds} rising. Therefore, no gate current flow through C_{gs} and i_g is all used to charge C_{gd}, as shown in Fig. 4(a).

However, in the actual turn-OFF process of SiC MOSFETs, as shown in Fig. 5, due to the small parasitic capacitance, v_{gs} is no longer constant during v_{ds} rising stage [5], [26]. With the increase of i_g and the decrease of load current I_L, v_{gs} will drop faster. If v_{gs} drops from V_{mil} to V_{th} before the end of v_{ds} rising, ZTL or quasi-ZTL can be achieved. In this article, it is assumed that v_{gs} decreases linearly during the stage of v_{ds} rising [26], [27], and v_{ds} rises from the pinch-off voltage V_{pin} to the bus voltage V_{BUS} in this stage.

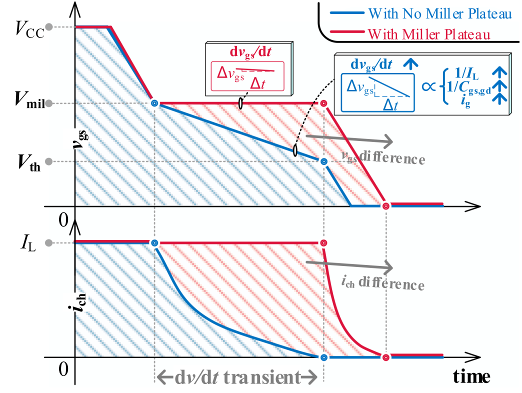


Fig. 5. Switching behaviors with and without Miller plateau.

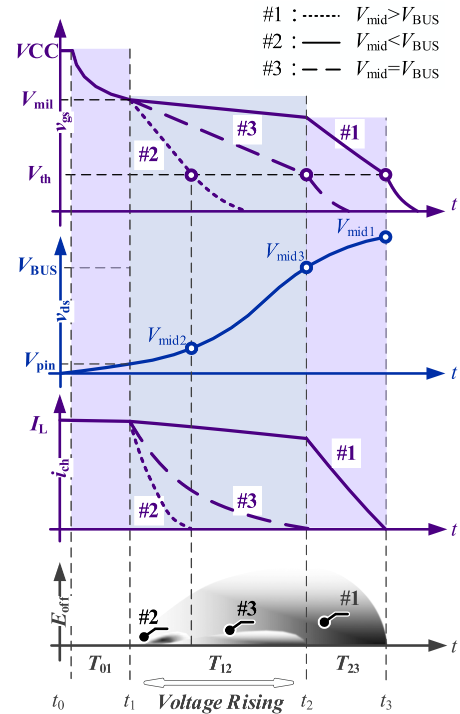


Fig. 6. Typical transient waveforms during SiC MOSFETs' turn-OFF process.

The turn-OFF transient waveforms under no Miller plateau are shown in Fig. 6. In order to obtain the determination criterion of ZTL, stage t_1-t_2 of the dv/dt transient is studied. Drain-source voltage V_{mid} is defined as the point when v_{gs} is decreased to V_{th}, and i_{ch} reaches to zero. Constructing the analytical expressions of V_{mid} under different operation conditions is the prerequisite to determine ZTL.

According to the simultaneous change of $v_{\rm gs}$ and $v_{\rm ds}$, an equation of the drive loop and the power loop over time can be built as

$$-\frac{V_{\rm mil}-V_{\rm th}}{{\rm d}\bar{v}_{\rm gs}/{\rm d}t}=\frac{V_{\rm mid}-V_{\rm pin}}{{\rm d}\bar{v}_{\rm ds}/{\rm d}t} \tag{2}$$

where ${\rm d}\bar{v}_{\rm gs}/{\rm d}t$ represents the average dropping rate of $v_{\rm gs}$ and ${\rm d}\bar{v}_{\rm ds}/{\rm d}t$ represents the average dropping rate of $v_{\rm ds}$. $V_{\rm th}$, $V_{\rm mil}$, and $V_{\rm pin}$ are the inherent device parameters under given working condition, while ${\rm d}\bar{v}_{\rm gs}/{\rm d}t$ and ${\rm d}\bar{v}_{\rm ds}/{\rm d}t$ are the key variables determining $V_{\rm mid}$. The larger $|{\rm d}\bar{v}_{\rm gs}/{\rm d}t|$ and the smaller ${\rm d}\bar{v}_{\rm ds}/{\rm d}t$ are, the smaller $V_{\rm mid}$ will be.

As shown in Fig. 4(b), $C_{\rm gd}$ and $C_{\rm oss}$ ($C_{\rm gd}+C_{\rm ds}$) are approximately connected in parallel at the drain-source side. Hence, ${\rm d}\bar{v}_{\rm ds}/{\rm d}t$ can be represented by the charging speeds of $C_{\rm gd}$ and $C_{\rm oss}$, respectively.

Adopting the charging speed of $C_{\rm gd}$ to indicate ${\rm d}\bar{v}_{\rm ds}/{\rm d}t$**:** The charging speed of $C_{\rm gd}$ is related to $i_{\rm g}$ in the drive loop. $A_{\rm GD}$ is a finite value without Miller plateau. $i_{\rm g}$ will not be fully used to charge $C_{\rm gd}$, so the charging speed of $C_{\rm gd}$ is no longer equal to $i_{\rm g}/C_{\rm gd}$. As shown in Fig. 3(b), based on the Miller's theorem, the equivalent impedance of $C_{\rm gs}$ at the gate-drain end is obtained

$$C_{\rm gd(eq)}=(1+A_{\rm GS})C_{\rm gs}+C_{\rm gd} \tag{3}$$

where $A_{\rm GS}$ is the ratio of the switching rate of drain-source voltage ${\rm d}v_{\rm ds}/{\rm d}t$ to the switching rate of the gate-drain voltage ${\rm d}v_{\rm gd}/{\rm d}t$.

According to the linear decreasing characteristic of $v_{\rm gs}$, the average gate current $\bar{i}_{\rm g}$ can be expressed as

$$\bar{i}_{\rm g}=\frac{\bar{v}_{\rm gs}}{R_{\rm g}}=\frac{(V_{\rm mil}+V_{\rm th})/2-V_{\rm EE}}{R_{\rm g}} \tag{4}$$

where $V_{\rm EE}$ is the negative power supply of the gate driver and $R_{\rm g}$ is the overall gate resistance. Hence, ${\rm d}\bar{v}_{\rm ds}/{\rm d}t$ expressed by the average charging speed of $C_{\rm gd}$ is

$$\frac{{\rm d}\bar{v}_{\rm ds}}{{\rm d}t}=\frac{\bar{i}_{\rm g}}{C_{\rm gd(eq)}}=\frac{\bar{i}_{\rm g}}{(1+A_{\rm GS})C_{\rm gs}+C_{\rm gd}}. \tag{5}$$

Adopting the charging speed of $C_{\rm oss}$ to indicate ${\rm d}\bar{v}_{\rm ds}/{\rm d}t$**:** The charging speed of $C_{\rm oss}$ is related to the load current $I_{\rm L}$ in the power loop. Since the actual current flowing into $C_{\rm oss}$ is $i_{\rm oss}=I_{\rm L}-i_{\rm ch}$, ${\rm d}\bar{v}_{\rm ds}/{\rm d}t$ expressed by the average charging speed of $C_{\rm oss}$ becomes

$$\frac{{\rm d}\bar{v}_{\rm ds}}{{\rm d}t}=\frac{i_{\rm oss}}{C_{\rm oss}}=\frac{I_{\rm L}-\bar{i}_{\rm ch}}{C_{\rm oss}} \tag{6}$$

where $\bar{i}_{\rm ch}$ is the average channel current. Since $I_{\rm L}$ remains unchanged during the turn-OFF process, $\bar{i}_{\rm ch}$ determines ${\rm d}\bar{v}_{\rm ds}/{\rm d}t$. The larger the $\bar{i}_{\rm ch}$ is, the smaller the ${\rm d}\bar{v}_{\rm ds}/{\rm d}t$ will be. Since SiC MOSFETs are in saturation region during the stage of t_1-t_2, $i_{\rm ch}$ is controlled by $v_{\rm gs}$, as [12], [21]

$$i_{\rm ch}=K_{\rm n}(v_{\rm gs}-V_{\rm th})^x \tag{7}$$

where $K_{\rm n}$ is the conductance constant and x is the transfer equation exponent. As $v_{\rm gs}$ decreases linearly from $V_{\rm mil}$ to $V_{\rm th}$,

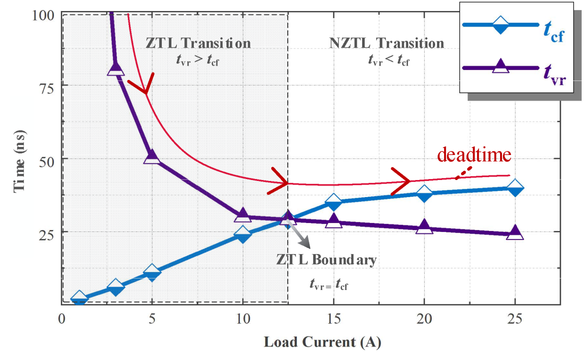


Fig. 7. Relationship between the switching time and $I_{\rm L}$ of SiC MOSFETs.

$\bar{i}_{\rm ch}$ can be further represented as

$$\bar{i}_{\rm ch}=\frac{\int_{V_{\rm th}}^{V_{\rm mil}}K_{\rm n}(v_{\rm gs}-V_{\rm th})^x{\rm d}v_{\rm gs}}{(V_{\rm mil}-V_{\rm th})}=\frac{1}{x+1}I_{\rm L}. \tag{8}$$

Hence, ${\rm d}\bar{v}_{\rm ds}/{\rm d}t$ can also be expressed as

$$\frac{{\rm d}\bar{v}_{\rm ds}}{{\rm d}t}=\frac{(I_{\rm L}-\bar{i}_{\rm ch})}{C_{\rm oss}}=\frac{xI_{\rm L}}{(x+1)C_{\rm oss}}. \tag{9}$$

Equalizing (5) and (9) as

$$\frac{\bar{i}_{\rm g}}{C_{\rm gd(eq)}}=\frac{xI_{\rm L}}{(x+1)C_{\rm oss}}. \tag{10}$$

Combing (3) and (9), the analytical expression of ${\rm d}\bar{v}_{\rm gs}/{\rm d}t$ is

$$\frac{{\rm d}\bar{v}_{\rm gs}}{{\rm d}t}=-\frac{C_{\rm oss}\bar{i}_{\rm g}\,(x+1)-C_{\rm gd}I_{\rm L}x}{C_{\rm oss}\,(x+1)\,(C_{\rm gs}+C_{\rm gd})}. \tag{11}$$

Finally, combining (9) and (11), $V_{\rm mid}$ can be derived as

$$\begin{aligned}V_{\rm mid}=\;&(C_{\rm oss}V_{\rm pin}(x+1)(V_{\rm mil}+V_{\rm th}-2V_{\rm EE})\\&+2I_{\rm L}R_{\rm g}x(V_{\rm mil}-V_{\rm th})(C_{\rm gs}+C_{\rm gd})\\&-2C_{\rm gd}I_{\rm L}R_{\rm g}xV_{\rm pin})/\\&(C_{\rm oss}(x+1)(V_{\rm mil}+V_{\rm th}-2V_{\rm EE})\\&-2C_{\rm gd}I_{\rm L}R_{\rm g}x).\end{aligned} \tag{12}$$

As $V_{\rm mid}$ is a key variable to determine ZTL, three different turning OFF transitions for different $V_{\rm mid}$ will be discussed below.

1) Case 1: $V_{mid} > V_{BUS}$: This case generally occurs under the heavy load, that is, $v_{\rm gs}$ is always greater than $V_{\rm th}$ before $v_{\rm ds}$ rising ends. Therefore, $i_{\rm ch}$ is relatively large and a great amount of turn-OFF loss will be produced. As the solid line (#1) in Fig. 6, SiC MOSFETs can be regarded under non-ZTL (NZTL) transition. The rising speed of drain-source voltage is determined by the charging speed of $C_{\rm gd}$ through $i_{\rm g}$. The turn-OFF speed is relatively fast and the channel current falling time $t_{\rm cf}$ is greater than the drain-source voltage rising time $t_{\rm vr}$, as shown in the white area of Fig. 7. The deadtime in half-bridge circuits should take the higher value of $t_{\rm vr}$ and $t_{\rm cf}$ [28], which will be $t_{\rm cf}$. The deadtime is relatively small in this case

$$E_{\rm NZTL}=\int_{t_1}^{t_3}v_{\rm ds}i_{\rm ch}{\rm d}t\approx\frac{1}{2}V_{\rm BUS}\times I_{\rm L}\times T_{13}\propto I_{\rm L} \tag{13}$$

$$\frac{d\bar{v}_{ds}}{dt} = \frac{\bar{i}_g}{C_{gd(eq)}} \propto \bar{i}_g. \tag{14}$$

2) Case 2: $V_{mid} < V_{BUS}$: If i_{ch} decreases to zero before the end of v_{ds} rising, the overlap area of voltage and current is small, causing small turn-OFF loss, as the point line (#2) in Fig. 6. This case can be considered as ZTL. The rising speed of drain-source voltage is determined by the charging speed of C_{oss} through I_L, and dramatically decreases with the decrease of I_L, as shown in the gray area of Fig. 7. The deadtime in half-bridge circuits is determined by t_{vr} in this case. Longer deadtime will be required. Furthermore, active gate drivers will lost their controllability for switching transient adjustment under this scenario [29]

$$E_{ZTL} = \int_{t_1}^{t_2} v_{ds} i_{ch} dt \approx 0 \tag{15}$$

$$\frac{d\bar{v}_{ds}}{dt} = \frac{x I_L}{(x+1) C_{oss}} \propto I_L. \tag{16}$$

3) Case 3: $V_{mid} = V_{BUS}$: When $V_{mid} = V_{BUS}$, as the dotted line (# 3) in Fig. 6, t_{cf} is the same as t_{vr}. As shown in Fig. 7, this point can be regarded as the boundary of ZTL, defined as ZTL_{bdy}. At ZTL_{bdy}, low turn-OFF loss and small deadtime can be obtained simultaneously. Thus, ZTL_{bdy} is preferable for engineering applications. The load current at this point is defined as $I_{L(CRI)}$, which can be solved by combing (12) and (17)

$$I_{L(CRI)} = K_n (V_{mil} - V_{th})^x. \tag{17}$$

ZTL_{bdy} is employed in the subsequent discussions.

B. Key Parameter Extraction

In order to determine ZTL_{bdy}, it is necessary to extract device-related parameters such as V_{th}, C_{gd}, and C_{oss}. However, due to the inconsistency in testing conditions, large prediction errors will exist for parameters extraction just based on the I-V and C-V curve of datasheets. In order to improve the accuracy of ZTL_{bdy} determining, a more accurate multicurve parameter extraction approach is proposed, which combines C-V curve with the gate charge and transfer characteristic curves, suitable under dynamic switching transitions. SiC device C3M0016120K from Wolfspeed is adopted in this analysis [32].

1) Extraction of C_{gs} and C_{gd}: The C-V curve is tested at $v_{gs} < V_{th}$, corresponding to the cut-OFF state of SiC MOSFETs [18], [30]. However, the device is in the saturation state during v_{ds} rising, which corresponds to $v_{gs} > V_{th}$. As shown in Fig. 8(a), the gate capacitance can be divided into the overlap capacitance C_{ov1} between the gate and the N+ contact, C_{ov2} between the gate and the source metallization, C_{g1} between the gate and the channel, C_{g2} between the gate and the JFET area, the depletion capacitance C_{ch}, and the JFET depletion capacitance C_{JFET} [31]. When SiC MOSFETs is in the cut-OFF state with closed channel, as shown in Fig. 8(b), the gate-source capacitance C_{gs} is formed by the sum of C_{ov1}, C_{ov2} with the series capacitances formed by C_{g1} and C_{ch}. The Miller capacitance C_{gd} is composed by series connection of C_{g2} and C_{JFET}. When the channel is formed, C_{ch} disappears and inversion layer resistance R_{ch} is formed. C_{g1} is transformed into a portion of C_{gd}. Therefore, a portion of

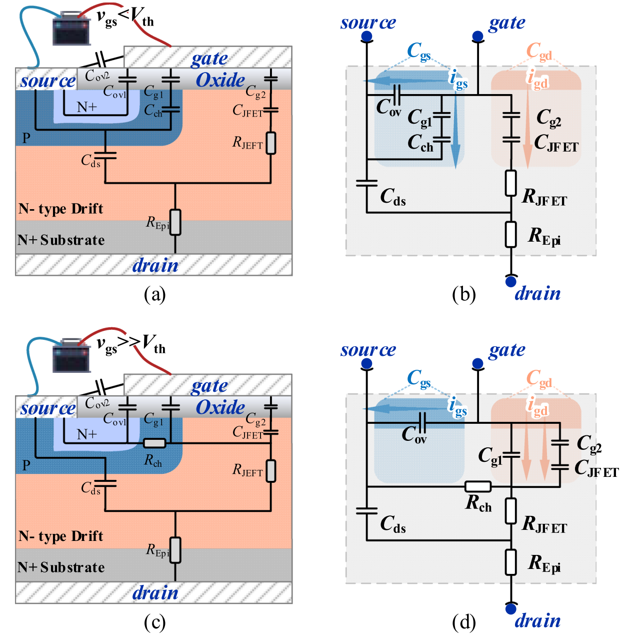


Fig. 8. Detailed schematics of SiC MOSFET and corresponding equivalent small signal circuits for channel not being formed ($v_{gs} < V_{th}$) (a), (b) and channel being formed ($v_{gs} > V_{th}$) (c), (d).

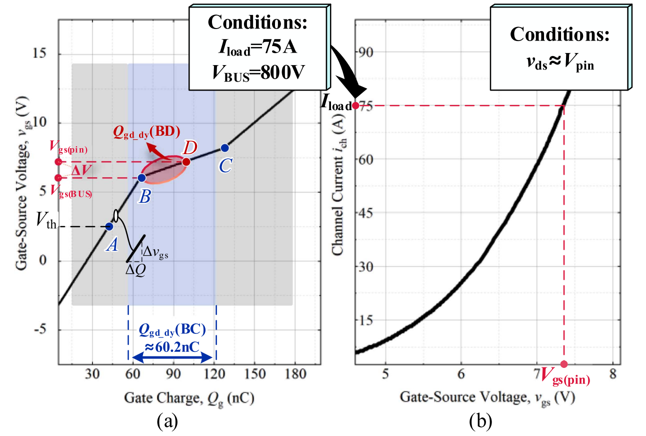


Fig. 9. (a) Gate charge characteristics curve and (b) transfer characteristic curve from Wolfspeed C3M0016120K datasheet.

gate current i_{gs} will flow into C_{gd}, making the dynamic Miller charge Q_{gd_dy} increase. C_{gs} and C_{gd} become larger than those in cut-OFF state. Therefore, the actual dv_{ds}/dt will be slower than the predicted results with parasitic capacitor extracted from the C-V curve, resulting in large prediction errors of the boundary point ZTL_{bdy}. To accurately extract C_{gs} and C_{gd}, the gate charge and transfer characteristic curves are combined with the C-V curve to compensate the dynamic Miller charge effect.

The gate charge characteristics curve is recorded at the actual switching process of the power device. Therefore, the dynamic changes of C_{gs} and C_{gd} after channel being formed can be predicted. As shown in Fig. 9(a), line AB corresponds to i_{ch} falling stage and line BC corresponds to v_{ds} rising stage in the turn-OFF transition. At the AB stage, the device is turned ON

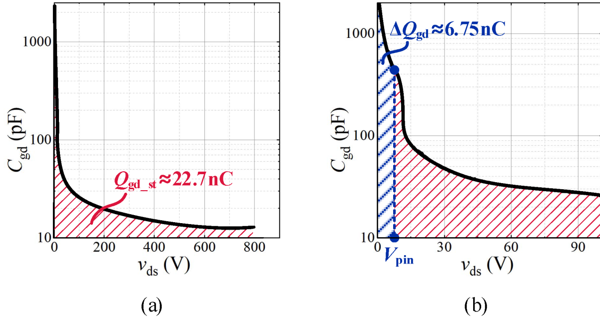


Fig. 10. (a) Static Miller charge $Q_{\mathrm{gd_st}}$ integrated from the C-V curve of the datasheet and (b) the C-V curve highly nonlinear in low voltage region ($V_{\mathrm{ds}} < V_{\mathrm{pin}}$) from Wolfspeed C3M0016120K datasheet.

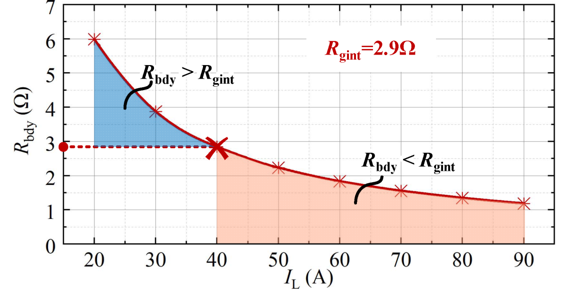


Fig. 11. Required resistance R_{bdy} on $\mathrm{ZTL_{bdy}}$ condition versus I_{L}.

and v_{ds} is at high level, where C_{gd} is negligible and C_{gs} can be approximately solved as

$$C_{\mathrm{gs}} \approx C_{\mathrm{iss}} = \Delta Q_{\mathrm{g}}/\Delta v_{\mathrm{gs}} \tag{18}$$

where C_{iss} is the input capacitance. In line BC stage, the channel has been formed. The dynamic Miller charge $Q_{\mathrm{gd_dy}}(\mathrm{BC})$ calculated for this interval is 60.2 nC from Wolfspeed C3M0016120K datasheet. However, the static Miller charge $Q_{\mathrm{gd_st}}$ obtained by integrating the C-V curve, as shown in Fig. 10(a), is only 22.7 nC. In addition, the line BC stage corresponds to v_{ds} changing from the conduction voltage $V_{\mathrm{ds(on)}}$ to V_{BUS} at turning OFF, while V_{mid} and $I_{\mathrm{L(CRI)}}$ at $\mathrm{ZTL_{bdy}}$ are solved by v_{ds} changing from V_{pin} to V_{BUS}. As ΔQ_{gd} and C_{gd} have large variations in the region of v_{ds} from $V_{\mathrm{ds(on)}}$ to V_{pin}, as shown in Fig. 10(b), larger prediction misalignment will occur if using line BC directly. Alternatively, the gate-source voltage $V_{\mathrm{gs(pin)}}$ at $v_{\mathrm{ds}} \approx V_{\mathrm{pin}}$ can be found on the transfer characteristic curve and marked as point D on the gate charge characteristics curve. Therefore, line BD is adopted to extract $Q_{\mathrm{gd_dy}}$. $Q_{\mathrm{gd_st}}$ is also found by integration of C-V curve from V_{pin} to V_{BUS}. C_{g1} can be extracted by

$$C_{\mathrm{g1}} = \frac{Q_{\mathrm{gd_dy}} - Q_{\mathrm{gd_st}} - C_{\mathrm{gs}}\Delta V}{V_{\mathrm{BUS}} - V_{\mathrm{pin}}} \tag{19}$$

where ΔV is difference between $V_{\mathrm{gs(pin)}}$ and $V_{\mathrm{gs(BUS)}}$. The total C_{gd} can be expressed as the sum of dynamic C_{g1} and static $C_{\mathrm{gd_st}}$

$$C_{\mathrm{gd}} = C_{\mathrm{g1}} + C_{\mathrm{gd_st}} = C_{\mathrm{g1}} + \frac{\int_{V_{\mathrm{pin}}}^{V_{\mathrm{BUS}}} C_{\mathrm{gd_st}} \mathrm{d}v_{\mathrm{ds}}}{V_{\mathrm{BUS}} - V_{\mathrm{pin}}}. \tag{20}$$

2) Extraction of Transfer Equation Exponent x: Another important parameter is the transfer characteristic, which determines i_{ch} dropping rate during SiC MOSFETs turning OFF. The traditional method directly extracts transfer function from the I-V curve in the datasheets, but the I-V curve is measured at low v_{ds} at around 20 V, with large deviation from actual switching conditions. At high v_{ds}, the DIBL effect will cause V_{th} to decrease and actual i_{ch} becomes larger than that at low v_{ds}. It will make the predicted i_{ch} falling speed slower than the actual switching process. To obtain more accurate prediction, the transfer characteristic curve combined with the gate charge characteristics curve are adopted to extract x at high v_{ds}.

As shown in Fig. 9(a), point B in the gate charge characteristics curve is the intersection of i_{ch} dropping and v_{ds} rising stages at turning OFF. Moreover, v_{ds} at point B is V_{BUS} and the corresponding i_{ch} and v_{gs} can be found from I_{load} and $V_{\mathrm{gs(BUS)}}$ in the curve. The solution steps are shown as follows:

First, K_{n} and x_{low} at V_{pin} can be obtained by curve fitting of transfer characteristic curve in Fig. 9(b). Next, at $V_{\mathrm{gs(BUS)}}$, by substituting I_{load} and K_{n} into the transfer equation, x_{high} can be obtained. It should be noted that v_{ds} switches from V_{pin} to V_{BUS} during i_{ch} falling interval at $\mathrm{ZTL_{bdy}}$ transition. Hence, x is chosen as the average of x_{low} and x_{high}. The specific solution process is as below:

$$I_{\mathrm{load}} = K_{\mathrm{n}}(V_{\mathrm{gs(BUS)}} - V_{\mathrm{th}})^{x_{\mathrm{high}}} \rightarrow x_{\mathrm{high}} \tag{21}$$

$$x = \frac{x_{\mathrm{low}} + x_{\mathrm{high}}}{2}. \tag{22}$$

In summary, by combing the C-V curve with the gate charge characteristics curve, dynamic C_{gs} and C_{gd} during the turn-OFF process can be accurately extracted. By combining the gate charge characteristics curve with the transfer characteristic curve, the transfer equation exponent x can be accurately extracted. The improvement in parameter extraction will greatly improve the accuracy of solution of $\mathrm{ZTL_{bdy}}$.

III. Different Implementations of ZTL

Different implementations of ZTL will be discussed in this session with pros and cons analyzed. A novel gate current compensated approach, which acquires charge from the power side and feedback to the gate driver side to realize $\mathrm{ZTL_{bdy}}$ and accelerate the drain-source transition speed, is proposed.

A. Gate Current Adjustment: R_g Adjustment

The larger the gate current i_{g} is, the stronger the driving capability and the dropping rate of the channel current i_{ch} will be. Adjusting R_{g} is the most straightforward approach to change i_{g}. According to (12) with $V_{\mathrm{mid}} = V_{\mathrm{BUS}}$, the required R_{bdy} to realize $\mathrm{ZTL_{bdy}}$ is

$$R_{\mathrm{bdy}} = C_{\mathrm{oss}}(x+1)(V_{\mathrm{BUS}} - V_{\mathrm{pin}})(V_{\mathrm{mil}} + V_{\mathrm{th}} - 2V_{\mathrm{EE}})/ \\ (2I_{\mathrm{L}}x(C_{\mathrm{gd}}(V_{\mathrm{BUS}} - V_{\mathrm{pin}}) + (C_{\mathrm{gs}} + C_{\mathrm{gd}})(V_{\mathrm{mil}} - V_{\mathrm{th}}))). \tag{23}$$

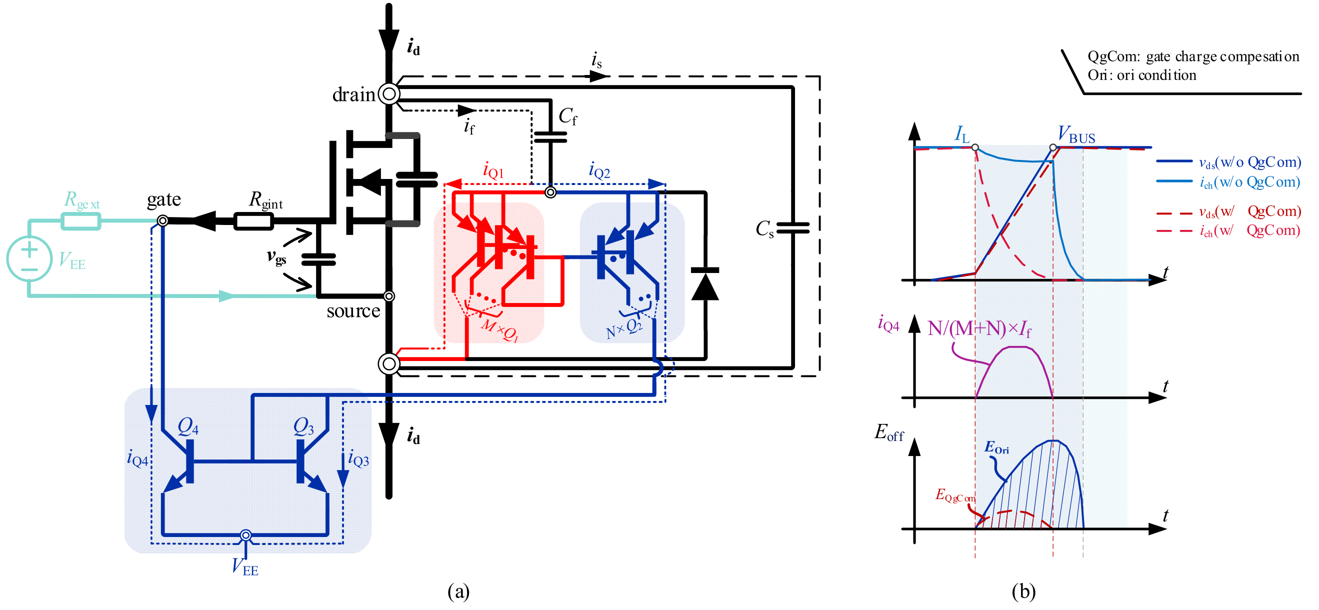


Fig. 12. Gate charge compensation scheme: (a) schematic and (b) main working waveforms.

Fig. 11 shows ZTL_{bdy} required R_{bdy} under different I_{L}. Due to the existence of the overall internal gate resistance R_{gint}, R_{g} adjustment approach has limitations. When $R_{\text{bdy}} < R_{\text{gint}}$, ZTL_{bdy} cannot be achieved. Moreover, too fast gate driving speed will cause severe voltage oscillation and EMI.

B. Channel Current Adjustment: Drain-Source Capacitor Paralleling

The smaller the load current I_{L} is , the slower the $\text{d}v_{\text{ds}}/\text{d}t$ will be. Paralleling extra capacitor C_{ext} at the drain-source terminal of the device will reduce i_{ch} to achieve ZTL_{bdy}. According to (12) with $V_{\text{mid}} = V_{\text{BUS}}$, the required C_{bdy} to realize ZTL_{bdy} is

$$C_{\text{bdy}} = 2I_{\text{L}}R_{\text{g}}x(C_{\text{gs}}V_{\text{mil}} + C_{\text{gd}}(V_{\text{BUS}} - V_{\text{pin}} + V_{\text{mil}} - V_{\text{th}}))/ ((x+1)(V_{\text{BUS}} - V_{\text{pin}})(V_{\text{mil}} - 2V_{\text{EE}} + V_{\text{th}})) - C_{\text{oss}}. \tag{24}$$

However, C_{ext} slows down v_{ds} switching transient, leading to increased deadtime and reduced converter efficiency.

C. Gate Current and Channel Current Coadjustment: Proposed Gate Charge Compensation Approach

To realize wide-range adjustment and avoid slowing down the turning OFF transient, a new scheme based on the gate charge compensation to realize the coadjustment of gate and channel current is proposed.

1) Operation Principle: The main idea of the gate charge compensation is to acquire charge from the power side and send back to the gate side to adjust switching speed. As shown in Fig. 12(a), the shunt capacitor C_{s} and the feedback capacitor C_{f} form paralleled current acquisition branch of I_{L}. I_{f} is extracted from I_{L}, which corresponds to $C_{\text{f}} \times \text{d}\bar{v}_{\text{ds}}/\text{d}t$. I_{f} is further divided into two branches by a current mirror composed of $M+N$ identical PNP bipolar junction transistors (BJTs). The

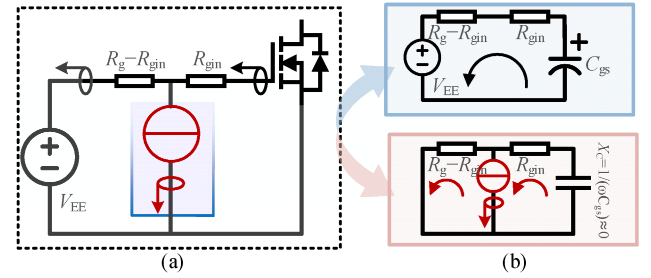


Fig. 13. (a) Drive loop considering the device internal gate resistor R_{gin} and (b) the small signal equivalent circuits.

current branch composed of M parallel PNPs on the left side flows into the power loop through the device's source terminal, while the right branch composed of N parallel PNPs is connected to a current mirror composed of two identical NPNs Q_3 and Q_4. The compensated charge, which flows through Q_4, is fed back to the gate loop to adjust the gate driving speed. The reason to use M and N PNPs is to provide the capability to adjust the charge feeding back to the gate side. As shown in Fig. 12(b), $N/(M+N) \times I_{\text{f}}$ is extracted from the gate side during the $\text{d}v/\text{d}t$ transient, which increases $|\text{d}\bar{v}_{\text{gs}}/\text{d}t|$ and makes i_{ch} drops to zero faster

$$\text{d}\bar{v}_{\text{gs}}/\text{d}t = -\frac{C_{\text{oss}}(x+1)(\bar{i}_{\text{g}} + I_{\text{f}}/2) - C_{\text{gd}}I_{\text{L}}x}{C_{\text{oss}}(x+1)(C_{\text{gs}} + C_{\text{gd}})}. \tag{25}$$

2) Parameter Design: In the proposed gate charge compensation approach, C_{s} is determined by ZTL boundary point ZTL_{bdy}. C_{f}, M, and N determine the compensated gate charge and v_{ds} rising speed. In addition, the influence of device internal resistor also needs to be considered. As shown in Fig. 13, the current mirror is equivalent to a current source. Using the superposition theorem and Kirchhoff's law, the actual current

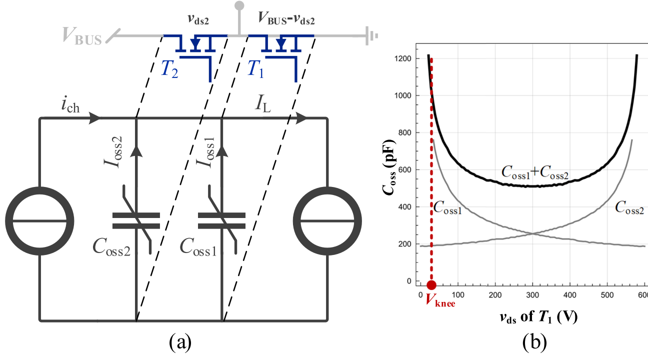


Fig. 14. (a) Equivalent circuit of the half-bridge circuit during the voltage transient of T_2 and (b) the nonlinear characteristic of the junction capacitance C_{oss} in the half-bridge circuit.

flowing into C_{gs} is

$$\frac{(R_{\text{g}}-R_{\text{gin}})NI_{\text{f}}}{(R_{\text{g}}+X_{\text{C}})\,(M+N)}\approx\frac{(R_{\text{g}}-R_{\text{gin}})NI_{\text{f}}}{R_{\text{g}}\,(M+N)} \tag{26}$$

where R_{gin} is the device internal resistor and X_{C} is the impedance of C_{gs}. Therefore, under the required $\mathrm{d}\bar{v}_{\text{ds}}/\mathrm{d}t$, with (25) and (2), C_{s} and C_{f} at ZTL$_{\text{bdy}}$ can be obtained as

$$\begin{aligned}C_{\text{f}}=&\frac{M+N}{2N}((V_{\text{BUS}}-V_{\text{pin}})(V_{\text{mil}}+V_{\text{th}}-2V_{\text{EE}})\\&+2C_{\text{gd}}R_{\text{g}}\mathrm{d}\bar{v}_{\text{ds}}/\mathrm{d}t(V_{\text{pin}}-V_{\text{BUS}}-V_{\text{mil}}+V_{\text{th}})\\&+2C_{\text{gs}}R_{\text{g}}\mathrm{d}\bar{v}_{\text{ds}}/\mathrm{d}t(-V_{\text{mil}}+V_{\text{th}}))/\\&(\mathrm{d}\bar{v}_{\text{ds}}/\mathrm{d}t(R_{\text{gin}}-R_{\text{g}})(V_{\text{BUS}}-V_{\text{pin}}))\end{aligned} \tag{27}$$

$$C_{\text{s}}=I_{\text{L}}x/((x+1)\mathrm{d}\bar{v}_{\text{ds}}/\mathrm{d}t)-C_{\text{oss}}-C_{\text{f}}. \tag{28}$$

It can be seen that the feedback compensated charge from the power side increases the gate current driving capability during the $\mathrm{d}v/\mathrm{d}t$ interval.

D. Applications in the Half-Bridge Circuit

Fig. 14(a) shows the equivalent circuit of the half-bridge circuit. When T_2 is turning OFF, its junction capacitance C_{oss2} will be charged with the junction capacitance C_{oss1} of T_1 discharged. The discharging of C_{oss1} and charging of C_{oss2} have the same absolute value of $\mathrm{d}v_{\text{ds}}/\mathrm{d}t$. Therefore, the actual junction capacitance adopted in the above model in the half-bridge circuit should include the junction capacitances of T_1 and T_2 in parallel, as $C_{\text{oss1}}+C_{\text{oss2}}$.

In addition, shown in Fig. 14(b), C_{oss} varies greatly in the low-voltage and high-voltage regions [12]. Here, V_{knee} is defined at around 10–20 V, and the extraction of equivalent capacitance for T_2 at the half-bridge circuit can be defined as

$$C_{\text{oss(eq)}}=\frac{\int_{V_{\text{pin}}}^{V_{\text{BUS}}-V_{\text{knee}}}C_{\text{oss2}}\mathrm{d}v_{\text{ds}}+\int_{V_{\text{knee}}}^{V_{\text{BUS}}-V_{\text{pin}}}C_{\text{oss1}}\mathrm{d}v_{\text{ds}}}{V_{\text{BUS}}-V_{\text{knee}}-V_{\text{pin}}}. \tag{29}$$

Therefore, C_{oss} in (12), (23), (24), and (28) needs to be replaced by $C_{\text{oss(eq)}}$ in (29) in the half-bridge circuit.

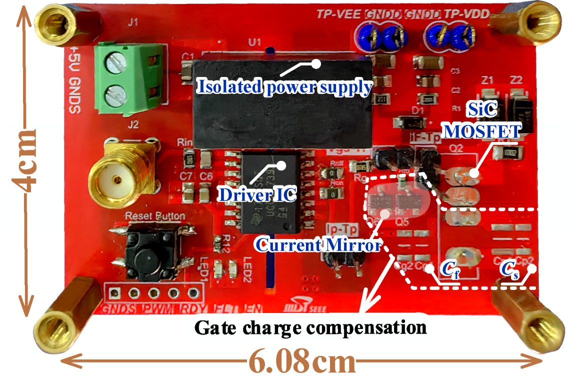


Fig. 15. Designed gate driver prototype with the gate charge compensation.

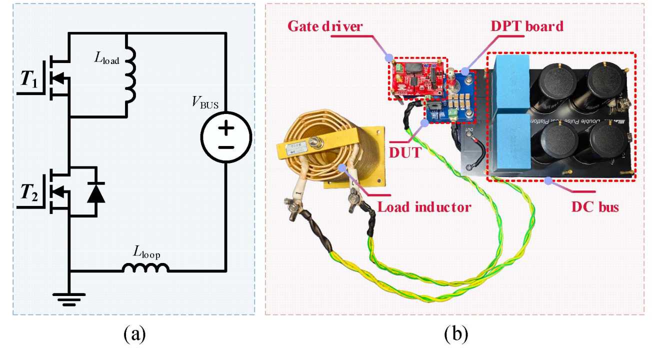


Fig. 16. (a) Schematic and (b) DPT testing platform used in the experiment.

IV. Prototype and Experimental Verification

The prototype of the gate driver with the proposed gate charge compensation is shown in Fig. 15. The isolated power supply is MGJ2D052005SC and the gate driver is UCC21739QDWQ1. NPN and PNP BJTs selected for the gate feedback current mirrors are 2SD2657 and 2SB1695, respectively. As shown in Fig. 16, the double pulse test (DPT) platform is adopted to verify the ZTL determination and realization approaches with SiC MOSFET C3M0016120K employed.

Oscilloscope MSO56 from Tektronix is employed. Drain-to-source voltage v_{ds} is measured by the high-voltage differential probe THDP0200 and drain current i_{d} is measured by the high-bandwidth (2 GHz) current shunt resistor SDN-414-10 from T&M research. The gate loop and power loop stray inductances are measured as 17.1 nH and 45.3 nH, respectively, by impedance analyzer. The extracted C_{gs} is 6537 pF, C_{gd} is 20.44 pF, x_{low} is 3.31, x_{high} is 3.90, and x is 3.61, as shown in Table I using the methods discussed in Section II-B.

A. Verification of ZTL Determining Criterion

The verification of ZTL determination includes the verification of the parameter extraction and the verification of the ZTL boundary point. First, the verification of the parameter extraction is through the comparison of switching transient waveforms with the numerical simulation results [11], which are drawn both with device parameters extracted by traditional parameters extraction

TABLE I
PARAMETERS AND PARASITIC VALUES OF THE DPT CIRCUIT

	Parameter	Value
Power stage	V_{BUS}	600 V
Gate driver	R_{gext}	9.1 Ω
	V_{CC}	15 V
	V_{EE}	-5 V
SiC MOSFETs	$R_{ds(on)}$	16 mΩ
	R_{gint}	(2.6+0.3) Ω
	Extracted C_{gs}	6537 pF
	Extracted C_{gl}	20.44 pF
	Extracted x	3.61

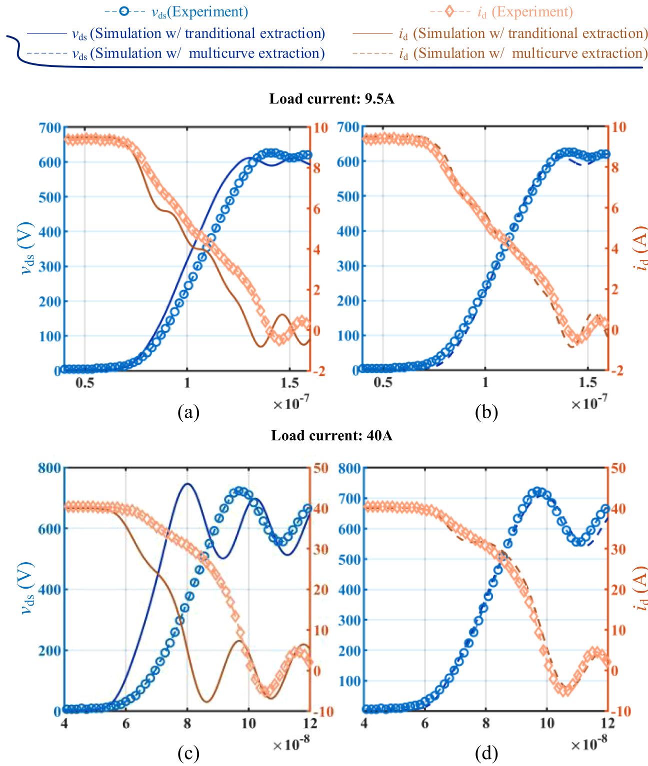
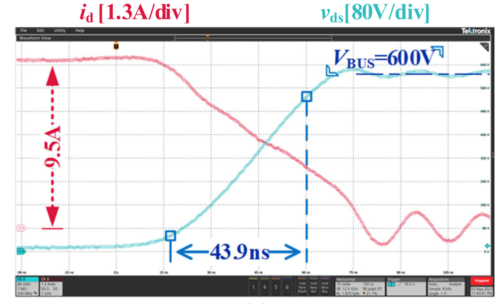
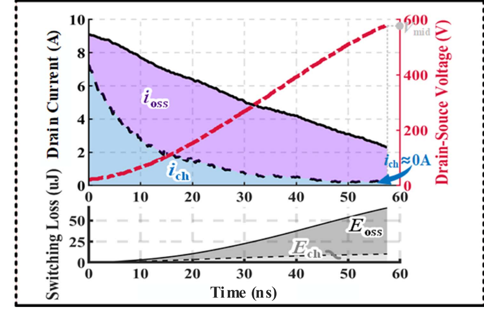


Fig. 17. Comparison of simulated and experimental v_{ds} and i_d waveforms. (a) With traditional parameter extraction and (b) with multicurve parameter extraction at $I_L = 9.5$ A; (c) with traditional parameter extraction and (d) with multicurve parameter extraction at $I_L = 40$ A.



(a)



(b)

Fig. 18. Experimental waveforms at measured critical load current $I_{L(cri_mea)}$ of 9.5 A: (a) original waveforms and (b) waveforms with extracted i_{ch}.

approach and the proposed multicurve parameter extraction approach. Fig. 17 shows transient waveforms of v_{ds}, i_d of the turn-OFF transient at 9.5 and 40 A, respectively. The predicted v_{ds} adopting traditional parameter extraction falls much faster compared to the experiment results, especially at large I_L. Under 40 A load current, the measured turn-OFF dv/dt is 26.0 V/ns, while the predicted result with traditional parameter extraction approach is 35.0 V/ns with mismatch error of 34.5%. The predicted dv/dt with proposed multicurve parameter extraction approach is 25.1 V/ns with mismatch error of 3.5%. Therefore, the extracted parameter by proposed approach shows good consistency with the actual dynamic characteristic of SiC device.

The measured critical load current $I_{L(cri_mea)} = I_{L(CRI)}$ at ZTL$_{bdy}$ is compared with the calculation value $I_{L(cri_cal)}$ to verify the accuracy of the proposed ZTL determining criterion. As the device's i_{ch} is essential and cannot be directly measured, i_{ch} is calculated from the measured of v_{ds} and i_d, as follows:

$$i_{ch} = i_d - (C_{oss} + C_{ext})\frac{dv_{ds}}{dt}. \tag{30}$$

In this experiment, $I_{L(cri_mea)}$ is measured to be 9.5 A and its corresponding turn-OFF waveforms are shown in Fig. 18(a). The waveform with extracted i_{ch} is shown in Fig. 18(b), and i_{ch} corresponding to $v_{ds} = V_{mid} = V_{BUS} - V_{knee}$ with $V_{knee} = 20$V is zero. This confirms the determination of $I_{L(CRI)}$ is accurate. t_{vr} from 10% to 90% V_{BUS} is measured to be 43.9 ns, and the turn-OFF loss is calculated to be 10.2 μJ.

By adopting (12) with $V_{mid} = V_{BUS} - V_{knee}$ and (17) with the extracted device's parameters, the theoretical calculation of the critical load current $I_{L(cri_cal)}$ is 10.4 A. The turn-OFF waveforms at $I_{L(cri_cal)}$ are shown in Fig. 19(a), and t_{vr} is 40.7 ns. Fig. 19(b) shows the waveform with extracted i_{ch} and i_{ch} corresponding to $v_{ds} = V_{mid}$ is 0.13 A, close to zero. Hence, the proposed quantitative model of ZTL$_{bdy}$ is verified with prediction error of 9.5%, calculated as

$$\text{error} = \left|\frac{I_{L(cri_cal)} - I_{L(cri_mea)}}{I_{L(cri_mea)}}\right| \times 100\%. \tag{31}$$

The predictions of the critical load current are compared with state-of-art approaches, including the method considering no Miller plateau but with traditional parameter extraction and the method based on the analytical model [12], [13] considering Miller plateau but with the multicurve parameter extraction proposed in Section II-B. The predicted critical load currents

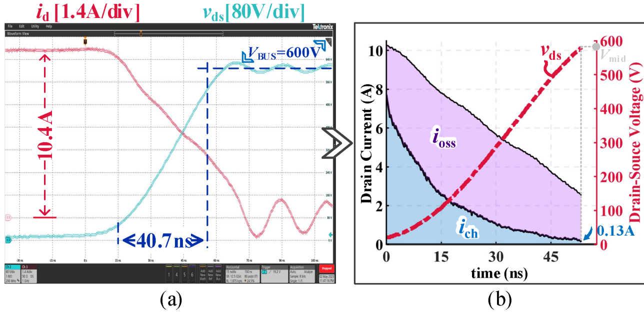


Fig. 19. Experimental waveforms at calculated critical load current $I_{L(\mathrm{cri_cal})}$ of 10.4 A: (a) original waveforms and (b) waveforms with extracted i_{ch}.

TABLE II
COMPARISON OF DIFFERENT METHODS OF ZTL DETERMINATION

Turn-OFF ZTL Determining Methods	Actual critical load current	Predicted critical load current	error
Proposed Method w/ Multicurve Extraction	9.5 A	10.4 A	9.5%
Proposed Method w/ Traditional Extraction	9.5 A	14.4 A	51.6%
Analytical Model w/ Multicurve Extraction	9.5 A	20.1 A	111.6%

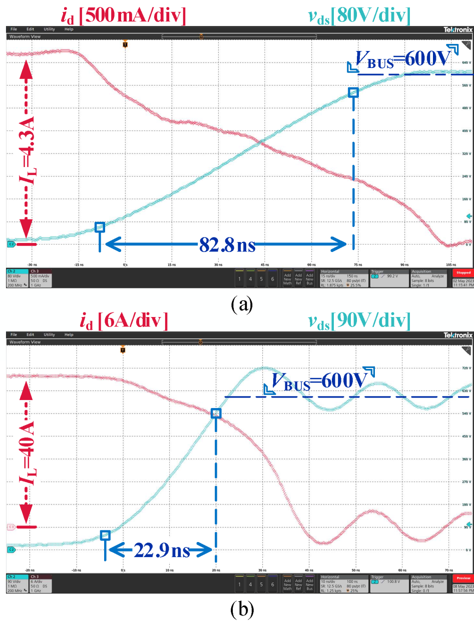


Fig. 20. Measured turn-OFF waveforms at different I_L: (a) I_L of 5.6 A and (b) I_L of 40 A.

of the above two methods are 14.4 A and 20.1 A, respectively. Experimental data are summarized as Table II. The predicted error of the traditional analytical model reaches 111.6%, while the ZTL determination criterion proposed in this article has the smallest error of only 9.5%.

The switching characteristics under different load currents are further compared. At I_L= 5.6 A, SiC device is at ZTL transition as plotted in Fig. 20(a). t_{vr} is measured as 68.7 ns, which is 56.5%

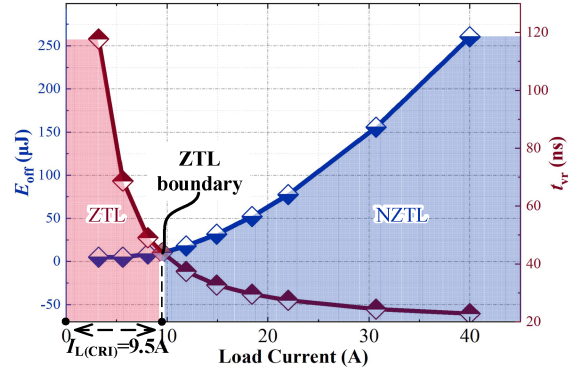


Fig. 21. Turn-OFF loss E_{off} and drain-source voltage rising time t_{vr} under different load currents.

TABLE III
DESIGN PARAMETERS OF ZTL IMPLEMENTATION METHODS

Load current	I_L (A)	40	50	60
R_g adjustment	R_g (Ω)	2.84	2.23	1.83
Drain-source capacitor paralleling	C_{ext} (pF)	2780	3770	4780
Gate charge compensation	C_s (pF)	566	950	1342
	C_f (pF)	133	142	147

higher than the condition with $I_L = I_{L(\mathrm{CRI})}$. When $I_L = 40$ A, the SiC device turns OFF at NZTL transition shown in Fig. 20(b). The calculated turn-OFF loss is 260.5 μJ, which is 24 times higher than that at $I_L = I_{L(\mathrm{CRI})}$. Fig. 21 summarizes the turn-OFF loss and t_{vr} under different I_L. It can be seen that the turn-OFF loss hardly changes with I_L less than $I_{L(\mathrm{CRI})}$, and increases rapidly when I_L is high than $I_{L(\mathrm{CRI})}$. On the other hand, t_{vr} is reversely proportional to I_L. Therefore, the ZTL boundary point is the optimal point considering both the low turn-OFF loss and fast turn-OFF speed.

B. Verification of ZTL Implementations

Three different ZTL implementation methods are verified, including R_g adjustment, drain-source capacitor paralleling, and gate charge compensation. Three approaches are compared at I_L ranging from 40 A to 60 A. $\mathrm{d}\bar{v}_{ds}/\mathrm{d}t$ is set to 20 V/ns for the experiment with the gate charge compensation. The boundary point of ZTL is selected as the operation point and the design parameters are summarized in Table III. The overall internal gate resistor R_{gint} is 2.9 Ω, which is composed by the internal 2.6 Ω gate resistor R_{gin} of SiC C3M0016120K with the internal 0.3 Ω pulldown resistance of the gate driver IC UCC21739QDWQ1. $\mathrm{ZTL_{bdy}}$ can only be achieved through R_g adjustment when the required gate resistor is larger than R_{gint}. However, according to (23), the required R_{bdy} is 2.84 Ω under I_L of 40 A. In this experiment, no external gate resistor is applied.

The transient waveforms during the turn-OFF process under the original circuit at NZTL and the three ZTL implementation methods at $I_L = 40$A are shown in Fig. 22. t_{vr} are 22.9 ns in the original circuit, 9.6 ns in the method of R_g adjustment, 51.4 ns in the drain-source capacitor paralleling approach, and 25.0 ns in

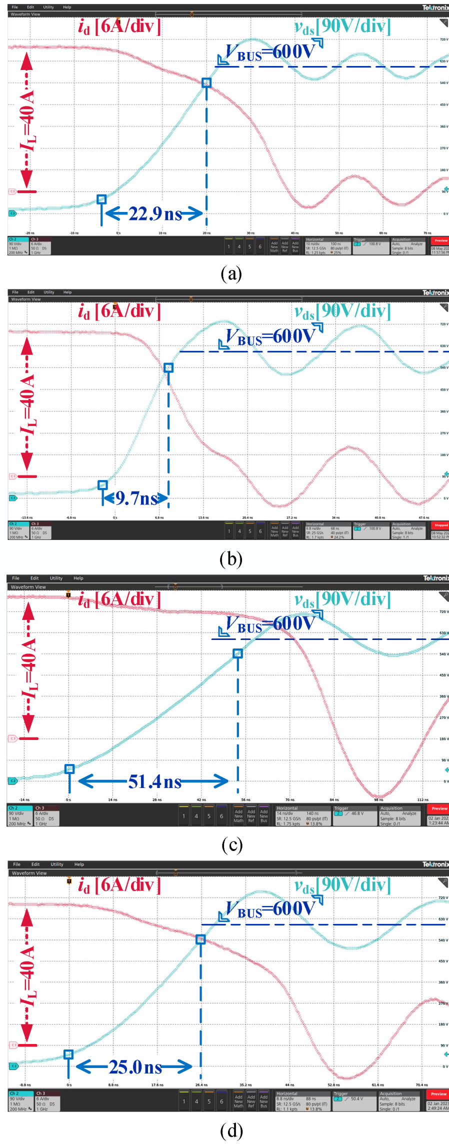


Fig. 22. Measured turn-OFF waveforms at $I_L = 40$ A for (a) the original circuit under NZTL, and the three ZTL implementations with (b) the R_g adjustment, (c) drain-source capacitor paralleling, and (d) gate charge compensation approach.

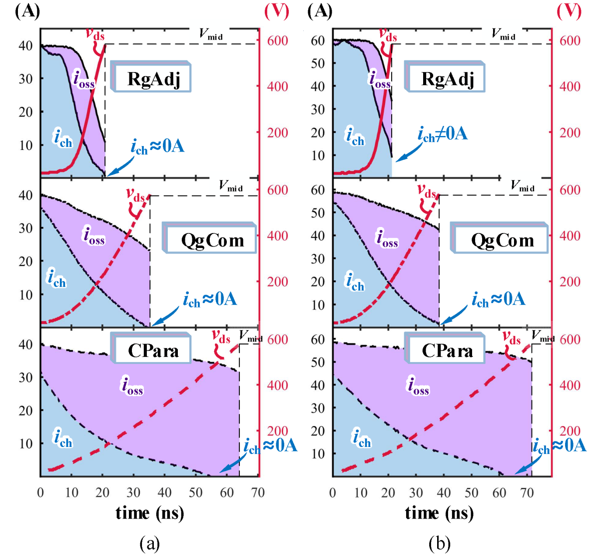


Fig. 23. Extracted waveforms of the methods of R_g adjustment, drain-source capacitor paralleling, and gate current compensation are compared under different I_L. (a) $I_L = 40$ A. (b) $I_L = 60$ A.

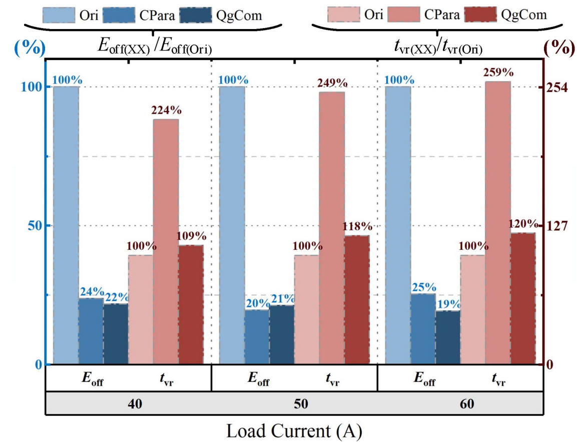


Fig. 24. Comparison of the turn-OFF loss E_{off} and the drain-source voltage rise time t_{vr} in the original circuit and different ZTL implementation methods.

the gate charge compensation approach. The turn-OFF transients with calculated i_{ch} are further plotted in Fig. 23 at two different I_L, where the subscripts "RgAdj" corresponds to R_g adjustment, "CPara" corresponds to drain-source capacitor paralleling, and "QgCom" corresponds to gate current compensation. It can be seen that i_{ch} corresponding to $v_{ds} = V_{mid}$ is close to zero under all the three methods at $I_L = 40$ A, proving the accuracy of the parameters design for achieving $\mathrm{ZTL_{bdy}}$ transition. However, at I_L of 60 A, ZTL is not achieved under R_g adjustment due to the required gate resistor smaller than the overall internal gate resistor.

Fig. 24 further gives the comparison of the turn-OFF loss and t_{vr} among the original circuit (Ori) and ZTL implementations under different I_L. As the R_g adjustment approach fails to achieve ZTL under all the three current levels, this method is not taken for comparison. The turn-OFF loss E_{off} and t_{vr} are normalized to the value of the original circuit for a fair comparison. It can be observed that E_{off} is greatly reduced when working under ZTL. The turn-OFF losses with drain-source capacitor paralleling are 24%, 20%, and 25% of the original circuit at I_L of 40, 50, and 60 A, respectively. The turn-OFF losses with the proposed gate charge compensation approach are 22%, 21%, and 19% of the original circuit, respectively. The two implementations have almost the same effect for turn-OFF loss reduction. For t_{vr}, the method of drain-source capacitor paralleling causes 159% increasement compared with the original circuit, while the maximum increasement in t_{vr} is only 20% for the gate charge compensation approach at $I_L = 60$ A. Compared with capacitor paralleling, the drain-source voltage rising time of gate charge compensation is decreased up to 52.6% at almost same turn-OFF energy reduction at I_L= 50 A. From all the above, the superiority of the proposed gate charge compensation approach is verified.

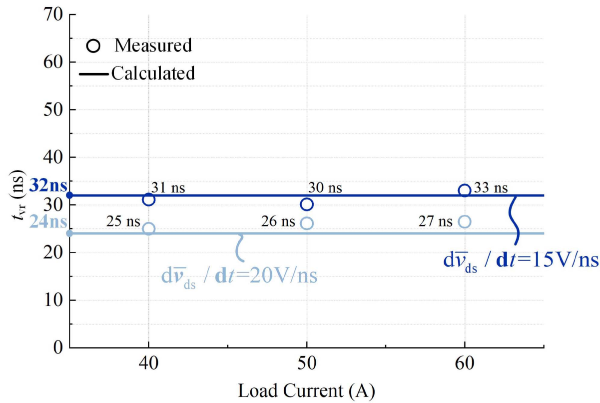


Fig. 25. Comparison of the drain-source voltage rising time t_{vr} between the theoretical calculations and experimental measurements.

To illustrate the capability of turn-OFF speed control of the proposed gate charge compensation approach at ZTL_{bdy}, $d\bar{v}_{ds}/dt$ is further set to be 15 V/ns. Fig. 25 compares the theoretical calculation and experimental results of t_{vr} for $d\bar{v}_{ds}/dt$ of 15 V/ns and 20 V/ns, respectively. The average errors between theoretical values and measurement results for $d\bar{v}_{ds}/dt$ of 15 V/ns and 20 V/ns are 4.1% and 7.2%, respectively, indicating its ability of accurate speed control at ZTL_{bdy}.

V. Conclusion

A quantitative determination of ZTL and its boundary condition for SiC MOSFETs considering no Miller plateau is first revealed in this article. Different from the conventional turn-OFF transient, ZTL is analyzed with no Miller plateau. The association of the gate-source voltage and drain-source voltage at the turn-OFF transient based on the Miller's theorem is derived for the determining criterion of ZTL. The ZTL boundary (ZTL_{bdy}) is further defined as the optimal point of low turn-OFF loss and high dv/dt.

In addition, the differences in testing conditions between datasheets and the actual switching process will lead to large parameter extraction errors. To solve this problem, a multicurve parameter extraction approach combing the C-V curve with the gate charge and the transfer characteristic curves is formed to extract device's dynamic parasitic capacitors and transfer characteristic. It helps to further improve the accuracy of ZTL determining.

A novel ZTL implementation based on the gate charge compensation with adjustable high turn-OFF speed is first proposed in this article. A parallel capacitor branch is added to the drain-source terminal of the device for charge extraction and current mirrors are used to control the feedback charge to the gate loop.

Experiments have verified the accuracy of the proposed determination and implementation of ZTL. The prediction error of the ZTL boundary point is less than 9.5% and the proposed ZTL implementation can reduce the turn-OFF loss up to 81% with only 20% increasement in turn-OFF time at ZTL_{bdy} in comparison to the origin circuit. Moreover, compared with capacitor paralleling at same turn-OFF energy reduction, the proposed approach achieves 52.6% reduction in drain-source voltage rising time t_{vr}. Finally, the adjustment error of t_{vr} at ZTL_{bdy} is verified to be less than 7.2%.

References

[1] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, May 2014, doi: 10.1109/TPEL.2013.2268900.

[2] S. Hazra et al., "High switching performance of 1700-V, 50-A SiC power MOSFET over Si IGBT/BiMOSFET for advanced power conversion applications," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4742–4754, Jul. 2016, doi: 10.1109/TPEL.2015.2432012.

[3] M. Mu and F. C. Lee, "Comparison and optimization of high frequency inductors for critical model GaN converter operating at 1MHz," in *Proc. Int. Power Electron. Appl. Conf. Expo.*, 2014, pp. 1363–1368.

[4] Wolfspeed, *C3M0015065K Silicon Carbide Power MOSFET C3MTM MOSFET Technology, Datasheet Rev. 6*, Mar. 2022. [Online]. Available: https://assets.wolfspeed.com/uploads/2020/12/C3M0015065K.pdf

[5] B. Nguyen, X. Zhang, A. Ferencz, T. Takken, R. Senger, and P. Coteus, "Analytic model for power MOSFET turn-off switching loss under the effect of significant current diversion at fast switching events," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2018, pp. 287–291, doi: 10.1109/APEC.2018.8341024.

[6] X. Li et al., "Switching loss model of SiC MOSFET promoting high frequency applications," in *Proc. 31st Int. Symp. Power Semicond. Devices ICs*, 2019, pp. 231–234, doi: 10.1109/ISPSD.2019.8757669.

[7] H. Wen, D. Jiao, C.-S. Yeh, and J.-S. Lai, "Channel turn-off energy model for zero-voltage-switching wide bandgap devices," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 4, pp. 4016–4025, Aug. 2021, doi: 10.1109/JESTPE.2020.2980216.

[8] X. Li, L. Zhang, S. Guo, Y. Lei, A. Q. Huang, and B. Zhang, "Understanding switching losses in SiC MOSFET: Toward lossless switching," in *Proc. IEEE 3rd Workshop Wide Bandgap Power Devices Appl.*, 2015, pp. 257–262, doi: 10.1109/WiPDA.2015.7369295.

[9] X. Li et al., "Achieving zero switching loss in silicon carbide MOSFET," *IEEE Trans. Power Electron.*, vol. 34, no. 12, pp. 12193–12199, Dec. 2019, doi: 10.1109/TPEL.2019.2906352.

[10] Y. Xie, Y. Yan, S. Luan, C. Chen, and Y. Kang, "Turn-off period improved switching model of SiC devices with stray capacitances and inductances," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2019, pp. 3229–3234, doi: 10.1109/ECCE.2019.8912570.

[11] Y. Xie, C. Chen, Y. Yan, Z. Huang, and Y. Kang, "Investigation on ultralow turn-off losses phenomenon for SiC MOSFETs with improved switching model," *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 9382–9397, Aug. 2021, doi: 10.1109/TPEL.2021.3050544.

[12] D. Christen and J. Biela, "Analytical switching loss modeling based on datasheet parameters for MOSFETs in a half-bridge," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3700–3710, Apr. 2019, doi: 10.1109/TPEL.2018.2851068.

[13] A. Hu and J. Biela, "Evaluation of the I_{max}-f_{sw}-dv/dt trade-off of high voltage SiC MOSFETs based on an analytical switching loss model," in *Proc. 22nd Eur. Conf. Power Electron. Appl.*, 2020, pp. P.1–P.11, doi: 10.23919/EPE20ECCEEurope43536.2020.9215911.

[14] Y. Xiong, S. Sun, H. Jia, P. Shea, and Z. John Shen, "New physical insights on power MOSFET switching losses," *IEEE Trans. Power Electron.*, vol. 24, no. 2, pp. 525–531, Feb. 2009, doi: 10.1109/TPEL.2008.2006567.

[15] K. Peng, S. Eskandari, and E. Santi, "Analytical loss model for power converters with SiC MOSFET and SiC schottky diode pair," in *Proc. IEEE Energy Conv. Congr. Expo.*, 2015, pp. 6153–6160, doi: 10.1109/ECCE.2015.7310522.

[16] X. Wang, Z. Zhao, K. Li, Y. Zhu, and K. Chen, "Analytical methodology for loss calculation of SiC MOSFETs," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 1, pp. 71–83, Mar. 2019, doi: 10.1109/JESTPE.2018.2863731.

[17] S. K. Roy and K. Basu, "Analytical estimation of turn on switching loss of SiC MOSFET and Schottky diode pair from datasheet parameters," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 9118–9130, Sep. 2019, doi: 10.1109/TPEL.2018.2889342.

[18] R. Stark, A. Tsibizov, N. Nain, U. Grossner, and I. Kovacevic-Badstuebner, "Accuracy of three interterminal capacitance models for SiC power MOSFETs under fast switching," *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 9398–9410, Aug. 2021, doi: 10.1109/TPEL.2021.3053330.

[19] T. Basler, D. Heer, D. Peters, T. Aichinger, and R. Schoerner, "Practical aspects and body diode robustness of a 1200 V SiC trench MOSFET," in *Proc. Eur. Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, 2018, pp. 1–7.

[20] P. Hofstetter, R. W. Maier, and M.-M. Bakran, "Influence of the threshold voltage hysteresis and the drain induced barrier lowering on the dynamic transfer characteristic of SiC power MOSFETs," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2019, pp. 944–950, doi: 10.1109/APEC.2019.8721772.

[21] Z. Dong, X. Wu, H. Xu, N. Ren, and K. Sheng, "Accurate analytical switching-on loss model of SiC MOSFET considering dynamic transfer characteristic and $\mathrm{Q_{gd}}$," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 12264–12273, Nov. 2020, doi: 10.1109/TPEL.2020.2988899.

[22] P. Yang, W. Ming, J. Liang, I. Lüdtke, S. Berry, and K. Floros, "Hybrid data-driven modeling methodology for fast and accurate transient simulation of SiC MOSFETs," *IEEE Trans. Power Electron.*, vol. 37, no. 1, pp. 440–451, Jan. 2022, doi: 10.1109/TPEL.2021.3101713.

[23] H. Sakairi, T. Yanagi, H. Otake, N. Kuroda, and H. Tanigawa, "Measurement methodology for accurate modeling of SiC MOSFET switching behavior over wide voltage and current ranges," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7314–7325, Sep. 2018, doi: 10.1109/TPEL.2017.2764632.

[24] A. Hu and J. Biela, "An analytical switching loss model for a SiC MOSFET and Schottky diode half-bridge based on nonlinear differential equations," in *Proc. 23rd Eur. Conf. Power Electron. Appl.*, 2021, pp. P.1–P.11, doi: 10.23919/EPE21ECCEEurope50061.2021.9570661.

[25] J. M. Miller, "Dependence of the input impedance of a three-electrode vacuum tube upon the load in the plate circuit," *Sci. Papers Bur. Standards*, vol. 15, no. 351, pp. 367–385, 1920.

[26] B. Agrawal, M. Preindl, B. Bilgin, and A. Emadi, "Estimating switching losses for SiC MOSFETs with non-flat miller plateau region," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2017, pp. 2664–2670, doi: 10.1109/APEC.2017.7931075.

[27] C. Li et al., "Analytical model and design of voltage balancing parameters of series-connected SiC MOSFETs considering non-flat miller plateau of gate voltage," *Energies*, vol. 15, no. 5, Feb. 2022, Art. no. 1722, doi: 10.3390/en15051722.

[28] Z. Zhang, H. Lu, D. J. Costinett, F. Wang, L. M. Tolbert, and B. J. Blalock, "Model-based dead time optimization for voltage-source converters utilizing silicon carbide semiconductors," *IEEE Trans. Power Electron.*, vol. 32, no. 11, pp. 8833–8844, Nov. 2017, doi: 10.1109/TPEL.2016.2645578.

[29] J. Cao, Z.-K. Zhou, Y. Shi, and B. Zhang, "On-chip active turn-off driving technique to prevent channel current from disappearing prematurely in SiC MOSFET's applications," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 70, no. 2, pp. 660–664, Feb. 2023, doi: 10.1109/TCSII.2022.3213556.

[30] N. Phankong, T. Funaki, and T. Hikihara, "Characterization of the gate-voltage dependency of input capacitance in a SiC MOSFET," *IEICE Electron. Exp.*, vol. 7, no. 7, pp. 480–486, Apr. 2010, doi: 10.1587/elex.7.480.

[31] R. Stark, A. Tsibizov, I. Kovacevic-Badstuebner, T. Ziemann, and U. Grossner, "Gate capacitance characterization of silicon carbide and silicon power MOSFETs revisited," *IEEE Trans. Power Electron.*, vol. 37, no. 9, pp. 10572–10584, Sep. 2022, doi: 10.1109/TPEL.2022.3164360.

[32] Wolfspeed, *C3M0016120K Silicon Carbide Power MOSFET C3MTM MOSFET Technology, Datasheet Rev.*, 2019. [Online]. Available: https://assets.wolfspeed.com/uploads/2020/12/C3M0016120K.pdf

Shijie Song (Graduate Student Member, IEEE) received the B.S. degree in electrical engineering from Southwest Jiaotong University, Chengdu, China, in 2022. He is currently working toward the Ph.D. degree with the School of Electrical and Electronic Engineering, Huazhong University of Science and Technology, Wuhan, China.

His current research interests include high-frequency, high power-density gate driver, switching behavior modeling and applications of wide-bandgap power devices.

Han Peng (Senior Member, IEEE) received the B.S. degree from Southeast University, Nanjing, China, and the Ph.D. degree from Rensselaer Polytechnic Institute, Troy, NY, USA, in 2006 and 2011, respectively, all in electrical engineering.

From 2011 to 2017, she was the Lead Electrical Engineer with the Global Research Center, General Electric Company, Niskayuna, NY, USA. Since 2018, she has been a Professor with Huazhong University of Science and Technology, Wuhan, China. Her research interests include high-frequency, high-power density power management IC design, high-frequency supply modulators and applications of wide bandgap power devices, energy harvesting, healthcare electronics, electrical aircraft systems, and electric vehicles. She has published more than 50 articles in refereed journals and international conference proceedings. She has hold four U.S. patents and four Chinese patents.

Dr. Peng has been an Associate Editor of the IEEE Transactions on Power Electronics. Since 2017, she has been the Associate Technical Program Chair for IEEE 11th Annual Energy Conversion Congress and Exposition 2019.

Xinbo Chen (Student Member, IEEE) received the B.S. degree in electrical engineering and automation from Hunan University, Changsha, China, in 2022. He is currently working toward the M.S. degree in electrical engineering with the Huazhong University of Science and Technology, Wuhan, China.

His research interests include applications of wide bandgap devices, switching behavior modeling, and active gate drivers.

Qing Xin received the B.S. degree in electrical engineering from the Wuhan University of Technology, Wuhan, China, in 2021. She is currently working toward the M.S. degree with the School of Electrical and Electronic Engineering, Huazhong University of Science and Technology, Wuhan, China.

Her research interest focuses on applications of wide-bandgap power devices and high-frequency and high power-density gate drive modules.

Yong Kang (Fellow, IEEE) was born in Hubei Province, China, on October 16, 1965. He received the B.E., M.E, and Ph.D. degrees in electrical engineering from Huazhong University of Science and Technology, Wuhan, China, in 1988, 1991, and 1994, respectively.

In 1994, he joined Huazhong University of Science and Technology as a Lecturer, where he was promoted to an Associate Professor in 1996 and a Full Professor in 1998. He is the author of more than 60 technical articles. His research interests include power electronic converters, ac drivers, electromagnetic compatibility, their digital control techniques, and WBG device packaging and applications.