Design of Active-Clamped Push–Pull-Based DC/DC Converter With High Step-Up Ratio and High Power Conversion Efficiency

Kuan-Pin Huang and Rong-Jong Wai, *Senior Member, IEEE*

***Abstract*—This article proposes an active-clamped push–pull-based dc/dc converter with a high step-up ratio and a high conversion efficiency. Using an active-clamped circuit on the primary side of a transformer in the proposed framework can reduce the voltage stress requirements of main switches. Moreover, all power switches' zero-voltage switching operation helps achieve high power conversion efficiency. Using a single input energy storage inductor with a center-tapped transformer structure to make the input current frequency twice the switching frequency, the input current ripple and the inductance of an input inductor can be relatively reduced. In addition, a voltage doubler circuit composed of capacitors and diodes to be used on the secondary side of the transformer can double the corresponding voltage gain via only one capacitor and two diodes. The effectiveness of the proposed converter is verified by an experimental prototype with the specifications of an input voltage from 25 to 40 V, an output voltage of 400 V, and a maximum output power of 2 kW. By observing experimental results, the maximum conversion efficiency is 97.5%, and the full-load conversion efficiency is 96.2% when the input voltage is 40 V. When the input voltage is 25 V, the maximum conversion efficiency is 96.4% and the full-load conversion efficiency is 92.3%.**

***Index Terms*—Active clamping, dc/dc converter, high conversion efficiency, high step-up ratio, push–pull structure, zero-voltage switching (ZVS).**

I. Introduction

RENEWABLE energy demand is thriving because of the global warming issue [1]. In particular, solar power generation systems [2] and wind power generation systems [3] are the mainstays of expansion and installation worldwide. However, most renewable energy resources have the problems of uncertain powers without energy storage functions. Thus, the demand for energy storage systems has received more attention in recent years [4], [5]. Since renewable energy and energy storage systems are generally low-voltage dc power sources and the generating power varies significantly with climate conditions, high step-up dc/dc converters are necessary for voltage conversion and energy transmission to dc microgrids or high-voltage loads.

Generally speaking, renewable energies have the standard features of low-output voltages and high-output currents. Power converters with high step-up ratios and conversion efficiency are always required for wider range applications. A conventional boost converter is a simple step-up method [6], but its low-voltage gain and low efficiency are unsuitable for renewable energy applications. A high step-up converter can be achieved by combining several common circuit elements, such as switched inductors [7], switched capacitors [8], coupled inductors [9], and cascade structures [10]. Nonisolated frameworks with high turns-ratio coupled inductors are often selected for high step-up applications [11], [12] due to the advantages of higher conversion efficiency and fewer components. By adopting switching capacitors or switching inductor topologies, the voltage stresses of semiconductor elements can be further reduced, which makes it possible to use power switch components with lower $R_{\mathrm{DS\text{-}ON}}$ to minimize conduction losses caused by high currents, improving the corresponding conversion efficiency. The current stresses of semiconductor elements can also be reduced by applying the interleaving technique [13]. However, the galvanic isolation requirement for grid-connected devices cannot be satisfied, and the power capacities of these structures are relatively limited.

Transformer-based isolated dc/dc converters can effectively increase voltage gains [14], [15], while high-frequency transformers can provide galvanic isolation and prevent electromagnetic interference. Full-bridge types [16], resonant half-bridge types [17], and push–pull types [18] are traditional transformer-isolated structures. Because their original architectures to be voltage-fed topologies cannot provide the voltage step-up ability on the input terminal, additional boost structures or higher transformer turns ratios are required for high step-up applications, resulting in higher core losses. Besides, there is no inductor on the input terminal of the voltage-fed structure for regulating input currents, causing discontinuous currents that will easily affect the life cycle of the power source.

Among the variations of transformer-based isolated topologies, current-fed structures with regulating inductors to be placed at the input terminals have been widely applied for full-bridge circuits [19], [20], push–pull circuits [21], and dual-active-bridges circuits [22] to reduce the current ripple on the input terminal. The current-fed terminal also provides an initial

Manuscript received 17 May 2023; revised 6 August 2023; accepted 2 September 2023. Date of publication 8 September 2023; date of current version 23 October 2023. This work was supported by the Ministry of Science and Technology of Taiwan under Grant MOST 111-2221-E-011-063-MY3. Recommended for publication by Associate Editor F.D. Freijedo. *(Corresponding author: Rong-Jong Wai.)*

The authors are with the Department of Electronic and Computer Engineering, National Taiwan University of Science and Technology, Taipei 106, Taiwan (e-mail: leo5282013@gmail.com; rjwai@mail.ntust.edu.tw).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3313103.

Digital Object Identifier 10.1109/TPEL.2023.3313103

step-up ability similar to a boost circuit, thereby reducing the demands of the transformer's turn ratio. In practical designs, the input inductors are often introduced into the design of coupling inductors [23] for providing extra voltage gain. The topology in [24] utilizes the input inductor as a high-frequency transformer, providing galvanic isolation between the input and output terminals. It is important to note that input inductors as the energy storage component and transformers as the energy transfer components have very different design considerations. Combining elements will increase the converter's power density but might cost a fair amount of efficiency. Besides, the current-fed architecture also raises some issues related to the specification requirements of the circuit. The active switches and the inductor connected in series are prone to severe voltage overshoot or oscillation during the switching [25], which significantly increases the voltage stresses across active switches, hence stringently limiting the selection of circuit components. To solve the voltage surge issue, lossless snubbers composed of inductors and diodes were used in [26], and an active switch snubber circuit was introduced in [27]. Another branch of this type of auxiliary circuit is the active-clamped circuit composed of active switches and capacitors [28].

Different soft-switching techniques are introduced to reduce power converters' switching losses. Resonant-based or quasi-resonant-based soft-switching techniques have been widely used [29], [30], but the accuracy requirement for the switching timing raises the difficulty of design. Topologies that contain resonant tanks, e.g., *LLC* or *CLLC*, can achieve very high conversion efficiency by operating at the resonant frequency of the tank [31]. However, the conversion efficiency drops rapidly as the switching frequency deviates from the resonance frequency. Besides, reactive currents result in high conduction losses under the light-load condition and potential duty-cycle losses. If active snubber or clamped circuits are adopted into the converter, these additional active switches also need to achieve soft switching to reduce switching losses [32], [33].

By observing previous literature on high step-up conversion topologies, Yang et al. [34] presented an interleaved structure with double input inductors to further reduce the input current ripple by raising the input current frequency to twice the switching frequency. In [35], two isolated coupled inductors were highly integrated on the same core to minimize the number of magnetic components. A variation of push–pull circuits with input inductors integrated with transformers was proposed in [36] to reduce the number of cores and increase the converter's power density. In applications with a higher tolerance of the output current ripple, secondary-side voltage multiplier circuits composed of capacitors and diodes were widely adopted [37]. Nguyen et al. [38] introduced an isolated Z-source topology to provide additional step-up capability on the primary side of the transformer. Another structure with fewer active switches was proposed in [39] to possess considerable advantages in low-power applications.

In this article, an active-clamped push–pull-based high step-up dc/dc converter with a single input inductor is investigated to maintain the continuity of the input current while reducing the demand for the input inductance. An active-clamped circuit in this converter design can reduce the inductance requirement of the transformer for zero-voltage switching (ZVS) conditions, which also reduces the losses of the transformer and duty cycles. A voltage doubler circuit is set up on the secondary side of the transformer to provide additional voltage gain and further reduce the turns-ratio requirement of the transformer. Moreover, all active switches in the proposed converter can achieve zero-voltage turn-ON property. The rest of the article is organized as follows. The circuit topology and operation principle of the proposed converter are presented in Section II. The design considerations of circuit components in the proposed converter are explained in Section III. Experimental results and efficiency measurements are provided in Section IV to validate the effectiveness of the proposed converter. Section V provides some comparisons with current research to justify that the design in this article is new and advantageous over existing ones. Finally, Section VI concludes this article.

The significant features of this article compared to the existing works [33], [34], [35], [36], [37], [38], [39] are summarized as follows:

1) The push–pull-based structure with a single input inductor is proven to reduce the input current ripple effectively, and the number of the input inductor can be reduced by one compared with the conventional *L-L* structure with double input inductors.
2) The energy losses from ZVS participated by the active-clamped circuit are less than conventional resonant methods because there is no circulating current. The currents required for discharging the parasitic capacitors of the active switches cycle between the leakage inductor and the clamped capacitor only.
3) Although the circuit volume will increase by separating the transformer and the input inductor, the better the coupling coefficient of the transformer, the more available conduction duty cycles of the switches can be provided. Moreover, a lower leakage inductance also prevents additional transformer core loss.

II. Circuit Topology and Operation Principle

In general, there are two categories composed of different input terminals in conventional isolated dc/dc converters, including the voltage-fed terminal in Fig. 1(a) and the current-fed terminal in Fig. 1(b)–(d). Due to the high input current ripple, the voltage-fed terminal is unsuitable for the power source applications to be sensitive to current ripples. To reduce the current ripple, an input inductor with a high transient impedance is added at the input terminal to provide continuous current along with the switching activity, resulting in the current-fed terminal, as shown in Fig. 1(b). Although the current ripple in Fig. 1(b) is smaller than the one caused by the voltage-fed terminal in Fig. 1(a), it still has a certain degree of current ripple amplitude. Therefore, an *L-L* type circuit with dual input inductors, shown in Fig. 1(c), is always adopted to alleviate the entire input current ripple. The current ripple of two input inductors will compensate for each other and further reduce the magnitude of the input current ripple in Fig. 1(c) by half with the same switching frequency.

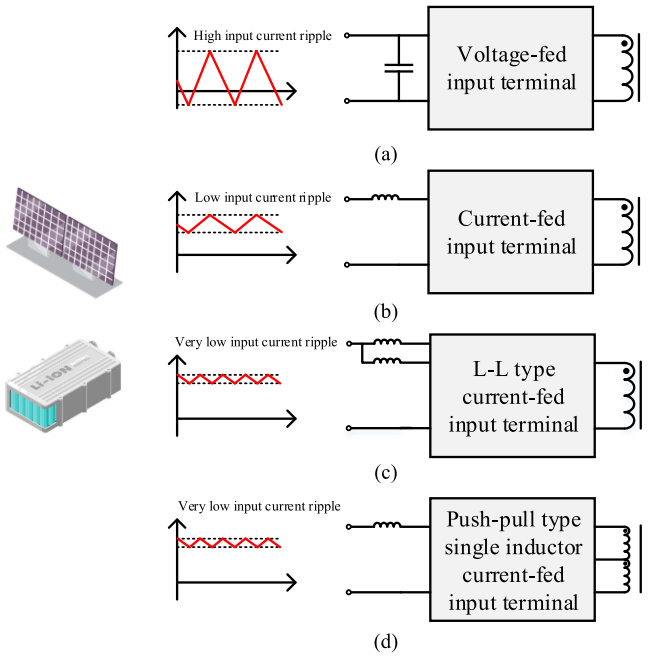

Fig. 1. Input current ripple effects by different input terminal structure. (a) Voltage-fed. (b) Current-fed. (c) *L-L* type current-fed. (d) Push–pull-type single inductor current-fed.

However, this additional inductor will significantly increase the circuit volume and the manufacturing cost. To solve this drawback, this article introduces a push–pull-based architecture with a single inductor and a center-tapped transformer, shown in Fig. 1(d). This single inductor structure can relax the inductance requirement and increase the converter's power density.

A. Circuit Topology of Active-Clamped Push–Pull-Based DC/DC Converter

The circuit framework of the proposed active-clamped push–pull-based dc/dc converter is depicted in Fig. 2. This converter consists of the input terminal circuit, the first winding circuit, the second winding circuit, the first active-clamped circuit, the second-active-clamped circuit, the voltage doubler circuit, the output terminal circuit, and the control mechanism. In this converter, conventional proportional–integral (PI) control frameworks are utilized to implement the stable output voltage control via the voltage error produced by the output voltage feedback and the voltage command. A microcontroller unit XMC4700 manufactured by Infineon Technologies is adapted to execute the PI control to generate pulsewidth modulation (PWM) signals for power switches. Fig. 3 performs the equivalent circuit of the proposed active-clamped push–pull-based dc/dc converter. The symbol representations are expressed as follows. V_{in} and V_o are the input and output voltages, respectively. L_{in} is the input inductor. Q_1 and Q_2 are the main switches in the first winding circuit and the second winding circuit, respectively; Q_3 and Q_4 are the clamped switches corresponding to the main switches (Q_1 and Q_2); and C_{C1} and C_{C2} are the clamped capacitors corresponding to the clamped switches (Q_3 and Q_4). The transformer (T_r) consists of the first winding (L_1) and the second winding (L_2) on

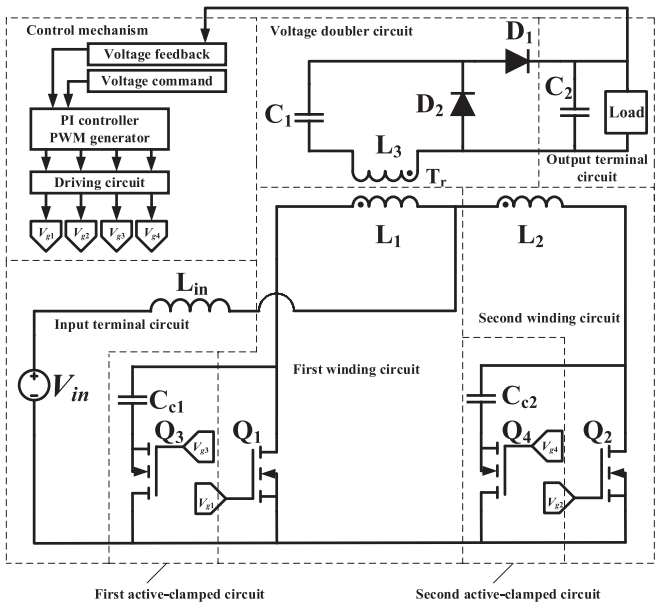

Fig. 2. Circuit framework of active-clamped push–pull-based dc/dc converter.

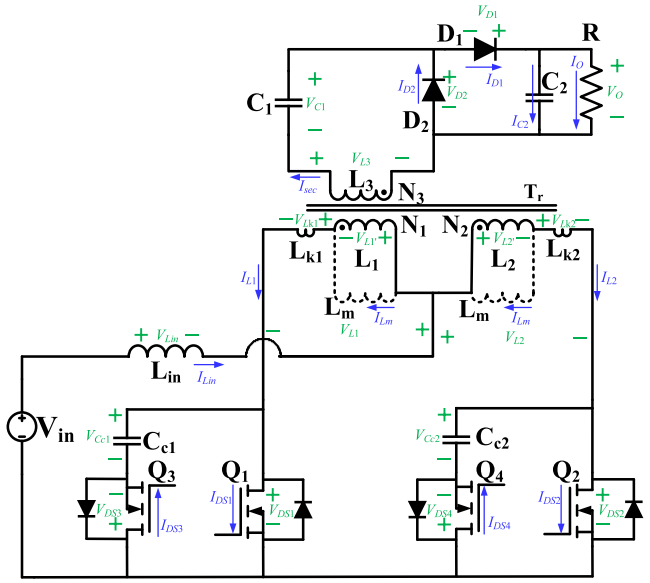

Fig. 3. Equivalent circuit of active-clamped push–pull-based dc/dc converter.

the primary side, the tertiary winding (L_3) on the secondary side, the leakage inductors (L_{k1} and L_{k2}) corresponding to the first winding (L_1) and the second winding (L_2), and the magnetizing inductor (L_m). The numbers of turns in the first winding (L_1) and the second winding (L_2) are defined as N_1 and N_2, and the number of turns in the tertiary winding (L_3) is defined as N_3. Individual turns ratios of the transformer are denoted as $N_{31} = N_3/N_1$ and $N_{32} = N_3/N_2$, respectively. On the secondary side of the transformer, it contains the pumped capacitor (C_1), the rectifying diodes (D_1 and D_2), and the regulated capacitor (C_2).

Fig. 4 shows the characteristic waveforms of the proposed active-clamped push–pull-based dc/dc converter. The switching frequency of power switches is defined as f_s, and one switching cycle is denoted as T_s. The duty cycle of the dead time is defined

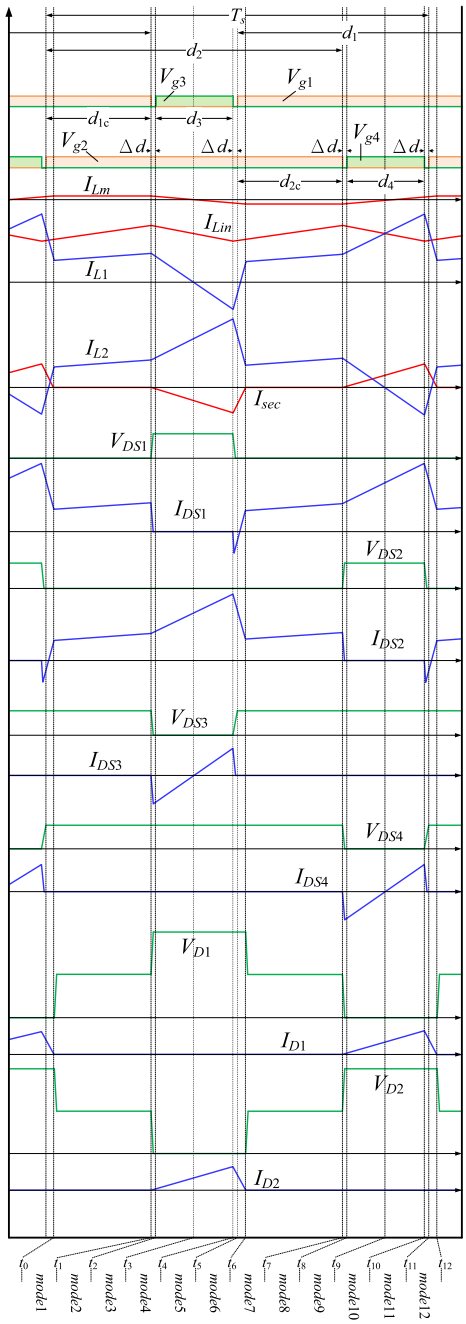

Fig. 4. Key waveforms of active-clamped push–pull-based DC/DC converter.

as Δd. The trigger signals of the main switches (Q_1 and Q_2) are PWM signals with 180° phase-shifted by each other. The conduction duty cycles of the main switches (Q_1 and Q_2) can be represented as $d_1 = 1- d_3-2\Delta d$ and $d_2 = 1 - d_4 - 2\Delta d$, respectively, where d_3 and d_4 are the corresponding conduction duty cycles of the clamped switches (Q_3 and Q_4). They are the complementary PWM signals of the duty cycles of main switches (d_1 and d_2). To reduce the input current ripple, the input inductor (L_{in}) will be operated at the continuous conduction mode (CCM). In the proposed converter, all active switches can achieve the objective of ZVS due to the action of active-clamped circuits.

To simplify the analyses, some reasonable assumptions are made in this article as follows:

1) The effects of parasitic elements in the circuit can be ignored.
2) Active switches Q_1–Q_4 are ideal devices with the existence of body diodes. Diodes D_1 and D_2 are ideal elements.
3) Capacitors C_{C1}, C_{C2}, C_1, and C_2 are large enough to be treated as constant voltage sources during a switching period.
4) The leakage inductors (L_{k1} and L_{k2}) on the primary side of the transformer are much smaller than the corresponding magnetizing inductor (L_m).

B. Operation Mode Analysis

To analyze the operation principle of the proposed converter, key waveforms are depicted in Fig. 4, and the switching cycle is divided into 12 operation modes, as shown in Fig. 5(a)–(l). The input inductor stores energy while the transformer is demagnetized and transmits the stored energy to the voltage doubler circuit on the secondary side of the transformer for achieving the objective of high step-up power conversion when the transformer is magnetized. Moreover, turn-OFF voltages (V_{DS1}–V_{DS4}) across power switches will be clamped by active-clamped circuits while ensuring ZVS on all active power switch conductions.

Mode 1 [t_0–t_1]: Fig. 5(a)

In this mode, the main switches (Q_1 and Q_2) are both turned ON for a span, and the clamped switches (Q_3 and Q_4) are turned OFF in this interval. Because the first winding (L_1) and the second winding (L_2) are magnetized with opposite polarities, the transformer (T_r) is completely demagnetized with zero across voltage. In this interval, the input inductor stores energy ($V_{L\text{in}} = V_{\text{in}}$), and the inductor current rises linearly. During this mode, the power of the output terminal is provided by the regulated capacitor (C_2). By using Kirchhoff's voltage law (KVL) in the input and output loops, the governing mathematical equations of mode 1 can be represented as

$$V_{\text{in}} = L_{\text{in}} \frac{dI_{L\text{in}}}{dt} + V_{L1} = L_{\text{in}} \frac{dI_{L\text{in}}}{dt} + V_{L2} \tag{1a}$$

$$C_2 \frac{dV_O}{dt} = \frac{-V_O}{R}. \tag{1b}$$

Mode 2 [t_1–t_2]: Fig. 5(b)

At $t = t_1$, the main switch (Q_1) is turned OFF. The clamped capacitor (C_{C1}) voltage is applied to the other end of the first winding (L_1). The transformer (T_r) is magnetized again by the second winding (L_2) with the input voltage (V_{in}) and the input inductor voltage ($V_{L\text{in}}$). The interval's voltage across the second winding (L_2) can be expressed as $V_{L2} = V_{\text{in}} - V_{L\text{in}}$. In this mode, the energy is transferred to the tertiary winding (L_3) on the secondary side of the transformer. The voltage across the tertiary winding (L_3) in this interval can be expressed as $V_{L3} = N_{32}V_{L2}$. The energy stored in the leakage inductor (L_{k1}) is released through the first winding (L_1) to the clamped capacitors (C_{C1}). Moreover, this path also passes through the body diode of the clamped switch (Q_3) for discharging the parasitic capacitor of

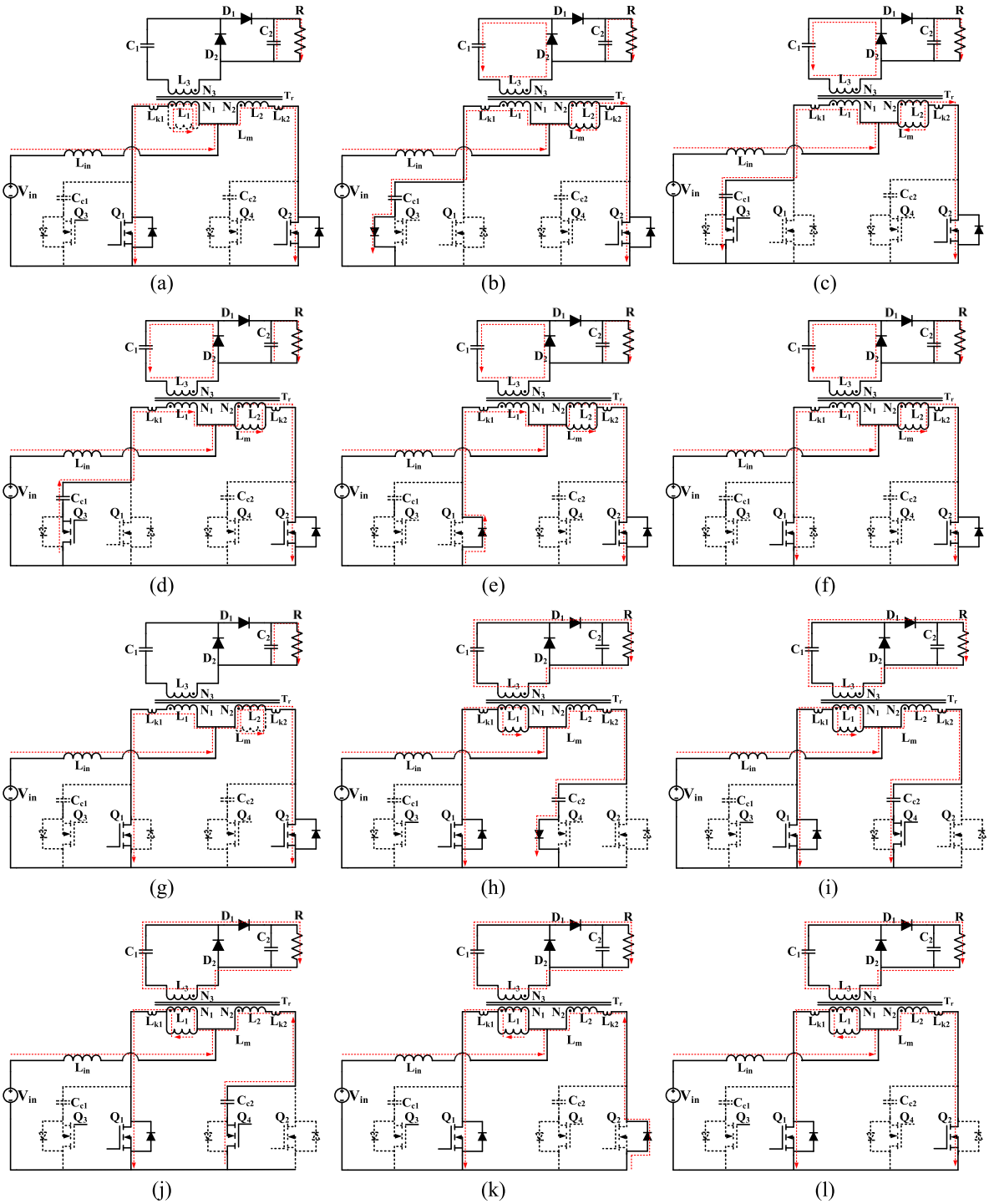

Fig. 5. Operation modes of active-clamped push–pull-based DC/DC converter. (a) Mode 1[t_0–t_1]. (b) Mode 2[t_1–t_2]. (c) Mode 3[t_2–t_3]. (d) Mode 4[t_3–t_4]. (e) Mode 5[t_4–t_5]. (f) Mode 6[t_5–t_6]. (g) Mode 7[t_6–t_7]. (h) Mode 8[t_7–t_8]. (i) Mode 9[t_8–t_9]. (j) Mode 10[t_9–t_{10}]. (k) Mode 11[t_{10}–t_{11}]. (l) Mode 12[t_{11}–t_{12}].

Q_3 to allow it to be conducted with ZVS in the next state. In this mode, the clamped capacitor (C_{C1}) absorbs the current from the leakage inductor (L_{k1}) and clamps the voltage across the main switch (Q_1) such that the turn-OFF voltage surge of $V_{\rm DS1}$ can be suppressed. In this interval, the magnetizing inductor current decreases, and the rectifying diode (D_2) is conducted to transmit the energy into the pumped capacitor (C_1). The voltage across the pumped capacitor (C_1) can be represented as $V_{C1} = -V_{L3}$. In addition, the regulated capacitor (C_2) still powered the output terminal during this mode.

Mode 3 [t_2–t_3]: Fig. 5(c)

At $t = t_2$, the clamped switch (Q_3) is turned ON under ZVS. The leakage inductor (L_{k1}) continuously releases its energy through the path of the clamped switch (Q_3) and charges the clamp capacitor (C_{C1}). When the power of the leakage inductor

(L_{k1}) releases completely (i.e., the current of I_{L1} decreases to zero), this mode ends.

By using KVL in the input and output loops, the governing mathematical equations of modes 2 and 3 can be represented as

$$V_{\text{in}} = L_{\text{in}} \frac{dI_{L\text{in}}}{dt} + V_{L1} + V_{Cc1} = L_{\text{in}} \frac{dI_{L\text{in}}}{dt} + V_{L2} \tag{2a}$$

$$C_2 \frac{dV_O}{dt} = \frac{-V_O}{R}. \tag{2b}$$

Mode 4 [t_3–t_4]: Fig. 5(d)

At $t = t_3$, the leakage inductor (L_{k1}) is completely discharged. Then, the clamped capacitor (C_{C1}) starts to discharge, and the first winding current (I_{L1}) changes its direction to forward pass through the clamped switch (Q_3). Under this situation, the first winding (L_1) and the second winding (L_2) can be considered the series transformer primary winding, and the corresponding magnetizing voltage is V_{Cc1}. Because the direction of the magnetizing current of the transformer is changed, the second winding (L_2) is magnetized and induces voltages across the first winding (L_1) and the tertiary winding (L_3). The clamped capacitor (C_{C1}) stabilizes the voltage across the first winding (L_1) while transmitting the energy to the secondary side of the transformer and charging the leakage inductor (L_{k1}) at the same time.

By using KVL in the input and output loops, the governing mathematical equations of mode 4 can be represented as

$$V_{\text{in}} = L_{\text{in}} \frac{dI_{L\text{in}}}{dt} + V_{L2} \tag{3a}$$

$$V_{Cc1} = V_{L2} - V_{L1} \tag{3b}$$

$$C_2 \frac{dV_O}{dt} = \frac{-V_O}{R}. \tag{3c}$$

Mode 5 [t_4–t_5]: Fig. 5(e)

At $t = t_4$, the clamped switch (Q_3) is turned OFF. The clamped capacitor (C_{C1}) stopped providing the magnetizing voltage, causing the decrease of the currents of the first winding (L_1) and the second winding (L_2). At the same time, the secondary-side current of the transformer also starts decreasing. The leakage inductor (L_{k1}) releases its energy charged by the clamped capacitor (C_{C1}) in the previous mode to maintain the continuous current of the first winding (L_1). This current is sustained by the path of the body diode of Q_1, and it also discharges the parasitic capacitor of the main switch (Q_1). Because the input voltage (V_{in}) is larger than the voltage across the second winding (L_2), the input inductor (L_{in}) starts charging, and the corresponding inductor current ($I_{L\text{in}}$) gradually rises.

By using KVL and KCL in the input and output loops, the governing mathematical equations of mode 5 can be represented as

$$V_{\text{in}} = L_{\text{in}} \frac{dI_{L\text{in}}}{dt} + V_{L2} \tag{4a}$$

$$I_{L\text{in}} = I_{L1} + I_{L2} \tag{4b}$$

$$C_2 \frac{dV_O}{dt} = \frac{-V_O}{R}. \tag{4c}$$

Mode 6 [t_5–t_6]: Fig. 5(f)

At $t = t_5$, the main switch (Q_1) conducts under ZVS. After the leakage inductor (L_{k1}) is completely discharged, the current of the first winding (L_1) changes its current direction, and the leakage inductor (L_{k1}) starts to store energy. Moreover, the voltage across the leakage inductor (L_{k2}) is reverse-biased, and it continues to transfer power to the secondary side of the transformer till $t = t_6$. Because the currents of the first winding (L_1) and the second winding (L_2) are equal at $t = t_6$, the transformer stops magnetizing. When the current of the rectifying diode (D_2) decreases to zero, this mode ends.

Mode 7 [t_6–t_7]: Fig. 5(g)

The actions of the primary side of the transformer in modes 7–12 are similar to the ones in modes 1–6. At $t = t_6$, the first winding (L_1) and the second winding (L_2) are both magnetized with opposite polarities. Thus, the transformer (T_r) is demagnetized, causing zero voltage across the tertiary winding (L_3), and the transformer stops transmitting energy. During this interval, the voltage across the input inductor (L_{in}) is the input voltage (V_{in}), and the input inductor current is linearly increased.

By using KVL in the input and output loops, the governing mathematical equations of modes 6 and 7 can be represented as

$$V_{\text{in}} = L_{\text{in}} \frac{dI_{L\text{in}}}{dt} + V_{L1} = L_{\text{in}} \frac{dI_{L\text{in}}}{dt} + V_{L2} \tag{5a}$$

$$C_2 \frac{dV_O}{dt} = \frac{-V_O}{R}. \tag{5b}$$

Mode 8 [t_7–t_8]: Fig. 5(h)

At $t = t_7$, the main switch (Q_2) is turned OFF. The voltage of the clamped capacitor (C_{C2}) is applied on the other end of the second winding (L_2). The transformer is magnetized by the first winding (L_1) with the input voltage (V_{in}) and the input inductor voltage ($V_{L\text{in}}$). The voltage across the first winding (L_1) during this interval can be expressed as $V_{L1} = V_{\text{in}} - V_{L\text{in}}$. In this mode, the energy is transferred to the tertiary winding (L_3) of the transformer, and the corresponding voltage across the winding (L_3) can be expressed as $V_{L3} = N_{31} V_{L1}$. When the magnetizing current of the transformer is decreased, the rectifying diode (D_1) conducts to transmit the energy stored by the pumped capacitor (C_1) in the previous half cycle (modes 2–6) along with the power provided from the primary side of the transformer into the output terminal. The output voltage (V_O) in this mode can be represented as $V_O = V_{C1} + V_{L3}$. Moreover, the leakage inductor (L_{k2}) releases its stored energy through the second winding (L_2). In addition, this path also passes through the body diode of the clamped switch (Q_4) for discharging the parasitic capacitor of Q_4 to allow it to be conducted with ZVS in the next state. In this mode, the clamped capacitor (C_{C2}) absorbs the current from the leakage inductor (L_{k2}) and clamps the voltage across the main switch (Q_2) such that the turn-OFF voltage surge of V_{DS2} can be suppressed.

Mode 9 [t_8–t_9]: Fig. 5(i)

At $t = t_8$, the clamped switch (Q_4) is turned ON under ZVS. The energy of the leakage conductor (L_{k2}) continues to

pass through the reverse path of the clamped switch (Q_4) for charging the clamped capacitor (C_{C2}). When the energy of the leakage inductor (L_{k2}) releases completely (i.e., the current of I_{L2} decreases to zero), this mode ends.

By using KVL in the input and output loops, the governing mathematical equations of modes 8 and 9 can be represented as

$$V_{\text{in}} = L_{\text{in}} \frac{dI_{L\text{in}}}{dt} + V_{L1} = L_{\text{in}} \frac{dI_{L\text{in}}}{dt} + V_{L2} + V_{Cc2} \tag{6a}$$

$$V_O = V_{C1} + N_{31} V_{L1}. \tag{6b}$$

Mode 10 [t_9–t_{10}]: Fig. 5(j)

At $t = t_9$, the second winding current (I_{L2}) changes its direction to pass through the clamped switch (Q_4). Under this situation, the first winding (L_1) and the second winding (L_2) can be considered the series transformer primary winding, and the corresponding magnetizing voltage is V_{Cc2}. Because the direction of the magnetizing current of the transformer is changed, the first winding (L_1) is magnetized and induces voltages across the second winding (L_2) and the tertiary winding (L_3). The clamped capacitor (C_{C2}) stabilizes the voltage across the second winding (L_2) while transmitting the energy to the secondary side of the transformer and charging the leakage inductor (L_{k2}) at the same time.

By using KVL in the input and output loops, the governing mathematical equations of mode 10 can be represented as

$$V_{\text{in}} = L_{\text{in}} \frac{dI_{L\text{in}}}{dt} + V_{L1} \tag{7a}$$

$$V_{Cc2} = V_{L1} - V_{L2} \tag{7b}$$

$$V_O = V_{C1} + N_{31} V_{L1}. \tag{7c}$$

Mode 11 [t_{10}–t_{11}]: Fig. 5(k)

At $t = t_{10}$, the clamped switch (Q_4) is turned OFF. The clamped capacitor (C_{C2}) no longer provides the magnetizing voltage for the transformer, causing the decrease of the currents of the first winding (L_1) and the second winding (L_2). At the same time, the secondary-side current also starts decreasing. The leakage inductor (L_{k2}) releases its energy charged by the clamped capacitor (C_{C2}) in the previous mode to maintain the continuous current of the second winding (L_2). This current is sustained by the path of the body diode of Q_2, and it also discharges the parasitic capacitor of the main switch (Q_2). Because the input voltage (V_{in}) is larger than the voltage across the first winding (L_1), the input inductor (L_{in}) starts charging, and the corresponding inductor current ($I_{L\text{in}}$) gradually rises.

By using KVL and KCL in the input and output loops, the governing mathematical equations of mode 11 can be represented as

$$V_{\text{in}} = L_{\text{in}} \frac{dI_{L\text{in}}}{dt} + V_{L1} \tag{8a}$$

$$I_{L\text{in}} = I_{L1} + I_{L2} \tag{8b}$$

$$V_O = V_{C1} + N_{31} V_{L1}. \tag{8c}$$

Mode 12 [t_{11}–t_{12}]: Fig. 5(l)

At $t = t_{11}$, the main switch (Q_2) is turned ON under ZVS to sustain the current of the second winding (L_2). After the leakage inductor (L_{k2}) is completely discharged, the current of the second winding (L_2) changes its direction, and the leakage inductor (L_{k2}) starts to store energy. In this state, the voltage across the leakage inductor (L_{k1}) is reverse-biased, and it continues to transfer power to the secondary side of the transformer till $t = t_{12}$. Because the currents of the first winding (L_1) and the second winding (L_2) are equal at $t = t_{12}$, the transformer stops magnetizing, and the state returns to mode 1.

By using KVL in the input and output loops, the governing mathematical equations of mode 12 can be represented as

$$V_{\text{in}} = L_{\text{in}} \frac{dI_{L\text{in}}}{dt} + V_{L1} = L_{\text{in}} \frac{dI_{L\text{in}}}{dt} + V_{L2} \tag{9a}$$

$$V_O = V_{C1} + N_{31} V_{L1}. \tag{9b}$$

C. Analysis of Steady-State Voltage Gain

To simplify the analysis, the dead time (Δd) in the switching period is ignored. Moreover, the same turns of the first winding (L_1) and the second winding (L_2) are designed as $N_1 = N_2$, and the corresponding turn ratio can be represented as $N = N_{31} = N_{32}$. In addition, the inductances of the leakage inductors on the first winding (L_1) and the second winding (L_2) are designated as the same as $L_{k1} = L_{k2} = L_k$, and the corresponding coupling coefficient of the transformer (T_r) can be defined as $k = L_m / (L_k + L_m)$. In this article, the input inductor (L_{in}) will be operated at the CCM.

During one switching period, the energy-releasing duty cycle and the energy-storing duty cycle of the main switch (Q_1) are d_3 (Modes 3 and 4) and d_{1c} (Modes 12–1), respectively; and the energy-releasing duty cycle and the energy-storing duty cycle of the main switch (Q_2) are d_4 (Mode 9 and 10) and d_{2c} (Mode 6 and 7), respectively. According to Fig. 5, the voltages across the input inductor (L_{in}) at the duty cycles of d_{1c}, d_{2c}, d_3, and d_4 can be, respectively, represented as

$$V_{L\text{in},d1c} = V_{L\text{in},d2c} = V_{\text{in}} \tag{10}$$

$$V_{L\text{in},d3} = V_{\text{in}} - V_{L2,d3} \tag{11}$$

$$V_{L\text{in},d4} = V_{\text{in}} - V_{L1,d4} \tag{12}$$

where the subscripts d_{1c}, d_{2c}, d_3, and d_4 in (10)–(12) means that the states at the duty cycles of d_{1c}, d_{2c}, d_3, and d_4, respectively. According to the volt-second principle [40] of the input inductor (L_{in}), one can obtain

$$V_{L2} = V_{\text{in}} \frac{d_3 + d_{1c}}{d_3} = V_{\text{in}} \left(1 + \frac{d_{1c}}{d_3}\right) \tag{13}$$

$$V_{L1} = V_{\text{in}} \frac{d_4 + d_{2c}}{d_4} = V_{\text{in}} \left(1 + \frac{d_{2c}}{d_4}\right). \tag{14}$$

According to the voltage translation relationship of the transformer (T_r), the voltage across the tertiary winding (L_3) can be written as

$$V_{L3,d3} = NkV_{L2} \tag{15}$$

$$V_{L3,d4} = NkV_{L1}. \tag{16}$$

Similarly, the voltage across the pumped capacitor (C_1) can be denoted as

$$V_{C1,d3} = V_{C1,d2} = -V_{L3,d3} \tag{17}$$

$$V_{C1,d4} = V_{C1,d1} = V_O - V_{L3,d4}\,. \tag{18}$$

Because the voltage across the pumped capacitor (C_1) must be balanced through the whole switching period, the following relations can be derived:

$$d_3(-V_{L3,d3}) + d_4(V_O - V_{L3,d4}) = 0 \tag{19}$$

$$V_O = \frac{1}{d_4}\left[d_3 N k V_{\text{in}}\left(1+\frac{d_{1c}}{d_3}\right) + d_4 N k V_{\text{in}}\left(1+\frac{d_{2c}}{d_4}\right)\right]. \tag{20}$$

The energy-releasing duty cycle of the input inductor (L_{in}) is defined as $d_r = d_3 + d_4$, and then its energy-storing duty cycle can be expressed as $(1 - d_r)$. It is assumed that the conduction duty cycles of the clamped switches (C_{C1} and C_{C2}) are equal ($d_3 = d_4 = d_r/2$), and the energy-storing duty cycle of the main switches (Q_1 and Q_2) are identical ($d_{1c} = d_{2c} = (1 - d_r)/2$). According to (11), the output voltage of the proposed converter can be represented as

$$V_O = 2NkV_{\text{in}}\left[1+\frac{(1-d_r)}{d_r}\right]. \tag{21}$$

Thus, the ideal voltage gain of the proposed active-clamped push–pull-based dc/dc converter can be obtained as

$$G_V = V_O \,/\, V_{\text{in}} = 2Nk/d_r. \tag{22}$$

When the converter is operating under high heavy load conditions, a high operating current will generate voltage drops across the parasitic resistance of the circuit components, affecting the voltage gain of the circuit. To further analyze the effect of internal resistance of the main circuit components, the following assumptions are made: $R_{L\text{in}}$ is the resistance of the input inductor (L_{in}); R_{pri} is the resistance of the first and second winding of the transformer (L_1 and L_2); R_{L3} is the resistance of the tertiary winding of the transformer (L_3); $R_{\text{DS,ON}}$ is the resistance of the main switches (Q_1 and Q_2); R_{C1} is the resistance of the pumped capacitor (C_1); and the dead time and other components' effects of the converter are still ignored. According to similar mathematical derivations in (10)–(21), the nonideal voltage gain of the converter can be calculated as

$$G_{V,\text{non-ideal}} = \frac{2Nk}{(2Nk)^2\left[\frac{(1-d_r)}{d_r}\frac{R_A}{R}+\frac{R_B}{R}\right]+\left(2d_r\frac{R_C}{R}+d_r\right)} \tag{23}$$

where $R_A = R_{L\text{in}} + \frac{1}{2}R_{\text{pri}} + \frac{1}{2}R_{\text{DS,on}}$, $R_B = R_{L\text{in}} + \frac{3}{4}R_{\text{pri}} + \frac{3}{4}R_{\text{DS,on}}$, and $R_C = R_{L3} + R_{C1}$.

III. Design Consideration of Circuit Components

To verify the high step-up ability and high conversion efficiency of the proposed active-clamped push–pull-based dc/dc converter, a 2-kW prototype converter is designed and tested. By considering an example application for the proposed converter with a paralleled photovoltaic (PV) module or a battery storage system as the input terminal and a high-voltage dc bus at the front-end of an inverter for the output terminal, the input voltage range is specified as 25–40 V_{dc}, converted to the output voltage of 400 V_{dc} through this innovative circuit structure.

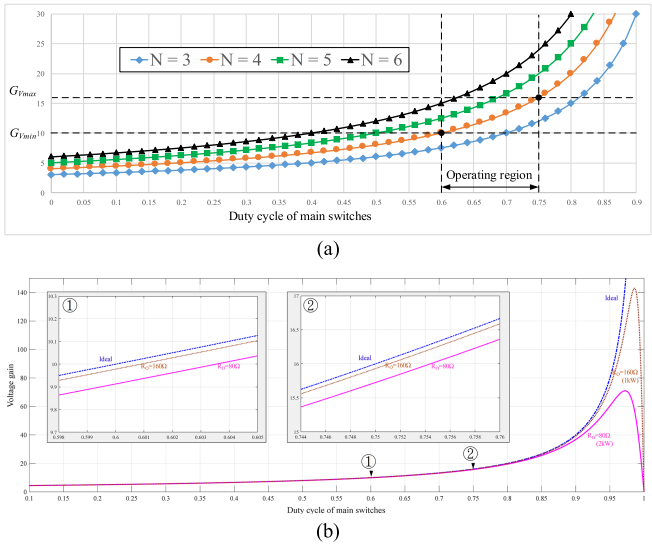

Fig. 6. (a) Ideal voltage gain (G_V) with respect to duty cycles of main switches under various turn ratios (N). (b) Nonideal voltage gain of active-clamped push–pull-based dc/dc converter ($N = 4$ and $k = 1$) under different output power conditions.

A. Design of Turns Ratio of Transformer and Conduction Duty Cycles of Main Switches

In this experiment, the input voltage of the converter prototype is 25–40 V_{dc}, and the output voltage is 400 V_{dc}. Thus, the maximum voltage gain of the proposed converter ($G_{V\max}$) can be calculated as $\frac{400}{25} = 16$, and the minimum voltage gain ($G_{V\min}$) can be obtained as $\frac{400}{40} = 10$. To design the transformer's turn ratio, it is necessary to consider the relationship between different turn ratios and the turn-ON duty cycles of the main switches. By assuming that the dead time (Δd) in the switching period is ignored, the conduction duty cycles of the clamped switches (Q_3 and Q_4) can be considered to be equal($d_3 = d_4 = \frac{d_r}{2}$), and the conduction duty cycles of the main switches (Q_1 and Q_2) are balanced and equal ($d_1 = d_2 = 1 - \frac{d_r}{2}$). In this case, the coupling factor of the transformer is assumed to be $k = 1$. From (22), the ideal voltage gain (G_V) concerning different conduction duty cycles of the main switches($1 - \frac{d_r}{2}$) under various transformer turns ratios ($N = 3$–6) is presented in Fig. 6(a).

As for the minimum voltage gain of the proposed converter ($G_{V\min} = 10$), the conduction duty cycles of the main switches (Q_1 and Q_2) will be less than 0.5, and they will not overlap if the transformer turns ratio of $N = 5$ or $N = 6$ has been chosen. Therefore, the transformer cannot realize fully demagnetization characteristics. Although the voltage across the primary-side switches can be reduced by using a larger turns ratio (N), the practical currents flowing through the primary side of the transformer will also increase, causing more conduction losses under heavy load conditions. As for the maximum voltage gain of the proposed converter ($G_{V\max} = 16$), the individual conduction duty cycles of the main switches (Q_1 or Q_2) will be too short

if the transformer turns ratio of $N = 3$ was chosen. The reserve duty cycle for transferring energy to the secondary side of the transformer will be less than 0.2, generating high current peaks on the secondary side to increase the corresponding losses.

When the turns ratio is selected as $N = 4$ by considering the maximum voltage gain ($G_{V\max} = 16$), the conduction duty cycles of the main switches are 0.75, with the overlapping duty cycle of 0.5, and each main switch still has an individual conduction duty cycle of 0.25. The duty cycle that sends energy to the output terminal is only 0.25 due to the voltage doubler structure on the secondary side of the transformer. When the turns ratio is selected as $N = 4$ by considering the minimum voltage gain ($G_{V\min} = 10$), the conduction duty cycles of the main switches are 0.6, with the overlapping duty cycle of 0.2, to be capable of using the demagnetization characteristic of the transformer. According to the above analyses, the transformer turns ratio of $N = 4$ is selected for this converter prototype.

Fig. 6(b) shows how the actual components resistances of the prototype converter affect the voltage gain, where $R_{\rm lin} = 0.011\ \Omega$; $R_{\rm pri} = 0.58\ \Omega$; $R_{L3} = 1.8\ \Omega$; $R_{C1} = 0.0047\ \Omega$; and $R_{\rm DS,ON} = 0.015\ \Omega$, respectively. The conduction currents increase along with the output power increment, resulting in more duty losses in the circuit. For the operating range designed in this article, the required voltage gain is 10 at an input voltage of 40 V. The required duty cycle of main switches is 0.6 under the curve of ideal voltage gain in Fig. 6(a); i.e., in Fig. 6(b), approximately 0.001 additional duty cycle is required for 1 kW output power, and 0.0035 additional duty cycle is required for 2 kW output power. When the input voltage is 25 V, the required voltage gain is 16. By the curve of ideal voltage gain in Fig. 6(a), the required duty cycle of main switches is 0.75, i.e., in Fig. 6(b), approximately 0.001 additional duty cycle is required for 1 kW output power and 0.0045 additional duty cycle is required for 2 kW output power.

B. Design Considerations of Input Inductor

The current ripple of the input inductor is defined as $\Delta I_{\rm Lin}/I_{\rm Lin\_avg}$, where $\Delta I_{\rm Lin}$ and $I_{\rm Lin\_avg}$ are the amplitude value and the average value of the input inductor current. Considering the most severe condition of the input current ripple with a 2 kW output power and a 25 V input voltage and setting the ripple ratio of the input inductor current as 10%, $\Delta I_{\rm Lin}$ and $I_{\rm Lin\_avg}$ can be calculated as 8 and 80 A, respectively. Because the switching frequency (f_s) of the proposed circuit is designed as 40 kHz in this article, the effective charging/discharging frequency of the input inductor ($L_{\rm in}$) will be 80 kHz due to the push–pull-based structure on the input terminal. In this situation, the converter is operated under a full-load condition with conduction duty cycles of the main switches at 0.75. Therefore, the charging time of the input inductor can be calculated as 6.25 μs, and the input inductor value should be selected to be larger than 9.77 μH according to the volt-second principle [41]. To ensure that the input inductor is operated under the CCM throughout the entire output power range (10%–100% rated power), the input inductor is designed under the boundary conduction mode condition at a 10% rated output power (200 W) with an input voltage of $V_{\rm in} = 40$ V. If the coupling coefficient of the transformer k is set as 1, and the conduction duty cycles of the main switches are equal. By considering the coupling coefficient of the transformer ($k = 1$) and balanced conduction duty cycles and substituting the input voltage of $V_{\rm in} = 40$ V into (22), the discharging duty cycle ($d_r = 0.8$) and the charging duty cycle ($1 - d_r = 0.2$) of the input inductor can be determined. The average current of the input inductor is 5 A (200 W/40 V). In this situation, the charging period of the input inductor can be calculated as 2.5 μs according to its charging/discharging frequency of 80 kHz (12.5 μs). Considering the voltage across the input inductor is equal to the input voltage in this period, the input inductor value should be selected to be larger than 10 μH. In the converter prototype, three paralleled CS777026 MPP cores are winded together to build this input inductor, and its actual inductance is measured as 13 μH.

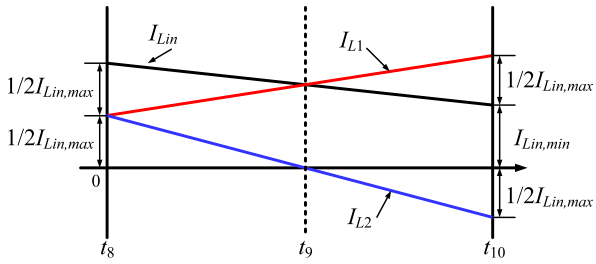

Fig. 7. Relationship of primary-side windings currents of transformer from mode 8 to mode 10.

C. Design Considerations of Magnetizing Inductor of Transformer

Due to the converter's switching frequency ($f_s = 40$ kHz), individual conduction periods of the main switches (Q_1 and Q_2) are 6.25 μs when their conduction duty cycles are 0.75. Considering the variation range of the input voltage from 25 to 40 $V_{\rm dc}$, and (10) and (15), voltages across the first and second windings will vary from 50 to 80 V. If the transformer's magnetizing current variation is assumed as $\Delta I_{Lm} = 2.5$ A, the magnetizing inductance of 125 μH can be calculated according to the volt-second principle. The actual transformer in the converter prototype is built with an EE-65 core and a magnetized inductance of 142 μH. The primary-side and secondary-side turns of the transformer are chosen as 4 and 16 according to the turn ratio of $N = 4$ in Section III-A.

By analyzing the key waveforms from mode 8 to mode 10 of the proposed converter in Fig. 4, the currents of the first winding (I_{L1}) and the second winding (I_{L2}) will divide the input inductor current ($I_{\rm Lin}$) in this period ($I_{\rm Lin} = I_{L1} + I_{L2}$) with the increase of I_{L1} and the decrease of I_{L2}. Assuming that the push–pull-based circuit is balanced and their conduction duty cycles are equal, the relationship of the primary-side winding currents (I_{L1} and I_{L2}) of the transformer can be obtained as Fig. 7 by applying the amp-second principle on the clamped capacitor (C_{C2}).

At $t = t_8$ (mode 9), the clamped switch (Q_4) is turned ON, and the leakage inductor (L_{k2}) to pass through the second winding (L_2) releases its energy into the clamped capacitor (C_{C2}). At

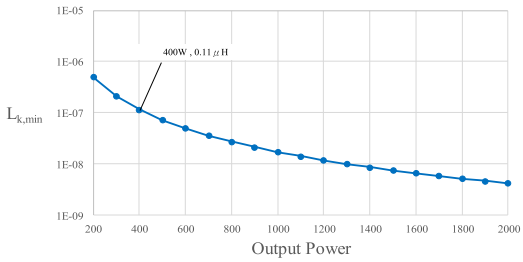

Fig. 8. Relationship between minimum required transformer leakage inductances and converter output powers.

$t = t_9$ (mode 10), the clamped capacitor (C_{C2}) to pass through the second winding (L_2) releases this energy back into the leakage inductor (L_{k2}) reversely. The positive and negative peaks of the second-winding current (I_{L2}) during this charge/discharge cycle will be equal due to the amp-second principle of the clamped capacitor (C_{C2}). At $t = t_{10}$ (mode 11), the clamped switch (Q_4) is turned OFF to stop the clamped capacitor (C_{C2}) from releasing energy. The second-winding current can be expressed as $I_{Lk2} = I_{L2(t\,=\,t10)} = -(1/2)I_{\mathrm{Lin,max}}$. Since the transformer's primary-side windings (L_1 and L_2) can be considered as the series transformer primary-side winding, the leakage inductors on the first and second windings (L_{k1} and L_{k2}) will change polarity at the same time. It will release the energy of the parasitic capacitor of the main switch (Q_2). For the main switch (Q_2) to achieve the objective of ZVS, the energy stored in the leakage inductors (L_{k1} and L_{k2}) has to be greater than the energy stored in the parasitic capacitor of the main switch (Q_2). By assuming that the leakage inductance of the first winding and the second winding are the same ($L_{k1} = L_{k2} = L_k$), the following relationship can be obtained:

$$\left(L_{k1}I^2{}_{L1} + L_{k2}I^2{}_{L2}\right)/2 \geq \left(C_{Q2}V^2{}_{\mathrm{DS2}}\right)/2 \tag{24}$$

$$L_k \geq \left(C_{Q2}V^2{}_{\mathrm{DS2}}\right) / \left(I^2{}_{L1(t=t10)} + I^2{}_{L2(t=t10)}\right). \tag{25}$$

The most severe condition for the switches to achieve ZVS is when the proposed converter is operated at the maximum input voltage ($V_{\mathrm{in,max}} = 40$ V). Moreover, the input current ripple under this situation can be calculated as 3.846 A based on the input inductance of $L_{\mathrm{in}} = 13$ μH determined in Section III-B. The maximum and minimum values of the input inductor current ($I_{L\mathrm{in,max}}$ and $I_{L\mathrm{in,min}}$) under different output power conditions can be obtained, and the currents of the primary-side windings at $t = t_{10}$ ($I_{L1(t\,=\,t10)}$ and $I_{L2(t\,=\,t10)}$) also can be calculated accordingly. In this article, two IRFPS3815 MOSFETs are connected in parallel for one main switch. Thus, the total parasitic capacitor of one main switch is 2.54 nF. By substituting the corresponding parameters into (25), the required minimum transformer leakage inductances concerning different output powers are depicted in Fig. 8.

In this experiment, the main switches are designed to achieve ZVS with more than 20% of the output power of the proposed converter, i.e., 400 W. By observing Fig. 8, the minimum required leakage inductor is $L_{k,\mathrm{min}} = 0.11$ μH. In reality, to prevent the conduction duty cycles of the main switches and the corresponding clamped switches from overlapping, enough

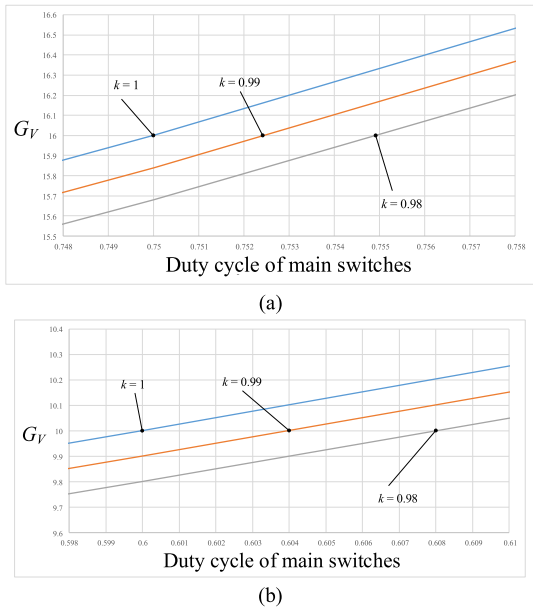

Fig. 9. Voltage gain variation in response to different coupling coefficients. (a) Maximum voltage gain condition ($G_{V,\mathrm{max}} = 16$). (b) Minimum voltage gain condition ($G_{V,\mathrm{min}} = 10$).

dead time should be added between the conduction duty cycles of the main switches and the corresponding clamped switches. As for this design, a 0.3% duty cycle is set as the dead time, and the leakage inductance is measured as 0.21 μH. Since the value of the leakage inductance is vital for achieving ZVS, it is necessary to analyze further the effect of leakage inductance on the voltage gain of the proposed converter. When the transformer turns ratio is selected as $N = 4$, the voltage gain (G_V) variation in response to different coupling coefficients (k) is depicted in Fig. 9. In Fig. 9, the maximum required voltage gain ($G_{V,\mathrm{max}} = 16$) occurs at the minimum input voltage ($V_{\mathrm{in,min}} = 25$ V). The minimum voltage gain ($G_{V,\mathrm{min}} = 10$) occurs at the maximum input voltage ($V_{\mathrm{in,max}} = 40$ V). When the coupling coefficient is set as $k = 1$, the required conduction duty cycles of the main switches under the maximum voltage gain condition and the minimum voltage gain condition are 0.75 and 0.6, respectively. As the increase of the leakage inductance will lower the corresponding coupling coefficient (k), the required conduction duty cycle will increase slightly. When the coupling coefficient is varied from $k = 1$ to $k = 0.98$, the conduction duty cycles of the main switches are increased by 0.65% at the maximum voltage gain condition, as shown in Fig. 9(a), and increased by 1.3% at the minimum voltage gain condition as shown in Fig. 9(b).

D. Voltage and Current Stresses of Switches and Diodes

Assuming that the push–pull-based circuit is balanced and their conduction duty cycles are equal, the voltage stresses of the main switches and the clamped switches should be identical due to the clamping effect from the clamped capacitors (C_{C1} and C_{C2}). The maximum voltages across the main switches (V_{DS1} and V_{DS2}) occur during the releasing-energy duty cycles of the input inductor (d_3 and d_4). By analyzing the circuit with KVL

[42], one can obtain

$$V_{\mathrm{DS1},d3} = V_{Cc1} = -V_{Lk1,d3} - V_{L1',d3} + V_{L2',d3} + V_{Lk2,d3} \tag{26}$$

$$V_{\mathrm{DS2},d4} = V_{Cc2} = -V_{Lk2,d4} - V_{L2',d4} + V_{L1',d4} + V_{Lk1,d4} \tag{27}$$

where the subscripts d_3 and d_4 in (26) and (27) means that the states at the duty cycles of d_3 and d_4, respectively. Here, the voltages across the leakage inductors and the windings can be calculated separately. $V_{L1'}$ and $V_{L2'}$ denote the voltages across the first winding (L_1) and the second winding (L_2), respectively. The relations of $V_{L1',d3} = -V_{L2',d3}$ and $V_{L2',d4} = -V_{L1',d4}$ can be obtained. By rewriting (15) and (16) as

$$V_{L3,d3} = k\ (NV_{L2',d3} + V_{Lk2,d3}) = NV_{L2',d3} \tag{28}$$

$$V_{L3,d4} = k\ (NV_{L1',d4} + V_{Lk1,d4}) = NV_{L1',d4}. \tag{29}$$

Because the conduction duty cycles of the push–pull-based circuit are equal ($d_3 = d_4$), the voltage across the tertiary winding (L_3) at the duty cycles of d_3 and d_4 can be obtained as $V_{L3,d3} = V_{L3,d4} = \frac{V_O}{2}$ by (19). Considering the aforementioned parameters, the transformer turns ratio is $N = 4$, the transformer winding leakage $L_{k1} = L_{k2} = L_k = 0.11\ \mu$H, and the coupling coefficient $k = 0.999$. When the output voltage is set as $V_O = 400$ V, the following states can be calculated as $V_{L2',d3} = V_{L1',d4} = 50$ V, $V_{L1',d3} = V_{L2',d4} = -50$ V, and $V_{Lk2,d3} = V_{Lk1,d4} = 0.05$ V. Moreover, the maximum voltages across the leakage inductors ($V_{Lk1,d3}$ and $V_{Lk2,d4}$) can be obtained as $V_{Lk1,d3,\max} = V_{Lk2,d4,\max} = 0.21$ V by considering the condition of maximum leakage inductor current ($I_{Lk1,d3,\max}$ and $I_{Lk2,d4,\max}$) with the input voltage of $V_{\mathrm{in}} = 25$ V and the output power of 2 kW. According to (26) and (27), the voltage stresses of the active switches can be calculated as 100.26 V.

According to Fig. 4, the maximum currents of the main switches occur at $t = t_{10}$ and $t = t_4$ and are equal to the maximum currents of the first winding current (I_{L1}) and the second winding current (I_{L2}). Thus, the current stresses of the main switches can be calculated by analyzing the illustration in Fig. 7. At $t = t_{10}$, the value of I_{L1} can be obtained by $I_{L1,t10} = 0.5I_{\mathrm{Lin,max}} + I_{\mathrm{Lin,min}}$. Because of the input inductance of $L_{\mathrm{in}} = 13\ \mu$H to be determined in Section III-B, the maximum and minimum values of the input inductor current ($I_{\mathrm{Lin,max}}$ and $I_{\mathrm{Lin,min}}$) at the maximum output power of 2 kW can be calculated as $I_{\mathrm{Lin,max,2kW}} = 88$ A and $I_{\mathrm{Lin,min,2kW}} = 72$ A, and the current stresses of the main switches can be calculated as $\mathrm{I_{DS1,max}} = I_{L1,t10} = 116$ A. The current stresses of other power switches also can be calculated similarly. Considering the parasitic elements' effects, IRFPS3815 MOSFETs with 150 V breakdown voltages and 105 A drain currents are chosen as the power switches and the clamped switches in the proposed converter, and two IRFPS3815 MOSFETs are connected in parallel for one main switch. On the other hand, the maximum reverse bias voltages across the rectifying diodes (D_1 and D_2) at modes 7 and 10 are $V_{D1} = V_{D2} = V_O = 400$ V. By observing Fig. 4, the maximum currents of D_1 and D_2 also occur at $t = t_{10}$ and $t = t_4$. The current of the series transformer primary winding composed of the first winding (L_1) and the second winding (L_2) under this situation also can be calculated as $I_{\mathrm{primary},t10} = I_{L1,t10} + (-I_{L2,t10}) = I_{\mathrm{Lin,max}} + I_{\mathrm{Lin,min}}$.

TABLE I
CONVERTER CIRCUIT COMPONENTS

Circuit components	Symbol	Values and types
Input voltage	V_{in}	25–40 V_{dc}
Output voltage	V_O	400 V_{dc}
Switching frequency	f_s	40 kHz
Full-load output power	$P_{O,max}$	2 kW
Transformer	T_r	N=4, L_m=142 μH, L_k=0.21 μH
Input inductor	L_{in}	13 μH
Main switches	Q_1, Q_2	IRFPS3815*2
Clamped switches	Q_3, Q_4	IRFPS3815
Clamped capacitors	C_{C1}, C_{C2}	20 μF
Rectifying diodes	D_1, D_2	MUR1560*3
Pumped capacitor	C_1	20.4 μF
Filter capacitor	C_2	27.2 μF

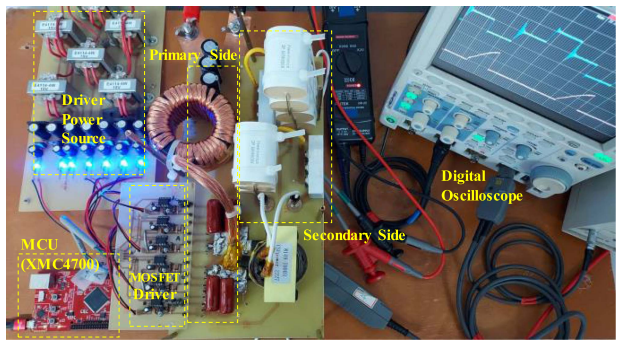

Fig. 10. Practical photograph of proposed converter.

The maximum current of the rectifying diode (D_1) is equal to the reflect current of $I_{\mathrm{primary},t10}$, which can be represented as $(I_{\mathrm{Lin,max}} + I_{\mathrm{Lin,min}})/N$. According to the consideration under the maximum output power with $I_{\mathrm{Lin,max,2kW}} = 88$ A, $I_{\mathrm{Lin,min,2kW}} = 72$ A, and $N = 4$, the maximum current of the rectifying diode (D_1) is $I_{D1,\max} = (88+72)/4 = 40$ A. The current stress of another rectifying diode (D_2) also can be calculated similarly. The type of MUR1560 is adopted in this article. Three diodes are connected in parallel for D_1 and D_2.

IV. EXPERIMENTAL RESULTS AND EFFICIENCY ANALYSIS

To verify the high step-up capability and high-power conversion efficiency of the proposed active-clamped push–pull-based dc/dc converter, a 2 kW prototype with 25–40 V_{dc} input voltage and 400 V_{dc} output voltage is built in this article. According to the circuit analyses in Section II and the design considerations in Section III, the circuit components of the proposed converter are summarized in Table I.

The practical photograph of the proposed converter is depicted in Fig. 10. Moreover, the PWM duty cycle is produced by an industrial microcontroller XMC4700, and the corresponding

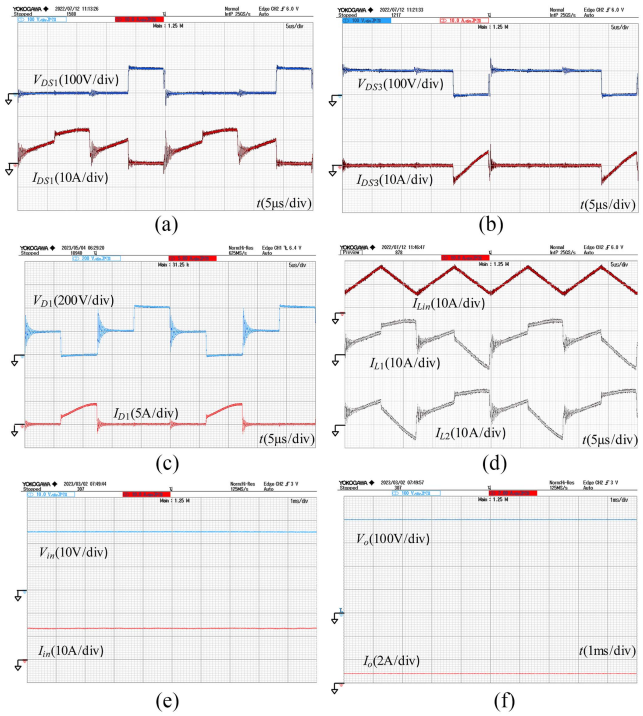

Fig. 11. Experimental waveforms of main switch, clamped switch, rectifying diode, input inductor, and primary-side windings of transformer at $V_{\rm in} = 25$ V and $P_O = 320$ W. (a) Q_1. (b) Q_3. (c) D_1. (d) $L_{\rm in}$ and T_r. (e) Input terminal. (f) Output terminal.

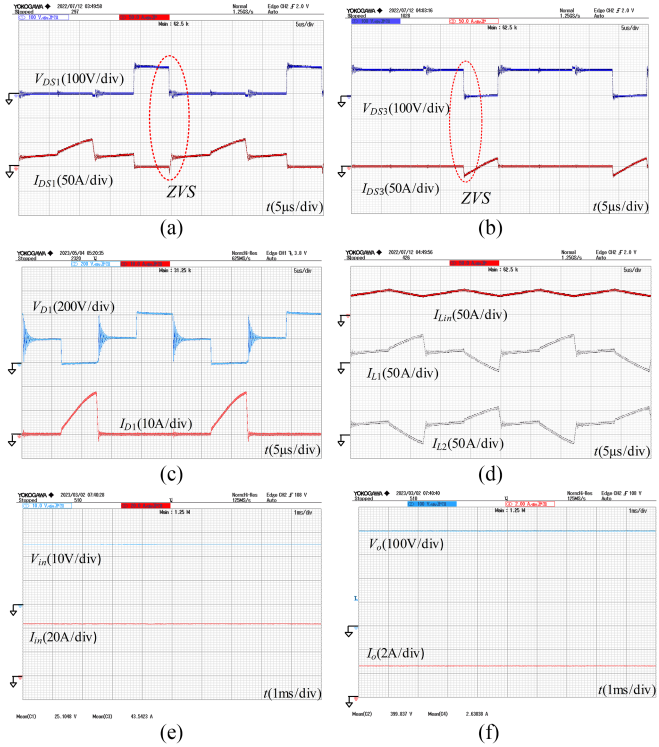

Fig. 12. Experimental waveforms of main switch, clamped switch, rectifying diode, input inductor, and primary-side windings of transformer at $V_{\rm in} = 25$ V and $P_O = 1060$ W. (a) Q_1. (b) Q_3. (c) D_1. (d) $L_{\rm in}$ and T_r. (e) Input terminal. (f) Output terminal.

control signals are sent to MOSFET drivers for triggering power switches. The measured waveforms of the main switch (Q_1), the clamped switch (Q_3), the rectifying diode (D_1), the input inductor ($L_{\rm in}$), the transformer (T_r), the input terminal, and the output terminal in the proposed converter under the input voltage of 25 $V_{\rm dc}$ and the output power of 320 W are depicted in Fig. 11. From Fig. 11(a), the main switch (Q_1) is not able to achieve ZVS under this circumstance, while the voltage across Q_1 is clamped at 100 V by the active-clamped circuit. In addition, the energy recycling activity of the first active-clamped circuit can be observed in Fig. 11(b). When the main switch (Q_1) is turned OFF, the leakage inductor (L_{k1}) continues to store its energy into the clamped capacitor (C_{C1}) while assisting the zero-voltage turn-ON of the clamped switch (Q_3). Relatively, when the clamped switch (Q_3) is turned OFF, the clamped capacitor (C_{C1}) releases this energy back into the leakage inductor (L_{k1}) reversely while assisting with zero-voltage turn-ON of the main switch (Q_1). There is no energy loss during these exchange procedures. The voltage-boosting effect of the voltage doubler structure on the secondary side of the transformer is depicted in Fig. 11(c). As can be seen from Fig. 11(c), the voltage on the secondary side of the transformer is doubled by the voltage doubler circuit to achieve the objective of the output voltage of $V_O = 400$ V. Fig. 11(d) indicates that the input inductor ($L_{\rm in}$) of the proposed converter operates under the CCM, and its charging/discharging frequency is twice the switching frequency of the proposed converter. According to Fig. 11(e) and (f), the power conversion efficiency can be calculated at about 95.14%.

The measured waveforms of the main switch (Q_1), the clamped switch (Q_3), the rectifying diode (D_1), the input inductor ($L_{\rm in}$), the transformer (T_r), the input terminal, and the output terminal of the proposed converter under the input voltage of 25 V and the output power of 1060 W are depicted in Fig. 12. As can be seen from Fig. 12(a), the main switch (Q_1) can achieve the objective of ZVS. The energy inside the parasitic capacitor of the main switch (Q_1) is released by the current path of the leakage inductor at the moment before the conduction of Q_1. Without any redundant circulation current, extra conduction losses and duty cycle loss of the transformer can be avoided. From Fig. 12(a) and (b), the clamped voltages of the main switches increase a little bit along with the increment of the output power. The main reason is the effect of the parasitic inductance in the circuit since more voltage will generate along the increment of the currents on the primary-side windings. By observing Fig. 12(c), the voltage oscillation occurs because of the resonance between the parasitic capacitance of the rectifying diodes and the parasitic inductance inside the circuit. Fortunately, the maximum voltage of the change is clamped to the output voltage (V_O) by the regulated capacitor (C_2), and there is no current oscillation. Thus, it does not significantly impact the selection of circuit components. The boosting ability of the voltage doubler remains stable under different output powers. Moreover, the continuous conduction feature of the input inductor can be observed in Fig. 12(d). According to Fig. 12(e) and (f), the power conversion efficiency can be calculated at about 96.21%.

The measured waveforms of the main switch (Q_1), the clamped switch (Q_3), the rectifying diode (D_1), the input inductor ($L_{\rm in}$), the transformer (T_r), the input terminal, and the output terminal of the proposed converter under the input voltage of 25

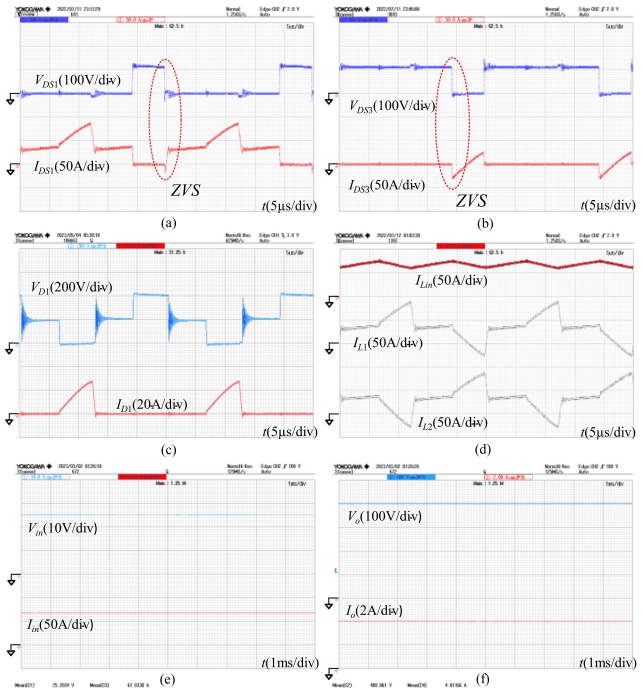

Fig. 13. Experimental waveforms of main switch, clamped switch, rectifying diode, input inductor, and primary-side windings of transformer at $V_{\rm in} = 25$ V and $P_O = 1600$ W. (a) Q_1. (b) Q_3. (c) D_1. (d) $L_{\rm in}$ and T_r. (e) Input terminal. (f) Output terminal.

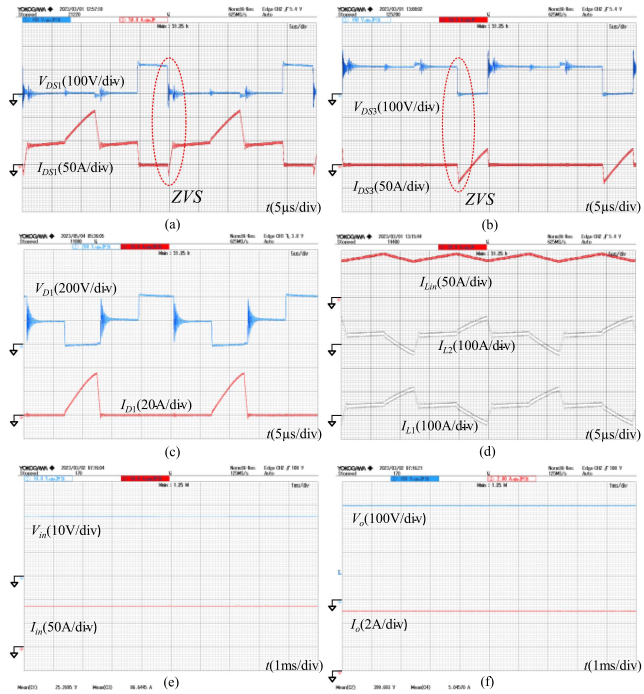

Fig. 14. Experimental waveforms of main switch, clamped switch, rectifying diode, input inductor, primary-side windings of transformer, input terminal, and output terminal at $V_{\rm in} = 25$ V and $P_O = 2$ kW. (a) Q_1. (b) Q_3. (c) D_1. (d) $L_{\rm in}$ and T_r. (e) Input terminal. (f) Output terminal.

$V_{\rm dc}$ and the output power of 1600 W are depicted in Fig. 13. The ZVS characteristic of the main switch (Q_1) can be observed in Fig. 13(a). As can be seen from Fig. 13(a) and (b), the clamped voltages of the main switches are further increased due to large currents passing through the parasitic inductance on the primary side of the transformer, but there is no apparent voltage surge. According to Fig. 13(e) and (f), the power conversion efficiency can be calculated at about 94.25%.

The measured waveforms of the main switch (Q_1), the clamped switch (Q_3), the rectifying diode (D_1), the input inductor ($L_{\rm in}$), the transformer (T_r), the input terminal, and the output terminal of the proposed converter under the input voltage of 25 $V_{\rm dc}$, and the output power of 2 kW are depicted in Fig. 14. The ZVS characteristic of the main switch (Q_1) can be observed clearly in Fig. 14(a). As can be seen from Fig. 14(a) and (b), the clamped voltages of the main switches are increased to 120 V due to the even larger currents passing through the parasitic inductance on the primary side of the transformer. According to Fig. 14(e) and (f), the power conversion efficiency can be calculated at about 92.11%. By observing Figs. 11(d), 12(d), 13(d), and 14(d), since the leakage inductance in the proposed converter is small [i.e., the coupling coefficient of the transformer (k) is close to 1], the output power variation will not affect the required conduction duty cycles of the switches significantly, which ensures sufficient margins of modulation for different output powers.

The ZVS operations of the MOSFETs can be determined by observing the conduction of parasitic diodes in power switches. When the parasitic diode is conducted, the current direction from drain to source will be negative. In the dead time between the turn-OFF of the clamped switches and the turn-ON of the

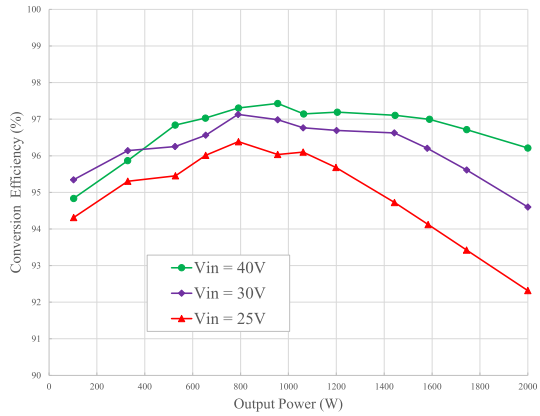

Fig. 15. Conversion efficiency of proposed converter under different input voltages and output powers.

main switches, as shown in Figs. 12(a), 13(a), and 14(a), the continuous current generated by the leakage inductors of the transformer will discharge the parasitic capacitors of the main switches, causing the parasitic diodes forward biased and creating an instantaneous reverse current. In the dead time between the turn-OFF of the main switches and the turn-ON of the clamped switches, as shown in Figs. 12(b), 13(b), and 14(b), the clamped switches receive the continuous current from the transformer and their parasitic diodes naturally conduct, creating ZVS turn-ON condition for the clamped switches.

The conversion efficiencies under different input voltages and output powers are depicted in Fig. 15. The experimental results reveal that when the input voltage is 25 $V_{\rm dc}$, the maximum conversion efficiency of 96.4% occurs at the output power of 800 W and the conversion efficiency reaches 92.3% at the full-load

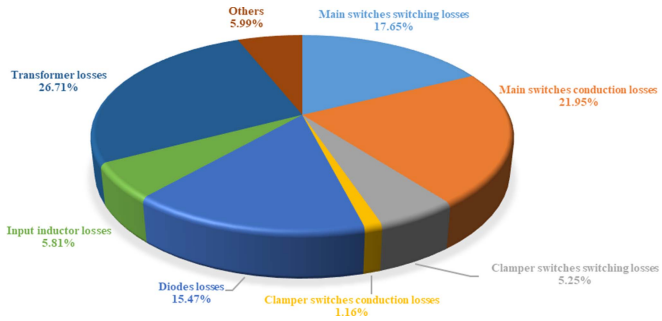

Fig. 16. Power loss estimation for proposed converter at $V_{\rm in} = 25$ V and $P_O = 1060$ W.

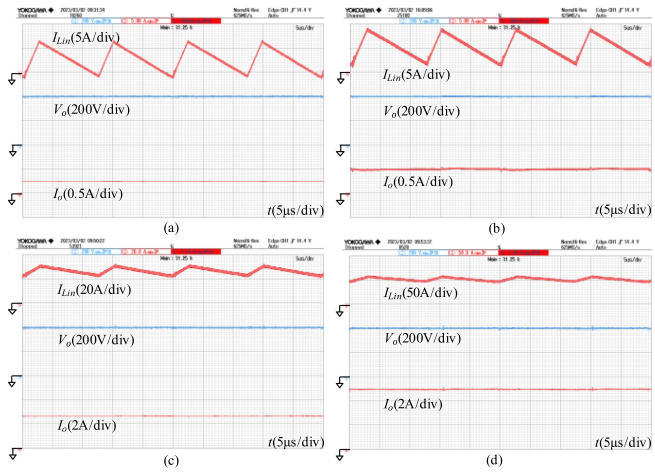

Fig. 17. Experimental waveforms of input inductor and output terminal at $V_{\rm in} = 40$ V with different output powers. (a) $P_O = 100$ W. (b) $P_O = 200$ W. (c) $P_O = 1060$ W. (d) $P_O = 2$ kW.

output power of 2 kW. When the input voltage is 30 $V_{\rm dc}$, the maximum conversion efficiency of 97.1% occurs at the output power of 800 W and the conversion efficiency reaches 94.6% at the full-load output power of 2 kW. When the input voltage is 40 $V_{\rm dc}$, the maximum conversion efficiency of 97.5% occurs at the output power of 960 W and the conversion efficiency reaches 96.2% at the full-load output power of 2 kW. The significant loss of the proposed converter is the conduction loss from large currents on the primary side of the transformer. In Fig. 15, the conversion efficiency of 40 $V_{\rm dc}$ input voltage is lower than that of 30 $V_{\rm dc}$ input voltage under the light-load condition. This is because the transformer's primary-side winding currents are too small, so the switches cannot achieve the objective of ZVS in this situation. In addition, the averaged operating efficiency can be calculated based on the efficiency data in Fig. 15. By using the weighting coefficients of EUR efficiency to calculate the averaged operational efficiency, the corresponding results are 96.67% for $V_{\rm in} = 40$ V, 96.16% for $V_{\rm in} = 30$ V, and 95.11% for $V_{\rm in} = 25$ V, respectively.

The power loss estimation of the proposed converter under the input voltage of 25 $V_{\rm dc}$ and the output power of 1060 W is depicted in Fig. 16, where the total loss of the converter under this circumstance is 43.05 W. The loss estimation caused by the main switches and the clamped switches contained the corresponding conduction losses and turn-OFF switching losses. Since the voltage stresses across active switches are suppressed by adapting the active-clamping technique, MOSFET components (IRFPS3815) with low conduction resistances (15 mΩ) were chosen in this prototype to reduce the conduction losses substantially (about 9.45 W on main switches and 0.5 W on clamped switches). However, the proposed topology was designed without soft-switching techniques for turn-OFF situations of active switches to result in significant amounts of turn-OFF switching losses (about 7.6 W on main switches and 2.26 W on clamped switches). If the active switches can achieve the objective of soft switching in the future design, the conversion efficiency can be further improved. The loss inside rectifier diodes is about 6.66 W, caused by the 1.5 V forward conduction voltage of MUR1560. Because there is only one input inductor in the proposed topology, the iron loss is much lower than that of the *L-L* structure with double input inductors, and the total loss of the input inductor is about 2.5 W. The transformer loss accounts for most of the total loss, mainly due to the conduction losses caused by high currents on the primary side of the transformer, and the theoretical transformer loss is about 11.5 W. The remaining losses caused by the equivalent series resistant of capacitors and the parasitic effects on PCB are merged at approximately 2.58 W.

The proposed converter's input inductor currents (I_{Lin}) under various output powers (P_O) are shown in Fig. 17. When the converter is operating with the input voltage of $V_{\rm in} = 40$ V, the designed operating current of the input inductor is minimal, which is the most severe condition for the input inductor to enter the CCM. In Fig. 17(a), the input inductor current (I_{lin}) does not enter the CCM region because of low output power, $P_O = 100$ W, and partial current flows back to the input terminal. Fig. 17(b) shows that the input inductor can enter the CCM region at the output power of $P_O = 200$ W. From Fig. 17(c) and (d), the input inductor operates under stable CCM conditions at $P_O = 1060$ W and $P_O = 2$ kW. This demonstrates that the inductance of the input inductor follows the design considerations in Section III-B, i.e., the input inductor can enter the CCM region for $P_O = 200$ W or above when the converter operates with input voltage $V_{\rm in} = 40$ V. As demonstrated in Fig. 17(a), the discontinuous current mode (DCM) operation of the input inductor does not affect the stabilizing ability of the converter's output voltage. Although the DCM operation of the input inductor may affect the open-loop voltage gain in (22), the output voltage stabilization can still be achieved by the closed-loop controller.

It is easier for the main switches to enter the operation region of less than 50% duty cycle when the converter operates at a high input voltage with a low-voltage gain requirement. Meanwhile, a fixed load can reduce the impact of the voltage gain of the converter. Therefore, the condition of the input voltage $V_{\rm in} = 40$ V and the load $R = 200\ \Omega$ is chosen for the open-loop testing of various main switch duty cycles. The corresponding results are shown in Fig. 18, where Fig. 18(a) to (d) demonstrates the converter's output voltage variations with main switches operating under 30%, 40%, 50%, and 60% duty cycles. Moreover, the corresponding output voltages are 226, 264, 320, and 400 V,

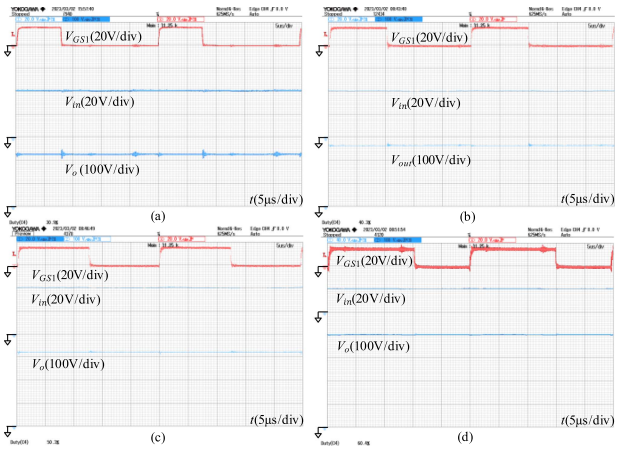

Fig. 18. Experimental waveforms of main switch, input terminal, and output terminal at $V_{\rm in} = 40$ V and $R = 200\ \Omega$ with different main switch duty cycle. (a) Duty cycle $= 30\%$, $V_o = 226$ V. (b) Duty cycle $= 40\%$, $V_o = 264$ V. (c) Duty cycle $= 50\%$, $V_o = 320$ V. (d) Duty cycle $= 60\%$ (normal), $V_o = 400$ V.

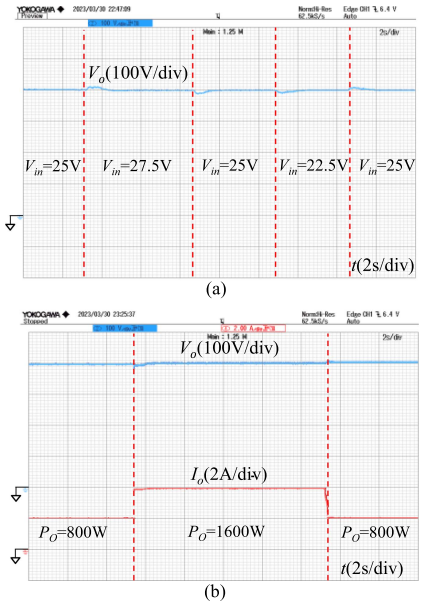

Fig. 19. Measured dynamic responses of proposed converter. (a) $V_{\rm in} = 25$ V with $\pm 10\%$ variations at $P_O = 1060$ W. (b) Step changes of output powers from $P_O = 800$ to $P_O = 1600$ W.

respectively, and the voltage gains can be calculated as 5.6, 6.6, 8, and 10, respectively. The converter operates within the originally designed operating zone with output voltage $V_o = 400$ V, as shown in Fig. 18(d). The experiment results in Fig. 18 satisfy the relationship curves between the voltage gains and the duty cycles of the main switches in Fig. 6, with the transformer turns ratio $N = 4$. In other words, the proposed converter circuit can still operate normally with the main switches' duty cycle below 50%. As for the output voltage stabilization of $V_o = 400$ V, it depends on the closed-loop controller to adjust the required duty cycles.

The dynamic responses of the proposed converter with the input voltage of 25 V with $\pm 10\%$ variations are depicted in Fig. 19(a). Although there are some output voltage oscillations on the output terminal during the transient input voltage variations, it will eventually converge to the designed voltage of 400 V. In Fig. 19(b), the dynamic responses of the proposed converter with step output-power changes between $P_O = 800$ W and $P_O = 1600$ W are depicted. The output voltage can be stably adjusted with little voltage variations and without spike currents occurring at the sudden power change.

V. Comparison and Discussion

To exhibit the advantages of the proposed converter, comprehensive comparisons of other isolated high-step-up dc/dc converters in previous article are summarized in Table II. As can be seen from Table II, the conversion efficiency of the proposed converter is higher than those in other references. Less active switches are adopted in the proposed converter than in [33]. The *L-L* topology with double input inductors is used in [34] and [37], resulting in more circuit volume and manufacturing costs. Although the dual-active-bridge structure in [35] only needs a single core to create two isolated coupled inductors for storing and transferring energy, a low coupling coefficient will decrease the voltage gain and the core utilization rate. The circuit framework in [36] is similar to the proposed converter in this article. The number of components can be significantly reduced by integrating the input inductor into the transformer windings, and two active-clamped circuits share the same clamped capacitor. However, the main disadvantage is that two transformers are used [36]. In this way, the transformer's coupling coefficient will drop significantly to use the transformer for energy storage, causing crucial duty cycle loss between the primary and secondary sides of the transformer. Additional active switches are required in [37] for synchronous rectification such that the control signals are complex, with some of the active power switches unable to achieve the soft-switching function. A variation of the isolated Z-source structure was introduced in [38]. Unfortunately, additional diodes connected on the low-voltage side will cause more conduction losses, while the input capacitor limits the maximum power potential of this structure [38]. To reduce the number of active switches, only one power switch with its corresponding clamped circuit was applied [39]. Because the transformer in [39] only operates in the first quadrant, the utilization of the transformer is worse.

The power density of magnetic components is also compared in Table II. The proposed converter has a higher power density than most references, except for the one in [36]. It is because that only one input inductor is adopted in the proposed converter, and the coupling coefficient of the transformer is good. Thus, this circuit's total magnetic component volume is relatively minor. The power density of magnetic components of [36] is higher than the proposed converter because its operating frequency is over double the proposed one. Even so, the maximum power conversion efficiency of the proposed converter is higher than the one in [36].

Ma et al. [43] investigated a resonant current-fed push–pull converter with active clamping for the vehicle inverter application. Although the proposed converter framework in this article is similar to [43], the circuit structure in [43] is mainly operated

TABLE II
PERFORMANCE COMPARISONS OF PROPOSED CONVERTER WITH PREVIOUS RESEARCH

	This study	[33]	[34]	[35]	[36]	[37]	[38]	[39]
Circuit framework	Active-clamped push-pull-based circuit	Dual active-clamped quasi-resonant boost scheme	*L*-*L* type full-bridge scheme	Dual active bridge with coupled inductor	Interleaved boost scheme with coupled inductors	Interleaved boost scheme with semi-active quadrupler rectifiers	Quasi-switched boost scheme	Isolated boost scheme with active clamping
Active switches number	4	6	4	8	4	6	4	2
Passive components number	7	8	8	1	5	10	8	9
Switching frequency	40 kHz	12 kHz	25 kHz	100 kHz	100 kHz	100 kHz	10 kHz	70 kHz
Input inductor value	13 μH	1 mH	320 μH×2	8 μH	4 μH×2	50 μH×2	3 mH	120 μH
Transformer number	1	1	1	1	2	1	1	1
Turn ratio (N)	4	2	2	1.5	8	2	2.5	5
Core volume utilization rate	10.9 W/cm^3	–	1.45 W/cm^3	1.28 W/cm^3	13.89 W/cm^3	–	4.46 W/cm^3	8.01 W/cm^3
Maximum efficiency	97.5% @ near 1 kW	95.1% @ 1 kW	91.5% @ 400 W	96.4% @ 4k W	94.88% @ 80 W	96.33% @ near 260 W	95.5% @ near 170 W	96.7% @ 90 W

in the resonant mode. As a result, the current stresses flowing through power switches in [43] are significant, and the ZVS conditions of power switches are complex. On the other hand, the converter circuit proposed in this article uses the continuous current ability of leakage inductances in the transformer to make power switches accomplish the objective of ZVS. The operation mode between them is entirely different, resulting in a higher power conversion efficiency, and the output power of the converter proposed in this article can be effectively increased.

Ma et al. [43] proposed a circuit structure in as a current-fed push–pull converter with an active-clamping technique. To achieve soft switching for semiconductor components, two design methods, including the primary-side resonance and the secondary-side resonance, were proposed in [43]. Unfortunately, these two methods cannot operate simultaneously. The secondary-side resonance method was used in the experiment of [43] to achieve soft switching for rectifier diodes. Here, numerical simulations of the main switch waveforms of [43] via the PSIM software are redone and performed in Fig. 20(a). Significantly, the voltage and current waveforms are intersected at the moment of switching. Therefore, soft switching of the main switches is unachievable. The effect also can be observed in the experimental results of [43] that the conversion efficiency of the experimental prototype is lower than 93%.

As for the design consideration of the proposed converter in this article, the primary-side soft-switching technique is chosen because the primary-side switching loss has a high proportion of the total losses under a relatively high input voltage of 40 V. Numerical simulations of the main switch waveforms of the proposed converter are also given in Fig. 20(b) to compare with Fig. 20(a). At the moment of switching, the current waveform is negative due to the conduction of parasitic diodes, which indicates that the parasitic capacitor has been discharged and the soft switching is successful. In addition, the soft-switching operation of the proposed converter is to discharge the parasitic capacitor by using the leakage inductance current on the primary side of

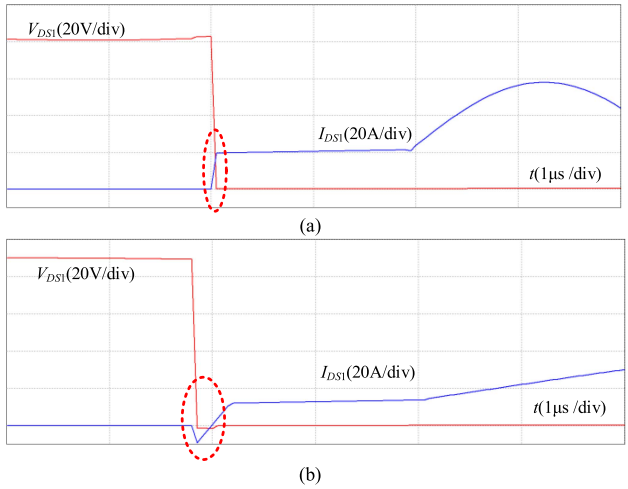

Fig. 20. Numerical simulations of main switch waveforms at 1 kW output power. (a) Main switch voltage (V_{DS1}) and current (I_{DS1}) of [43]. (b) Main switch voltage (V_{DS1}) and current (I_{DS1}) of this article.

the transformer and achieving the zero-voltage turn-ON property. Because it is unnecessary via the complicated calculation for resonance-related capacitance and inductance demonstrated in [43], the design procedure in this article is much easier.

Fig. 21 shows the comparisons of simulated efficiency and duty cycles of [43] and this article under the output power from 800 W to 2 kW, where the turns ratio of the transformer is set to 5, and the operating frequency is set to 100 kHz. As can be seen from Fig. 21, every 100 W increase in output power requires an additional 1.5% duty cycle on average when the converter in [43] is operated above 1 kW output power, and the variation of duty cycle is up to 17.5% for the output power range from 800 W to 2 kW. This is because the converter deviates from the ideal operating area over a wide range of the output power, causing the distortion of the resonance waveforms, which results in surge duty cycle losses and reduces the conversion efficiency at the

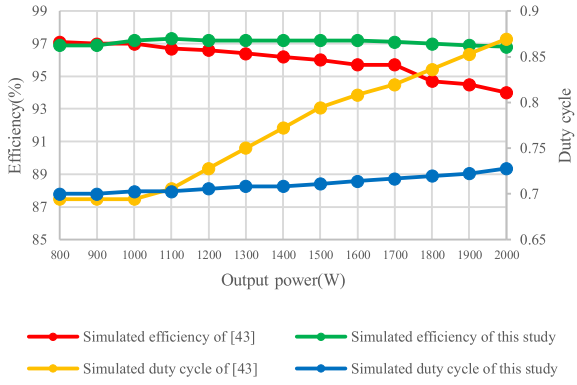

Fig. 21. Comparison of simulated efficiency and duty cycles of [43] and this article.

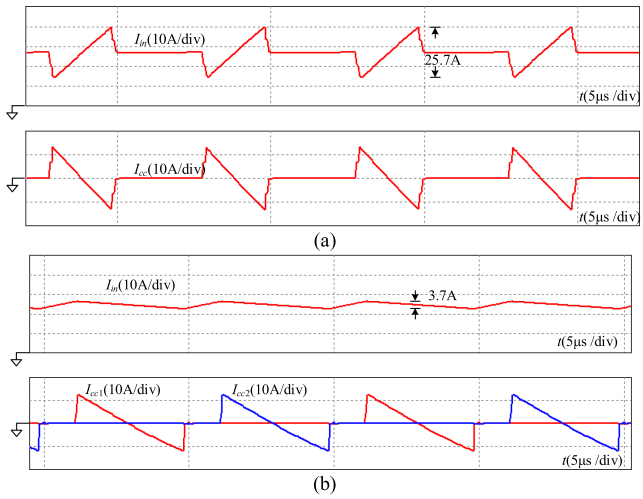

Fig. 22. Simulated waveforms at 40 V input voltage and 1 kW output power. (a) Input port current ($I_{\rm in}$) and clamped capacitor current ($I_{\rm CC}$) of [44]. (b) Input port current ($I_{\rm in}$) and clamped capacitor current ($I_{\rm CC1}$, $I_{\rm CC2}$) of proposed converter.

same time. On the contrary, the soft-switching method applied in this article uses the energy from the leakage inductance on the primary side of the converter. Without relying on the resonance method, the duty cycle varies by only 2.8% over the output power range from 800 W to 2 kW, and the overall conversion efficiency above 1 kW is higher than the one in [43]. Conversion efficiency of the proposed converter outperforms that in [43] by 3% at 2 kW output power

Delshad and Farzanehfard [44] investigated a current-fed push–pull architecture with an active-clamping technique. There are two critical differences between [44] and the proposed converter in this article. One is the connection position of the clamping capacitor, which is connected to the input port in the converter framework [44]. The simulated waveforms of the input port current ($I_{\rm in}$) and the clamping capacitor current ($I_{\rm cc}$) under the operating condition of 40 V input voltage and 1 kW output power are depicted in Fig. 22(a). It can be observed that the input port current ($I_{\rm in}$) is affected by the clamping capacitor current ($I_{\rm cc}$), and the amplitude of the current ripple reaches 25.7 A, which makes it contrary to the intention of the current-fed structure design. On the contrary, the clamping capacitor is

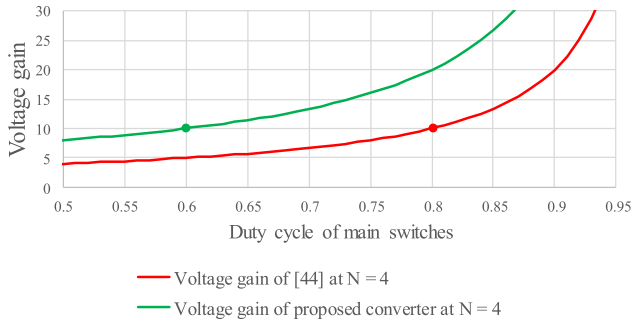

Fig. 23. Comparisons of voltage gains with $N = 4$ in [44] and proposed converter.

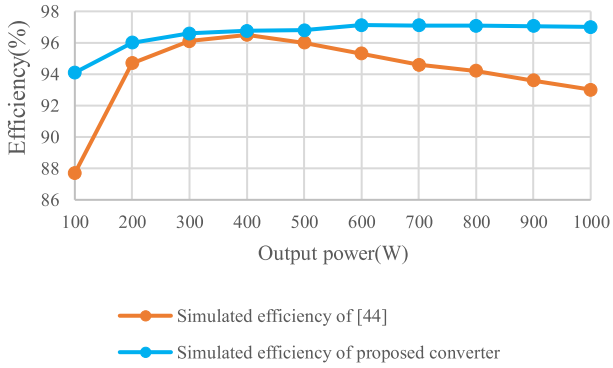

Fig. 24. Comparisons of simulated efficiency and duty cycle of [44] and proposed converter.

connected to the ground terminal of the primary side of the proposed converter in this article. The simulated waveforms of the proposed converter under the same operating condition are given in Fig. 22(b). It demonstrates that the clamping capacitor current does not affect the input current, and the amplitude of the input-port current ripple is only 3.7 A, which is only 14% of the one in Fig. 22(a). This indicates that the proposed converter structure can achieve low current ripple characteristics at the input port.

The other critical difference is that the converter in [44] uses the bridge rectifier structure on the secondary side of the transformer, which makes the voltage gain only $N/[2(1-D)]$. In contrast, by applying a voltage doubler structure on the secondary side of the transformer in this article, the voltage gain can be increased to $N/(1-D)$ in the proposed converter. The comparisons of the simulated voltage gain in [44] and the proposed converter with $N = 4$ are depicted in Fig. 23. For the operating condition of 40 V input voltage, the required duty cycle of the converter in [44] is 0.8, which is higher than the one in the proposed converter, which is only 0.6. As a result, the utilization of the duty cycle is better in the proposed converter. Moreover, the comparison of the simulated efficiencies of [44] and the proposed converter under the output power from 100 W to 1 kW is also depicted in Fig. 24. It is evident that the overall efficiency of the proposed converter in this article performs better than the one in [44]. The simulated efficiency of the proposed structure is higher than that in [44] by 4% at 1 kW output power. Additionally, by observing the experimental waveform of the

main switch in Fig. 8(a) of [44], the ZVS phenomenon is interfered with by the resonance between parasitic inductors and conductors. On the contrary, as can be seen from Fig. 12(a) in this article, it is evident that the parasitic diode conducts at the moment of switching, which indicates the ZVS ability of the main switches.

VI. Conclusion

This article has successfully designed an active-clamped push–pull-based dc/dc converter, and rich experimental results are provided to verify the superiority of the proposed converter compared with previous article. The proposed framework combines the push–pull structure, the active-clamping technology, and the voltage doubler circuit. The active-clamping technology allows all switches to achieve the ability of zero-voltage conduction while effectively reducing the voltage stresses on the semiconductor components to improve the power conversion efficiency. Moreover, the volume and current ripple of the input inductor can be further reduced because its charging and discharging frequency is twice the switching frequency. It also can decrease the installed capacity of the input power source and extend the corresponding lifetime. An experimental 2 kW circuit prototype is built and examined to prove the correctness of the theoretical analysis of the circuit. The related experimental results are the full-load conversion efficiencies of 92.3%, 94.6%, and 96.2% at the input voltages of 25, 30, and 40 V, respectively. The main advantages of the proposed converter are summarized as follows:

1) A low input current ripple can be generated with a lower inductance value under the same switching frequency.
2) The voltage stresses on power switches can be clamped by the active-clamping technology, allowing the selection of power switches with lower $R_{\text{DS-ON}}$ values to reduce conduction loss and manufacturing cost simultaneously.
3) The requirement of the leakage inductance for the property of ZVS in the proposed converter can be relaxed, and all power switches can be operated under ZVS, such that the transformer can be built with a good coupling coefficient. While reducing the iron loss also decreases the conduction cycle loss of the primary and secondary sides of the transformer.

The defects of the proposed framework in this article are the voltage oscillation problem of the parasitic capacitance of the secondary-side diode, the range in which the converter transmits energy to the output terminal to be minor, and the current ripple at the output terminal to be relatively large. These drawbacks could be improved in future article.

This article aims to develop an active-clamped push–pull-based dc/dc converter with a high step-up ratio and a high conversion efficiency. For PV applications, the maximum power tracking algorithm of the PV array is required to design in the future. For battery energy storage applications, controlling the charge and discharge in combination with the system power is often necessary. In future article, active power switches should replace the rectifying diodes to redesign the converter circuit and the corresponding operational modes.

References

[1] International Energy Agency, *World Energy Outlook 2022*, Nov. 2022.
[2] M. Shafiullah, S. D. Ahmed, and F. A. Al-Sulaiman, "Grid integration challenges and solution strategies for solar PV systems: A review," *IEEE Access*, vol. 10, pp. 52233–52257, 2022.
[3] P. Roy, J. He, T. Zhao, and Y. V. Singh, "Recent advances of wind-solar hybrid renewable energy systems for power generation: A review," *IEEE Open J. Ind. Electron. Soc.*, vol. 3, no. 1, pp. 81–104, Jan. 2022.
[4] V. Sharma, A. Cortes, and U. Cali, "Use of forecasting in energy storage applications: A review," *IEEE Access*, vol. 9, pp. 114690–114704, 2021.
[5] J. I. Leon, E. Dominguez, L. Wu, A. Marquez Alcaide, M. Reyes, and J. Liu, "Hybrid energy storage systems: Concepts, advantages, and applications," *IEEE Ind. Electron. Mag.*, vol. 15, no. 1, pp. 74–88, Mar. 2021.
[6] Y. Guan, C. Cecati, J. M. Alonso, and Z. Zhang, "Review of high-frequency high-voltage-conversion-ratio DC–DC converters," *IEEE J. Emerg. Sel. Topics Ind. Electron.*, vol. 2, no. 4, pp. 374–389, Oct. 2021.
[7] T. Yao, C. Nan, and R. Ayyanar, "A new soft-switching topology for switched inductor high gain boost," *IEEE Trans. Ind. Appl.*, vol. 54, no. 3, pp. 2449–2458, May/Jun. 2018.
[8] A. Ajami, H. Ardi, and A. Farakhor, "A novel high step-up DC/DC converter based on integrating coupled inductor and switched-capacitor techniques for renewable energy applications," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4255–4263, Aug. 2015.
[9] R. J. Wai and R. Y. Duan, "High step-up converter with coupled-inductor," *IEEE Trans. Power Electron.*, vol. 20, no. 5, pp. 1025–1035, Sep. 2005.
[10] M. S. Bhaskar, D. J. Almakhles, S. Padmanaban, F. Blaabjerg, U. Subramaniam, and D. M. Ionel, "Analysis and investigation of hybrid DC–DC non-isolated and non-inverting nx interleaved multilevel boost converter (Nx-IMBC) for high voltage step-up applications: Hardware implementation," *IEEE Access*, vol. 8, pp. 87309–87328, 2020.
[11] A. Rajabi, A. Rajaei, V. M. Tehrani, P. Dehghanian, J. M. Guerrero, and B. Khan, "A non-isolated high step-up DC-DC converter using voltage lift technique: Analysis, design, and implementation," *IEEE Access*, vol. 10, pp. 6338–6347, 2022.
[12] K. R. Kothapalli, M. R. Ramteke, H. M. Suryawanshi, N. K. Reddi, and R. B. Kalahasthi, "A coupled inductor based high step-up converter for DC microgrid applications," *IEEE Trans. Ind. Electron.*, vol. 68, no. 6, pp. 4927–4940, Jun. 2021.
[13] M. L. Alghaythi, R. M. O'Connell, N. E. Islam, M. M. S. Khan, and J. M. Guerrero, "A high step-up interleaved DC-DC converter with voltage multiplier and coupled inductors for renewable energy systems," *IEEE Access*, vol. 8, pp. 123165–123174, 2020.
[14] Q. Zhao and F. C. Lee, "High-efficiency, high step-up DC-DC converters," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 65–73, Jan. 2003.
[15] T.-J. Liang, J.-H. Lee, S.-M. Chen, J.-F. Chen, and L.-S. Yang, "Novel isolated high-step-up DC–DC converter with voltage lift," *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1483–1491, Apr. 2013.
[16] H. Wu, T. Mu, H. Ge, and Y. Xing, "Full-range soft-switching-isolated buck-boost converters with integrated interleaved boost converter and phase-shifted control," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 987–999, Feb. 2016.
[17] I.-H. Cho, Y.-D. Kim, and G.-W. Moon, "A half-bridge LLC resonant converter adopting boost PWM control scheme for hold-up state operation," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 841–850, Feb. 2014.
[18] P. Jia and Y. Mei, "Derivation and analysis of a secondary-side LLC resonant converter for the high step-up applications," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 5, pp. 5865–5882, Oct. 2021.
[19] S. Jalbrzykowski and T. Citko, "Current-fed resonant full-bridge boost DC/AC/DC converter," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1198–1205, Mar. 2008.
[20] R.-Y. Chen, T.-J. Liang, J.-F. Chen, R.-L. Lin, and K.-C. Tseng, "Study and implementation of a current-fed full-bridge boost DC–DC converter with zero-current switching for high-voltage applications," *IEEE Trans. Ind. Appl.*, vol. 44, no. 4, pp. 1218–1226, Jul./Aug. 2008.
[21] D. R. Nayanasiri, G. H. B. Foo, D. M. Vilathgamuwa, and D. L. Maskell, "A switching control strategy for single- and dual-inductor current-fed push–pull converters," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 3761–3771, Jul. 2015.
[22] Y. Shi, R. Li, Y. Xue, and H. Li, "Optimized operation of current-fed dual active bridge DC–DC converter for PV applications," *IEEE Trans. Ind. Electron.*, vol. 62, no. 11, pp. 6986–6995, Nov. 2015.
[23] M. Forouzesh, Y. Shen, K. Yari, Y. P. Siwakoti, and F. Blaabjerg, "High-efficiency high step-up DC–DC converter with dual coupled inductors for grid-connected photovoltaic systems," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 5967–5982, Jul. 2018.

[24] G. Spiazzi and S. Buso, "Analysis of the interleaved isolated boost converter with coupled inductors," *IEEE Trans. Ind. Electron.*, vol. 62, no. 7, pp. 4481–4491, Jul. 2015.
[25] P. Xuewei and A. K. Rathore, "Novel interleaved bidirectional snubberless soft-switching current-fed full-bridge voltage doubler for fuel-cell vehicles," *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5535–5546, Dec. 2013.
[26] J.-H. Lee, T.-J. Liang, and J.-F. Chen, "Isolated coupled-inductor-integrated DC–DC converter with nondissipative snubber for solar energy applications," *IEEE Trans. Ind. Electron.*, vol. 61, no. 7, pp. 3337–3348, Jul. 2014.
[27] R. Faraji, H. Farzanehfard, M. Esteki, and S. A. Khajehoddin, "A lossless passive snubber circuit for three-port DC–DC converter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 2, pp. 1905–1914, Apr. 2021.
[28] X. Pan, H. Li, Y. Liu, T. Zhao, C. Ju, and A. K. Rathore, "An overview and comprehensive comparative evaluation of current-fed-isolated-bidirectional DC/DC converter," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2737–2763, Mar. 2020.
[29] A. K. Singh, P. Das, and S. K. Panda, "Analysis and design of SQR-based high-voltage LLC resonant DC–DC converter," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4466–4481, Jun. 2017.
[30] S. Tandon and A. K. Rathore, "Analysis and design of series LC partial-resonance-pulse-based ZCS current-fed push-pull converter," *IEEE Trans. Ind. Appl.*, vol. 57, no. 4, pp. 4232–4241, Jul./Aug. 2021.
[31] J.-I. Baek, J.-K. Kim, J.-B. Lee, H.-S. Youn, and G.-W. Moon, "A boost PFC stage utilized as half-bridge converter for high-efficiency DC–DC stage in power supply unit," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7449–7457, Oct. 2017.
[32] G. Spiazzi, P. Mattavelli, and A. Costabeber, "High step-up ratio flyback converter with active clamp and voltage multiplier," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3205–3214, Nov. 2011.
[33] J. Liu, K. Wang, Z. Zheng, C. Li, and Y. Li, "A dual-active-clamp quasi-resonant isolated boost converter for PV integration to medium-voltage DC grids," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 4, pp. 3444–3456, Dec. 2020.
[34] N. Yang, J. Zeng, R. Hu, and J. Liu, "Analysis and design of an isolated high step-up converter without voltage-drop," *IEEE Trans. Power Electron.*, vol. 37, no. 6, pp. 6939–6950, Jun. 2022.
[35] Z. Wang, Z. Zheng, and C. Li, "A high-step-up low-ripple and high-efficiency DC-DC converter for fuel-cell vehicles," *IEEE Trans. Power Electron.*, vol. 37, no. 3, pp. 3555–3569, Mar. 2022.
[36] Y. Wang, W. Liu, H. Ma, and L. Chen, "Resonance analysis and soft-switching design of isolated boost converter with coupled inductors for vehicle inverter application," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1383–1392, Mar. 2015.
[37] Y. Lu, Y. Xing, and H. Wu, "A PWM plus phase-shift controlled interleaved isolated boost converter based on semiactive quadrupler rectifier for high step-up applications," *IEEE Trans. Ind. Electron.*, vol. 63, no. 7, pp. 4211–4221, Jul. 2016.
[38] M.-K. Nguyen, Y.-C. Lim, J.-H. Choi, and G.-B. Cho, "Isolated high step-up DC–DC converter based on quasi-switched-boost network," *IEEE Trans. Ind. Electron.*, vol. 63, no. 12, pp. 7553–7562, Dec. 2016.
[39] K. Zaoskoufis and E. C. Tatakis, "Isolated ZVS-ZCS DC–DC high step-up converter with low-ripple input current," *IEEE J. Emerg. Sel. Topics Ind. Electron.*, vol. 2, no. 4, pp. 464–480, Oct. 2021.
[40] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications, and Design*. Hoboken, NJ, USA: Wiley, 2007.
[41] R.-J. Wai and Z.-F. Zhang, "High-efficiency single-input triple-outputs DC-DC converter with zero-current switching," *IEEE Access*, vol. 7, pp. 84952–84966, 2019.
[42] R.-J. Wai and Z.-F. Zhang, "Design of high-efficiency isolated bidirectional DC/DC converter with single-input multiple-outputs," *IEEE Access*, vol. 7, pp. 87543–87560, 2019.
[43] H. Ma, L. Chen, and Z. Bai, "An active-clamping current-fed push-pull converter for vehicle inverter application and resonance analysis," in *Proc. IEEE Int. Symp. Ind. Electron.*, 2012, pp. 160–165, doi: 10.1109/ISIE.2012.6237077.
[44] M. Delshad and H. Farzanehfard, "A new soft switched push pull current fed converter for fuel cell applications," *Energy Convers. Manage.*, vol. 52, no. 2, pp. 917–923, Aug. 2011.

Kuan-Pin Huang was born in Taipei, Taiwan, in 1991. He received the B.S. degree in electric engineering from the National Taiwan Ocean University, Keelung, Taiwan, in 2014, and the M.S. degree in electrical engineering from the Chung Yuan Christian University, Chung Li, Taiwan, in 2016. He is currently working toward the Ph.D. degree in electronic and computer engineering with the National Taiwan University of Science and Technology, Taipei, Taiwan.

His research interests include power electronics and battery charger.

Rong-Jong Wai (Senior Member, IEEE) was born in Tainan, Taiwan, in 1974. He received the B.S. degree in electrical engineering and the Ph.D. degree in electronic engineering from the Chung Yuan Christian University, Chung Li, Taiwan, in 1996 and 1999, respectively.

From 1998 to 2015, he was with the Yuan Ze University, Chung Li, Taiwan, where he was the Dean of General Affairs from 2008 to 2013, and the Chairman of the Department of Electrical Engineering from 2014 to 2015. Since August 2015, he has been with the National Taiwan University of Science and Technology, Taipei, Taiwan, where he was the Dean of General Affairs from 2018 to 2021, and he is currently a Distinguished Professor, and the Director of the Energy Technology and Mechatronics Laboratory. He has authored more than 180 conference papers, more than 210 international journal papers, and 61 inventive patents. His research interests include power electronics, motor servo drives, mechatronics, energy technology, and control theory applications. The outstanding achievement of his research is for contributions to real-time intelligent control in practical applications and high-efficiency power converters in energy technology.

Dr. Wai is a fellow of the Institution of Engineering and Technology (U.K.). He was the recipient of the Excellent Research Award in 2000, and the Wu Ta-You Medal and Young Researcher Award in 2003 from the National Science Council, Taiwan. In addition, he was the recipient of the Outstanding Research Award in 2003 and 2007 from the Yuan Ze University, Taiwan; the Excellent Young Electrical Engineering Award and the Outstanding Electrical Engineering Professor Award in 2004 and 2010 from the Chinese Electrical Engineering Society, Taiwan; the Outstanding Professor Award in 2004 and 2008 from the Far Eastern Y. Z. Hsu-Science and Technology Memorial Foundation, Taiwan; the International Professional of the Year Award in 2005 from the International Biographical Centre, U.K.; the Young Automatic Control Engineering Award in 2005 from the Chinese Automatic Control Society, Taiwan; the Yuan-Ze Chair Professor Award in 2007, 2010, and 2013 from the Far Eastern Y. Z. Hsu-Science and Technology Memorial Foundation, Taiwan; the Electric Category-Invent Silver Medal Award in 2007, the Electronic Category-Invent Gold and Silver Medal Awards in 2008, the Environmental Protection Category-Invent Gold Medal Award in 2008, the Most Environmental Friendly Award in 2008, the Power Category-Invent Bronze Medal Award in 2012, and the Electronic Category-Invent Gold and Silver Medal Awards in 2015 from the International Invention Show and Technomart, Taipei, Taiwan; the University Industrial Economic Contribution Award in 2010 from the Ministry of Economic Affairs, Taiwan; the Ten Outstanding Young Award in 2012 from the Ten Outstanding Young Person's Foundation, Taiwan; the Taiwan Top 100 MVP Managers Award in 2012 from MANAGER today magazine, Taiwan; the Outstanding Engineering Professor Award in 2013 from the Chinese Institute of Engineers, Taiwan; the Green Technology Category-Scientific Paper Award in 2014 from the Far Eastern Y. Z. Hsu-Science and Technology Memorial Foundation, Taiwan, the Scopus Young Researcher Lead Award-Computer Science in 2014 from Taiwan Elsevier; the Outstanding Research Award in 2016, 2018, and 2020, and the Excellent Research Award in 2022 from the National Taiwan University of Science and Technology, Taiwan; the Most Cited Researchers Award in 2016 (Field: Electrical & Electronics Engineering); and the World's Top 2% of Scientists (Rank 17th in 2020, Rank 19th in 2021, and Rank 20th in 2022, Field: Electrical & Electronics Engineering), the Teaching Excellence Award in 2021 from the National Taiwan University of Science and Technology, Taiwan, and the Top Scientists in Taiwan (301th Ranking in World and 3rd Ranking in Taiwan, Field: Electronics and Electrical Engineering) published by Research.com in 2022.