Demonstration of Low *DV/DT* Class-Φ_2 DC-DC Converter With 50% Duty Cycle

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***Abstract*—This article presents the frequency-domain-based modified impedance tuning analysis (ITA) method and its demonstration in designing a class-Φ_2 dc–dc converter with load-independent zero voltage switching (ZVS) characteristics. By adjusting the second-order harmonic voltage, a near trapezial drain-to-source voltage ($V_{\rm DS}$) is achieved with beneficially reduced voltage stresses across the main power devices. A complete non-iteration design procedure is established. Comparing to traditional ITA design theory, this modified ITA method leads to low *dv/dt* and low $V_{\rm DS}$ stress, even at 50% switching duty cycles. In addition, thanks to the finite input resistance of the rectifier, the output resonant network and rectifier designed following this frequency-domain method feature the extensive load-independent ZVS characteristic. The 5 MHz prototype aiming for a true short-circuit to open-circuit load-independent ZVS is designed using modified ITA method, assembled, and measured. Under 16 V input, the measured conversion efficiency maintains 76.8%–89.5% in the testable load range from 7.4 to 16.8 W.**

***Index Terms*—DC power conversion, frequency domain analysis, impedance tuning analysis (ITA), wide load operation.**

I. Introduction

HIGH-EFFICIENT power converters are widely demanded in modern industrial electronics. In the past decade, the wide bandgap power semiconductor has boosted converters into higher switching frequency regimes [1], [2] and higher voltage regimes [3], [4]. Among various topologies, the single-ended resonant dc/dc converter (SRDC) requires fewer power switches and simple driving circuitries and becomes attractive in compact, efficient, and MHz applications. However, it is essential to ensure that the SRDC maintains the soft switching or zero voltage switching (ZVS) characteristic to avoid power switch conduction loss overheads [5], [6], [7], [8], [9], [10], [11].

In [12], the class-E SRDC was firstly introduced at MHz operations. The SRDC achieves soft switching characteristics with ZVS across the power switch. Hence, thanks to the merits of ZVS and tunable output power, the class-E SRDC have been widely explored by the academy and industry [13], [14], [15], [16], [17], [18]. However, the drain-to-source voltage ($V_{\rm DS}$) stress across the power switch is as high as $>4V_{\rm IN}$, which consequently presents a bottleneck to power device voltage ratings and limits the input voltage range of the SRDCs [19].

To tackle the $V_{\rm DS}$ stress issue, an extra resonant tank stores/releases resonance energy in the class-E inverter, whose topology was later named the class-Φ_2 inverter [20]. The class-Φ_2 converter features a quasi-trapezoidal $V_{\rm DS}$ waveform, which tackles the $V_{\rm DS}$ stress by reducing its maximal value. The waveform results mainly from the superposition of the fundamental and third-order harmonics of switching frequency, where all of the second harmonic components is shorted to be null. Among the state-of-art of class-Φ_2 converter, the low voltage stress was achieved with a switching duty cycle smaller than 0.4 [21], [22]. For example, a 10 MHz step-down Class-Φ_2 dc–dc converter with only four resonant elements was proposed in [23], it operates with $V_{\rm DS}$ voltage stress of 2.2–2.5 $V_{\rm IN}$ under a switching duty cycle of 0.37–0.4. In [24], a 27.12 MHz Class-Φ_2 dc—ac inverter was proposed, it operates with $V_{\rm DS}$ voltage stress of $2V_{\rm IN}$ under a switching duty cycle of 0.3. The small duty cycle, however, leads to very short turn-ON time at high switching frequency which challenges the design of gate driver. Recently, time-domain method was proposed to model the class-Φ_2 converter with linear differential equations so that the converter operates with quasi-trapezoidal $V_{\rm DS}$ waveform at any switching duty cycle [25]. The equations successfully guide the design of class-Φ_2 converters; however, the specific boundary conditions are required to simplify the complicated resonance which requires parameter tuning for low *dv/dt* and ZVS [26]. As shown in Fig. 1, all the existing class-Φ_2 circuits feature a switching duty cycle less than 0.4.

In this article, we establish a modified impedance tuning analysis (ITA) method for the class-Φ_2 SRDC designs, aiming for the 50% duty cycle operation. It builds a nonlinear parameteitic model for controlling the *dv/dt* of the $V_{\rm DS}$ waveform, and a fundamental-frequency equivalent circuit model for the power transfer analysis. It enables a near-trapezoidal $V_{\rm DS}$ waveform by adjusting the amplitude of the second-order harmonic voltage and realizes the ZVS feature without tuning the switching duty cycle. Typically, the ZVS is hard to maintain in SRDCs due to load variation and different resonant modals of the output resonant network (ORN) and load conditions [27]. In this article,

Manuscript received 5 April 2023; revised 1 July 2023 and 9 August 2023; accepted 8 September 2023. Date of publication 12 September 2023; date of current version 23 October 2023. The work was supported by the National Natural Science Foundation of China under Grant U2241220. Recommended for publication by Associate Editor L. Corradini. *(Corresponding author: Fanyi Meng.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3314445.

Digital Object Identifier 10.1109/TPEL.2023.3314445

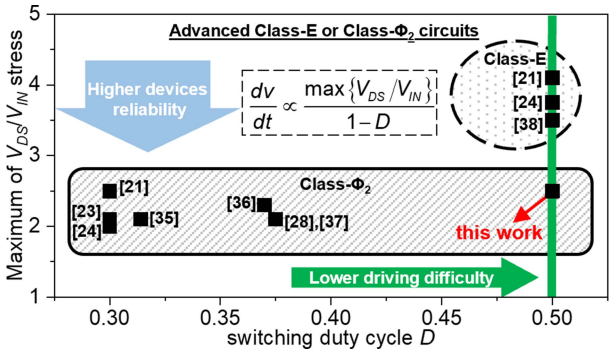

Fig. 1. Switching duty cycles and max V_{DS}/V_{IN} stress of the state-of-the-art class-E [21], [24], [38] and class-Φ_2 [21], [23], [24], [28], [35], [36], [37] based circuits, including DC-to-AC and DC-to-DC ones.

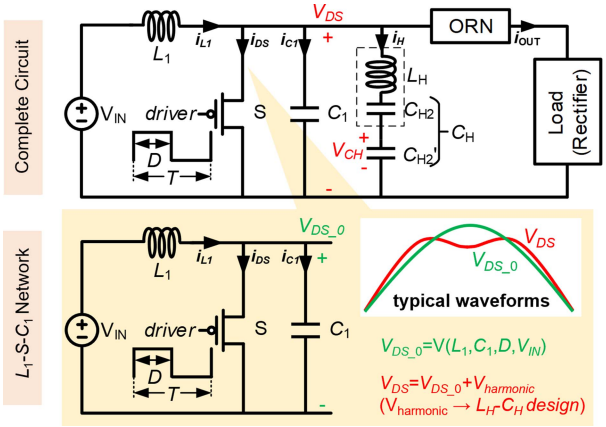

Fig. 2. Schematic of class-Φ_2 based dc–dc converter (capacitor C_H is divided into C_{H2} and C_{H2}' to facilitate the analysis) as well as the L_1-S-C_1 network.

the quality-factor the characteristic impedance of the rectifier is co-optimized together with the ORN, ensuring little $V_{\rm DS}$ waveform distortion and good ZVS feature at wide-range load conditions without the help of any external control circuit.

The rest of the article is organized as follows: Section II presents the proposed modified ITA design method with theoretical derivations. Section III discusses the effects of the ORN and rectifier on the ZVS realization of the class-Φ_2 inverter and the parallel resonator and cascaded Class-DE for load-independent ZVS extension. Section IV summarizes the design procedure and presents the experimental results of a 5 MHz prototype. Finally, Section V gives the discussion and concludes the article.

II. Modified ITA Method

Fig. 2 gives the block schematic of a class-Φ_2 dc–dc converter, where the power switch S is driven by signals with frequency f_0 and duty cycle D. For simplify, the ORN and load branches are ignored at first [26], the passive network is treated as a parallel connection of L_1-C_1 pair and L_H-C_H pair. Then the impedance of the network seen from the drain port of S, denoted as $Z_{\rm DS}$, is written as

$$Z_{\rm DS}=\frac{j\omega L_1(1-\omega^2 L_H C_H)}{\omega^4 L_1C_1L_HC_H-\omega^2(L_1C_1+L_HC_H+L_1C_H)+1}. \quad (1)$$

According to the traditional ITA design theory [20], [22], [23], the second-order harmonic voltage should be a zero of $Z_{\rm DS}$, and the poles of $Z_{\rm DS}$ must locate near the fundamental and the third-order harmonic frequencies. The first pole is a bit higher than the fundamental frequency to achieve ZVS, and the second pole is a bit lower than third-order harmonic frequency to ensure an in-phase response [16], [24], [28]. However, as shown in Fig. 3(a), the V_{DS} waveform following the traditional design theory shows large dv/dt and voltage stress at 50% switching duty cycle. The following conditions are assumed for the following analysis.

1) All passive elements are lossless and linear.
2) The power device is treated as an ideal switch.
3) The duty cycle of the power switch is denoted as D, while the switching frequency and period are f_0/ω_0 and T, respectively.

A. L_1-S-C_1 Network

In this section, the three-element circuit L_1-S-C_1 is primarily analyzed (neglecting other elements). As shown in Fig. 2, the power switch S is paralleled with input inductor L_1 and capacitor C_1, driven by signal with duty cycle of D. As S turns on at $(1-D_0)T < t < T$ period, the $V_{\rm DS\_0}$ is clamped to zero. As S turns OFF at $(1-D_0)T < t < T$ period, the $V_{\rm DS\_0}$ close-form expressions are derived as

$$\begin{cases} L_1C_1\dfrac{dV_{\rm DS\_0}^2}{dt^2}+V_{\rm DS\_0}=V_{\rm IN} \\ V_{\rm DS\_0}|_{t=0}=0,\ \dfrac{2}{T}\int_0^{(1-D)T}V_{\rm DS\_0}=2V_{\rm IN} \\ V_{\rm DS\_0}=[A\sin(\lambda_1\omega_0 t)-\cos(\lambda_1\omega_0 t)+1]\,V_{\rm IN} \\ A=\dfrac{\lambda_1\pi+\sin(\lambda_1\pi)}{1-\cos(\lambda_1\pi)} \\ \lambda_1=\dfrac{1}{\omega_0\sqrt{L_1C_1}} \end{cases}. \quad (2)$$

It is noted that the $V_{\rm DS\_0}$ generated by the L_1-S-C_1 network is merely a function of λ_1. Then the zero points of the $V_{\rm DS\_0}$ expression (t_{01} and t_{02}) can be solved with a switching duty cycle, as follows:

$$t_{01}=\frac{2n\pi}{\lambda_1\omega_0}, t_{02}=\frac{\pi/2+2\varphi+n\pi}{\lambda_1\omega_0}, n=0,1,2,\ldots, \quad (3)$$

where $\varphi=\arctan(1/A)$, if $n=0$, the critical duty cycle D_0 that makes the $V_{DS\_0}|_{t=(1\text{-}D0)T}$ just drop to zero is obtained. Thus, the $V_{\rm DS\_0}$ generated by the L_1-S-C_1 network is able to be treated as a half-sine waveform (like the green curve in Fig. 2) with fundamental frequency $f_{\rm eq}$ (angular frequency is $\omega_{\rm eq}$). The parameters D_0 and $\omega_{\rm eq}$ are written as

$$D_0=\frac{(4\lambda_1-1)\pi+4\varphi}{4\pi\lambda_1}, \omega_{\rm eq}=2\pi f_{\rm eq}=\frac{\pi}{D_0T}. \quad (4)$$

B. Inclusion Effect of Second-Order Harmonic Voltage

Instead of forcing the second-order harmonic impedance of $Z_{\rm DS}$ to zero, the role of second harmonic voltage is customized in the proposed modified ITA method [see Fig. 3(b)]. In time-domain waveform analysis, the quasi-trapezoidal $V_{\rm DS}$ is

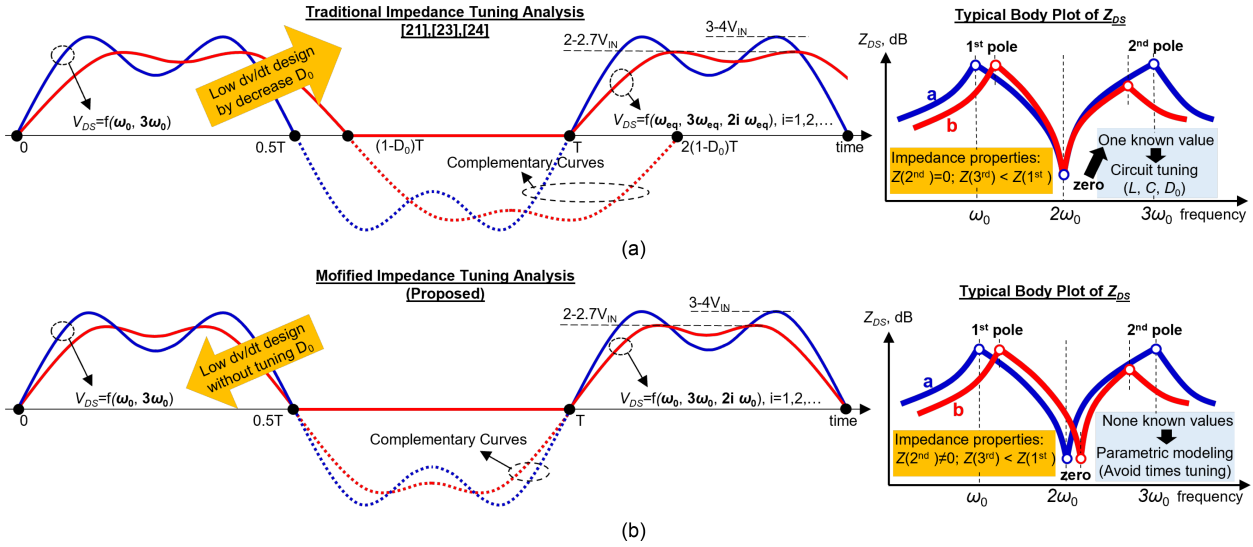

Fig. 3. Frequency-domain design and V_{DS} waveforms according to (a) traditional ITA and (b) proposed modified ITA method.

expressed as follows:

$$V_{\mathrm{DS}}=\begin{cases}0, & -2\pi\left(1-D_0\right)<t<0\\ A_0\left[\sin\left(\omega_{\mathrm{eq}}t\right)+k_3\sin\left(3\omega_{\mathrm{eq}}t+\phi_3\right)\right], & 0<t<2\pi D_0\end{cases} \tag{5}$$

where k_3 refers to the amplitude factor of the third-order harmonic voltage component with respect to the fundamental, the phase φ_3 is ignored as 0. Deriving with the Fourier expansion, (5) is written as

$$V_{\mathrm{DS}}\left(\mathrm{t}\right)=\frac{a_0}{2}+\sum_{m=0}^{\infty}\left(a_m\cos\left(m\omega_{\mathrm{eq}}t\right)+b_m\sin\left(m\omega_{\mathrm{eq}}t\right)\right). \tag{6}$$

Specifically, the expression of V_{DS} is written as (7) shown at the bottom of this page, when $\omega_{\mathrm{eq}}=2\pi/T$ ($D_0=0.5$). It is seen from (7) that the *dv/dt* of V_{DS} is contributed from the third and series of oven-order voltage harmonic components. Each amplitude coefficient of the corresponding voltage harmonic term in (7) is plotted in Fig. 4(a), normalized by A_0. Fig. 4(a) shows that the second/fourth harmonic voltage components negatively/positively affect the content of the third harmonic voltage, respectively. It is also noted that all the harmonic voltages can be normalized through parameter k_3. It is inconvenient for the class-Φ_2 topology to adjust the fourth-order voltage harmonic, this is because another pole (higher than fourth harmonic frequency) is required to place a zero near fourth harmonic frequency and one more resonant branch must be added, so it becomes a proper choice to achieve different *dv/dt* by adjusting the second-order harmonic voltage component.

According to Fig. 2, a series branch L_H-C_H ($C_H=C_{H2}\|C_{H2}$') is paralleled across the shunting capacitor C_1. By setting the

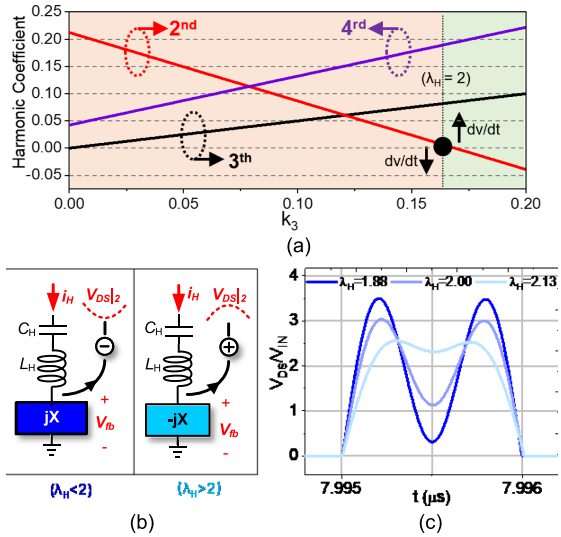

Fig. 4. (a) Harmonic coefficients as function of parameter k_3. (b) Schematic of the mechanism of tuning the second harmonic voltage with the harmonic branch L_H-C_H. (c) V_{DS} waveforms of different λ_H values. (The waveforms are simulated at 5MHz, $D_0=0.5$, $L_1/L_H=0.5$, the value of λ_H is only controlled by adjusting C_H).

resonant frequency of L_H-C_{H2} branch to $2\omega_{\mathrm{eq}}$, a pure second-order harmonic current is generated, as follows:

$$i_H=I_H\sin\left(2\omega_{\mathrm{eq}}t\right),\ \frac{1}{\sqrt{L_HC_{H2}}}=2\omega_{\mathrm{eq}}. \tag{8}$$

Considering the equivalent circuits of L_H-C_H branch shown in Fig. 4(b), where an external negative/positive impedance (the jX or $-jX$ are seen at $2\omega_{\mathrm{eq}}$) is series connected with the L_H–C_{H2} pair as $\lambda_H>2/\lambda_H<2$ respectively. A positive impedance jX

$$V_{\mathrm{DS}}(t)=A_0\left\{\frac{6+2k_3}{3\pi}+\frac{1}{2}\sin\left(\omega_{\mathrm{eq}}t\right)+\frac{k_3}{2}\sin\left(3\omega_{\mathrm{eq}}t\right)-\sum_m\left\{\left[\frac{2}{\pi\left(m^2-1\right)}+\frac{2k_3}{\pi\left(m^2-9\right)}\right]\cos\left(m\omega_{\mathrm{eq}}t\right)\right\}\right\},(m=2,4,\ldots)., \tag{7}$$

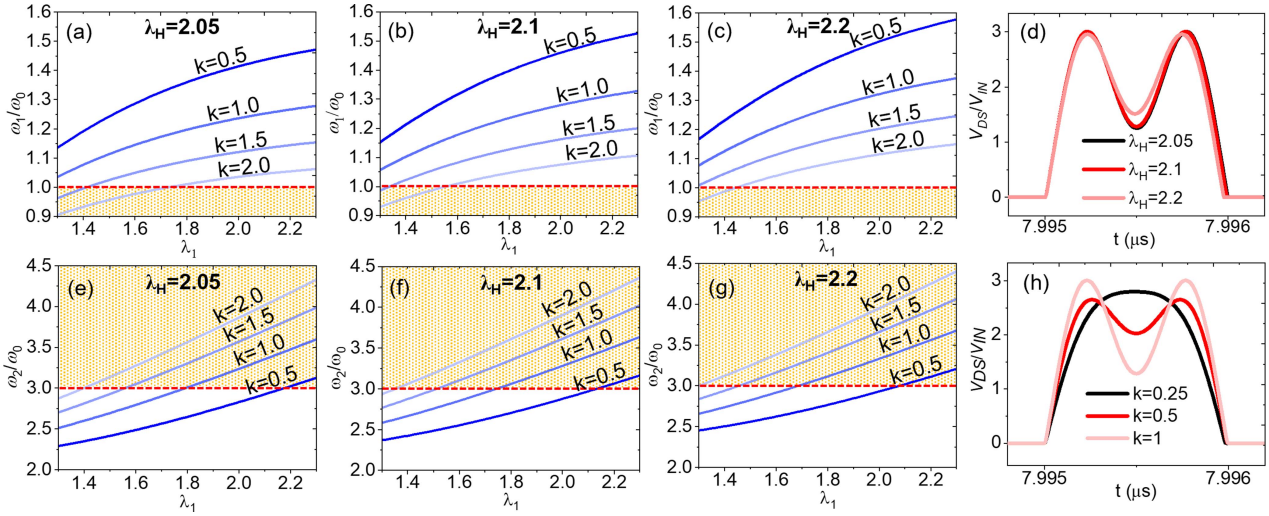

Fig. 5. Solutions of ω_1 in condition of (a) $\lambda_H = 2.05$, (b) $\lambda_H = 2.1$, (c) $\lambda_H = 2.2$; Solutions of ω_2 in condition of (e) $\lambda_H = 2.05$, (f) $\lambda_H = 2.1$, (c) $\lambda_H = 2.2$. (d) $V_{\rm DS}$ waveforms for different λ_H values with $k = 1$. (h) $V_{\rm DS}$ waveforms for different k values with $\lambda_H = 2.1$. $D = 0.5$. (λ_1: $1.29 \sim 2.3$).

($\lambda_H < 2$) will generate a negative second harmonic voltage $V_{\rm DS}|_2$, while a negative impedance *-jX* ($\lambda_H > 2$) leads a positive second harmonic voltage $V_{DS}|_2$. Fig. 4(a) has indicated that a positive second harmonic coefficient is helpful to mitigate the *dv/dt*, therefore, the resonant L_H−C_H pair should show negative impedance at $2\omega_{\rm eq}$.

For obtaining the negative impedance, a series capacitor C_{H2}' is connected to the C_{H2}, which makes the branch L_H-C_H show capacitive at $2\omega_{\rm eq}$. As shown in Fig. 4, If the resonant frequency of L_H-C_H is $\lambda_H\omega_{\rm eq}$, then the relationship between the C_{H2} and C_{H2}' is written as:

$$\frac{1}{\sqrt{(L_H C_{H2} C'_{H2})/(C_{H2}+C'_{H2})}} = \lambda_H \omega_{\rm eq}. \tag{9}$$

Fig. 4(c) presents a set of simulated $V_{\rm DS}$ waveforms with different λ_H values, the max voltage stress of the waveform with $\lambda_H = 2.13$ is only $2.5V_{\rm IN}$, thus low *dv/dt* is also achieved.

C. Modified ITA Application in Class-Φ_2 Inverter

Base on the above analysis, the values of L_1 and C_1 determine the fundamental component of $V_{\rm DS}$ waveform and ZVS realization of the single ground-connected power switch, while the values of the L_H and C_H determine the harmonic voltage components and the *dv/dt* of the $V_{\rm DS}$ waveform. In the analysis of this section, the ORN and load are neglected. Then, the $Z_{\rm DS}$ expression in (1) is modified according to the frequency-domain principle, as follows:

$$Z_{\rm DS} = \frac{j\omega L_1 \left(1 - (\omega/\omega_0)^2 \cdot \left(1/\lambda_H^2\right)\right)}{(\omega/\omega_0)^4 - (\omega/\omega_0)^2 \left(\lambda_H^2 + \lambda_1^2 + k\lambda_1^2\right) + \lambda_1^2\lambda_H^2}, \tag{10}$$

where $k = L_1/L_H$, ω_0 is equal to $\omega_{\rm eq}$ as $D_0 = 0.5$. Locating the poles of $Z_{\rm DS}$ at specific frequencies has been studied to be efficient for shaping the $V_{\rm DS}$ waveform [23], where the first pole should be a bit larger than ω_0 and the other pole should be a bit lower than $3\omega_0$.

The poles of (10) ((ω_1/ω_0) and (ω_2/ω_0)) are solved as follows:

$$\left(\frac{\omega_1}{\omega_0}\right) = \frac{\lambda_H^2 + (k+1)\lambda_1^2 - \sqrt{[\lambda_H^2 + (k+1)\lambda_1^2 - 4\lambda_H^2\lambda_1^2]}}{2} \tag{11}$$

$$\left(\frac{\omega_2}{\omega_0}\right) = \frac{\lambda_H^2 + (k+1)\lambda_1^2 + \sqrt{[\lambda_H^2 + (k+1)\lambda_1^2 - 4\lambda_H^2\lambda_1^2]}}{2}. \tag{12}$$

If the value of λ_H is predetermined, the poles are function of k and λ_1. Fig. 5(a), (b) and (c) present the located frequencies of (ω_1/ω_0) ver. λ_1 at different k and λ_H, while Fig. 5(e), (f), and (g) present those results for located frequencies of (ω_2/ω_0). To maintain low *dv/dt* at $D_0 = 0.5$, the λ_H is set as 2.05, 2.1 and 2.2. When k is lower than 1, the poles contents $(\omega_1/\omega_0)>1$ and $(\omega_2/\omega_0) < 3$ across wide range of parameter λ_1, indicating that these circuits have more free adjustment margin for ZVS realization. Fig. 5(d) and (h) plot the simulated V_{DS} waveforms in condition of fixing k and λ_H. The waveforms have no obvious correlation with λ_H, but are shown as almost linear function with k. Specially, the V_{DS} returns to half-sine waveform as the parameter $k < 0.25$. Thus, in practical design, low *dv/dt* $V_{\rm DS}$ is guaranteed by two conditions: λ_H is a bit higher than 2, which is the fixed value in traditional ITA method; and k is between 0.25 to 2.

It is seen that λ_1 and λ_H refer to the relationships between L_1, C_1 and L_H, C_H, whereas the parameter k describes the relationship between L_1 and L_H. Then, all the resonant elements are determined after selecting L_1 and L_H. In practice, the values of L_1 and L_H are selected according to the amplitude of loop current in the inverter stage following the equation:

$$\vec{V}_{\rm DS} - V_{\rm IN} = (j\omega L_1)\,\vec{I}_{L_1} \tag{13}$$

$$\vec{V}_{\rm DS} = \left(j\omega L_H + \frac{\lambda_H^2 \omega_{\rm eq}^2 L_H}{j\omega}\right)\vec{I}_H \tag{14}$$

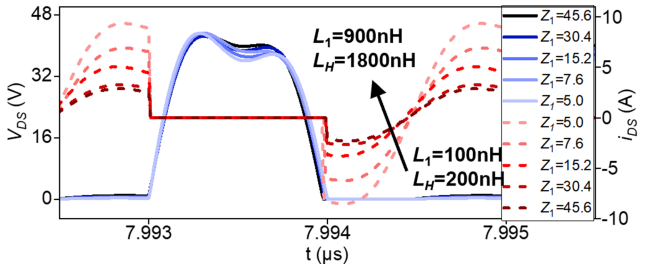

Fig. 6. Simulated V_{DS} and i_{DS} waveforms under L_1 ranged from 100 nH to 900 nH, where $k = 0.5$, $\lambda_H = 2.08$, $f_{\rm eq} = 5$ MHz, and $V_{\rm IN} = 16$ V. The output power of any case is 16.8 W.

TABLE I
TUF COMPARISON OF ZVS RESONANT CONVERSION TOPOLOGIES

	Topology	V_{DS_p}/V_{IN}	N	TUF
Simulated low *dv/dt* Class-Φ_2 in this work	Class-Φ_2 (D=50%, Z_1=5.0)	2.62	1	0.08
	Class-Φ_2 (D=50%, Z_1=7.6)	2.62	1	0.11
	Class-Φ_2 (D=50%, Z_1=15.2)	2.62	1	0.18
	Class-Φ_2 (D=50%, Z_1=30.4)	2.62	1	0.25
	Class-Φ_2 (D=50%, Z_1=45.6)	2.62	1	0.29
Data from [29]	Class-Φ_2 (D=30%)	2.1	1	0.25
	Class-E	3.6	1	0.18
	Push-pull Class-Φ_2	2.1	2	0.25
	Series-Stacked PPT Φ_2	1.05	2	0.25
	Class-DE	1	2	0.26
	Class-D	1	2	0.32

$$\vec{I}_{L_1} = \vec{I}_{\rm DS} + \vec{I}_{C_1} + \vec{I}_H\,. \tag{15}$$

It is noted from (15) that the high loop current i_{L1} and i_H lead to high injection currents into the power switch, and increase the conduction loss. To properly select the inductance of L_1 and L_H, the transistor utilization factor (TUF) is utilized, which is defined as the ratio of the output power to the total product of the peak of $V_{\rm DS}$ ($V_{\rm DS\_p}$) and the root-mean-square value of $i_{\rm DS}$ ($I_{\rm DS\_r}$) [29], as follows:

$$\text{TUF} = \frac{P_{\rm OUT}}{N \cdot V_{\rm DS\_p} \cdot I_{\rm DS\_r}} \times 100\% \tag{16}$$

where N refers to the number of power switches. Fig. 6 shows the simulated $V_{\rm DS}$ and $i_{\rm DS}$ waveforms under different L_1. It is noted that the case with larger L_1 shows smaller switch current, indicating lower conduction loss and larger conversion efficiency. A general definition of L_1 is as follows:

$$L_1 = \frac{Z_1}{\lambda_1 \omega_{\rm eq}}, Z_1 = \sqrt{\frac{L_1}{C_1}}. \tag{17}$$

The inductance of L_1 varies with the fundamental frequency $\omega_{\rm eq}$, so it is useful for designer to select L_1 by setting parameter Z_1 (Z_1 is independent to circuit's frequency and power) at different operation frequency and specific λ_1. Table I gives the TUF of the cases in Fig. 6 and other popular ZVS resonant conversion topologies for comparison. The Class-Φ_2 SRDC shows TUF of larger than 0.18 as Z_1 is larger than 15.2. When $Z_1 = 15.2$, the proposed SRDC has the same TUF to the class-E topology, but features lower V_{DS} stress. In this prototype, a TUF of no less than 0.18 serves as guideline for selecting Z_1 (L_1 and L_H).

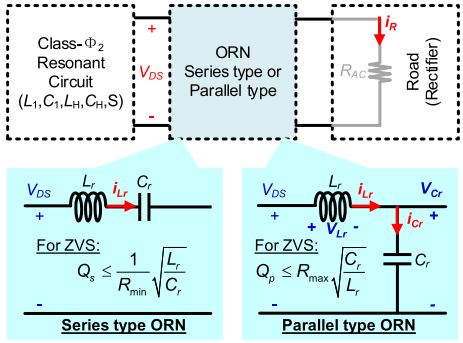

Fig. 7. Schematic of the class-Φ_2 SRDC with series-type ORN and parallel-type ORN.

In addition, the inductance L_1 has a maximum design value at specific $\omega_{\rm eq}$, this is because the minimum value of shunting capacitor C_1 is the drain-to-source parasitic capacitor of the power switch ($C_{\rm ds}$), the maximum design value of L_1 ($L_{1\_\max}$) is written as follows:

$$L_{1\_\max} = \frac{1}{\lambda_1^2 \omega_{\rm eq}^2 C_{\rm ds}}. \tag{18}$$

III. MODIFIED ITA-BASED CONVERTER DESIGN

It has been proved in Section II-A, that the resonant sub-circuit L_1-C_1-S is able to operate with ZVS performance by adjusting parameter λ_1. However, the network is merely a voltage chopper, because the output voltage is zero under the switch ON period. Hence, an ORN is used to transfer the $V_{\rm DS}$ voltage to a fundamental-signal dominated ac current, enabling the rectifier to work simultaneously. However, the ORN and R_{AC} will affect the frequency response of the L_1-C_1-S network and reshape the $V_{\rm DS}$ waveform, which risks of ZVS losses. The following analysis targets the generic solutions of ORN, R_{AC}, and rectifier.

A. Load-Independent ZVS

The overall design goal of the ORN and rectifier is to achieve ZVS and low *dv/dt* over wide load range. For SRDC with series-type ORN in Fig. 7, a design guideline has been derived and adopted in many previous works about class-E or class-EF$_2$ topologies [21], [24], as follows:

$$\begin{aligned} Q_s &= \frac{1}{R_{\rm AC}}\sqrt{\frac{L_r}{C_r}} \le \frac{1}{R_{\rm min}}\sqrt{\frac{L_r}{C_r}}, R_{\rm min} \\ &= \frac{1}{k_m}\sqrt{\frac{L_1}{C_1}}, 0.2 < k_m < 1.5 \end{aligned} \tag{19}$$

where Q_s refers to the quality factor of the series-type ORN and $R_{\rm AC}$. Thus, the SRDC with series-type ORN maintains ZVS as the load R_{AC} is no less than $R_{\rm min}$. A similar concept of quality factor can be defined in for parallel-type ORN cascaded with $R_{\rm AC}$. In the SRDC with parallel-type ORN, the following expressions are derived:

$$\begin{cases} i_{L_r} = i_{C_r} + i_R = i_{C_r} + \dfrac{V_{C_r}}{R_{\rm AC}} \\ V_{\rm DS} = V_{L_r} + V_{C_r} \end{cases}. \tag{20}$$

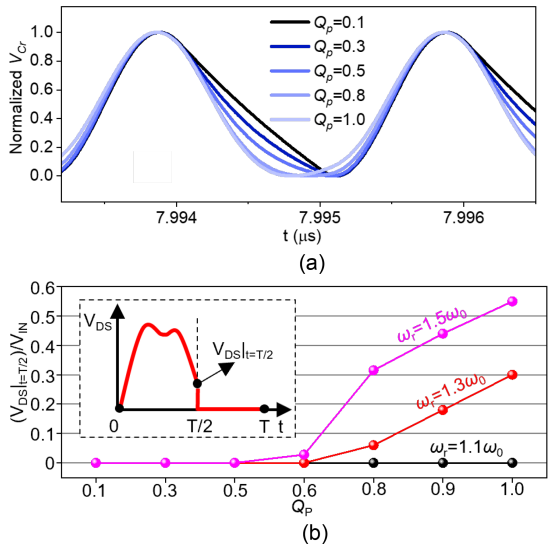

Fig. 8. Simulated (a) normalized V_{Cr} waveforms and (b) normalized $V_{DS}|_{t\,=\,T/2}$ value as $Q_p = 0.1$ to 1 at different ω_r. The design parameters are: $\lambda_1 = 1.61$, $\omega_r = 1.1\omega_0/1.3\omega_0/1.5\omega_0$, the switching frequency is 5 MHz.

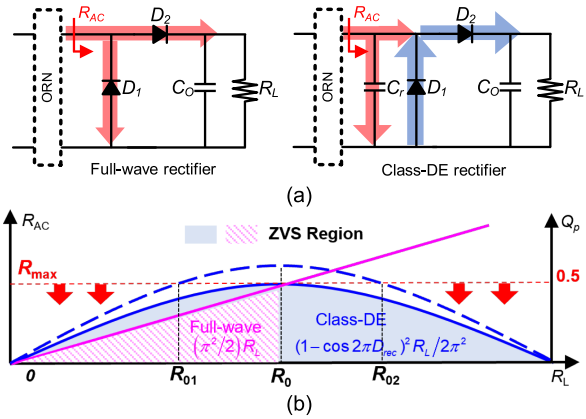

Fig. 9. (a) Diagram of the class-Φ_2 based SRDC with class-DE rectifier. (b) Schematic of input resistance versus load resistance R_L and load quality factor in class-DE rectifier and full-wave rectifier.

Based on linear differential equations of passive elements, the relationship between the $V_{\rm DS}$ and V_{Cr} is derived as follows:

$$\frac{L_r C_r}{R_{\rm AC}^2}\frac{dV_{Cr}^2}{dt^2} + \frac{L_r}{R_{\rm AC}}\frac{dV_{Cr}}{dt} + V_{Cr} = V_{\rm DS}. \tag{21}$$

The roots of (19) is solved as follows:

$$x_1 = \frac{-1-\sqrt{1-4Q_p^2}}{2C_r R_{\rm AC}}, x_2 = \frac{-1+\sqrt{1-4Q_p^2}}{2C_r R_{\rm AC}} \tag{22}$$

where Q_p refers to the quality-factor of the parallel-type ORN and $R_{\rm AC}$, expressed by follows:

$$Q_p = R_{\rm AC}\sqrt{\frac{C_r}{L_r}}. \tag{23}$$

When $Q_p \le 0.5$, V_{Cr} is formed as a trigonometric function (includes a number of harmonic voltage). When $Q_p > 0.5$, the V_{Cr} waveform is close to sinusoidal shape, as shown in Fig. 8(a). In addition, the effect of the Q_p values on the ZVS feature in the fundamental block is shown in Fig. 8(b), where the circuit loss ZVS as $Q_p > 0.5$. The above results indicate that the class-Φ_2 module operation is not affected by ORN if the quality-factor.

$Q_p \le 0.5$, which guides the design of the rectifier. Similar to (17), as shown in Fig. 7, the ZVS design guideline for SRDC with parallel-type ORN is written as

$$Q_p \le R_{\rm max}\sqrt{\frac{C_r}{L_r}}, R_{\rm max} = 0.5\sqrt{\frac{L_r}{C_r}}. \tag{24}$$

B. Rectifier

The class-DE resonant rectifier, evolved from class-DE power amplifier [30], was first proposed in [31], featuring low *dv/dt* and soft switching on the diode. Unlike a full-wave rectifier, a resonant capacitor C_r is shunted across the diode D_1. Both the full-wave rectifier and the class-DE rectifier are shown in Fig. 9. The input resistance $R_{\rm AC}$ of the wide-used full-wave rectifier is linearly positive with R_L, indicating that the SRDC will loss ZVS when the R_{AC} becomes larger than $R_{\rm max}$. For class-DE rectifier, part of the resonant current from ORN will flow in C_r, and the input resistance of the rectifier is not only related to R_L, but the switching-ON duty cycle of the diode, written as follows [32], [33]:

$$R_{\rm AC} = \frac{R_L(1-\cos(2\pi D_{\rm rec}))^2}{2\pi^2} \tag{25}$$

where $D_{\rm rec}$ is the ON-state duty cycle of the diode. The R_{AC} gets the maximum value at duty cycle $D_{\rm rec} = 0.25$ or $D_{\rm rec} = 0.75$. If the quality-factor Q_p at the maximal $R_{\rm AC}$ is higher than 0.5, there will exist two resistors R_{01} and R_{02} that make $Q_p = 0.5$. When the class-DE rectifier cascaded with parallel-type ORN, the ZVS maintains within two load range (0, R_{01}] and [R_{02}, ∞), a design example in [34] verifies this statement. A perfect occasion is achieved if the quality-factor Q_p at maximum $R_{\rm AC}$ is less than 0.5, the ZVS performance is able to be maintained from short-circuit (SC) to open-circuit (OC), as shown in Fig. 9(b). The design equation of the true load-independent ZVS is as follows:

$$\omega_r = \frac{1}{\sqrt{L_r C_r}} \le \frac{\pi\omega_0}{2} \approx 1.57\omega_0 \tag{26}$$

where ω_r is the resonant frequency of L_r-C_r pair.

C. Output Power Analysis

For desired power conversion, the parallel ORN should be designed in detail. As shown in Fig. 7, the $V_{\rm DS}$ serves as constant voltage source, delivering the fundamental voltage component to the ORN and load. The V_{Cr} is derived as follows:

$$V_{Cr} = \frac{V_{\rm DS\_1}\cdot(|1/j\omega C_r| \,\|R_{\rm AC})}{|1/j\omega C_r| + R_{\rm AC}}, V_{\rm DS\_1} = \frac{4V_{IN}}{\pi} \tag{27}$$

where $V_{\rm DS\_1}$ refers to the amplitude of the $V_{\rm DS}$' fundamental voltage component, calculated from the squire waveforms with 50% duty cycle and peak-peak value of $2V_{\rm IN}$. The values of L_r and C_r are determined with (23) and (26), so the output power

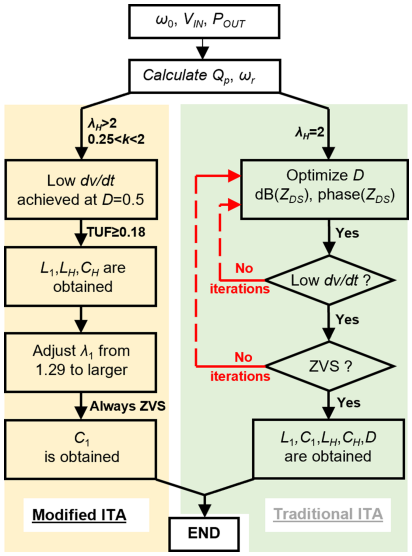

Fig. 10. Design procedures comparisons between the proposed modified ITA method and the traditional ITA method for the class-Φ_2 based SRDC.

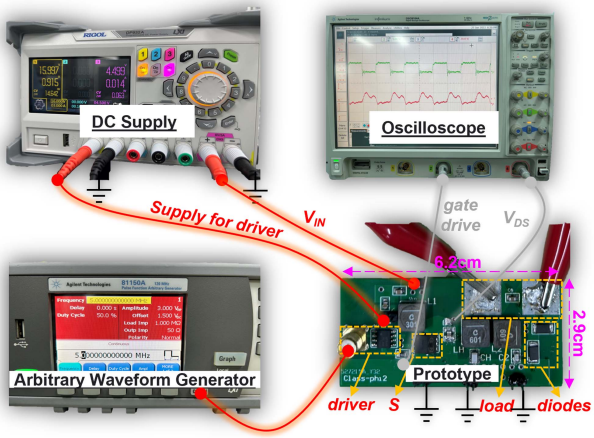

Fig. 11. Experimental set up of the prototype.

P_{OUT} is written as follows:

$$P_{\mathrm{OUT}} = \frac{V_{Cr}^2|_{\omega=\omega_0}}{R_{\mathrm{AC}}} = \frac{16V_{\mathrm{IN}}^2}{\pi^2\left(\frac{\omega_0}{\omega_r Q_p} + \frac{\omega_0^2}{\omega_r^2} + 1\right)R_{\mathrm{AC}}}. \quad (28)$$

Thus, it is practical to select the ω_r value according to (26) and (28), then the components L_r and C_r are determined with the values of ω_r and Q_p.

IV. Prototype and Experiments

Fig. 10 gives the design procedures for class-Φ_2 based SRDC using the proposed modified ITA method (left) and traditional ITA method (right). The proposed parametric modified ITA completely alleviates the optimization iteration.

For prototype verifying, the V_{IN} and switching frequency of the prototype are set as 16 V and 5 MHz. Using the modified ITA design flow, all circuit parameters are calculated and optimized, as given in Table II. The enhancement mode gallium nitride transistor Infineon-GaN System GS-065-011-1-L is employed as the power switch, and a TI UCC27614 is used as the gate driver. Keysight 81150A generates the switching pulse signal, the electronic load DL3021A serves as the variable loads. The capacitors C_1 and C_r do not comprise the parasitic capacitances

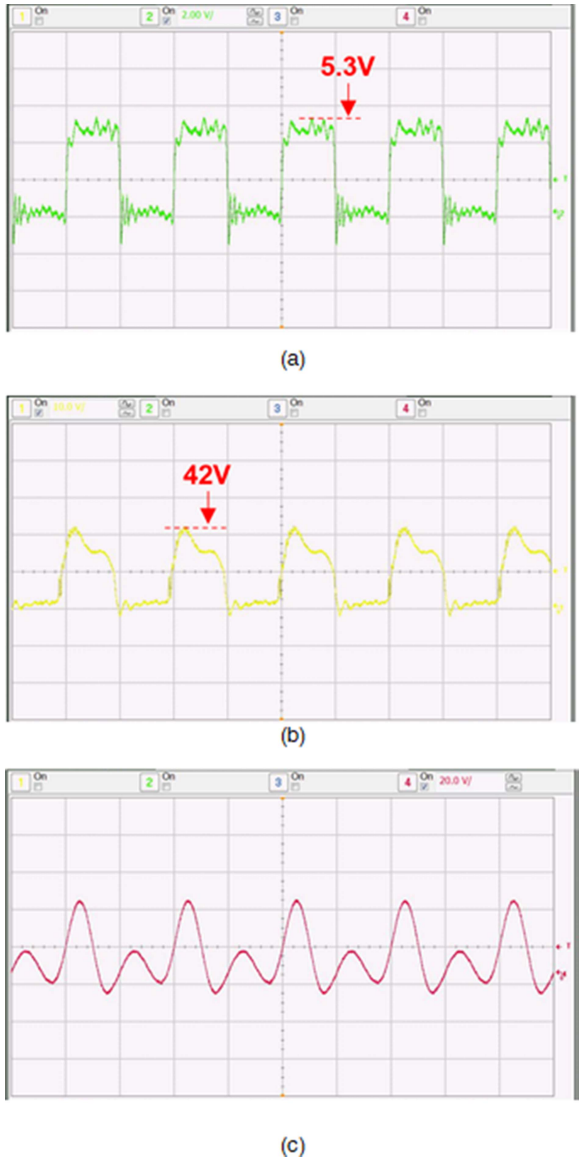

Fig. 12. Measured (a) gate driving waveform; (b) V_{DS} waveform and (c) V_{CH} waveform at switching duty cycle of 50% and V_{IN} = 16 V andP_{OUT} = 16.8 W.

TABLE II
Design Parameters of the Converter Prototype

Parameter	Value
L_1	300 nH (k=0.5)
L_r	600 nH (ω_r=ω_0, Q_p=0.5)
C_1	1.3 nF (λ_1=1.61)
C_r	1.5 nF (ω_r=ω_0, Q_p=0.5)
L_H	600 nH (k=0.5)
C_H	390 pF (λ_H=2.08)
R_L	SC to OC (R_0=100 Ω)
f_0	5 MHz
D	50%

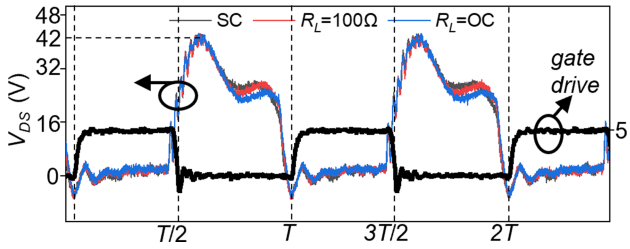

Fig. 13. Measured $V_{\rm DS}$ waveforms at different loads, $V_{\rm IN} = 16$ V.

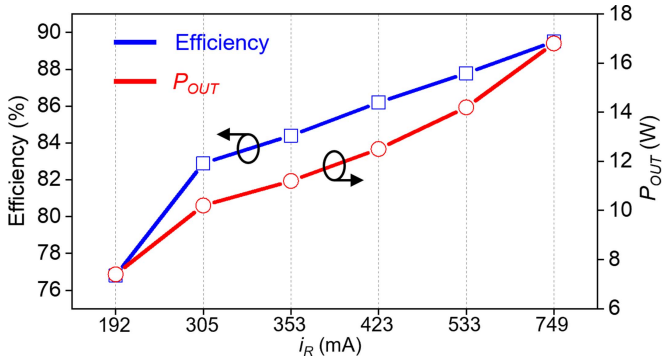

Fig. 14. Measured curves of conversion efficiency and output power of the prototype as function of load current i_R. The measured results are tested at $V_{\rm IN} = 16$ V.

of the power switches and diodes. Fig. 11 shows the assembled converter board and experimental setup. Fig. 12 shows the measured gate-drive, $V_{\rm DS}$ and V_{CH} waveforms under working condition. Fig. 13 shows the measured $V_{\rm DS}$ waveforms at different load current conditions. All the measured $V_{\rm DS}$ waveforms fall to zero before the power switch turns on, indicating an excellent ZVS performance from SC to OC. The maximal $V_{\rm DS}$ stress is also proven to be reduced to $\sim$2.6$V_{\rm IN}$ in all tested conditions.

Fig. 14 shows the measured voltage conversion ratios and conversion efficiency. The full load of the prototype achieves 16.8 W. The conversion efficiency decreases with load current due to the Joule heat in parasitic resistances but maintains higher than 76% in the tested load range from 192 to 749 mA, which is limited by the accuracy of the electric load. The high conversion efficiency is attributed mainly to the load-independent ZVS feature with zero switching losses.

V. Conclusion

This article presents a new resonant step-up dc/dc converter comprising a class-Φ_2 inverter and a class-DE rectifier for MHz range power transfer. The circuit was designed using a straightforward modified ITA method to tackle the limited ZVS load range and $V_{\rm DS}$ stress issues. The harmonic tuned circuit $L_{\rm H}$-$C_{\rm H}$ resonates higher at $2f_0$, forming a feedback second-order harmonic voltage to shape the $V_{\rm DS}$ waveform to be near trapezoidal in 50% of switching duty cycle. Compared to the traditional ITA design theory, the proposed modified ITA requires fewer design steps and has higher accuracy of element parameter selections. The 5 MHz prototype achieves a true SC-to-OC load-independent ZVS feature with reduced $V_{\rm DS}$ stress. The proposed design method and techniques are a suitable candidate for load-varying power conversion systems, even at the MHz regime.

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