Conducted EMI Reduction by Active Power Filter Embedded in Neutral-Point-Clamped Converters

Jun-Hyung Jung, *Member, IEEE*, Jang-Mok Kim, *Member, IEEE*, and Marco Liserre, *Fellow, IEEE*

***Abstract*—This article proposes a novel modulation strategy with an active power filter (APF) for reducing conducted electromagnetic interference (EMI) in three-level neutral-point-clamped ac/dc pulsewidth modulation (PWM) converters. Common-mode (CM) voltage is identified as one of the main causes of EMI in power electronics systems driven by PWM converters. To address this issue, the article proposes a CM voltage reduction strategy using a fourth-leg APF with shunt capacitors, which overcomes the limitations of existing methods. The proposed strategy allows for the complete elimination of CM voltage, and compensation is proposed to eliminate residual CM voltages due to the dead time effect. In addition, the article presents a design procedure for the APF circuit to obtain a proper reduction performance. Simulation and experimental results demonstrate the effectiveness of the proposed strategy in reducing both CM voltage and current, as well as conducted EMI.**

***Index Terms*—Active power filter (APF), common-mode (CM) voltage, electromagnetic interference (EMI), three-level neutral-point-clamped (NPC) converter.**

I. Introduction

COMMON-MODE (CM) voltage is one of the main causes of conducted electromagnetic interference (EMI) in pulsewidth modulation (PWM) converters [1], [2], [3]. Rapid changes in the CM voltage (dV_{CM}/dt) due to the switching operations induce the CM current, which can flow into adjacent devices as conducted EMI and generates radiated EMI [4], [5], [6], [7]. This EMI can degrade the reliability and stability of adjacent devices. In motor drives, CM voltage induces a leakage current that can damage the motor bearings. For these reasons, CM voltage and its effects should be alleviated to comply with various standards pertaining to EMC, such as FCC, CISPR, and IEC.

Generally, isolation transformers and passive CM EMI filters, including CM choke and Y-capacitor, have been utilized to suppress the effects of CM voltage [8], [9], [10]. However, the volume and weight of isolation transformers are relatively large, and especially, as the power system capacity increases, they increase the system weight and volume considerably. In passive CM EMI filters, large CM chokes and Y-capacitors are required to adequately attenuate the conducted EMI in low-frequency bands.

As alternative solutions to reduce the size, weight, and volume of passive components are required, many researchers have proposed various methods, such as reduced CM voltage (RCMV) PWM methods [11], [12], [13], [14], [15] and active CM EMI filters (AEFs) [16], [17], [18], [19], [20], [21]. The PWM sequences of RCMV PWM methods are usually combined with voltage vectors to generate small or zero CM voltages. Consequently, these methods effectively reduce the magnitude and number of occurrences of CM voltage without additional circuits and components. Nevertheless, RCMV PWM methods have drawbacks, for example, the magnitude of harmonics in the phase current increases when the voltage vectors are modified to reduce the CM voltage [22], [23]. By contrast, AEFs can reduce the conducted EMI, especially in the frequency range of 30 kHz to 150 MHz, without affecting the performance of PWM converters. AEFs generally consist of an amplifier comprising OP-amps [16], [17], [18] or BJT-based push-pull emitter followers (PPEF) [19], [20], [21], and a CM transformer or shunt capacitors for measuring the conducted noise and injecting the voltage or current output from the amplifier. Although AEFs can effectively reduce conducted EMI, the design procedure of AEFs is complex, and AEFs require an additional power supply to the amplifier. Furthermore, the application of AEFs to high-power medium-voltage applications is not straightforward because the rated output voltage and current of the amplifiers used in AEFs are low to handle high levels of power [24].

To compensate for the limitations of AEFs, many papers have studied CM active power filters (APFs) [24], [25], [26], [27], [28], [29], [30], [31], [32]. APFs generally use a single-leg PWM converter composed of IGBTs or MOSFETs as an amplifier instead of OP-amps or PPEFs. Discrete voltage output by the leg is injected into three-phase lines via a CM transformer (CMT) for voltage-type APFs or shunt capacitors for the current-type APFs, to cancel CM voltage generated by the three-phase converter. This makes APFs suitable for higher voltage and power applications. In particular, the size reduction of passive filter offered by APF is an attractive solution for aerospace and marine applications, where volume and weight requirements are stringent [33], [34]. It should be noted, however, that the

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effective noise reduction bandwidth is limited to a few MHz because the APF output voltage is not ideally linear and cannot eliminate high-frequency ringing due to switching behavior [29], [35].

For effective CM voltage reduction with APFs, modified PWM techniques are generally applied to three-phase converters, despite the consequent increase in current harmonics. This approach aims to limit the CM voltage levels due to the fact that the voltage levels produced by the fourth leg are typically fewer than the potential CM voltage levels. For instance, in the case of two-level PWM converters, complete CM voltage reduction by the current-type APF can be achieved through the utilization of modified PWM techniques that abstain from using zero-voltage vectors, generating large CM voltage [24], [25], [26]. Otherwise, more complex circuits and control are needed for the fourth leg, as proposed in [27] and [31].

Three-level converters offer more flexibility in terms of possible PWM techniques due to the availability of more voltage vectors compared to two-level converters. For this reason, diverse research efforts have been carried out. Studies conducted in [27], [28], and [29] utilize a voltage-type APF with CMT to completely reduce CM voltage. However, this approach comes with disadvantages, such as the requirement for a more complex fourth leg [27] or a need for a separate auxiliary dc power supply [28]. Importantly, careful consideration is required when dealing with high power systems, as voltage-type APF presents a problem where an increase in system power leads to a proportional increase in the weight and volume of the CMT. On the other hand, current-type APFs that utilize shunt capacitors are less correlated with the power increase of the system, thereby making them more appropriate for higher power systems. In [30], a PWM technique for a four-leg three-level T-type converter is introduced as a means to decrease CM voltage. However, this modulation is incapable of entirely eliminating CM voltage, and the effects of the dead time is not considered. The authors in [31] and [32] proposed CM voltage reduction methods connecting the fourth leg to the neutral point of an electric machine. In [31], a complex five-level neutral-point-clamped (NPC) converter as the fourth leg is introduced to eliminate the CM voltage. However, the complexity and control of the fourth leg are challenges. Similarly, the APF with the three-level NPC leg is employed with a modified PWM to reduce CM voltage through the neutral point of the machine [32]. However, the use of modified PWM with small voltage vectors can result in significant dc voltage imbalance and it requires separate dc sources to the dc capacitors to solve the imbalance.

Therefore, the motivation behind this study is to develop an effective strategy that not only entirely eliminates CM voltage in grid-connected three-phase three-level ac/dc PWM converters, also presents a comprehensive solution including a robust design for the current-type APF. This article analyzes the CM voltage induced by the four-leg converter, revealing that the use of APF can successfully remove CM voltage. Based on this analysis, we propose a modulation strategy for the complete removal of CM voltage using an optimal PWM technique, particularly suited for the current-type APF. While the proposed strategy can eliminate CM voltage under ideal conditions, practical implementation needs to consider dead time in PWM signals, which could cause residual CM voltages. Therefore, this article also explains the impact of dead time on CM voltage and proposes a compensation scheme to eliminate the residual CM voltage. Furthermore, a design procedure and considerations are described to ensure the APF circuit can mitigate CM voltage without affecting the three-phase converter operation. To demonstrate the effectiveness of the proposed strategy with APF, various simulation and experimental results regarding CM voltage and current, and the measurement of conducted EMI, are presented. These results show that the proposed strategy effectively reduces CM voltage and current, as well as conducted EMI, which are crucial factors in power electronics systems driven by PWM converters.

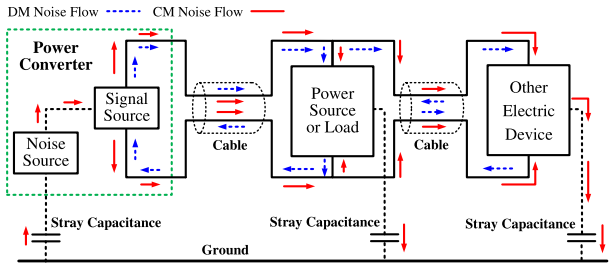

Fig. 1. Flow path of DM and CM noises.

The rest of this article is organized as follows. Section II analyzes and defines the CM voltage output by the four-leg three-level NPC converter that includes the APF circuits. Section III proposes a modulation strategy to eliminate CM voltage, including a scheme to compensate for the effects of dead time. Section IV describes the design procedure and considerations of the APF circuit. In Section V, simulation and experimental results related to the reduction of both CM voltage and current, as well as conducted EMI measurements, are presented. Finally, Section VI concludes this article.

II. CM Voltage Output From Four-Leg Three-Level NPC PWM Converter

CM voltage is one of the main reasons for the EMI generated by power conversion systems, which are composed of power semiconductors, such as IGBTs and MOSFETs. In three-phase PWM converters, the CM voltage ($V_{CM.\text{conv}}$) is defined in (1) as the average output voltage by each phase ($V_{xN}, x = A, B, C$), and it changes according to the switching state of each phase

$$V_{CM} = V_{CM.\text{conv}} = \frac{V_{AN} + V_{BN} + V_{CN}}{3}. \tag{1}$$

EMI can be classified into radiated and conducted noises. In addition, the conducted EMI can be divided into differential-mode (DM) and CM noises, as shown in Fig. 1, [6]. These two types of noise are generated from noise sources, such as PWM converters and are conducted through cables into grid voltage sources and other electrical devices. Among these two noises, CM noise passes through devices and returns to the noise source as CM current through stray capacitance. Changes in CM voltage generate this CM current, and it is defined in a simplified form as

$$i_{CM} = C_{\text{stray}} \frac{d}{dt} V_{CM}. \tag{2}$$

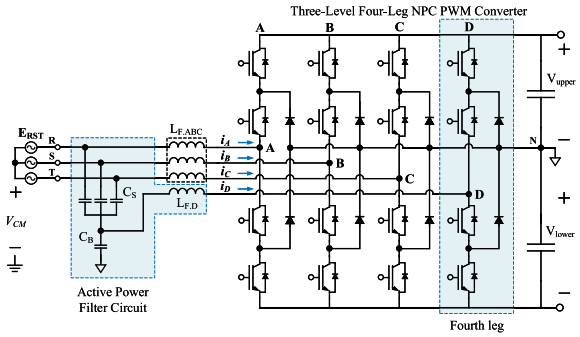

Fig. 2. Configuration of grid-connected four-leg three-level NPC PWM converter that includes the APF circuit.

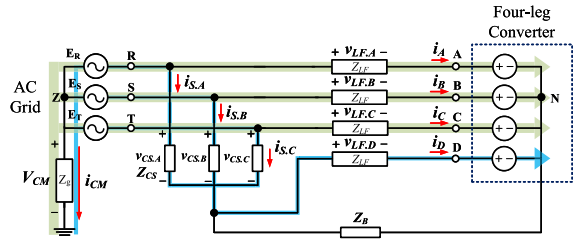

Fig. 3. Simplified equivalent circuit of four-leg converter.

It is confirmed from (2) that CM current is generated each time CM voltage changes, and the magnitude of CM current increases as changes in CM voltage become quicker and more significant. Therefore, the conducted CM EMI generated by PWM converters could be reduced if the number and magnitudes of the CM voltages are reduced.

Fig. 2 shows the configuration of a grid-connected four-leg three-level NPC PWM ac/dc converter. In the APF, the fourth leg is used as an amplifier. In addition, the shunt capacitors C_S and the inductor $L_{F.D}$ are connected to each phase for eliminating the CM voltage. Three single-phase inductors $L_{F.\mathrm{ABC}}$ are placed in each phase, and it is identical to the inductor of the fourth leg. This circuit configuration is called the current-type APF because the CM voltage can be eliminated by the current flowing through the shunt capacitors. If the CMT is connected to the three phases for reducing the CM voltage, the resulting configuration represents the voltage-type APF. In addition to C_S and $L_{F.D}$ in the APF circuit, a bypass capacitor C_B is connected for passing a high-frequency CM current into the ground. This circuit configuration is similar to the four-leg converter described in literature, such as [36] and [37]. However, the fourth leg used for the proposed strategy is used not to remove low-frequency CM voltages and supply balanced voltage under an unbalanced load or source, but to reduce the discrete CM voltage output by the three-phase converter in the switching frequency range.

Fig. 2 can be simplified into the equivalent circuit shown in Fig. 3 to explain the reduction of CM voltage in the four-leg PWM converter, and this equivalent circuit can be analyzed using the Kirchhoff's law. In case of the three-phase converter, the output voltage and grid voltage of each phase can be expressed as

$$V_{CM} + E_R - Z_{LF.A} i_A - V_{AN} = 0 \tag{3}$$

$$V_{CM} + E_S - Z_{LF.B} i_B - V_{BN} = 0 \tag{4}$$

$$V_{CM} + E_T - Z_{LF.C} i_C - V_{CN} = 0 \tag{5}$$

where $Z_{LF.x}$ and i_x denote the impedance of each single-phase inductor connected to the three phases and the phase current, respectively.

The equation for the CM (6) can be obtained by summing (3)–(5). It is assumed that the three-phase grid voltages are in equilibrium with each other, and the impedance of each three-phase inductor is equal to Z_{LF}

$$3V_{CM} - Z_{LF}(i_A + i_B + i_C) - (V_{AN} + V_{BN} + V_{CN}) = 0. \tag{6}$$

By substituting the sum of the three-phase currents in (7) into (6), the equation for the current in the fourth leg (8) can be obtained

$$i_{CM} + i_D = -(i_A + i_B + i_C) \tag{7}$$

$$i_D = \frac{(V_{AN} + V_{BN} + V_{CN}) - 3V_{CM}}{Z_{LF}} - i_{CM}. \tag{8}$$

In the same way as the process from (3)–(6), an equation for the fourth leg and grid voltages can be derived as follows:

$$V_{CM} - Z_{CS} i_D/3 - Z_{LF.D} i_D - V_{DN} = 0 \tag{9}$$

where Z_{CS} and $Z_{LF.D}$ denote the impedance of the shunt capacitors and the inductor $L_{F.D}$, respectively.

The second expression for the fourth leg (10) can be obtained from (9)

$$i_D = \frac{V_{CM} - V_{DN}}{Z_{CS}/3 + Z_{LF.D}}. \tag{10}$$

Equation (12) can be derived by substituting (10) into (8) and replacing CM current with CM voltage and its impedance, as expressed in (11). According to (12), the CM voltage in the four-leg PWM converter can be defined in terms of the output voltage of each phase as in (13)

$$i_{CM} = \frac{V_{CM}}{Zg} \tag{11}$$

$$\frac{V_{CM} - V_{DN}}{Z_{CS}/3 + Z_{LF.D}} = \frac{(V_{AN} + V_{BN} + V_{CN}) - 3V_{CM}}{Z_{LF}} - i_{CM} \tag{12}$$

$$V_{CM} = \frac{(V_{AN}+V_{BN}+V_{CN})(Z_{CS}/3 + Z_{LF.D}) + V_{DN} Z_{LF}}{(Z_{CS}/3+Z_{LF.D}) Z_{LF}/Z_g + (Z_{LF} + 3(Z_{CS}/3 + Z_{LF.D}))}. \tag{13}$$

As mentioned above, each single-phase inductor is identical, and Z_{CS} is considerably smaller than $Z_{LF.D}$ at the switching frequency. Therefore, as expressed in (14), the impedance of the *LC* circuit in the APF circuit is almost the same as Z_{LF}

$$Z_{CS}/3 + Z_{LF.D} \approx Z_{LF}. \tag{14}$$

In addition, because the impedance Z_g is significantly large, the associated expressions are negligible. Therefore, the CM voltage

TABLE I
VOLTAGE VECTORS AND SWITCHING STATES OF THREE-LEVEL NPC PWM CONVERTER [38]

Vectors	Magnitude	Switching states	CM voltage
Zero	$0V$	[PPP]	$V_{DC}/2$
		[OOO]	$0V$
		[NNN]	$-V_{DC}/2$
Small	$\frac{1}{3}V_{DC}$	[POO],[OPO],[OOP]	$V_{DC}/6$
		[ONN],[NON],[NNO]	$-V_{DC}/3$
		[PPO],[POP],[OPP]	$V_{DC}/3$
		[OON],[ONO],[NOO]	$-V_{DC}/6$
Medium	$\frac{\sqrt{3}}{3}V_{DC}$	[PON],[OPN],[NPO] [NOP],[ONP],[PNO]	$0V$
Large	$\frac{2}{3}V_{DC}$	[PPN],[PNP],[NPP]	$V_{DC}/6$
		[NNP],[NPN],[PNN]	$-V_{DC}/6$

of (13) can be approximated as

$$V_{CM} = \frac{V_{AN} + V_{BN} + V_{CN} + V_{DN}}{4}. \tag{15}$$

From (15), it is confirmed that the CM voltage generated by the four-leg converter can be 0 V if the sum of the voltages output by the four-leg converter is 0 V.

III. PWM METHOD FOR ELIMINATING CM VOLTAGE

A. PWM Method for Four-Leg PWM Converter

In Section II, the CM voltage generated by the four-leg PWM converter is defined based on an analysis of the equivalent circuit. From the viewpoint of the fourth leg described in (15), the output voltage of the fourth leg (V_{DN}) should be the same as the sum of the three-phase output voltages, but the sign must be opposite. Because the fourth leg is based on the three-level NPC PWM converter, the fourth leg can output three levels of V_{DN}, namely, $V_{DC}/2$, 0 V, and $-V_{DC}/2$. Therefore, the three-phase three-level PWM converter must be controlled such that the sum of the output voltages should be $V_{DC}/2, 0\,V$, or $-V_{DC}/2$ to eliminate CM voltage from the four-leg three-level NPC converter. That is, the CM voltage should be $V_{DC}/6$, 0 V, or $-V_{DC}/6$.

Table I lists the voltage vectors and switching states used in the three-phase three-level NPC PWM converter, and the CM voltages corresponding to the various switching states. As mentioned in the preceding paragraph, the three-phase PWM converter should use the switching states that generate a CM voltage of $V_{DC}/6, 0\,V$, or $-V_{DC}/6$. Therefore, the zero-voltage vectors [PPP] and [NNN] and the six small-voltage vectors that generate the CM voltage of $\pm V_{DC}/3$ are not used for the three-phase PWM converter. Among the existing PWM techniques proposed in literature, the alternative phase opposite disposition (APOD) PWM [12] and large-medium-zero (LMZ) PWM [13] satisfy the aforementioned conditions, as shown in Fig. 4. In a single period of the APOD PWM, the CM voltage changes six times. In case of the LMZ PWM, by contrast, the CM voltage changes twice because the small-voltage vectors are not used, while they are used in case of the APOD PWM. Considering this characteristic, it is expected that the CM voltage reduction

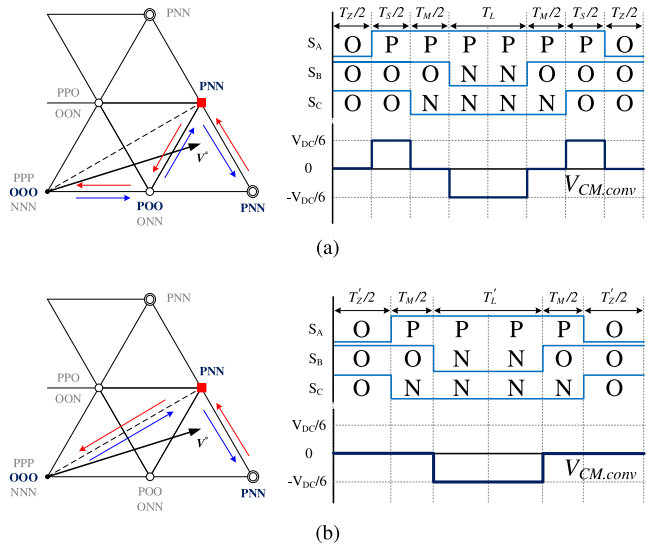

Fig. 4. Space vector diagram and switching sequence of APOD and LMZ PWM methods. (a) APOD PWM. (b) LMZ PWM.

result obtained using the LMZ PWM with the fourth leg would be superior to the results obtained using the APOD PWM. This is because it is difficult to eliminate the high-frequency CM voltage after each change in the CM voltage, even when applying the APF based on the fourth leg. Therefore, the proposed CM voltage strategy with the APF is based on the LMZ PWM, which is applied to the three-phase converter [13].

As shown in Fig. 4(b), the switching sequence of LMZ PWM is composed of zero-, medium-, and large-voltage vectors without the small voltage vector which has an impact on the deviation of the upper and lower dc voltages. As described in [38], the zero and large voltage vectors have no impact on the dc voltage imbalance, and the medium vector produces voltage ripples three times the fundamental frequency, but if the three-phase current is balanced, they have little effect on the rapid dc offset voltage imbalance [22].

The LMZ PWM can be implemented from the APOD PWM by replacing the small vector with zero and large vectors. The synthesized voltage reference of the APOD PWM ($\vec{V}^*_{\text{APOD}}$) can be expressed as follows:

$$\vec{V}^*_{\text{APOD}} = \vec{V}_Z T_Z + \vec{V}_S T_S + \vec{V}_M T_M + \vec{V}_L T_L$$
$$(T_{\text{PWM}} = (T_Z + T_S + T_M + T_L) \tag{16}$$

where $\vec{V}_Z$, $\vec{V}_S$, $\vec{V}_M$, and $\vec{V}_L$ represent zero-, small-, medium-, and large-voltage vectors in specific regions, respectively. T_Z, T_S, T_M, and T_L denote the switching times of each voltage vector, and their sum is T_{PWM}, which is a single period of PWM. According to (16), the synthesized voltage reference of the LMZ PWM can be obtained by adding a half of T_S in (17) to T_Z and T_L, respectively, as in (18)

$$T_S = \frac{|V^*_{\max}| - |V^*_{\min}|}{V_{DC}/2} T_{\text{PWM}} \tag{17}$$

$$\vec{V}^*_{\text{LMZ}} = \vec{V}_Z T'_Z + \vec{V}_M T_M + \vec{V}_L T'_L$$

TABLE II
PWM SEQUENCE FOR FOUR-LEG THREE-LEVEL PWM CONVERTER WITH PROPOSED CM VOLTAGE REDUCTION STRATEGY

Sector	Angle	Switching sequence				
		$T_Z^{'}$	T_M	$T_L^{'}$	T_M	$T_Z^{'}$
1	$0 < \theta \leq \pi/6$	[OOOO]	[PONO]	[PNNP]	[PONO]	[OOOO]
2	$\pi/6 < \theta \leq \pi/3$	[OOOO]	[PONO]	[PPNN]	[PONO]	[OOOO]
3	$\pi/3 < \theta \leq \pi/2$	[OOOO]	[OPNO]	[PPNN]	[OPNO]	[OOOO]
4	$\pi/2 < \theta \leq 2\pi/3$	[OOOO]	[OPNO]	[NPNP]	[OPNO]	[OOOO]
5	$2\pi/3 < \theta \leq 5\pi/6$	[OOOO]	[NPOO]	[NPNP]	[NPOO]	[OOOO]
6	$5\pi 6 < \theta \leq \pi$	[OOOO]	[NPOO]	[NPPN]	[NPOO]	[OOOO]
7	$\pi < \theta \leq 7\pi/6$	[OOOO]	[NOPO]	[NPPN]	[NOPO]	[OOOO]
8	$7\pi/6 < \theta \leq 4\pi/3$	[OOOO]	[NOPO]	[NNPP]	[NOPO]	[OOOO]
9	$4\pi/3 < \theta \leq 3\pi/2$	[OOOO]	[ONPO]	[NNPP]	[ONPO]	[OOOO]
10	$3\pi/2 < \theta \leq 5\pi/3$	[OOOO]	[ONPO]	[PNPN]	[ONPO]	[OOOO]
11	$5\pi/3 < \theta \leq 11\pi/6$	[OOOO]	[PNOO]	[PNPN]	[PNOO]	[OOOO]
12	$11\pi/6 < \theta \leq 2\pi$	[OOOO]	[PNOO]	[PNNP]	[PNOO]	[OOOO]

$$(T_{\text{PWM}} = T_Z' + T_M + T_L') \tag{18}$$

where $|V_{\text{max}}^*|$ and $|V_{\text{min}}^*|$ are the absolute values of the maximum and minimum voltage references, respectively. In the LMZ PWM, the newly defined switching times $T_Z^{'}$ and $T_L^{'}$ are, respectively, equivalent to the following expressions:

$$T_Z' = T_Z + T_S/2 \tag{19}$$

$$T_L' = T_L + T_S/2. \tag{20}$$

As described above, the LMZ PWM can be implemented by adjusting the dwell time for three phases without additional turn-ON and -OFF operation of switches. For this reason, the losses caused in a three-phase converter are almost no different than when using general modulation, such as in-phase disposition (IPD) PWM [38].

The above process is the same as adding an offset voltage to the three-phase voltage references, as in (21). The offset voltage can be obtained from (17), as expressed in (22)

$$v_{xs}^* = v_{xn}^* + v_{off}\ (x = A, B, C) \tag{21}$$

$$v_{off} = -\frac{V_{\text{max}}^* + V_{\text{min}}^*}{2} = \frac{V_{\text{mid}}^*}{2}. \tag{22}$$

In the LMZ PWM, the switching time of the large vector is related to the medium value V_{mid}^*, among the three-phase voltage references, and it can be derived as follows:

$$T_L' = \left(\frac{|V_{\text{mid}}^*|}{V_{DC}/2} + \frac{1}{2}\frac{|V_{\text{max}}^*| - |V_{\text{min}}^*|}{V_{DC}/2}\right) T_{\text{PWM}}$$
$$= \frac{2T_{\text{PWM}}}{V_{DC}}\left|\frac{3}{2}V_{\text{mid}}^*\right|. \tag{23}$$

Because the CM voltage in the LMZ PWM is generated only because of the large vector, the switching time of the fourth leg is equal to T_L, and the sign of the voltage reference of the fourth leg is the opposite to that of the reference corresponding to the medium value, as follows:

$$v_{Ds}^* = \frac{V_{\text{max}}^* + V_{\text{min}}^*}{2} - V_{\text{mid}}^* = -\frac{3}{2}V_{\text{mid}}^*$$
$$(V_{\text{max}}^* + V_{\text{mid}}^* + V_{\text{min}}^* = 0). \tag{24}$$

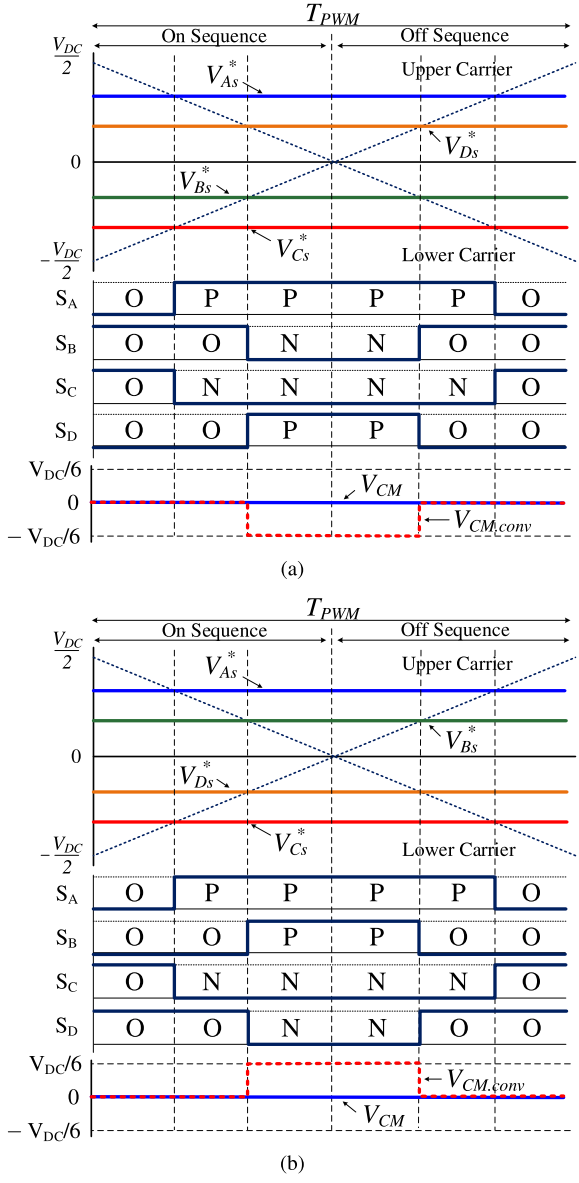

Fig. 5. Proposed modulation strategy for CM voltage reduction of four-leg three-level NPC PWM converter. (a) Sector 1. (b) Sector 2.

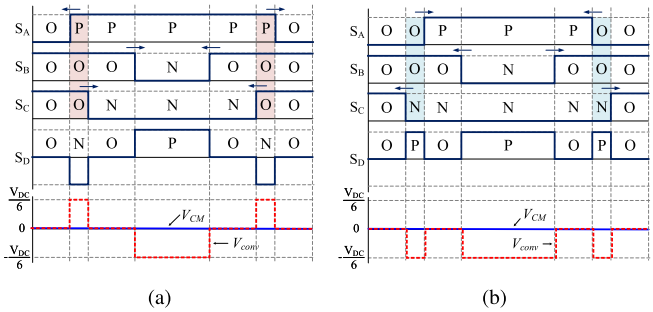

Fig. 6. PWM sequences for balancing DC voltages. (a) With P-type small vector. (b) With N-type small vector.

Fig. 5 presents the PWM method for the four-leg three-level NPC converter to eliminate the CM voltage. In sector 1 ($0 < \theta \leq \pi/12$) shown in Fig. 5(a), V^*_{mid} is V^*_{Bn}, and its sign is negative. Therefore, the $V_{\text{conv}.CM}$ of $-V_{DC}/6$ is generated if the fourth-leg is not used and the size of V^*_{Ds} is the same size as that of V^*_{Bs} but a positive sign is input to the fourth leg. By contrast, in the case of sector 2 ($\pi/12 < \theta \leq \pi/6$), as shown in Fig. 5(b), V^*_{Bs} is positive, and the three-phase converter generates the CM voltage of $V_{DC}/6$. In addition, a negative V^*_{Ds} is needed to eliminate the CM voltage. Table II shows the PWM sequences of the four-leg converter in all sectors.

Inherently, LMZ PWM does not cause significant dc voltage unbalance, as it does not employ a small vector in the sequence. However, in the event of a critical voltage unbalance, it should be able to restore the balanced dc voltage state. As proposed in [13], it is possible to balance the dc voltage by allowing the small vector, P-type or N-type, as shown in Fig. 6, only for a short time. The CM voltage due to the small vector, which is $\pm V_{DC}/6$, can be reduced by the fourth leg.

B. Effect of Dead Time on CM Voltage and Compensation

In general PWM converter systems, dead time (T_D) is included in PWM signals to avoid the failure of power semiconductors due to short-circuit current. For the three-level NPC PWM converter, dead time is inserted between the transition states of a leg, and the states depend on the direction of the phase current, as shown in Fig. 7, [38]. Under negative current conditions, when the switching state is converted from N to O or O to P, the state does not immediately change to the next state during an interval, but the previous state is preserved. By contrast, the switching state immediately changes to the next state without delay under positive current conditions. This effect occurs in the four-leg converter addressed herein. Therefore, elimination of CM voltage using the proposed method may not be possible owing to dead time.

If the three-phase PWM converter is controlled using a unity power factor, a positive phase current usually flows through the leg when the voltage reference is positive, meaning that the leg is operated in the P and O states. Conversely, if the converter leg is operated in the N and O states under negative voltage reference, a negative phase current flows.

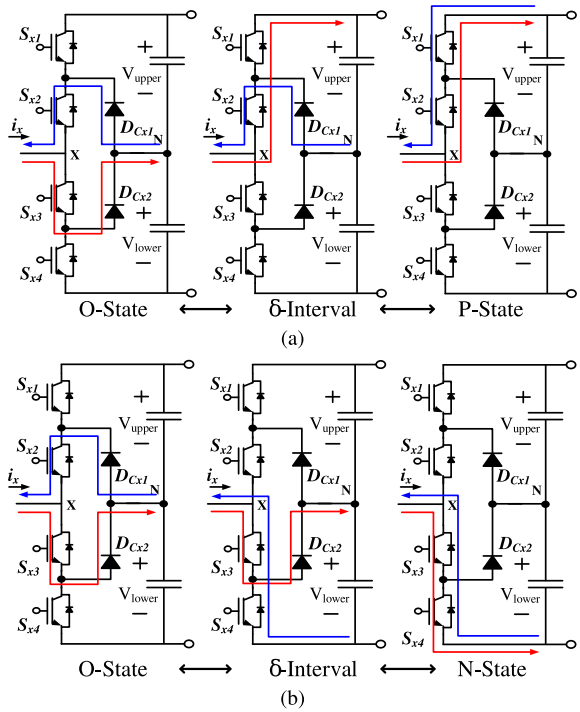

Fig. 7. Effect of dead time on a three-level NPC converter. (a) O-state to P-state. (b) O-state to N-state.

Fig. 8 shows the effects of dead time on each output phase voltage and CM voltage. As shown in Fig. 8(a) and (b), in most cases, the effect of dead time on the three-phase output voltage can be seen in the off-sequence of PWM. Consequently, the CM voltage changes as late as dead time in the off-sequence. Fig. 8(c) and (d) show the effect of dead time on the CM voltage when the phase voltage and phase current have different signs. This case occurs in very narrow areas near boundaries, for example, between sectors 1 and 2. In this case, the change in CM voltage is influenced during the on-sequence. The effect of dead time on the output voltage of the fourth leg is shown in Fig. 8(e) and (f). It is assumed that the APF circuit is correctly designed following the design procedure proposed herein. Considering the direction of current at the moment in which the state of the fourth leg is switched, the output voltage V_{DN} is generally unaffected by dead time. Thus, the effect of dead time appears during the off-sequence, as shown in Fig. 8(e) and (f), considering the CM voltage in Fig. 8(a) and (b).

In this study, the voltage reference of the fourth leg rather than utilizing the mid-value voltage reference is modified to eliminate the CM voltage due to dead time. Because modifying mid-value voltage reference affects the current control of the three-phase converter, and the associated implementation method is complex. Fig. 9 presents the compensation scheme for the CM voltage due to dead time in sector 1 as an example. Because the moment of CM voltage transition is delayed by T_D, the fourth leg should output a voltage a little longer by T_D. For this reason, the voltage computed using (25) is injected only in the off-sequence for compensation. In case of the condition in

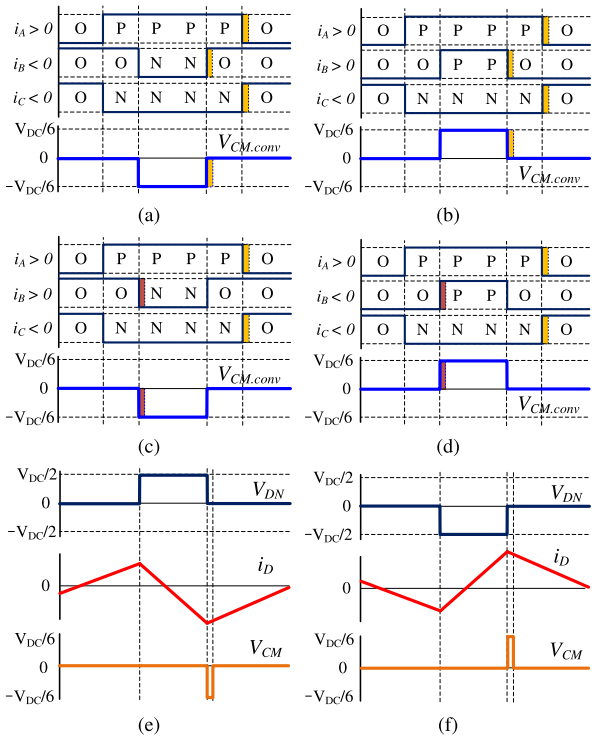

Fig. 8. Effect of dead time on the output voltage of the three-phase converter and fourth leg. (a) $V_{CM.\mathrm{conv}}$ in sector 1 ($i_B < 0$). (b) $V_{CM.\mathrm{conv}}$ in sector 2 ($i_B > 0$). (c) $V_{CM.\mathrm{conv}}$ in sector 1 ($i_B > 0$). (d) $V_{CM.\mathrm{conv}}$ in sector 2 ($i_B < 0$). (e) V_{DN} and V_{CM} in sector 1 ($i_B < 0$). (f) V_{DN} and V_{CM} in sector 2 ($i_B > 0$).

Fig. 8(c) and (d), the reference voltage of the fourth leg should be reduced by voltage corresponding to the dead time because the CM voltage occurs after the passage of the dead time.

$$V_{\mathrm{DTC}} = \frac{T_D}{T_{\mathrm{PWM}}} \frac{V_{DC}}{2}. \tag{25}$$

The overall control system for eliminating CM voltage by using the APF circuit in the grid-connected four-leg three-level NPC PWM converter is depicted in Fig. 10.

IV. Design of APF for CM Voltage Reduction

A. Passive Components

As shown in Fig. 3, the current-type APF consists of a single leg of the three-level converter, single-phase inductor $L_{F.D}$, and shunt capacitors C_S. In addition to this circuit, a bypass capacitor (C_B) is added to reduce high-frequency noises. In this article, the design procedure of three passive components in the APF circuit is provided for effective CM voltage reduction using APF. The design is conducted in the order of inductor, shunt capacitor, and bypass capacitor.

When designing the APF circuit, the circuit characteristics in three frequency bands, namely, low-, switching-, and high-frequency, should be considered, as presented in Fig. 11, like that described in [18]. Considering the main purpose of the APF circuit is to reduce the CM voltage by the fourth leg, it is important for satisfying the condition in (14) at the switching frequency, where the CM voltage cancellation is performed. As

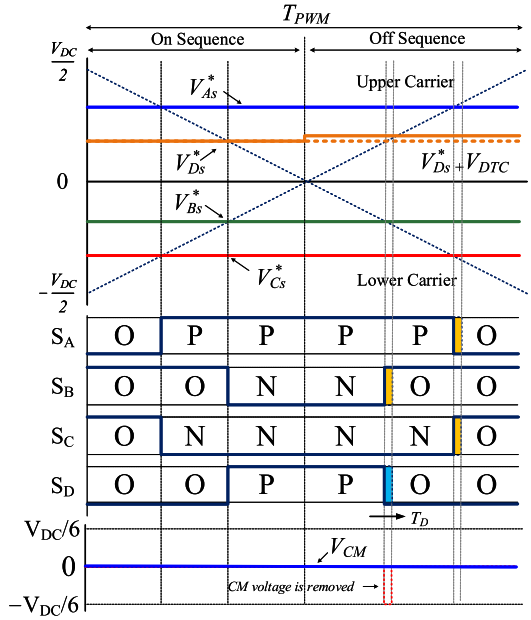

Fig. 9. Reduction of the remaining CM voltage applying dead-time effect compensation in sector 1.

a starting point of the design, an inductor ($L_{F.D}$), which has the biggest impedance at the switching frequency in the APF circuit, as shown in Fig. 11(b), is preferably designed with the same inductance, as the three-phase filter (L_F). Therefore, the single-phase inductor $L_{F.D}$ is designed as

$$L_{F.D} = L_F. \tag{26}$$

The next component to be designed is the shunt capacitor. This capacitor affects the impedance in two frequency bands, low and switching frequency, as shown in Fig. 11(a) and (b), respectively. Basically, as mentioned above, the capacitor C_S, must be designed with a value that satisfies the conditions in (14) in the switching frequency band to reduce the CM voltage. In addition, sufficient impedance should be provided for suppressing the current due to the difference between V^*_{off} and V^*_{Ds} generated in the low-frequency band, corresponding to the third-order of the fundamental frequency (180 Hz).

The impedance of the APF circuit excluding the bypass capacitor is defined, as expressed in (27), and Fig. 12 shows the impedance according to the shunt capacitor sizes

$$Z_{\mathrm{APF}.LC}(\omega) = j\left(\frac{3\omega^2 L_{F.D} C_S - 1}{3\omega C_S}\right) L_F. \tag{27}$$

In case the capacitor is high enough (e.g., 10 μF) to satisfy the condition in (14), it is difficult to suppress the current at the low frequency due to a very low impedance. This does not mean that the capacitor should be very small (e.g., 0.1 μF), to achieve high impedance at the low frequency, because it is not possible to obtain sufficient impedance to satisfy (14) at the switching frequency. Therefore, there is a need for generally applicable shunt capacitor design criteria.

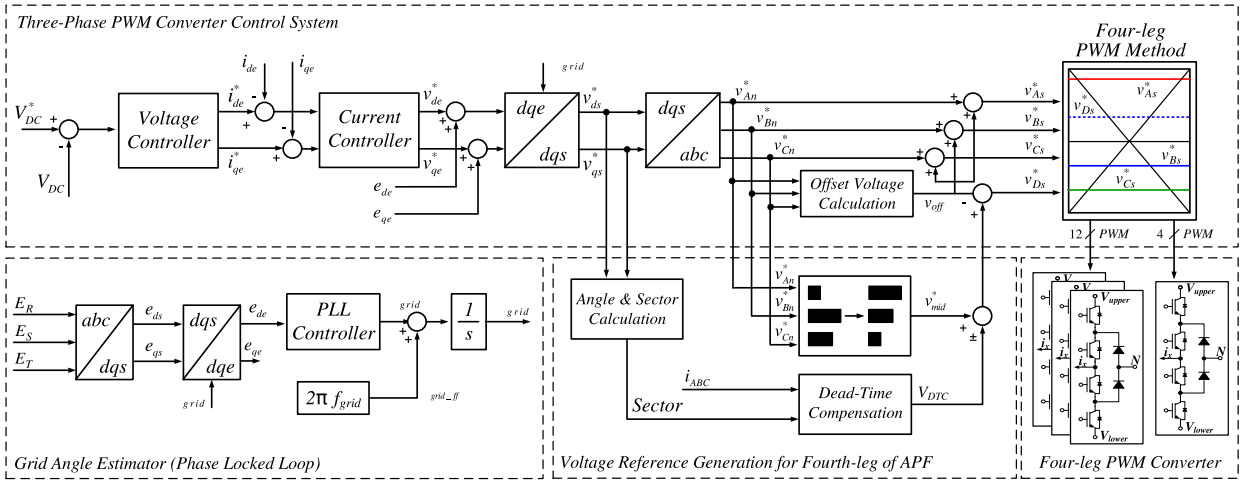

Fig. 10. Block diagram of the entire control system and PWM generator for the four-leg PWM converter that includes the APF circuit.

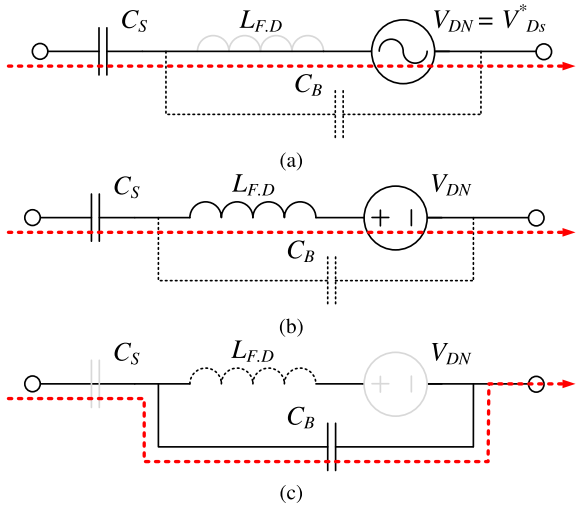

Fig. 11. APF circuit configuration and current path according to the frequency bands. (a) Low frequency. (b) Switching frequency. (c) High frequency.

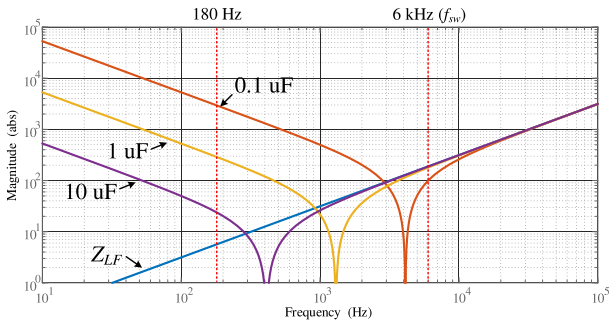

Fig. 12. Impedance analysis of the *LC* circuit in the APF according to shunt capacitor size.

Considering (14) and (27), the impedance relation at the switching frequency can be defined as

$$kZ_{LF}(\omega_{sw}) = Z_{\text{APF}.LC}(\omega_{sw}) \tag{28}$$

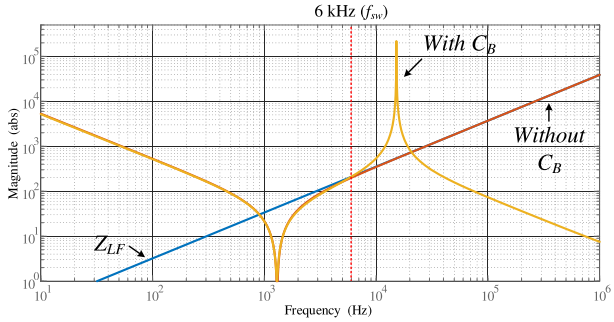

Fig. 13. Impedance analysis of the *LC* circuit with the bypass capacitor.

where ω_{sw} is the angular speed at the switching frequency and coefficient k means the impedance ratio between Z_{LF} and $Z_{\text{APF}.LC}$.

Since $Z_{\text{APF}.LC}$ is generally lower than Z_{LF} and the total impedance of the APF circuit increases by the connection of the bypass capacitor, the value of k can be selected between 0.9 and 0.95. As a result, the shunt capacitor can be designed as (29). For example, if $L_{F.D}$, f_{sw}, and k are 5 mH, 6 kHz, and 0.95, respectively; C_S should be more than 0.94 μF

$$C_S > \frac{1}{3(1-k)\omega_{sw}^2 L_{F.D}}. \tag{29}$$

The main purpose of connecting the bypass capacitor is to reduce high-frequency noise, as shown in Fig. 11(c). Fig. 13 shows the bypass capacitor connection allows the APF circuit to have a low impedance in the high-frequency band, in contrast to the *LC* circuit, which has a high impedance in the high-frequency band. In addition, the connection of the C_B also provides impedance compensation at the switching frequency. The impedance of the APF circuit (Z_{APF}) can be derived as (30), and the two resonant frequencies can be defined in (31)

$$Z_{\text{APF}}(\omega) = j\left(\frac{\omega^2 L_{F.D}(3C_S + C_B) - 1}{3\omega C_S(1 - \omega^2 L_{F.D} C_B)}\right) \tag{30}$$

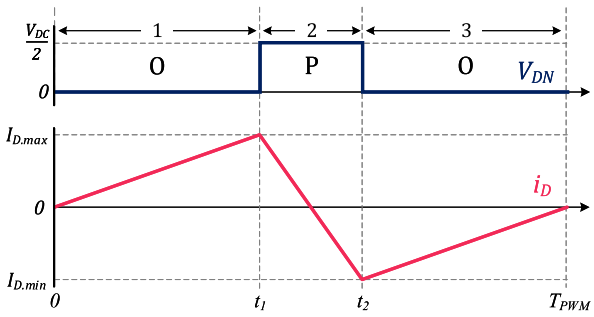

Fig. 14. Fourth leg current during a PWM period (O-P-O switching sequence).

$$f_{r1} = \frac{1}{2\pi\sqrt{L_{F.D}(C_B + 3C_S)}},\ f_{r2} = \frac{1}{2\pi\sqrt{L_{F.D}C_B}}. \tag{31}$$

Finally, the bypass capacitor should be designed so that the condition of the impedance at the switching frequency can satisfy (14). As a result, the capacity of the bypass capacitor can be selected as

$$C_B = \frac{1}{\omega_{sw}^2 L_{F.D}(3\omega_{sw}^2 L_{F.D}C_S + 1)}. \tag{32}$$

If C_B is higher than the result of (32), Z_{APF} increases and the resonant frequency f_{r2} decreases. Regarding the resonant frequency, it is recommended to be more than twice the switching frequency to avoid the effect of resonance.

B. Fourth-Leg Converter

To select proper power semiconductors composed in the fourth leg, it is required to analyze the fourth-leg current i_D, especially the peak current for calculating switching losses. From (8) and (9) in Section II, the fourth-leg current can be defined with V_{conv}, V_{DN} and shunt capacitor voltage (V_{sc}), as expressed in (33). i_{CM} can be negligible because it is a high-frequency current

$$i_D = \frac{3}{4L_F}(V_{\text{conv}} - V_{DN} - V_{sc}). \tag{33}$$

As illustrated in Fig. 14, the current i_D during one PWM cycle can be divided into three areas when the fourth leg operates with the O-P-O switching sequence in Fig. 8(e). Since the current under the condition of Fig. 8(f) is symmetrical to that of Fig. 8(e), the analysis can be applied in the same manner. Supposing an initial current is 0 A, the maximum and minimum peak current can be obtained at t_1 and t_2, respectively. Each peak current can be used to calculate the switching and conduction losses. In addition, the voltage across the shunt capacitor can be assumed as given in (34) considering the average V_{conv}, which is the same as the offset voltage in (22), and V_{Ds}^* in (24)

$$V_{sc} = V_{off} - V_{ds}^* = 2V_{\text{mid}}^*. \tag{34}$$

The time for areas 1 and 3 can be obtained by subtracting T_L from a PWM period T_{PWM}. As a result, two peak currents can

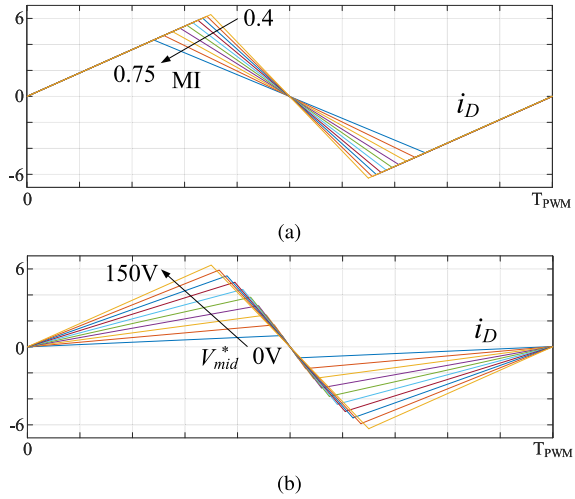

Fig. 15. Effect of V_{DC} and V_{mid}^* on fourth-leg current (L_F = 2.5mF, $T_{\text{PWM}} = 200\ \mu$s). (a) V_{DC} from 1500 to 800 V. (b) V_{mid}^* from 0 to 150 V.

be achieved as follows:

$$\begin{aligned} I_{D.\max} &= \frac{3}{4L_F}(-2V_{\text{mid}}^*)\frac{T_{\text{PWM}} - T_L'}{2} \\ &= -\frac{3}{4L_F}V_{\text{mid}}^*\left(1 - \frac{3\,|V_{\text{mid}}^*|}{V_{DC}}\right)T_{\text{PWM}} \end{aligned} \tag{35}$$

$$\begin{aligned} I_{D.\min} &= \frac{3}{4L_F}(V_{\text{conv}} - V_{DN} - 2V_{\text{mid}}^*)T_L' + I_{D.\max} \\ &= -\frac{3}{4L_F}\left(\frac{2V_{DC}}{3} + 2V_{\text{mid}}^*\right)\left(\frac{3\,|V_{\text{mid}}^*|}{V_{DC}}\right)T_{\text{PWM}} + I_{D.\max}. \end{aligned} \tag{36}$$

Under the ideal condition, it can be derived that the average current for one PWM period is 0 A because the change in current during the last region is equal to $I_{D.\max}$. In (35) and (36), the main factors affecting the fourth-leg current are the dc-link voltage and medium value among the three-phase voltage references. Among them, dc-link voltage has the most significant impact on the peak current, but the magnitude of the peak current is limited considering the generally used modulation index of about 0.4–0.7, as shown in Fig. 15(a). In the case of V_{mid}^*, even though it is related to the grid voltage, there is less impact on the current than V_{DC}, because it changes a little according to the output power. Fig. 15(b) shows the peak current when V_{mid}^* changes from zero to 150 V, which is near the maximum voltage if the line-to-line grid voltage is $380V_{\text{rms}}$.

In addition to the current analysis, switching characteristics of gate drivers and power semiconductors, such as turn-ON and -OFF times and propagation delay, must be considered when designing the fourth leg. If the switching characteristics are much different from those of a three-phase converter, the performance of the CM voltage reduction will be degraded. To minimize this, semiconductors with similar characteristics to the three-phase converter should be selected for the fourth leg. In addition, the gate driver circuit should also be designed to make the characteristics as close as those of the three-phase converter.

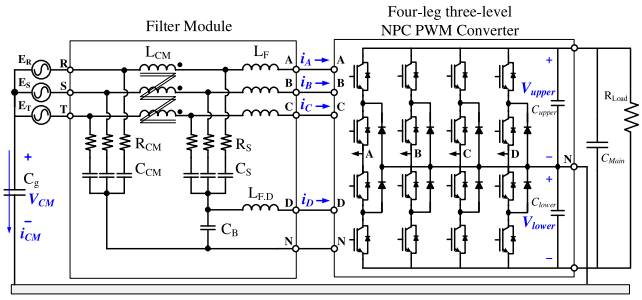

Fig. 16. Circuit configuration for the experiment.

TABLE III
CONDITIONS AND SPECIFICATIONS FOR SIMULATION AND EXPERIMENT

Symbol	Parameter	Value (Simulation)	Value (Experiment)
E_{RST}	Input grid voltage	380 V_{rms}	220 V_{rms}
f_{grid}	Grid frequency	60 Hz	60 Hz
V_{DC}	DC-link voltage	1500 V	400 V
f_{sw}	Switching frequency	5 kHz	6 kHz
T_D	Dead time	2 μs	2 μs
C_{dc}	Upper&lower dc capacitors	1 mF	660 μF
C_g	Leakage capacitor	10 pF	1 nF
C_{main}	Main dc capacitor	2 mF	1 mF
R_{load}	DC load resistor	-	98 Ω
P_{out}	Output power	0∼52 kW	1.6 kW
L_F	Inductor	2.5 mH	5 mH
C_S	Shunt capacitor	1.5 μF	1 μF
R_S	Damping resistor for C_S	1 Ω	3 Ω
C_B	Bypass capacitor	33 nF	22 nF
L_{CM}	CM inductor	-	2.5 mH
C_{CM}	CM capacitor	-	1.1 μF
R_{CM}	Damping resistor for C_{CM}	-	3 Ω

V. SIMULATION AND EXPERIMENTAL RESULTS

Fig. 16 shows the circuit configuration of the four-leg three-level NPC PWM converter with CM and DM filters and Table III presents the conditions and specifications of this configuration for simulation and experiment. In the simulation, a CM filter (L_{CM}, C_{CM}, and R_{CM}) is not considered and a variable current source is applied to the dc-link instead of a resistive load (R_{load}). In the experiment, the CM filter is connected to the converter and the CM capacitors C_{CM} are tied to the neutral point of dc-link, assuming an ungrounded system.

Fig. 17 shows simulation results of three-phase current, dc capacitor voltages, and CM voltage and current when the dc output power changes. It can be seen that the fourth leg starts to remove the CM voltage and current from 0.3 s, and this operation does not affect the three-phase current and dc voltages. Fig. 17(e) and (f) are zoomed-in waveforms of Fig. 17(d) and (e), respectively, at about 0.3 s. Before 0.3 s, CM voltage, which is a result of $V_{CM.\mathrm{conv}}$, changes at the switching frequency, and this voltage causes CM current, which flows into other systems as a form of EMI. On the other hand, after running the fourth leg from 0.3 s, the voltage corresponding to $V_{CM.\mathrm{conv}}$ is removed, and only the voltage applied to the shunt capacitors is observed.

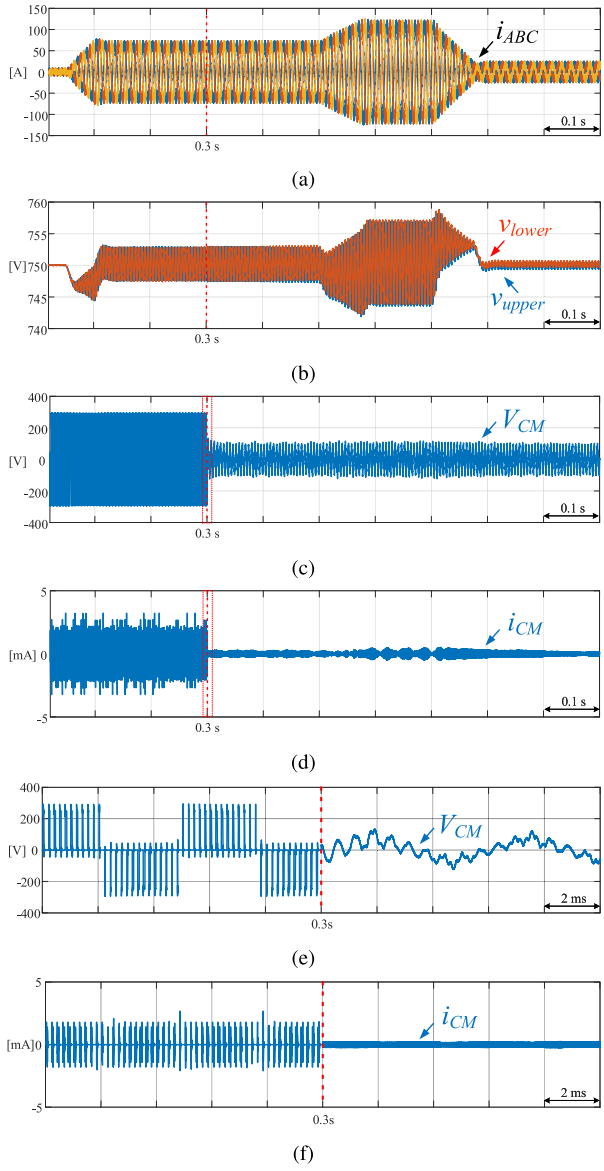

Fig. 17. Simulation results of CM voltage reduction under the dc output power change (a) Three-phase current. (b) Upper and Lower DC capacitor voltage. (c) and (d) CM voltage and current. (e) and (f) Zoomed-in waveform of CM voltage and current.

As a result, the CM current is also significantly reduced from about 2 to 0.3 mA. Furthermore, the CM voltage reduction is not affected by the change in dc output power. Even though the use of the APF and the output power changes, the dc voltage is not seriously unbalanced. This is because the small voltage vectors, which have a significant impact on dc capacitor voltage imbalance, are not used for the LMZ PWM method. supposing a crucial dc voltage imbalance occurs, the dc voltage can be balanced by allowing small vectors only for a short time and additional CM voltage can be removed by the APF, as shown in simulation results of Fig. 18.

For the experiment, a PWM converter module in Fig. 19(a) consists of the four legs of the three-level NPC PWM converter, and each leg is symmetrical. Moreover, a control board based on DSP TMS320c28346 and FPGA Cyclone IV is used as the PWM

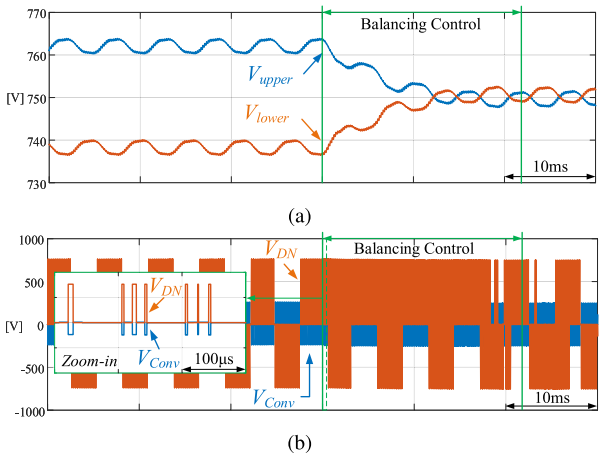

Fig. 18. Simulation results of DC voltage balancing control. (a) DC voltage. (b) $V_{CM.\text{conv}}$ and V_{DN}.

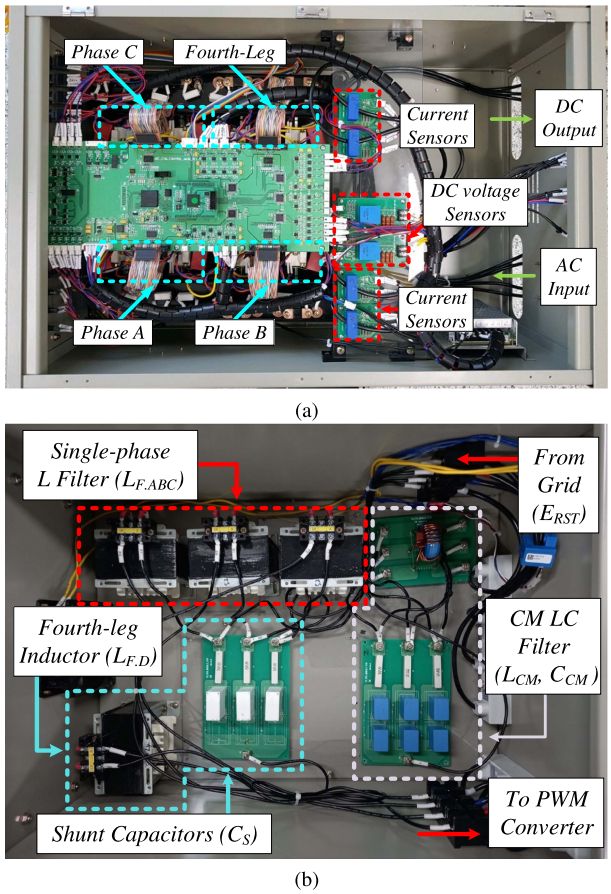

Fig. 19. Experimental setup. (a) Four-leg PWM converter module. (b) Filter module [L_F, C_S and CM filter (L_{CM}, C_{CM})].

converter. A filter module is equipped with four single-phase inductors, shunt capacitors, and a CM *LC* filter for reducing EMI, as presented in Fig. 19(b). As depicted in Fig. 16, the filter module is connected to the three-phase voltage source on the Y-connection side of the isolated transformer. The conditions and specifications for the experiment are shown in Table III.

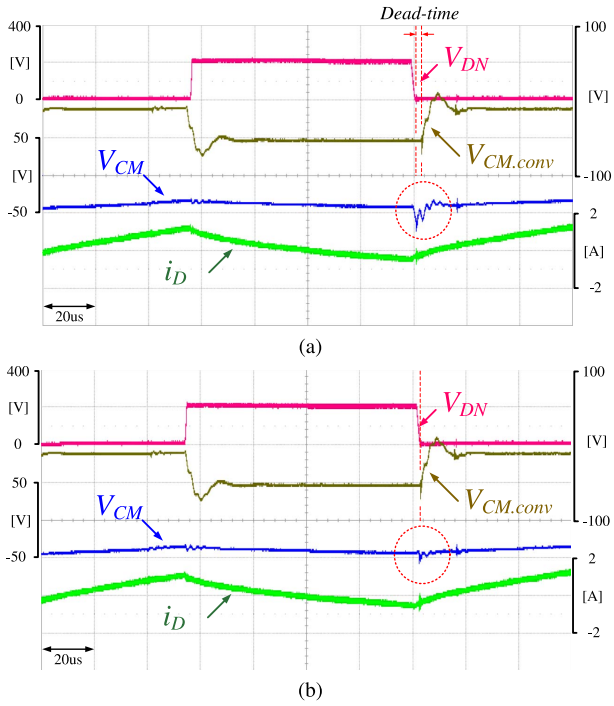

Fig. 20. Experimental results of the proposed CM voltage reduction using the APF. (a) Without dead-time compensation. (b) With dead-time compensation.

Fig. 20 shows the experimental results of the proposed CM voltage reduction using the APF. In Fig. 20(a), the CM voltage $V_{CM.\text{conv}}$ is generated by the three-phase PWM converter controlled with the LMZ PWM method. If the APF is not applied, the converter outputs the CM voltage $V_{CM.\text{conv}}$ to the grid. By applying the APF with the proposed method, $V_{CM.\text{conv}}$ can be reduced by V_{DN}, which is the voltage output of the fourth leg. However, there is residual CM voltage due to the effect of dead time, as indicated by the red circle. Fig. 20(b) shows the result obtained by applying the proposed dead time effect compensation scheme. As explained in Section III, a voltage equivalent to the dead time is injected into the voltage reference of the fourth leg (V_{Ds}^*) during the off-sequence to increase the on-time of V_{DN}. The remaining CM voltage in Fig. 20(a) is removed at the moment when the fall of V_{DN} coincides with the rise of $V_{CM.\text{conv}}$.

Fig. 21 presents the experimentally measured CM voltage and current waveforms. If the IPD PWM, which is generally used, is applied to the three-phase PWM converter, the CM voltage and current waveforms in Fig. 21(a) are obtained. In this case, the CM voltage changes six times during a single PWM period (T_{PWM}), and this voltage variation generates six CM current spikes, according to (2). Fig. 21(b) shows the CM voltage and current output of the three-phase converter with the LMZ PWM before application of the APF. The CM voltages of 0 V and $-V_{DC}/6$ (-66.7 V) are generated, and they change twice. The moments at which the CM voltage changes, the CM current rises. If the proposed strategy is applied without the dead time effect compensation, the CM voltage can be reduced, as illustrated in Fig. 21(c). However, the CM voltage and current

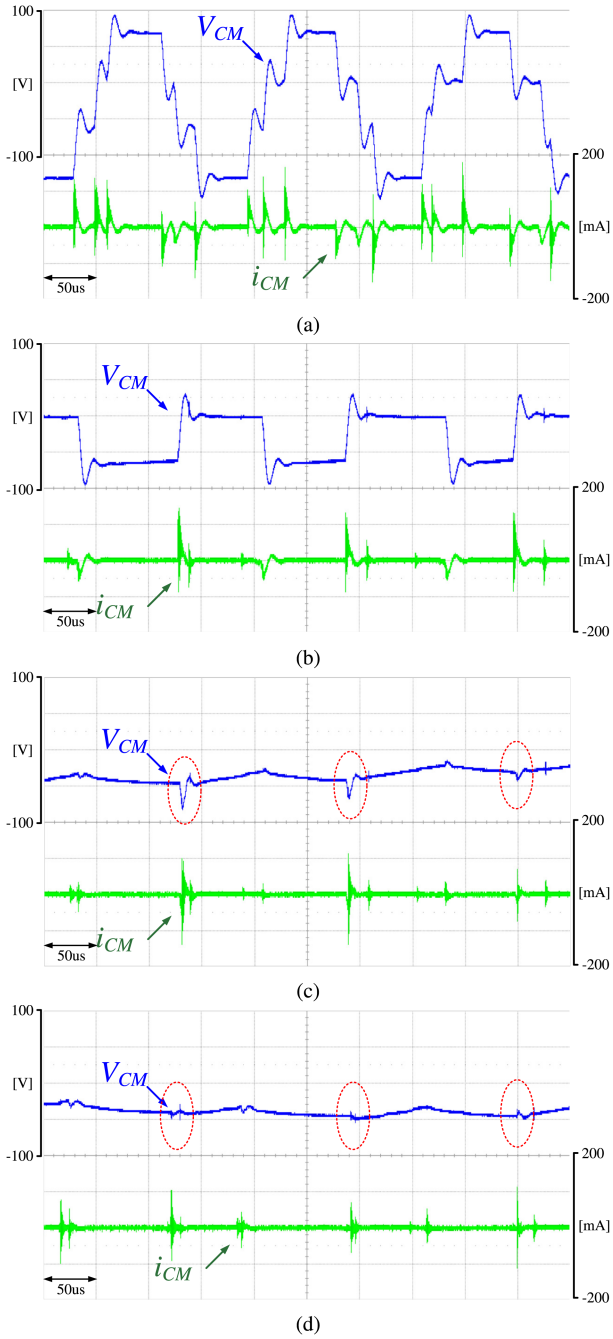

Fig. 21. Experimental results of CM voltage and current. (a) IPD PWM. (b) LMZ PWM. (c) Proposed strategy without dead-time compensation. (d) Proposed strategy including dead-time compensation.

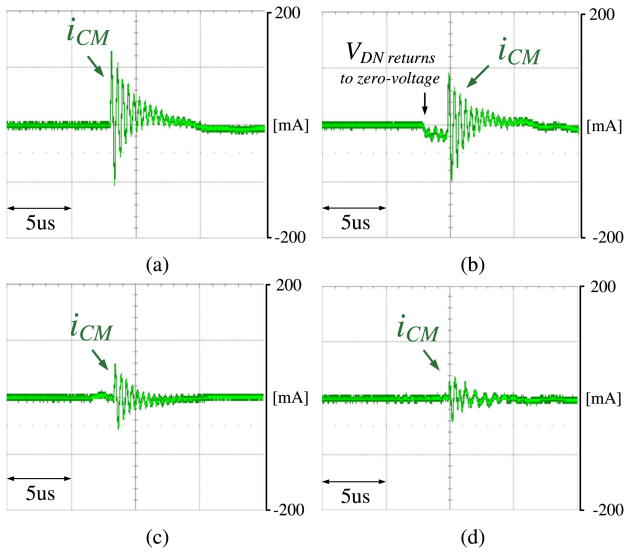

Fig. 22. Magnified CM current waveforms. (a) LMZ PWM without APF. (b) Proposed strategy without dead-time compensation. (c) Proposed strategy with dead-time compensation. (d) Proposed strategy with bypass capacitor.

still occur owing to the dead-time effect, even though the CM voltage and current are removed when the CM voltage changes from 0 V to $-V_{DC}/6$ in Fig. 20(a). Fig. 21(d) shows the result of the proposed strategy with the dead-time effect compensation. The CM voltage and the current due to the dead time are further reduced relative to the result in Fig. 21(c).

To verify that the proposed CM voltage reduction strategy with the APF is effective in reducing the CM current, Fig. 22 shows the magnified view of the current waveforms presented in Fig. 21. Before applying the APF, a CM current of up to 220 mA_{pk}, including a high-frequency resonance, occurs as shown in Fig. 22(a), which is a magnified view of the result shown in Fig. 21(b). Fig. 22(b) shows the CM current waveform obtained when the proposed strategy without the dead time compensation is used. As shown in Fig. 20(a), V_{DN} decreases to zero slightly ahead of the CM voltage $V_{CM.\text{conv}}$ by the dead time. As a result, a residual CM current remains owing to the V_{DN}. After the dead time of 2 μs, the CM current due to $V_{CM.\text{conv}}$ occurs. Fig. 22(c) shows that the CM current is reduced by about 100 mA_{pk} compared to the results presented in Fig. 22(a) and (b), after applying the proposed CM voltage reduction with the APF including the dead-time compensation. Finally, as shown in Fig. 22(d), the generated CM current is further reduced to 80 mA_{pk} or less when the bypass capacitor is added to the APF circuit.

Although the reduction of CM voltage and current with the proposed strategy is confirmed in Figs. 20–22, these experimental results are insufficient to demonstrate the reduction of EMI clearly. As shown in Fig. 23, therefore, this article presents conducted EMI measurements with EMC specifications [CISPR11 Group1(<20 kVA) QP] to prove the effectiveness of the proposed CM voltage reduction with the APF. The conducted EMI is measured using a signal analyzer (CXA 9000B, Keysight) through a line impedance stabilization network (LISN, ENV432, Rohde&Schwarz). Fig. 23(a) shows two measured conducted EMI depending on using the APF with the proposed CM voltage strategy. It can be seen that EMI exceeds the specified noise level defined in CISPR11 when the APF circuit is disconnected from the three-phase line. On the other hand, the measurement result with the APF circuit with the proposed strategy satisfies the requirement. It is confirmed that the conducted EMI is reduced by 10 –15 dB μ V on average at frequencies lower than 5.5 MHz. In particular, the proposed CM voltage reduction strategy with the APF is effective at frequencies less than 1 MHz, meaning the results can meet the specifications. Fig. 23(b) shows another EMI

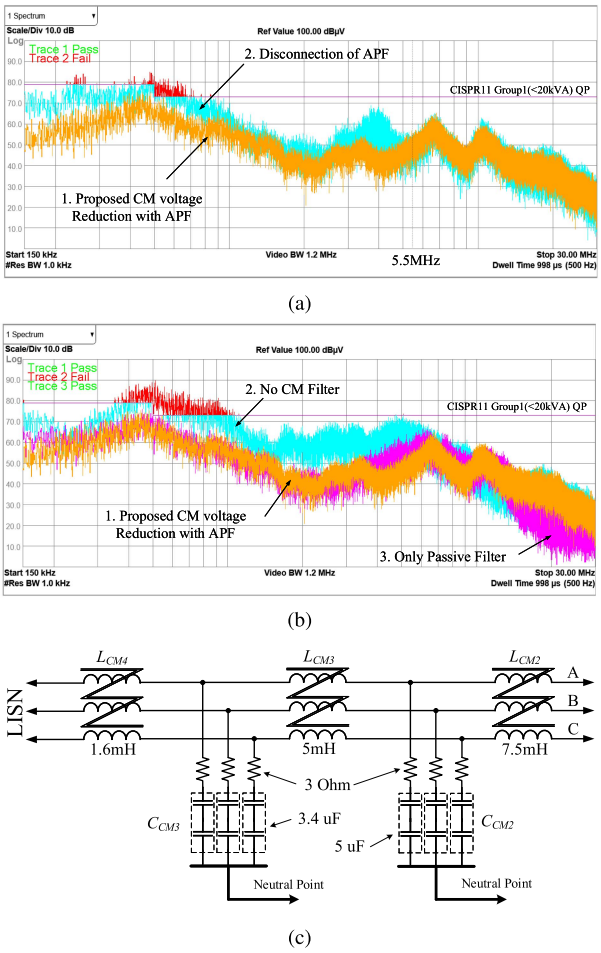

Fig. 23. Conducted EMI measurement result. (a) Effect of the proposed CM voltage reduction with APF. (b) Comparison between passive CM filters and the proposed method. (c) Passive CM filter circuits of Case 3 in (b).

measurement result under three conditions: 1) no CM filters, 2) only passive CM filters, and 3) with the proposed method. If there is no CM filter to reduce CM EMI generated by the converter, noise exceeds the limit by up to 15 dB μ V. After configuring passive CM filters depicted in Fig. 23(c), it is possible to measure satisfying the requirement, as shown in Fig. 23(b). From these results, it can be confirmed that using the proposed strategy can remove CM choke coils (L_{CM2}: 7.5 mH and L_{CM4}: 1.6 mH), and reduce the size of the filters, CM inductance, and capacitance (L_{CM3}, C_{CM2}, and C_{CM3}).

The proposed CM voltage reduction with the APF is based on the LMZ PWM used for the three-phase converter. When the LMZ PWM is used, the quality of phase current is inevitably worse than that when the widely used IPD PWM is employed because IPD PWM uses the three nearest voltage vectors to the voltage reference V^*. The main purpose of the APF proposed herein is to reduce the conducted EMI by eliminating the CM voltage, but it is necessary to evaluate the quality degradation of the phase current. Fig. 24 shows the experimental waveforms of the phase current and the FFT and THD results obtained using a power analyzer (WT3000, Yokogawa). As shown in Fig. 24(a), IPD PWM generates small harmonics at the switching frequency of 6 kHz, and the average THD of the three-phase

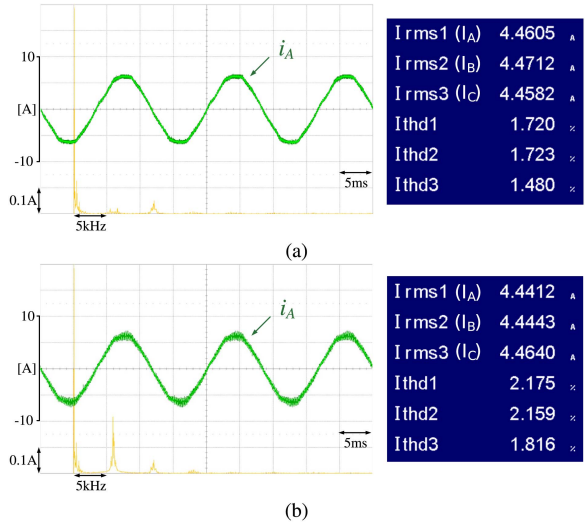

Fig. 24. FFT analysis and THD measurements of phase current. (a) IPD PWM. (b) Proposed strategy (LMZ PWM).

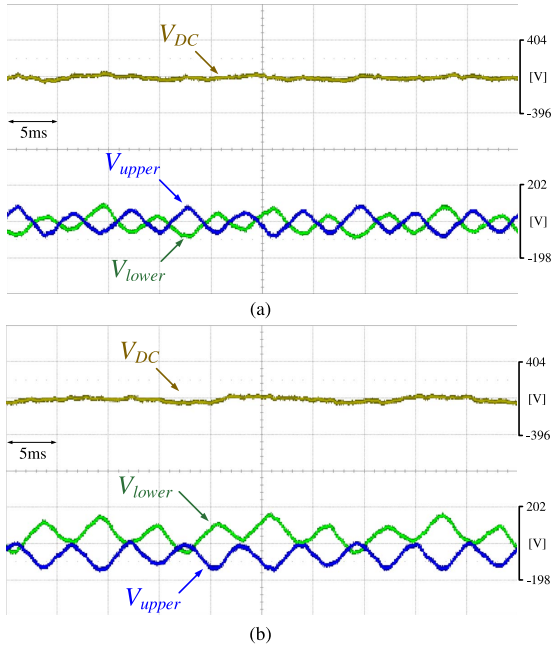

Fig. 25. Experimental results of DC voltages. (a) IPD PWM. (b) Proposed strategy (LMZ PWM).

current is 1.641 %. However, when the APF and the LMZ PWM are used, prominent harmonics are generated at the switching frequency, as shown in Fig. 24(b), and the average THD is 2.05 %, which is 24 % higher than that achieved with the IPD PWM. Therefore, tradeoffs must be considered when applying the proposed method. Nevertheless, a reduction in CM EMI over 10 dB μ V is beneficial enough.

Fig. 25 presents the effect of the proposed CM voltage reduction strategy on dc capacitor voltages. Fig. 25(a) shows the experimental waveforms of dc voltage when IPD PWM is used in the converter. Because the three-level NPC PWM converter is operated as an ac/dc active rectifier, the upper and lower dc voltages can be balanced naturally. Each upper and lower dc voltage contains ripple components with a peak-to-peak value

TABLE IV
LOSS AND EFFICIENCY OF THE ENTIRE CONVERTER SYSTEM AFTER APPLICATION OF THE PROPOSED STRATEGY

APF disconnection (only LMZ PWM)				With APF and proposed strategy				APF losses
$P_{in}[W]$	$P_{\text{out}}[W]$	Loss$[W]$	Eff.[%]	$P_{in}[W]$	$P_{\text{out}}[W]$	Loss$[W]$	Eff.[%]	
349.1	332.6	16.5	95.30	359.1	332.6	26.5	92.62	10.0
683.6	660.9	22.7	96.68	693.8	660.9	32.9	95.26	10.2
1023.1	993.1	30.0	97.06	1033.3	993.2	40.1	96.12	10.1
1358.4	1320.2	38.2	97.19	1368.3	1320.1	48.2	96.48	10.0
1699.2	1651.8	47.4	97.21	1709.3	1652.1	57.2	96.65	9.8

of approximately 1.3 V. These voltage ripples are caused by the medium-voltage vectors, which represent the third order (180 Hz) of the fundamental frequency, and are controlled within approximately 1 V. Fig. 25(b) shows dc voltage waveforms measured when the LMZ PWM is used with the proposed strategy with the APF. The LMZ PWM basically does not cause severe dc voltage imbalance because it does not use any small voltage vectors that affect dc voltage imbalance between upper and lower dc voltages. Only the medium-voltage vectors affect the dc voltages, but it merely creates a voltage ripple similar to that of Fig. 25(a). Even though the average upper and lower dc voltage differ by 1.5 V, they do not diverge more despite any changes in the output power from zero to 1.6 kW, as confirmed in the simulation result.

The proposed CM voltage reduction strategy is based on a single leg of the three-level NPC converter and shares the dc link of the three-phase PWM converter. For this reason, using the fourth leg is expected to reduce the efficiency of the entire converter system. Although the current flowing through the fourth leg and its adverse effects on efficiency are smaller than that of the three-phase converter, the losses due to the APF should be evaluated experimentally. Table IV summarizes the losses and efficiency of the entire converter and the losses due to the APF according to output power. The losses due to the APF can be determined by comparing the total losses before and after applying the proposed CM voltage reduction with the APF. For example, with disconnection of the APF circuit, the measured losses and efficiency are 47.4 W and 97.21 %, respectively, when the power output of the converter is 1651.8 W. With applying the APF with the proposed method, the losses and efficiency are approximately 57.2 W and 96.65 %, respectively, under the same output power condition. As a result, losses due to the APF is 9.8 W. It remains almost the same at approximately 10 W even if the output power increases. This is because the current flowing through the APF is nearly independent of the three-phase current and output power, as described in Section IV-B.

VI. CONCLUSION

This article proposes a modulation strategy with APF to reduce the conducted CM EMI output by grid-connected three-phase three-level NPC ac/dc PWM converters. In APF, the fourth leg is used as the amplifier to reduce the CM voltage through shunt capacitors and single-phase inductor. To eliminate CM voltage which is the main cause of EMI, this article proposed the modulation strategy based on LMZ PWM including the compensation scheme to remove residual CM voltage due to the dead time. In addition, this article describes the design procedure for the APF circuit for the effective reduction of CM voltage. The simulation and experimental results indicate that the proposed strategy is effective at eliminating CM voltage, which in turn reduces the CM current reduction by up to 60 %. Furthermore, the conducted EMI measurements indicate that the proposed strategy reduces conducted EMI by 10 dB μ V on average at frequencies lower than 5.5 MHz, which validates its performance. Finally, this article presents the effects of the proposed reduction strategy on the phase current, dc voltage imbalance, and losses.

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