Comprehensive Modeling, Optimization, and Experiment of 10-kV/15-kA Forced Resonant DC Circuit Breaker

Bei Zhang, Xiangyu Zhang, Jin Yang, Wei Li, and Lei Qi

***Abstract*—The dc circuit breaker (DCCB) is the core equipment for ensuring the safe and stable operation of the dc transmission system. It often requires high response times. In recent years, a new type of DCCB topology called forced resonant DCCB (FR-DCCB) has attracted widespread attention. It requires only a small amount of power electronic devices to provide mechanical switch zero crossing with *LC* circuit. And this topology offers advantages, such as multiple zero-crossing points, low cost, and the potential for faster response time. However, compared with the traditional DCCB solutions, the breaking process of FR-DCCB is extremely complex, which leads to the lack of mature control methods and parameter design theories. Therefore, to further improve the performance of FR-DCCB, this article proposes an efficient resonance control method based on the real-time feedback correction and a fast reclosing control method based on closing surge energy recovery, respectively, and also forms a complete optimization parameters design method. In addition, the parameters design method is presented to significantly reduce the oscillation time of FR-DCCB, thereby improving its response speed to meet engineering requirements. A prototype of FR-DCCB with the largest current breaking capacity has been developed and the effectiveness of the proposed methods has been verified.**

***Index Terms*—Fast reclosing method, forced resonant direct current circuit breaker (FR-DCCB), high efficient resonance control method, optimization parameters design method.**

I. Introduction

THE voltage-source converter-based dc transmission technology is widely used due to its low loss, strong controllability, and effective solutions for generation-grid-load coordinated control [1], [2], [3]. However, the dc transmission system is characterized by low impedance, fast fault diffusion, and high fault current rise rate, which pose a serious threat to the safe operation of the system. Fast and reliable fault isolation is a prerequisite for ensuring the safe and stable operation of the dc transmission system [4], [5]. Nevertheless, compared with ac systems, dc current lacks natural zero-crossing points, making it difficult to break dc fault current. The development of dc circuit breaker (DCCB) provides a solution to this problem [6], [7]. Currently, the DCCBs that have been widely utilized in engineering include the hybrid DCCB based on power electronic switches and the mechanical DCCB based on current injection [8], [9].

The hybrid DCCB utilizes series impedance to construct voltage or magnetic coupling induced voltage, enabling the transfer of current. The interruption of current is achieved by employing fully controlled power electronic devices. The first successful development of a hybrid DCCB was accomplished by Genji et al. A commercially valuable hybrid DCCB capable of breaking a fault current of 16 kA at a voltage level of 320 kV within 5 ms was introduced by ABB in 2011 [10]. In 2016, the State Grid Smart Grid Research Institute implemented a hybrid DCCB with specifications of 200 kV/15 kA/3 ms in the Zhejiang Zhoushan dc grid project [11]. In 2020, Tsinghua University achieved the application of a hybrid DCCB with specifications of 500 kV/25 kA/3 ms based on coupled negative voltage commutation in the Zhangbei dc grid project [12]. ABB also successfully developed a prototype of a hybrid DCCB with specifications of 320 kV/20 kA/3 ms in 2021. In 2013, North China Electric Power University proposed a thyristor-assisted hybrid DCCB that incorporates a current commutation function into the transfer branch, eliminating the need for a specially designed auxiliary commutation device. They successfully built a prototype with ratings of 3 kV and 6 kA [13]. However, the hybrid DCCBs require a significant amount of power electronic devices, which leads to high costs and limits their ability to break high current levels due to limitations in device switching capabilities [14], [15], [16]. At the same time, existing mechanical DCCBs only offer limited current zero-crossing points with mechanical switches (MSs), resulting in unreliable arc extinction [17], [18].

Consequently, in recent years, a new type of DCCB topology called forced resonant DCCB (FR-DCCB) has been proposed and attracted widespread attention due to its advantages of providing multiple zero-crossing points for MS and low cost. This structure mainly uses different forms to build a voltage source for the oscillation branch, forcing the voltage amplitude of the oscillation capacitor to increase continuously, thus increasing

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the amplitude of the oscillation current and offsetting the fault current to help the MS extinguish the arc. The FR-DCCB can be classified into two types based on the method of constructing the voltage source: precharged capacitor in the oscillation branch and variable resistor in the main branch. In 2016, SCiBreak AB proposed a DCCB scheme using a vacuum interrupter assisted by a power electronic converter, which requires only a small number of power electronic devices and has low requirements for their breaking capacity [19], [20]. In 2018, based on this scheme, SCiBreak AB formally proposed a voltage-source converter-assisted resonant current DCCB and then built a 40-kV prototype in 2020 to verify its ability to break 10-kA fault current within 3 ms, and indicated its potential for further application in multiport scenarios [21]. In 2021, North China Electric Power University proposed a forced resonant mechanical DCCB based on the variable resistor method in the main branch, which successfully built a 10-kV/8-kA prototype and further achieved an 80-kV/10-kA prototype experiment in 2022 [22], [23].

However, as the FR-DCCB is still in its early stages, many research works have not yet been conducted. Furthermore, this method requires coordination between the switching frequency of power electronic devices and the oscillation frequency of the oscillation branch, as well as coordination among the voltage-source level, impedance value of the oscillation branch, and fault current level, among other parameters, which are coupled together. As a result, the control and parameter design process of the FR-DCCB is more complex than that of the traditional DCCBs. Therefore, the reclosing method based on the FR-DCCB, mature control methods, and parameter optimization methods is lacking. Consequently, in this article, based on the characteristics of the FR-DCCB structure, a high efficient resonance control method based on real-time feedback correction is proposed to effectively counteract the influence of stray inductance on the oscillation efficiency. A fast reclosing control method based on closing surge energy recovery is also proposed, which eliminates the need for additional charging and discharging of the capacitor before the reclosing process. Finally, based on the above analysis, a complete optimization parameters design method is proposed, which reduces the cost of the oscillation branch by more than 50%. Then, a 10-kV/15-kA prototype is built to verify the effectiveness of the proposed methods.

The rest of this article is organized as follows. Section II introduces the working principle and characteristics of FR-DCCB. Section III proposes the efficient resonance control method. In Section IV, the fast reclosing method is proposed. Section V forms a complete optimization parameters design method. In Section VI, the prototype experiment is carried out. Finally, Section VII concludes this article.

II. Working Principle and Characteristics of FR-DCCB

A. Topology of FR-DCCB

The topology of FR-DCCB is shown in Fig. 1, which is composed of three parts in parallel: main branch, oscillation branch, and energy absorption branch. Among them, the main branch is composed of MS (MS), which is used to conduct the load current of the system with low loss. The oscillation branch

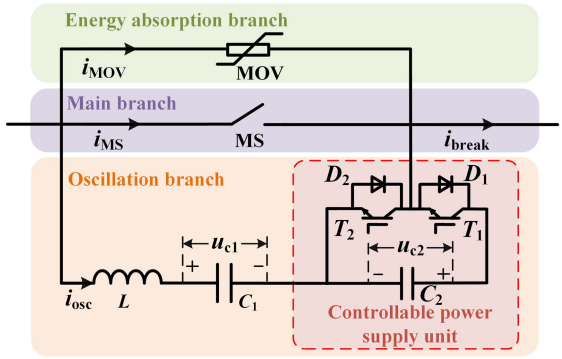


Fig. 1. Topology of FR-DCCB.

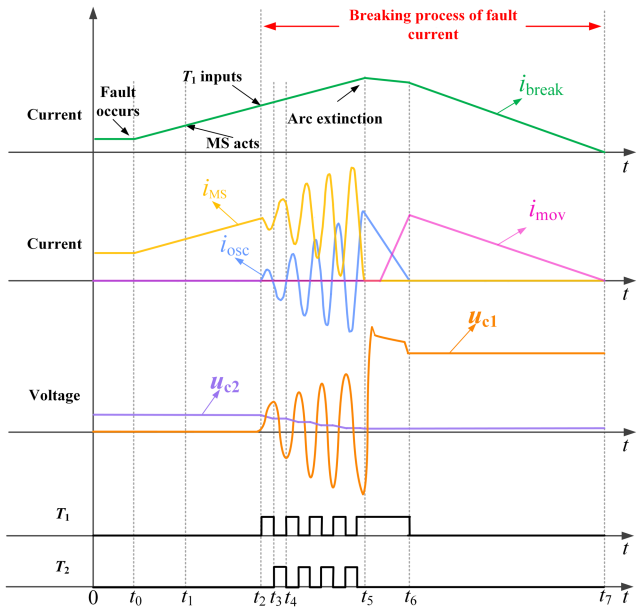


Fig. 2. Breaking waveforms of the FR-DCCB.

is composed of oscillation capacitor (C_1), inductor (L), and controllable power supply unit based on the half-bridge submodule, which is used to generate oscillation current with increasing amplitude and create multiple zero-crossing points for MS. The energy absorption branch is composed of a metal-oxide varistor (MOV), which is used to suppress the breaking voltage and absorb the energy stored by the inductive components.

B. Working Principle and Characteristics

The working principle of FR-DCCB is shown in Fig. 2. In Fig. 2, $i_{\rm break}$ is the current flowing through DCCB, $i_{\rm MS}$ is the current flowing through MS, $i_{\rm osc}$ is the current flowing through oscillation branch, and $i_{\rm mov}$ is the current flowing through the energy absorption branch. In addition, T_1 and T_2 are the control signals of the full control power electronic devices on the upper and lower bridge arms of the half-bridge module, respectively.

1) 0 - t_0: The MS is closed, T_1 and T_2 are turned OFF, and the capacitor C_2 is precharged by the external dc power supply.
2) t_0 - t_1: When a fault occurs at t_0, the DCCB sends the opening command to MS at t_1.

3) t_1 - t_2: The MS is triggered to separate at t_1 until reaching sufficient insulation distance at t_2 and the controllable power supply unit operates.
4) t_2 - t_3: T_1 is controlled to be turned ON, and T_2 is controlled to be turned OFF, forming an oscillation circuit of C_2 - T_1 - MS - L - C_1. C_1 is charged by C_2 through MS until the oscillation current ($i_{\rm osc}$) crosses zero at t_3.
5) t_3 - t_4: T_2 is turned ON and T_1 is turned OFF, and C_1 discharges through the T_2-L circuit until the oscillation current ($i_{\rm osc}$) crosses zero at t_4, and the voltage of C_1 reverses.
6) t_4 - t_5: Based on the natural frequency of the oscillation branch, when the positive and negative half waves of $i_{\rm osc}$ cross zero, T_1 and T_2 are alternately turned ON and turned OFF, and the processes of t_2 - t_3 and t_3 - t_4 are repeated until $i_{\rm osc}$ reverse offset with fault current at t_5. Then, $i_{\rm MS}$ crosses zero and MS extinguishes the arc, and the fault current is transferred from the main branch to the oscillation branch.
7) t_5 - t_7: After that, the C_1 will be charged by fault current until the MOV voltage reaches the reference voltage. The fault current is completely transferred from the oscillation branch to the energy absorption branch at t_6, and MOV will absorb energy. Finally, the whole breaking process is completed at t_7.

According to the above analysis of the working principle of the FR-DCCB, without considering the conduction loss of MS, T_1, and T_2, it can be concluded that the oscillation impedance ($Z_{\rm osc}$) and the oscillation frequency (f) of the oscillation circuit can refer to (1), respectively

$$\begin{cases} Z_{\rm osc} = \sqrt{\frac{L}{C_1}} \\ f = \frac{1}{2\pi\sqrt{LC_1}}. \end{cases} \tag{1}$$

Meanwhile, it can be obtained that, under ideal conditions, the $i_{\rm osc}$ gradually increases with the oscillation half-wave numbers. The $i_{\rm osc}$ and the oscillation capacitor voltage are shown as follows:

$$\begin{cases} i_{\rm osc} = \frac{nU_{\rm dc}}{Z_{\rm osc}} \sin \omega t \\ u_{c1} = -nU_{\rm dc} \cos \omega t + u_{\rm osc} \\ n = \left\lceil \frac{\omega t}{\pi} \right\rceil \end{cases} \tag{2}$$

where n is the half-wave number of $i_{\rm osc}$, u_{c1} is the voltage of C_1, $U_{\rm dc}$ is the precharged voltage of C_2, and $u_{\rm osc}$ is the output voltage of the controllable power supply unit.

III. High Efficient Resonance Control Method

A. Analysis of the Influence Mechanism of Stray Inductance

The analysis of the oscillation process in Section II is based on the ideal situation. In practical applications, the oscillation circuit is inevitably accompanied by stray inductance, leading to a change in oscillation frequency and oscillation impedance during the oscillation process, as shown in the following equation:

$$\begin{cases} Z_{\rm stray} = \sqrt{\frac{L+L_{\rm stray}}{C_1}} \\ f_{\rm stray} = \frac{1}{2\pi\sqrt{(L+L_{\rm stray})C_1}} \end{cases} \tag{3}$$

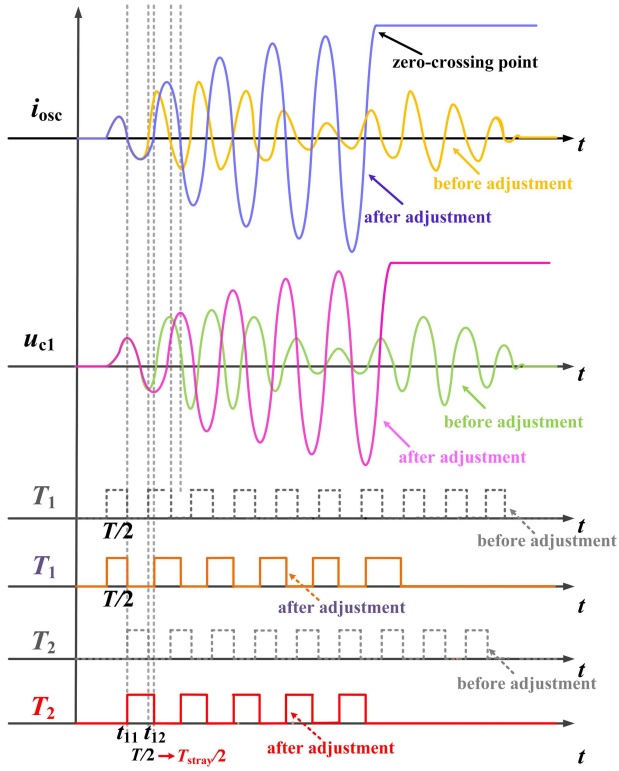


Fig. 3. Comparison of control signal before and after adjustment.

where $L_{\rm stray}$ represents the stray inductance value of the oscillation circuit, $Z_{\rm stray}$ represents the circuit impedance value after considering the stray inductance, and $f_{\rm stray}$ represents the circuit oscillation frequency value after considering the stray inductance.

The waveforms of its oscillation current and voltage are shown in Fig. 3 before adjustment. Referring to (2), the influence of the increase of impedance value on the amplitude of oscillation current is obvious. Nevertheless, the impact of the mismatch between the frequency of the oscillation circuit and power electronic devices being turned ON/OFF is more intricate, which is mainly divided into the following two aspects.

1) Influence on Voltage Accumulation of C_1*:* The mismatch of oscillation frequency will affect the accumulation of voltage value. Given the presence of stray inductance, the oscillation frequency of the oscillation circuit can be expressed as $f_{\rm stray}$, while the corresponding oscillation period is denoted as $T_{\rm stray}$. It follows that the duration of half waves is $T_{\rm stray}/2$. However, the frequency of the actual control signal remains f, resulting in a half-wave duration of $T/2$. As shown in the control signal of T_1 before adjustment in Fig. 3, the voltage value on C_1 after the end of the first positive half-wave oscillation of the current refers to the following equation:

$$\begin{aligned} U_{c1{\rm stray}1} &= \int_0^{T/2} \frac{i_{\rm osc}}{C_1} dt = \int_0^{T/2} \left(\frac{U_{\rm dc}}{C_1 Z_{\rm stray}} \sin \omega_{\rm stray} t \right) dt \\ &= -U_{\rm dc} \left(\cos \omega_{\rm stray} \frac{T}{2} - 1 \right) \end{aligned} \tag{4}$$

where ω_{stray} represents the angular frequency of the oscillation circuit after considering stray inductance, and ω_{stray} can refer to the following equation:

$$\omega_{\text{stray}} = \frac{2\pi}{T_{\text{stray}}}. \tag{5}$$

If there is no stray inductance, the frequency of power electronic devices being turned ON/OFF is consistent with the frequency of circuit oscillation, that is, $T_{\text{stray}} = T$, then $U_{c1\text{stray}1}$ reaches the maximum ($2U_{\text{dc}}$). If $T_{\text{stray}} > T$, as shown in the curve of u_{c1} before adjustment in Fig. 3, the voltage accumulation on C_1 will be less than $2U_{\text{dc}}$. Definition $a = T_{\text{stray}}/T$, obviously $a \leq 1$. Then, a is taken into (4), and the result refers to the following equation:

$$U_{c1\text{stray}1} = -U_{\text{dc}}(\cos(a\pi) - 1). \tag{6}$$

Furthermore, during the negative half-wave oscillation, the oscillation process of the final quarter cycle of the current concludes prematurely, precluding the voltage from fully reversing. Consequently, the voltage amplitude decreases once more, with the voltage amplitude of C_1 at the termination of the second half-oscillation wave ($U_{c1\text{stray}2}$) being shown as follows:

$$\begin{aligned} U_{c1\text{stray}2} &= U_{c1\text{stray}1} + \int_{T/2}^{T} \frac{i_{\text{osc}}}{C_1} dt \\ &= U_{c1\text{stray}1} + \int_{T/2}^{T} \left(\frac{U_{c1\text{stray}1}}{C_1 Z_{\text{osc}}} \sin \omega t \right) dt \\ &= -U_{\text{dc}}(\cos(a\pi) - 1)(1 - \cos(2a\pi) + \cos(a\pi)). \end{aligned} \tag{7}$$

Recursively, the voltage amplitude of C_1 at the end of the $N-1$ half-oscillation wave is shown in (8), and the voltage amplitude at the end of the N half-wave (all N are even numbers) is shown in (9)

$$\begin{aligned} &U_{c1\text{stray}(N-1)} = U_{c1\text{stray}(N-2)} \\ &-(U_{\text{dc}} - U_{c1\text{stray}(N-2)})(\cos((N-1)a\pi) - \cos((N-2)a\pi)) \end{aligned} \tag{8}$$

$$\begin{aligned} &U_{c1\text{stray}N} = U_{c1\text{stray}(N-1)} \\ &- U_{c1\text{stray}(N-1)}(\cos(Na\pi) - \cos((N-1)a\pi)). \end{aligned} \tag{9}$$

It can be found that the mismatch between the frequency of oscillation circuit and power electronic devices being turned ON/OFF will have a cumulative impact on the voltage amplitude of C_1 during the whole oscillation process, and then the impact on the amplitude of the oscillation current will be greater and greater. The greater the stray inductance, the greater the frequency offset, and the slower the voltage accumulation on C_1. Meanwhile, with the increase of the oscillation impedance, the amplitude of the oscillation current increases more slowly, which results in the slow breaking speed and even failure.

2) Phenomenon of Energy Backflow: The mismatch between the control signals of the oscillation circuit and the power electronic devices instigates the occurrence of a large current flowing through T_1 when it is turned OFF. At this time, there is a voltage difference between L and C_1, which causes the diodes

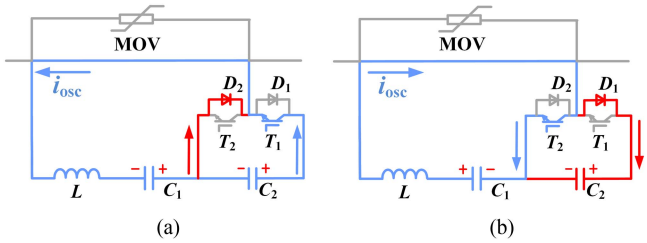


Fig. 4. Circuit of freewheeling (Only display the oscillation current path).

to withstand the positive voltage. This means that even when T_2 is turned ON after T_1 is turned OFF, the current will continue to flow through D_2, forming a circuit of C_1-D_2-MS-L, as shown in Fig. 4(a). If T_1 and T_2 are controlled according to the actual oscillation circuit frequency (f_{stray}), T_1 will be turned OFF when the oscillation current approaches zero. However, if they are controlled according to the originally intended frequency (f), the complete energy transfer process from C_2 to C_1 will be prematurely terminated. This results in a decrease in the accumulated voltage in C_1, which gradually accumulates with increasing oscillation period. Consequently, the oscillation current amplitude and efficiency are significantly reduced. Similarly, after T_2 is turned OFF, even if T_1 is turned ON, it will continue to flow through D_1, as shown in Fig. 4(b), forming a circuit of C_1 - L – MS - D_1 - C_2, which will cause the phenomenon of C_2 being charged by C_1 in reverse. With the increase of oscillation current, the higher the oscillation current is when T_2 is turned OFF, the more the voltage is transferred from C_1 to C_2, and the higher the energy loss is. As shown in u_{c1} before adjustment in Fig. 3, u_{c1} increases slowly, even negatively. When the current decreases again, T_2 is turned OFF with a shorter energy transfer time and less energy transfer. The voltage and current increase again, and then decrease again. Repeat the above process, resulting in a failure to break current.

B. High Efficient Resonance Control Method

In conventional control methods, the control signal frequency for T_1 and T_2 is initially set to f, which corresponds to the desired oscillation frequency. This results in T_1 and T_2 having a conduction time of $T/2$ in each period, as indicated by the gray control signals in Fig. 3. However, the presence of stray inductance in the actual oscillation circuit can significantly impede efforts to enhance the voltage and current amplitudes during the oscillation process. In order to ensure that the breaking process proceeds smoothly, it is imperative to promptly ascertain the actual oscillation period, which can be determined by utilizing the time ($T_{\text{stray}}/4$) from zero to the apex of the first half wave of the oscillation current in the experiment. This will facilitate the derivation of the actual circuit oscillation frequency and the determination of the stray inductance exhibited by the actual oscillation circuit.

After determining the real-time oscillation frequency, the feedback correction can reduce the frequency of the control signal to increase the conduction time of the power electronic devices in each cycle so that the voltage on C_1 can be accumulated

more, and the current and voltage waveforms in the oscillation process after adjustment can be obtained, as shown in Fig. 3. Initially, the control signal for T_1 has a conduction time of $T/2$ in the first cycle based on the predetermined frequency. However, subsequent real-time feedback testing reveals the oscillation period to be T_{stray}. As a result, in the following conduction process, both the control signals for T_1 and T_2 are adjusted to have a conduction time of $T_{\text{stray}}/2$, aligning with the adjusted frequency f_{stray}. As shown in Fig. 3, at the initiation of the second half-wave oscillation ($t = t_{11}$), the control signal is modified, and its period is changed from T to T_{stray}. Fig. 3 represents the turn-OFF time of T_2 at t_{12}, which has obviously changed to $T_{\text{stray}}/2$. At this time, the absolute value of C_1 reverse voltage amplitude has increased after adjustment. Therefore, the amplitude of the current and voltage of the next half wave increases. Through this process, it can be clearly seen that, after adjustment, the frequency of power electronic devices being turned ON/OFF to match the oscillation frequency of the oscillation circuit, the time growth of the positive half wave of the oscillation current makes the voltage on C_1 accumulate. The time growth of the negative half wave of the oscillation current makes the voltage on C_1 almost completely reverse, providing a greater voltage difference to lay the foundation for the growth of the amplitude of the next oscillation current. Furthermore, this method effectively suppresses the problem of C_1 energy backflow to C_2, which is more conducive to the increase of the amplitude of oscillation current and voltage. The amplitude of current and voltage gradually increases according to the new oscillation frequency until the amplitude of the oscillation current is equal to the fault current and the direction is opposite. Then, MS crosses zero to extinguish the arc, solving the problem that the fault current cannot be broken before. Therefore, it is very effective to suppress the negative effects of stray inductance in the oscillation circuit by the efficient resonance control method based on the real-time feedback correction.

IV. Fast Reclosing Control Method

In the case of a dc grid that utilizes overhead lines, the likelihood of transient faults occurring is relatively high, and such faults typically dissipate within a duration of 200 ms. As a result, there is significant value in investigating the fast reclosing to guarantee the dependability of dc system supply. Depending on the nature of the fault, the DCCB may encounter one of the two scenarios following the reclosing process.

1) If the fault is a transient fault, the fault has disappeared when the DCCB is reclosed. At this time, after the DCCB is closed, the system will resume normal operation.
2) If the fault is a permanent fault, the fault current shall be broken again after the reclosing process.

The following will analyze the reclosing and rebreaking process of the FR-DCCB based on the permanent fault, as shown in Fig. 5.

1) *t_7- t_8:* When the first breaking process of the FR-DCCB ends, MS opens, T_1 and T_2 are turned OFF, and C_1 withstands the rated voltage of dc system.
2) *t_8 - t_9:* After a certain delay, MS receives the system command to close at t_8, and T_1 and T_2 are still turned OFF. At this time, an oscillation circuit of C_1 - L - MS - D_1 - C_2 will be formed, and C_2 will be charged by C_1, as shown in Fig. 6(a).
3) *t_9- t_{10}:* When the current flowing D_1 crosses zero, D_2 is conducted to form an oscillation circuit of C_1 - D_2 - MS - L, as shown in Fig. 6(b), and the voltage of C_1 oscillates in reverse.
4) *t_{10}- t_{11}:* The above process is repeated. The D_1 and D_2 are conducted alternately to form an oscillation circuit. The energy of C_1 is gradually absorbed by C_2. When the problem of high voltage on C_1 is solved, the energy of C_2 rises again.
5) *t_{11}- t_{12}:* The fault still exists, MS is still closed, T_1 and T_2 are still turned OFF, and the fault current rises.
6) *t_{12}- t_{15}:* The fault current is broken again according to the first breaking process. Since neither the system oscillation frequency nor the impedance value of the oscillation circuit has changed, the oscillation commutation time during rebreaking process depends on the energy of C_2 during the reclosing process.

Typically, reclosing operations are performed after a 200 ms breaking process. However, during this time, C_1 retains a high voltage, at least equal to the system voltage, which cannot be safely discharged in a short period. This poses challenges in

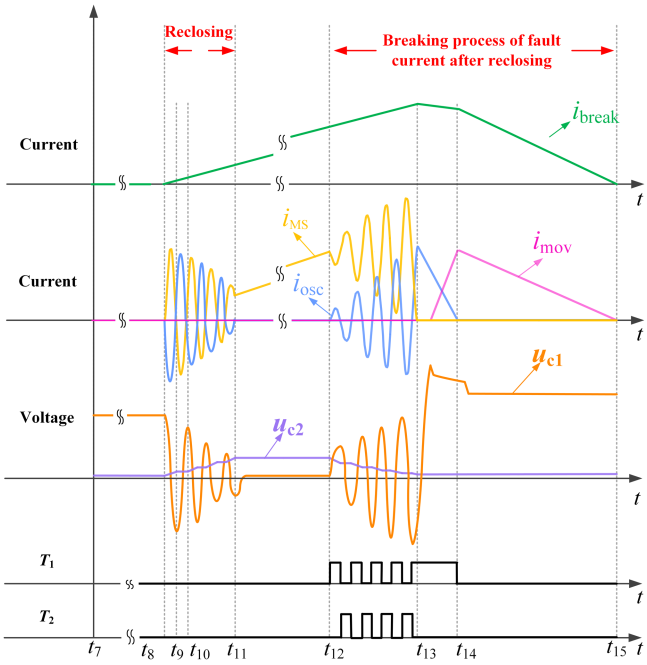


Fig. 5. Reclosing waveforms of the FR-DCCB.

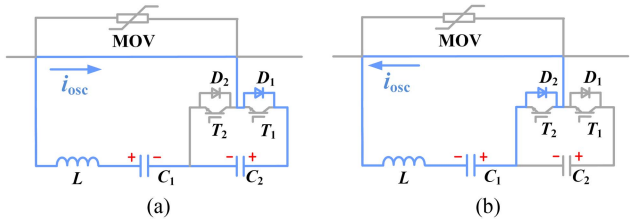


Fig. 6. Reclosing process of the FR-DCCB.

successfully achieving rebreaking process. Additionally, if C_2 is recharged using a precharging device after the voltage loss during the initial breaking process, it would result in a longer time cycle, thereby impacting the reclosing speed. To address these issues, the above novel reclosing method is proposed. During reclosing process, C_1 transfers its own energy to C_2 by instantaneous oscillation through diodes (D_1 and D_2) after MS is closed. There is no need to control fully controlled devices, and the operation is simple. At the same time, the spontaneous transfer process of energy not only solves the high-voltage problem of C_1 when the fault current is broken again but also enables the energy recovery of C_2, laying a foundation for the process of rebreaking the fault current under permanent fault.

The expression of oscillation frequency and circuit impedance value in the reclosing process is the same as (1). And the difference between the reclosing process and the first breaking process is that the voltage source changes from C_2 to C_1. In the meanwhile, there are two issues that need to be addressed. On the one hand, since C_1 withstands the system voltage after the first breaking process, with the increase of the dc voltage level of the system, the voltage value of C_1 is far greater than C_2, which may cause a large oscillation current problem even more than five times the fault current during the reclosing process. On the other hand, if the capacitance value of C_2 does not match the capacitance value of C_1, excessive energy absorbed by C_2 will cause a rise in its voltage and damage capacitors and devices (T_1 and T_2). In addition, the failure of rebreaking process may also occur due to too little energy recovery of C_2. Therefore, based on the discussion of the above two issues, the current safety and energy absorption issues in the reclosing process need to be addressed during the parameter design process, which will be discussed in Section V.

V. Optimization Parameters Design Method

A. Optimization Parameters Design Method

The cost of DCCB is an important index that restricts its realization of engineering application. Therefore, the goal of parameter design is to achieve the optimal cost on the premise of ensuring its functional completeness. The price of inductors is far less than that of capacitors and power electronic devices; therefore, the selection of capacitors (C_1 and C_2) and the numbers of power electronic devices will have a decisive impact on the final cost. The price of capacitors is proportional to their capacitance, and T_1 and T_2 are selected as injection-enhanced gate transistor (IEGT) in this design. Therefore, the optimal economic effect can be achieved by minimizing the value of capacitance and numbers of IEGT. To sum up, it can be concluded that the objective function for parameter design refers to (10), which needs to be minimized throughout the whole design process

$$\text{cost} = k_1\left(\frac{1}{2}C_1U_{c1}^2 + \frac{1}{2}C_2(kU_{\text{dc}})^2\right) + k_2N_pN_s \tag{10}$$

where k_1 is the price coefficient of capacitor, k_2 is the price of each IEGT, k is the voltage margin of C_2, N_p is the number of IEGT in parallel, which depends on the system fault current value, and N_s is the number of IEGT in series, which depends on the precharged voltage of C_2.

The minimum value of the objective function shall be guaranteed on the premise of ensuring the functional integrity of FR-DCCB, including breaking fault current, reclosing, and rebreaking, as well as the safe operation of key components. Taking account into the requirements of each process to achieve the functions of FR-DCCB, the specific constraints can be obtained as follows.

1) Reliable Break Fault Current: To ensure reliable breaking process, the peak value of i_{osc} shall be greater than the maximum value of fault current (I_{break})

$$i_{\text{osc}} > I_{\text{break}}. \tag{11}$$

In addition, in order to ensure the bidirectional breaking capacity of the FR-DCCB, if the maximum number of half waves generated in the oscillation process is N (considering bidirectional breaking, N is even), the oscillation current needs to reach the peak value of fault current in $N-1$ half waves. In that way, the oscillation frequency and precharged voltage shall meet the following equation:

$$(N-1)U_{\text{dc}} = (2fT_{\text{osc}} - 1)U_{\text{dc}} \geq \alpha I_{\text{break}}Z_{\text{osc}} \tag{12}$$

where α is the safety margin coefficient of the maximum breaking current, which is taken as 1.2 here. And T_{osc} is the oscillation time, that is, the time interval from the beginning of the oscillation to the zero-crossing point of i_{MS} will be subjected to the requirements of dc system for fault clearance time.

2) Oscillation Frequency: In order to improve the breaking speed of DCCB, the oscillation speed of i_{osc} should be as fast as possible. Referring to (12), it can be found that the higher the oscillation frequency is, the more beneficial it is to reduce the precharged voltage of C_2, reduce the number of fully controlled power electronic devices, and also reduce the parameters and volume of *LC* components. However, if the frequency is too high, it will bring risks to the reliable blocking after the MS is extinguished and safe operation of fully controlled power electronic devices. That is, the frequency should be selected as a higher value within the allowable range of safe operation of core components. Generally, the range of *di/dt* that can be interrupted by MS is 150–1000 A/μs [24], and the selection of oscillation frequency should refer to the following equation:

$$3\,\text{kHz} = f_{\min} \leq f \leq f_{\max} = 10\,\text{kHz}. \tag{13}$$

3) Limitation of Voltage Change Rate: In order to prevent the MS from rebreakdown, the growth rate of u_{c1} after the end of the oscillation commutation phase should be less than the dielectric strength recovery rate of MS ($U_{\text{MS}\cdot d}$) when the low current and fault current are broken

$$\frac{du_{c1}}{dt} = \frac{i_{\text{break}}}{C_1} < \frac{dU_{\text{MS\_}d}}{dt}. \tag{14}$$

4) Rated Voltage of Oscillation Capacitor: As C_1 will eventually withstand the dc system voltage, its rated voltage shall be selected higher than the rated voltage of dc system

$$U_{c1} \geq U \tag{15}$$

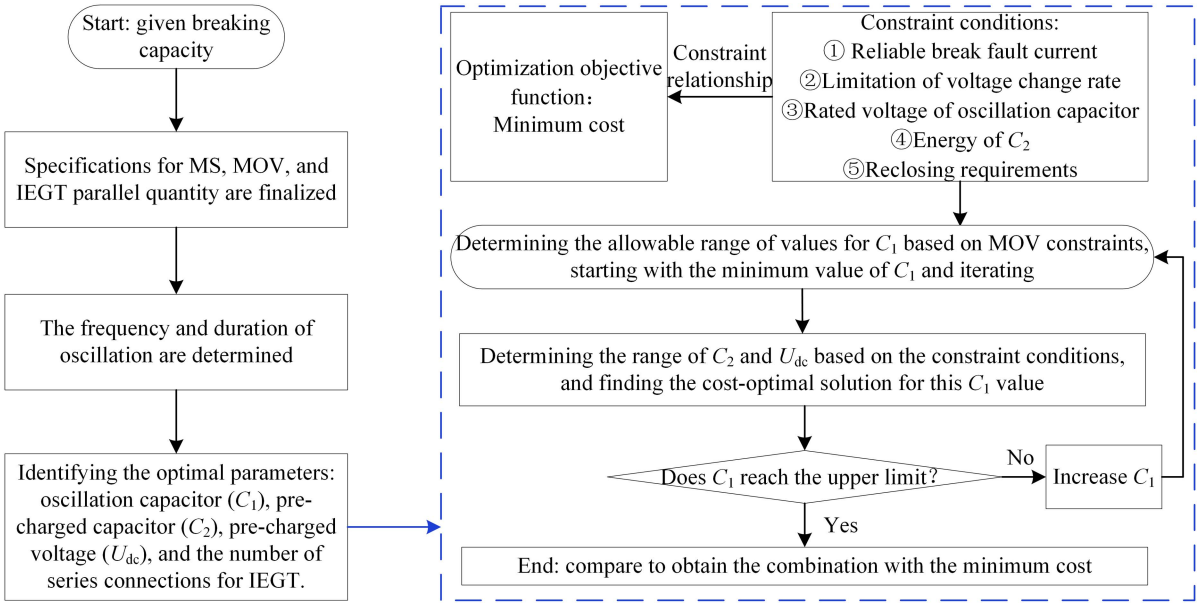


Fig. 7. Parameter design flowchart.

where U_{c1} is the rated voltage of C_1, and U is the rated voltage of dc system.

During the process of oscillation commutation, $i_{\rm osc}$ reaches the current amplitude in the $N-1$ (N) half-oscillation wave, at which time the voltage amplitude of C_1 is $NU_{\rm dc}$. In order to prevent C_1 from being broken down, the maximum voltage amplitude of C_1 in the process of oscillation commutation shall be lower than U_{c1}, as shown in the following equation:

$$NU_{\rm dc} \le U_{c1}. \tag{16}$$

5) Energy of C_2*:* The discharge of C_2 in the controllable power supply unit to C_1 and L is an energy transfer process. According to the law of energy conservation, after the end of the oscillation process, the energy stored on the L is zero, and all the energies released by C_2 are transferred to C_1. Therefore, in order to ensure the breaking reliability, the energy value of C_2 shall be greater than the energy value required by C_1. Taking into account the factors, such as energy loss in the oscillation process, it is necessary to reserve a certain margin (β), as shown in the following equation:

$$\frac{1}{2}C_2U_{\rm dc}^2 \ge \frac{1}{2}\beta C_1(NU_{\rm dc})^2 \tag{17}$$

where β is the margin of energy.

6) Reclosing: According to the above description of the reclosing process, it is necessary to ensure that the amplitude of the oscillation current is within the safety margin during the whole reclosing process, and the final voltage value of C_2 cannot exceed the limited value. If overvoltage and overcurrent problems occur, the safety of devices will be seriously challenged, even the devices will be damaged. That is to ensure that the energy absorbed by C_2 referring to (18) does not exceed 1.2 times of the energy released in the first breaking process, as shown in (19). Moreover, as the oscillation current amplitude will gradually decrease during the reclosing process, the current safety of the whole reclosing process can be guaranteed by ensuring that the amplitude of the first half-wave oscillation current referred to (20) is within the tolerance range of the device. It means that the current obtained from (20) is within the maximum current value that power electronic devices can withstand, as shown in (21)

$$W_{c2} = \frac{1}{2}C_2(\Delta U_{c2})^2 = W_{c1} = \frac{1}{2}C_1U_{c1\rm res}^2 = \frac{1}{2}C_1U^2 \tag{18}$$

$$\frac{1}{2}C_1U^2 \le 1.2\left(\frac{1}{2}C_2U_{\rm dc}^2 - \frac{1}{2}\beta C_1(NU_{\rm dc})^2\right) \tag{19}$$

$$I_{\rm reclosing} = \frac{U_{c1\rm res}}{Z_{\rm osc}} = \frac{U}{Z_{\rm osc}} \tag{20}$$

where U is the rated voltage of the dc system, $U_{c1\rm res}$ is the residual voltage on C_1 before the initiation of the reclosing process, and $I_{\rm reclosing}$ is the amplitude of the first half-wave oscillation current during the reclosing process

$$I_{\rm reclosing} \le I_{\rm IEGT}. \tag{21}$$

In conclusion, the parameter design procedure, as shown in Fig. 7, involves the following steps.

1) Begin by determining the voltage level of the FR-DCCB, its capability to break currents ($I_{\rm break}$), and the required breaking time.
2) Next, determine the rated voltage and breaking current capacity of the MS, which will guide the selection of the MOV. Additionally, based on the $I_{\rm break}$, the parallel quantity of T_1 and T_2 is determined.
3) Once the model of the MS is chosen, the frequency of the oscillation branch is determined. Moreover, the allowed oscillation time is established based on the time required for the MS to reach a sufficient insulation distance.
4) Based on the aforementioned conditions, select the values of C_1, C_2, $U_{\rm dc}$, and the number of series-connected IEGTs. The number of series-connected IEGTs remains constant

TABLE I
PERFORMANCE AND COST COMPARISON

Index	Before optimization	After optimization
Capacity	80 kV/15 kA	80 kV/15 kA
Frequency	10 kHz	10 kHz
C_1 value	30 μF	6.1 μF
C_1 cost	34.56 p.u.	7.03 p.u.
C_2 value/U_{dc}	5 mF/1.2 kV	10 mF/2.1 kV
C_2 cost	0.58 p.u.	3.53 p.u.
IEGT cost	10 p.u.	10 p.u.
Charing device	4 p.u.	4 p.u.
Total cost of oscillation branch (C_1, C_2, IEGT, and Charging device cost)	**49.14 p.u.**	**24.56 p.u.**
Safety of fast reclosing	Unsafe	Safe

The bold entities are emphasized to demonstrate their significance as the most intuitive and critical comparison data for the entire table, in order to illustrate the cost advantages of the optimization design method proposed in this article.

within a certain range of U_{dc} fluctuations. The selection process for these parameters can be carried out as follows.

a) The optimization objective is shown in (10).
b) The constraints are shown in (12), (14)–(17), (19), and (21).
c) Optimization method.
   i) The voltage rise rate of MOV at I_{break} must meet the requirement for its front wave time. Subsequently, the minimum value of C_1 is determined.
   ii) After the MS arcs, the current can be fully transferred to the MOV within a specified time (which depends on the required breaking time and the time for the MS to reach the sufficient insulation distance). Subsequently, the maximum value of C_1 is determined.
   iii) After determining the range of C_1 values, start the iteration from the minimum value of C_1. Furthermore, the range of C_2 values and U_{dc} values is determined within the specified constraints. Employ a program to search for the optimal combination that minimizes cost while satisfying the constraints at the specified C_1 value.
   iv) Continuously repeat the aforementioned process by iterating through the range of C_1 values. Then, compare the obtained results to identify the combination that yields the lowest cost.

By following this process, the optimal parameter combination can be obtained, ensuring the integrity of the FR-DCCBs breaking and reclosing functions under the required voltage level, breaking current level, and breaking time.

B. Cost Comparison

Using the aforementioned parameter optimization method, the cost comparison of the FR-DCCB before and after optimization for 80 kV/25 kA/3 ms is presented in Table I. The cost of each component is represented by the nominal value due to the differences in component costs across countries. In this article, 1 p.u. corresponds to 10 000 renminbi (RMB). The results show that after the parameter optimization process, the cost of the oscillation branch can be reduced by over 50% for the same voltage and current levels, and a safe reclosing process can be executed.

TABLE II
PARAMETERS OF THE FR-DCCB

The Parameter of FR-DCCB		Value
Oscillation branch	C_1 (μF)	30
	L (μH)	8
Controllable power supply unit	C_2 (mF)	5
	Precharged voltage U_{dc} (kV)	1.8
Energy absorption branch	Residual voltage of arrester U_{MOV} (kV)	16

VI. PROTOTYPE AND EXPERIMENTAL VERIFICATION

A. Parameter Selection and Prototype Development

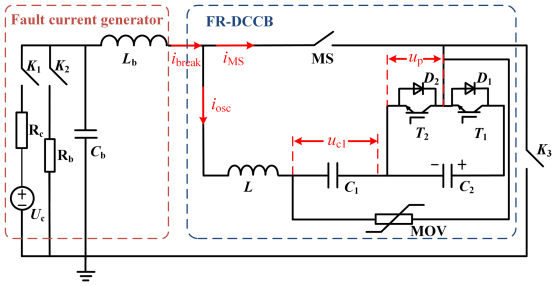
Taking the 10-kV DCCB as the research object, the experiment of breaking 15 kA within 3 ms and reclosing process are carried out using the topology, as shown in Fig. 1. The FR-DCCB parameters are selected, as shown in Table II, and T_1 and T_2 are selected as IEGT. Additionally, the energy coefficient (β) is selected as 1.7.

After determining the parameters of FR-DCCB, in order to simulate the actual situation, an experimental circuit is designed and a platform is built, as shown in Fig. 8.

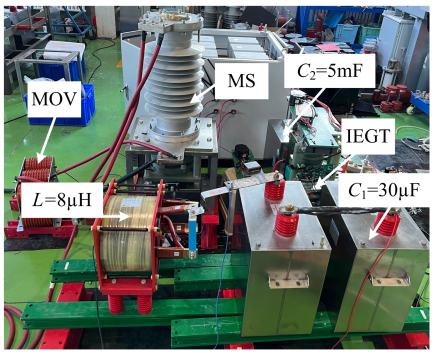
The platform is divided into fault current generator and experimental circuit. A fault current generator uses inductance (L_b) and capacitance (C_b) to simulate fault current waveform. To simulate the 15-kA fault current, the C_b is selected as 27.3 mF and the L_b is selected as 0.5 mH. When the C_b is charged to 2.2 kV, a 15-kA current can be generated to ensure the smooth running of the breaking test.

Regarding the selection of the placement location of the MOV in the energy absorption branch, for this experiment, the MOV is chosen to be connected in parallel between C_1 and the controllable power supply unit. This scheme ensures that the voltage across C_1 is limited near the MOV. During the energy absorption phase of the MOV, the fault current no longer flows through the controllable power supply unit, thereby protecting the power electronic devices.

In terms of MOV parameter selection, the reference voltage of the MOV should be higher than the maximum operating voltage of the system. The leakage current of the DCCB in the OFF-state should be controlled to a level at which the system



(a)



(b)

Fig. 8. Experimental setup. (a) Setup scheme. (b) Realized prototype.

isolation switch can be disconnected. In addition, the design of the MOV residual voltage should consider insulation and energy absorption levels. A lower residual voltage leads to a longer current clearing time and increased energy absorption for the same current breaking process. Conversely, a higher residual voltage increases the insulation level of the equipment but also raises the equipment cost. Generally, the MOV residual voltage is designed to be 1.4–1.6 times the system voltage. In order to match the system's rated voltage of 10 kV, the MOV with reference voltage of 11.5 kV and residual voltage of 16 kV is chosen. To ensure the safety of C_1 and the MS, as well as to minimize the steep wave voltage across the MOV, a front wave time of 1 μs is selected.

B. Design of Control Signal

Drawing upon the high efficient resonance control methodology, as outlined in Section III, the practical experimental process involves an initial measurement of stray inductance, followed by appropriate adjustments to the control signal, thereby mitigating the impact of stray inductance on the oscillation process. According to the selection of parameters in Table II, the oscillation frequency of oscillation circuit is 10 kHz, so the oscillation time of half a period is 0.05 ms. However, the actual measurement shows that the time of half-wave oscillation is 0.055 ms, so the actual oscillation frequency of the oscillation circuit is about 9.01 kHz. After the first half oscillation wave is completed, the frequency of the control signals of T_1 and T_2 needs to be adjusted.

The current and voltage waveforms of the control signal before adjustment are shown in the gray curve in Fig. 9. The maximum value of the oscillation current ($i_{\rm osc}$) only reaches 12.36 kA, which does not reach the fault current value, resulting

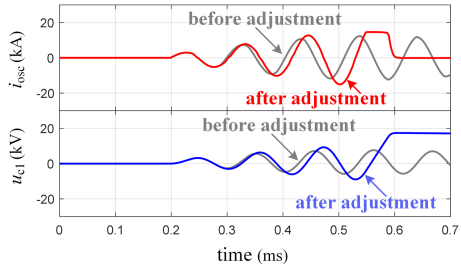


Fig. 9. Simulation comparison diagram before and after control signal adjustment.

in the failure of breaking. The current and voltage waveforms of the control signal after adjustment are shown in the red and blue waveforms in Fig. 9, respectively. The voltage on C_1 is continuously accumulated, forcing the amplitude of the oscillation current to rise. After 0.35 ms, that is, at the seventh half wave, $i_{\rm osc}$ and the fault current ($i_{\rm fault}$) are reversed offset, and the $i_{\rm MS}$ crosses zero to extinguish the arc, successfully realizing the breaking process. That is to say, the high efficient resonance control method based on real-time feedback correction can significantly improve the amplitude growth process of oscillation current and voltage, and can ensure the smooth progress of the breaking process.

C. Preliminary Test

In this experiment, it was first found through testing that when the oscillation frequency of the circuit is 9.01 kHz, the amplitude of oscillation current can reach 15 kA after 0.5 ms at a precharged voltage of 2.1 kV. However, when the oscillation frequency is 10 kHz and the precharged voltage is 1.8 kV, the amplitude of oscillation current can reach 15 kA within 0.425 ms. Furthermore, the MS used this time can achieve a current interruption of 15 kA at a maximum frequency of 10 kHz.

Therefore, 10 kHz is ultimately chosen as the oscillation frequency of this experiment, and the total inductance of the circuit after considering the stray inductance is adjusted to 8 μH.

What is more, the preliminary test before the whole experiment found that the time from sending the turn-OFF signal to the voltage of IEGT being fully established was about 8 μs, while the time from sending the turn-ON signal to the conduction of the IEGT was about 3 μs. Considering the offset of the turn-ON and turn-OFF delay time, and leaving a certain margin, 6 μs is selected as the deadtime of the final control signal, which can effectively prevent the simultaneous conduction of T_1 and T_2, avoid damaging the device and affecting the safe operation of the DCCB.

D. Experimental Verification

Based on the parameters selected in Table II, the oscillation frequency of the oscillation circuit is set at 10 kHz. Subsequently, the experiment of FR-DCCB interrupting 15-kA current is carried out. The current and voltage waveforms obtained in the experiment are shown in Fig. 10.

When $t = 0.1$ ms, K_3 is closed and $i_{\rm break}$ starts to rise, and the MS is triggered to separate at 3.3 ms. When $t = 5.3$ ms, MS

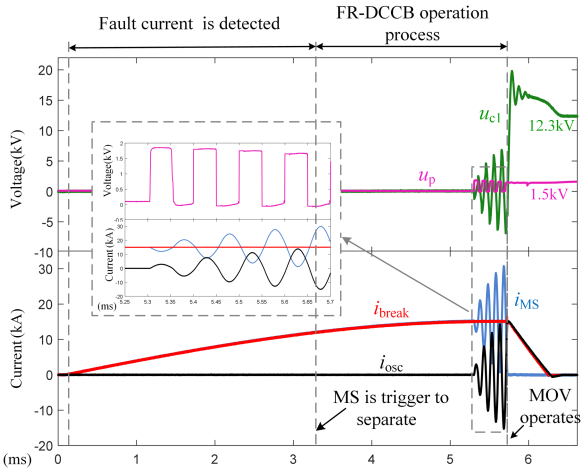


Fig. 10. Waveforms of 15-kA breaking experiment.

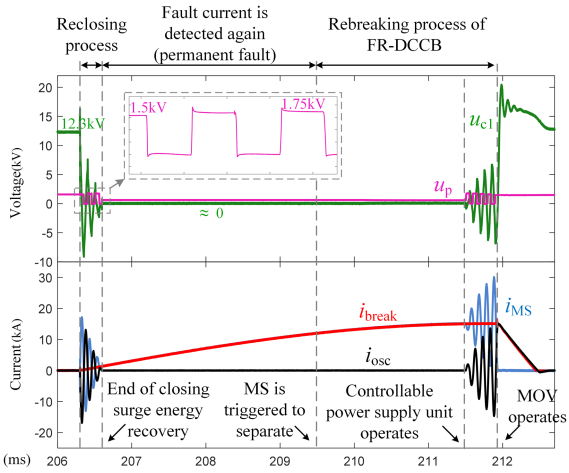


Fig. 11. Waveforms of reclosing and rebreaking experiment.

reaches sufficient insulation distance, and T_1 is triggered to turn ON, and the DCCB starts the internal oscillation commutation process. After that, T_1 and T_2 are conducted alternately at a fixed frequency until $t = 5.725$ ms, after nine half waves of oscillation current, i_{osc} reaches the value of fault current, which is offset against the fault current, and the MS crosses zero to extinguish the arc. Subsequently, the fault current is utilized to charge C_1, resulting in an achievement of the action voltage of MOV within 0.1 ms. Then, the fault current transfers to the energy absorption branch, and the MOV absorbs energy. In the whole breaking process, the opening time when the MS reaches sufficient insulation distance is 2 ms, and the time of oscillation is 0.425 ms. To elaborate, the inherent time required for breaking in the FR-DCCB is approximately 2.45 ms, thereby providing a substantial margin for breaking within 3 ms. Additionally, the upper and lower bridge arm devices are turned OFF when the current approaches zero during oscillation, effectively reducing the demands on the device's current turn-OFF capability by a significant degree. The maximum conduction current amplitude of T_1 and T_2 is 15 kA, and the maximum cumulative conduction time is about 0.25 ms. Thus, there is no need to configure a cooling system. It can be seen that the breaking capacity of the DCCB will not be restricted by the device breaking performance, which is conducive to greatly improving the overall breaking capacity. In addition, the maximum withstand voltage of T_1 and T_2 is 1.8 kV, there is no need to use a large number of devices in series to withstand voltage, which significantly reduces the number of fully controlled devices. After the first breaking process, the voltage of C_1 is 12.3 kV, and the voltage of C_2 is 1.5 kV.

Taking permanent faults as an example, experimental verification is conducted on the reclosing and rebreaking principles. After the first breaking process ends for 200 ms, this is, at $t = 206.3$ ms, the MS is triggered to reclose, and the reclosing process is started. The waveform of reclosing and rebreaking experiment is shown in Fig. 11. During the entire reclosing process, the C_2 is charged by C_1 through the D_1 and D_2 with an oscillation frequency of 10 kHz and a maximum oscillation current amplitude of 17 kA. After 0.3 ms, the voltage of C_2 rises from 1.5 to 1.75 kV, and the remaining voltage of C_1 is decreased to close to zero. Afterward, the system detected the fault again, and at $t = 209.5$ ms, the MS was triggered to separate again, and the fault current was broken according to the same process as the first breaking process. Finally, after nine half waves of oscillation current, the MS crosses zero. The voltage of C_2 is able to return to the initial precharged voltage during the reclosing process, considering the parameter design. However, due to the resistance of wires and power electronic devices in the circuit, as well as a small amount of energy that cannot be fully transferred from C_1 to C_2, there is a slight difference in voltage. Specifically, the voltage of C_2 increases to 1.75 kV, which is slightly lower than the initial precharged voltage of 1.8 kV. This minor discrepancy still enables the DCCB to accomplish the rebreaking process within the same timeframe as the initial breaking process. The reclosing and rebreaking capability of FR-DCCB and the effectiveness of the reclosing principle have been verified by the above experiment. What is more, from the end of the first breaking process to the entire reclosing and rebreaking process, there is no need for external energy supplementation to charge C_2, and the energy of C_2 can be automatically rebounded to close to the first precharged voltage during the reclosing process with the voltage of C_1 dropping to zero.

VII. Conclusion

The bidirectional breaking capability of FR-DCCB has attracted widespread attention as a means of improving the performance and economy of the DCCB. The FR-DCCB uses oscillation to boost the voltage of the capacitor, which forces the oscillation current to increase continuously. This ultimately offsets the fault current, causing the MS to cross zero and extinguish the arc. However, due to the relative novelty of the FR-DCCB and the existence of multiple parameter couplings, its control methods are more complex compared with the traditional DCCB. As a result, methods for fast reclosing, mature control method, and parameter optimization for FR-DCCB are lacking. Thus, this article proposes a high efficient resonance control method based on the real-time feedback correction to address the impact of stray inductance on oscillation efficiency in actual oscillation loops. A fast reclosing control method for FR-DCCB

is then presented, which can supplement C_2 energy by absorbing surge energy and releasing C_1 energy. This eliminates the need for energy supplementation and release when facing permanent fault that require another interruption. Based on these analyses, a complete optimization parameters design method is proposed, which can reduce oscillation branch costs by more than 50% for the same voltage, current, and frequency levels. Ultimately, a 10-kV/15-kA/3-ms prototype of FR-DCCB has been developed and the effectiveness of the proposed methods has been verified.

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