Cascaded Half-Bridge-Based Bidirectional Multilevel Bridgeless PFC With Multioutput Ports

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***Abstract*—Cascaded multilevel power factor correction (PFC) converters show great potential for applications that require high ac voltage input but low dc-bus voltage output, such as telecom power supply, battery formation, and Internet data centers. They are compact and put less voltage stress on power switches. To provide multidc outports with fewer power switches, a cascaded half-bridge-based multilevel multiport bridgeless PFC is proposed in this article. Compared with cascaded full-bridge multilevel PFC, the number of switches per power cell for the proposed PFC is reduced by half while maintaining the same dc outports. Due to the multilevel voltage, the volt–second on the boost inductor decreases, reducing the current ripple of the proposed PFC by $2n$ times with the same boost inductance as the conventional totem-pole PFC. By splitting the power into $2n$ cells with low voltage, the total switching losses are also reduced by $2n$ times with the same equivalent switching frequency. In addition, the proposed rectifier also reduces conduction losses as lower voltage switches with smaller conduction loss are adopted in half-bridge cells compared with conventional totem-pole PFC rectifiers. Finally, these benefits are analyzed and validated with experiments.**

***Index Terms*—AC/DC converter, bidirectional, bridgeless, cascaded half-bridge, multilevel, multiports, power factor correction (PFC).**

I. Introduction

THERE has been increasing demand for higher power density and higher efficiency power factor correction (PFC) rectifiers in applications of telecom power supply, battery formation, and Internet data centers. In this scenario, conventional boost-type PFC with a full-bridge diode can no longer meet such demanding requirements, because of high conduction losses caused by forward voltage drops of the diode bridge [1], [2].

Therefore, bridgeless PFC topologies have garnered wide interest [3], [4], [5]. However, the large volume of the boost inductor of bridgeless PFC remained the dominant challenge for further improving power density. To reduce the size of the boost inductor, bridgeless multilevel PFC rectifiers are proposed [6], [7], [8]. This is because the volt second of the boost inductor decreases significantly with the increase of voltage levels [9], [10].

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Multilevel PFC rectifier topologies can be categorized into neutral point clamped [11], [12], [13], flying capacitor clamped [14], [15], cascaded H-bridges [6], [16], and hybrid [17], [18], [19]. Both neutral point clamped and flying capacitor clamped multilevel rectifiers are widely used for 3-level applications, although the complexity of these PFC rectifiers may increase rapidly when voltage levels are high.

Typically, these clamped multilevel PFCs work with isolated resonant dc/dc converters as a two-stage power supply solution [20], where the PFC stage provides a high dc voltage bus to the following dc/dc converters stage [21]. For a PFC with three phase line input voltage of 380 VAC, for instance, the input dc-bus voltage for dc/dc stage could be as high as 1000 VDC. Then, the dc/dc stage converts the high dc input voltage to a lower dc voltage bus with high current, such as 15 V, 440 A in battery formation applications [22]. This solution may bring two problems to the bidirectional dc/dc stage. First, the power switches voltage stress on the input side of dc/dc stage is high. Higher voltage rating devices usually imply more losses and lower efficiency than low-voltage devices. Second and more importantly, the conversion from high-voltage bus to low-voltage bus requires a high transformer ratio (n_{trans}), which introduces resonant tank design challenges to the dc/dc stage. Taking the bidirectional CLLC dc/dc converter [23], [24] as an example, the required leakage inductance on the secondary side is generally designed as n_{trans}^2 smaller than the primary side leakage inductance [25]. If the transformer ratio is too high, the required secondary inductance would tend to be very low (nanohenry level) [26]. This low-level leakage inductance is challenging to precisely obtain in a transformer, and variation in the inductance may also lead to nonmonotonic bidirectional gain curves [27]. Cascaded full-bridge multilevel PFC [28] could be a solution to this challenge, as the dc-link capacitors in each cascaded full-bridge can serve as an output port to feed the dc/dc converters [29]. Therefore, high dc-bus voltage is shared among multiple dc/dc converters, and the transformer ratio of each dc/dc converter is reduced. Nevertheless, each cascaded full-bridge cell requires four power switches, which increases the costs and losses.

Motivated by these problems, a cascaded half-bridge-based multilevel multiport bridgeless PFC rectifier is proposed in this article, as shown in Fig. 1. It also has dc output ports available to feed multiple converter loads. Compared with cascaded full-bridge multilevel PFC, the number of switches per cell for the proposed topology is significantly reduced by half while maintaining the same output ports. The added two switches K_1

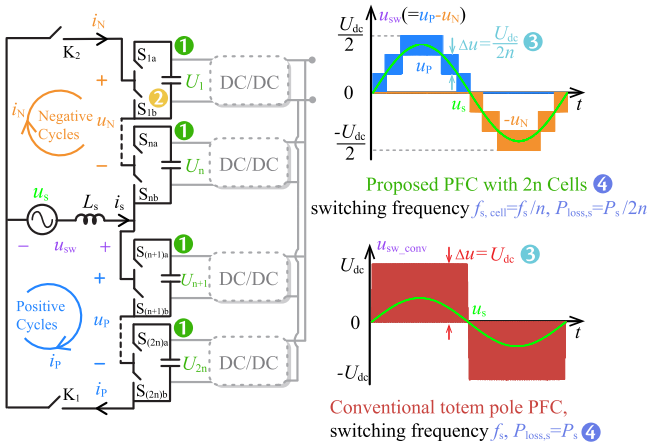


Fig. 1. Proposed half-bridge-based bidirectional multilevel PFC showing the following benefits. ❶ Multi-DC output ports via half bridges (maintaining the same DC out ports with half MOSFETs compared with cascaded full-bridge PFC. ❷ Lower voltage and lower R_{dson} MOSFETs for lower conduction loss. ❸ Volt–second reduction for smaller current ripple with same boost inductance. ❹ Switching loss reduction for the same equivalent f_s.

and K_2 are just working at grid frequency, and they can be simply replaced by two diodes if this proposed topology only works unidirectionally. Thanks to the volt–second reduction on the boost inductor brought by multilevel voltage, the input current ripple drops remarkably with the same boost inductance compared with conventional totem-pole PFC rectifiers. The switching loss can also benefit from the proposed cascaded half-bridge topology. Compared with cascaded full-bridge PFC with n full-bridge cells, the proposed PFC can have $2n$ half-bridge cells. Therefore, the switching voltage for each cell is lower than the cascaded full-bridge PFC, thereby causing lower switching loss. Moreover, the conduction losses can also benefit from the proposed rectifier as the lower voltage switches with smaller R_{ds_on} are adopted in half-bridge cells compared with conventional totem-pole PFC rectifiers.

The rest of this article is organized as follows. In Section II, detailed operation principles of the proposed cascaded half-bridge multilevel PFC are analyzed, and the steady-state model is proposed. In Section III, the proposed PFC is compared with conventional PFC topologies. Then, the parameter mismatch is analyzed and the control strategy is presented for the proposed PFC in Section IV. The effectiveness and performance are verified by experiments in Section V. Finally, Section VI concludes this article.

II. Operation Principles and Steady-State Model of Proposed Cascaded Half-Bridge PFC

In this section, the operation principles of the proposed cascaded half-bridge-based multilevel multiport PFC will be introduced. Then, the steady state model will be presented, which can help with developing the control strategy in Section IV.

A. Operation Mode Analysis

The proposed cascaded half-bridge PFC consists of an upper arm and a lower arm. The upper arm works during the negative grid voltage cycle ($u_s \leqslant 0$). The ac side voltage of upper arm cells is defined as u_N. Similarly, the lower arm works during the positive grid cycle ($u_s > 0$) and its ac side voltage is u_P. Each arm has n identical half-bridge cells in series. For simplicity, the proposed PFC with four cells, two cells in each arm, is adopted here as an example to demonstrate operation modes. There are eight operation modes, as shown in Fig. 2. K_1 and K_2 are complementary switches working at the grid voltage u_s frequency. During the positive grid cycle, K_1 is always ON and K_2 is always OFF and for the negative cycle, K_1 is always OFF and K_2 is always ON. Meanwhile, the switches of half-bridge cells in the upper and lower arms (S_{xa}, and S_{xb}, $x = 1, \ldots, 4$) also operate in a complementary fashion, but with switching frequency f_s. As there is no current charging C_1 and C_2 loads during the positive grid cycles, the load voltage is held up by C_1 and C_2. It is the same for the capacitors C_3 and C_4 to hold the loads in the negative grid cycle. This requirement does not necessarily bring additional cost to the capacitors of the proposed PFC converter, since the dc side capacitance of the PFC is generally designed to hold up half the grid cycle.

There are eight operation modes for the proposed cascaded half-bridge multiport PFC. When $u_s > 0$, the proposed cascaded half-bridge multilevel PFC works in Modes 1–4, and it works in Modes 5–8 when $u_s \leqslant 0$, as shown in Fig. 2.

Mode 1 [see Fig. 2(a)]: Switches S_{3a} and S_{4a} are turned OFF, so capacitors C_3 and C_4 are bypassed from the grid current i_s loop. The inductor current L_s rises, and the energy from the grid voltage u_s is stored in the L_s. The voltage at switching node u_{sw} equals the lower arm voltage, which is 0 V ($u_{sw} = u_P = 0$ V). During this mode, the energy and voltage of the load are provided by capacitors C_1 to C_4.

Mode 2 [see Fig. 2(b)]: Switch S_{3a} is turned ON while S_{4a} is turned OFF. In this mode, the capacitor C_3 is connected to the grid current loop although C_4 is still bypassed. The magnetic field in L_s will be reduced in energy to maintain the current toward C_3 and load R_3. Therefore, the polarity of L_s is reversed to negative on the left side. Consequently, two sources, i.e., u_s and L_s, are in series creating a higher voltage to charge C_3 and load R_3. The voltage at switching node $u_{sw} = u_P = U_{C3} = U_{dc}/4$.

Mode 3 [see Fig. 2(c)]: This mode is similar to Mode 2, but C_3 is bypassed while C_2 is connected to the power loop to be charged by u_s and L_s. The voltage at switching node $u_{sw} = u_P = U_{c4} = U_{dc}/4$.

Mode 4 [see Fig. 2(d)]: Both switches S_{3a} and S_{4a} are turned ON in this mode, so capacitors C_3 and C_4 are connected to the power loop. u_s and L_s are in series creating a higher voltage to charge C_3 and C_4 clockwise. The voltage at switching node u_{sw} is equal to the lower arm voltage u_P, which is the voltages of C_3 and C_4 in series, $u_{sw} = u_P = U_{C3} + U_{c4} = U_{dc}/2$.

Modes 5–8 [shown in Fig. 2(e)–(h)] are the proposed PFC working during the negative half-cycle. These modes resemble the corresponding Modes 1–4 of the positive half-cycle, so

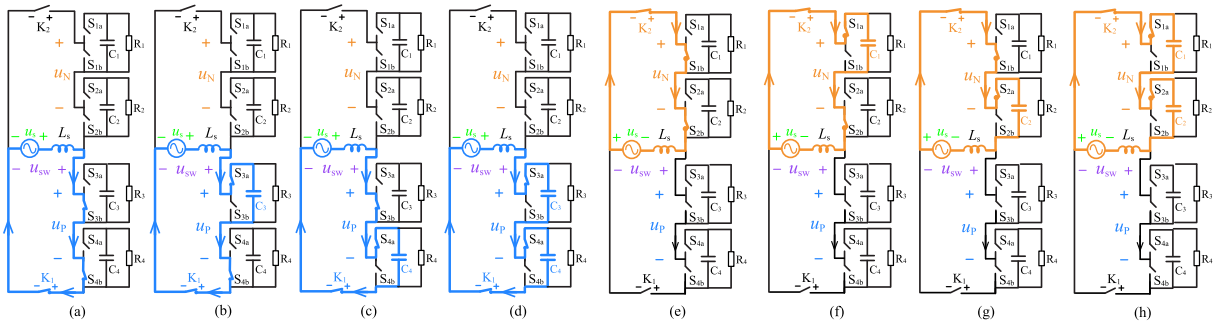


Fig. 2. Operation modes of the proposed PFC. (a)–(d) and (e)–(h) Eight different operation modes during the positive and negative half-cycles of the grid voltage u_s.

TABLE I
OPERATION MODES OF THE PROPOSED PFC

Modes	Grid Volt.	SW. Volt. u_{sw}	Charging Caps
Mode 1	$u_s > 0$	0	N/A
Mode 2 & 3	$u_s > 0$	$U_{dc}/4$	C_3 or C_4
Mode 4	$u_s > 0$	$U_{dc}/2$	C_3 and C_4
Mode 5	$u_s \leqslant 0$	0	N/A
Mode 6 & 7	$u_s \leqslant 0$	$U_{dc}/4$	C_1 or C_2
Mode 8	$u_s \leqslant 0$	$U_{dc}/2$	C_1 and C_2

they are not repeated here. These eight operation modes are summarized in Table I.

Fig. 3 shows how the multilevel switching node voltage $u_{\rm sw}$ changes with the grid voltage u_s. Each half-bridge cell has two switches, S_{xa} and S_{xb}, working in complementary. When S_{xa} turns ON and S_{xb} turns OFF, the cell is defined as the ON state, where the capacitor C_x and load R_x are connected to the power loop to be charged by energy from both the inductor and grid. Similarly, the cell is defined as the OFF state, where the capacitor C_x and R_x are bypassed. Therefore, the load energy and voltage are provided by the capacitor C_x. To simplify demonstration, only driving signals of S_{xa} are shown in Fig. 3. During the positive half-cycle, K_1 is always one while K_2 is OFF. The pulsewidth modulation (PWM) width of S_{3a} and S_{4a} varies sinusoidally. S_{1a} and S_{2a} are always OFF. From t_0 to t_1, the switching node voltage $u_{\rm sw}$ varies between 0 and $U_{\rm dc}/4$ in the positive cycle of grid voltage. According to Table I, the proposed cascaded half-bridge multilevel multiport PFC is working in Modes 1–3. For period t_1 to t_2, the $u_{\rm sw}$ switches between $U_{\rm dc}/4$ and $U_{\rm dc}/2$, thereby resulting in the proposed rectifier working in Modes 2–4. The operation during t_2 to t_3 resembles the period t_0 to t_1. As for the negative grid cycle, the periods $t_3 \sim t_4$, $t_4 \sim t_5$, and $t_5 \sim t_6$ are operating in Mode5–Mode7, Mode6–Mode8, and Mode5–Mode7, respectively.

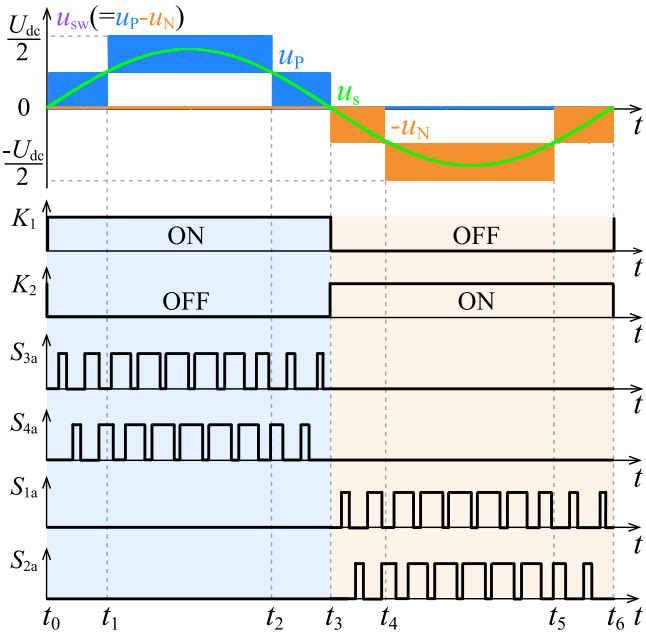


Fig. 3. Operation waveforms diagram of the proposed PFC. It is showing that multilevel switching node voltage $u_{\rm sw}$ changes sinusoidally with the grid voltage u_s. Switches K_1 and K_2 operate alternately with grid frequency. S_{3a} and S_{4a} switch during positive gird cycle, whereas S_{1a} and S_{2a} work during negative gird cycle. The width of gate driving signals of S_{1a}–S_{4a} varies sinusoidally during their working time.

B. Steady-State Model

In this section, the steady-state model will be presented for the proposed cascaded half-bridge multilevel multiport PFC. To ensure generality, there are n half-bridge cells in both lower and upper arm, so $2n$ cells are adopted in total. The steady-state model derived in this section will be used for the parameter mismatch analysis and control strategy derivation in Section IV.

The generalized topology with $2n$ cells is shown in the left of Fig. 1. Its electrical equivalent circuits for positive and negative grid cycles can be obtained, as shown in Fig. 4. The upper and lower arm voltages u_N and u_P are

$$\begin{cases} u_N = \sum_{i=1}^{n} S_i \cdot U_i \\ u_P = \sum_{j=n+1}^{2n} S_j \cdot U_j \end{cases}. \tag{1}$$

The upper and lower arm currents i_N and i_P are

$$\begin{cases} i_N = -\overline{S}_k i_s \\ i_P = S_k i_s \end{cases} \tag{2}$$

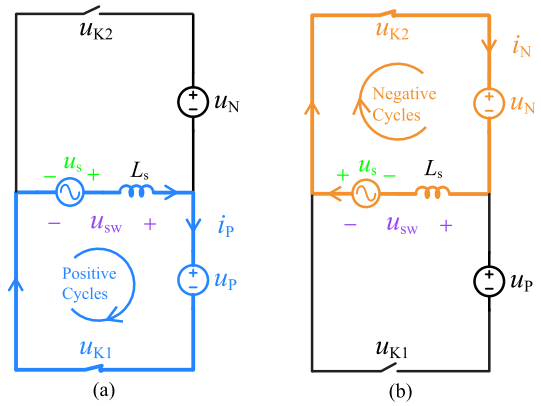


Fig. 4. Equivalent circuits for the proposed PFC in (a) positive u_s cycles and (b) negative u_s cycles.

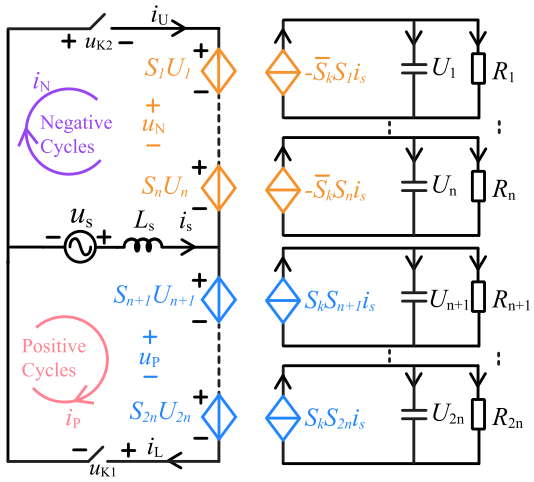


Fig. 5. Steady-state model for the proposed cascaded half-bridge-based multilevel multiport PFC. It can be regarded as two subsystems for the positive and negative grid cycles.

where

$$i = 1 \dots n \tag{3}$$

$$j = (n+1) \dots 2n \tag{4}$$

$$S_i = \begin{cases} 1 \text{ when } S_{ia} = 1,\ S_{ib} = 0 \\ 0 \text{ when } S_{ia} = 0,\ S_{ib} = 1 \end{cases} \tag{5}$$

$$S_j = \begin{cases} 1 \text{ when } S_{ja} = 1,\ S_{jb} = 0 \\ 0 \text{ when } S_{ja} = 0,\ S_{jb} = 1 \end{cases} \tag{6}$$

$$S_K = \begin{cases} 1 \text{ when } K_1 = 1,\ K_2 = 0 \\ 0 \text{ when } K_1 = 0,\ K_2 = 1 \end{cases} \tag{7}$$

$$\overline{S}_K = 1 - S_K. \tag{8}$$

With the KVL and the KCL, voltage and current equations of the equivalent circuit when $u_s > 0$ in Fig. 4(a) can be written as

$$\begin{cases} u_s = L_s \frac{di_s}{dt} + u_P + u_{K1} \\ C_j \frac{dU_j}{dt} = S_j i_P - \frac{U_j}{R_j} \end{cases} \tag{9}$$

where $u_{K1} = 0$ during the positive grid cycle when $S_K = 1$.

Combining (1), (2), and (9)

$$\begin{cases} L_s \frac{di_s}{dt} = u_s - \sum_{j=n+1}^{2n} S_j \cdot U_j - u_{K1} \\ C_j \frac{dU_j}{dt} = S_j S_k i_s - \frac{U_j}{R_j} \end{cases}. \tag{10}$$

Based on (10), the state space equation in the matrix form is

$$\begin{bmatrix} \frac{di_s}{dt} \\ \frac{dU_{n+1}}{dt} \\ \dots \\ \frac{dU_{2n}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{S_{n+1}}{L_s} & \dots & -\frac{S_{2n}}{L_s} \\ \frac{S_{n+1}S_k}{C_{n+1}} & \frac{-1}{C_{n+1}R_{n+1}} & \dots & 0 \\ \dots & \dots & \dots & \dots \\ \frac{S_{2n}S_k}{C_{2n}} & 0 & \dots & \frac{-1}{C_{2n}R_{2n}} \end{bmatrix} \begin{bmatrix} i_s \\ U_{n+1} \\ \dots \\ U_{2n} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_s} \\ 0 \\ \dots \\ 0 \end{bmatrix} u_s + \begin{bmatrix} \frac{u_{K1}}{L_s} \\ 0 \\ \dots \\ 0 \end{bmatrix}. \tag{11}$$

Similarly, during the negative grid cycle, Fig. 4(b) can be modeled as

$$\begin{cases} L_s \frac{di_s}{dt} = u_s + \sum_{i=1}^{n} S_i \cdot U_i + u_{K2} \\ C_i \frac{dU_i}{dt} = -S_i \overline{S}_k i_s - \frac{U_i}{R_i} \end{cases} \tag{12}$$

where $u_{K2} = 0$ during the negative grid cycle when $\overline{S}_K = 1$. Equation (12) can be written in matrix form as

$$\begin{bmatrix} \frac{di_s}{dt} \\ \frac{dU_1}{dt} \\ \dots \\ \frac{dU_n}{dt} \end{bmatrix} = \begin{bmatrix} 0 & \frac{S_1}{L_s} & \dots & \frac{S_n}{L_s} \\ \frac{-S_1\overline{S}_k}{C_1} & \frac{-1}{C_1R_1} & \dots & 0 \\ \dots & \dots & \dots & \dots \\ \frac{-S_n\overline{S}_k}{C_n} & 0 & \dots & \frac{-1}{C_nR_n} \end{bmatrix} \begin{bmatrix} i_s \\ U_1 \\ \dots \\ U_n \end{bmatrix} + \begin{bmatrix} \frac{1}{L_s} \\ 0 \\ \dots \\ 0 \end{bmatrix} u_s + \begin{bmatrix} \frac{u_{K2}}{L_s} \\ 0 \\ \dots \\ 0 \end{bmatrix} \tag{13}$$

according to (11) and (13), the steady-state model can be shown as Fig. 5.

In this section, the operation modes and steady-state model are presented to show how the proposed half-bridge-based PFC works. It can be regarded as two subsystems working for the positive and negative grid cycles, respectively. The switch functions S_i and S_j can be seen as the duty ratio factors. By adjusting the time applying S_i and S_j, the current charging the dc capacitors can be controlled, and then the dc voltage of each cell can be regulated. The analysis presented in this section provides a theoretical basis for the parameter mismatch analysis and control strategy, which will be discussed in Section IV.

III. Comparison With Conventional PFC Topologies

To demonstrate the advantages of the proposed cascaded half-bridge-based multilevel multiport PFC, this section will compare it with cascaded full-bridge PFC and conventional

TABLE II
COMPARISON OF CONVENTIONAL 3-LEVEL TOTEM-POLE PFC, CASCADED FULL-BRIDGES PFC, AND THE PROPOSED PFC

Topologies	Output Ports No.	MOSFETs No.	Volt. Levels	Eff. Sw. Freq.	Sw. Loss	Current Ripple	Power Factor	THD	Voltage Stress
Conventional totem-pole PFC	1	4	3	f_s	$P_{sw,on,tot,conv}$	$\Delta i_{\max,conv}$	Low	High	High
Cascaded full-bridge PFC	n	$4n$	$2n+1$	$n \cdot f_s$	$< \frac{2P_{sw,on,tot,conv}}{n}$	$\frac{\Delta i_{\max,conv}}{n}$	High	Low	Medium
The Proposed PFC	$2n$	$4n+2$	$2n+1$	$n \cdot f_s$	$< \frac{P_{sw,on,tot,conv}}{2n}$	$\frac{\Delta i_{\max,conv}}{2n}$	High	Low	Low

3-level bridgeless totem-pole PFC. In the following comparisons, the same input voltage, boost inductor, and output power will be assumed. For a cascaded full-bridge PFC with n cells, $4n$ MOSFETs are required. For a fair comparison, it is assumed that the proposed PFC topology also uses the same number of $4n$ MOSFETs. Since it is a half-bridge structure, the proposed PFC can have $2n$ half-bridge cells. The three topologies will be compared below in terms of switching loss, conduction loss, and current ripple. Since the equivalent frequency of the conventional totem-pole PFC is lower than the proposed PFC and cascaded full-bridge PFC, the switching loss, conduction loss, and current ripple are compared with the assumption that the conventional totem-pole PFC increases the switching frequency n times to achieve the same equivalent frequency with two cascaded topologies. The comparison results are summarized in Table II.

A. Switching Loss

For these three PFC topologies, the switching ON and OFF for MOSFET loss can be calculated based on the current and voltage overlapping area during the transition. The total turning ON and OFF loss of all MOSFETs can be written in equations as

$$P_{\text{sw,on,tot}} = 1/2 \cdot v_{\text{ds}} \cdot i_{\text{ds}} \cdot t_{\text{on}} \cdot f_s \cdot N_{\text{MOS}} \tag{14}$$

$$P_{\text{sw,off,tot}} = 1/2 \cdot v_{\text{ds}} \cdot i_{\text{ds}} \cdot t_{\text{off}} \cdot f_s \cdot N_{\text{MOS}} \tag{15}$$

where v_{ds} and i_{ds} are the voltage and current of drain to source pins of the MOSFETs, f_s is switching frequency, and N_{mos} means the total MOSFETs of a topology. The time of t_{on} and t_{off} are the overlapping time of current and voltage, which are related to the gate-drain charge (Q_{gd}) during the Miller plateau, gate resistors of turning ON and OFF (R_{on} and R_{off}), gate driving voltage ($V_{\text{gs,on}}$ and $V_{\text{gs,off}}$), and Miller plateau voltage (V_{plat}) as

$$t_{\text{on}} = \frac{Q_{\text{gd}}}{I_{g,\text{on}}} = \frac{R_{\text{on}} \cdot Q_{\text{gd}}}{V_{\text{gs,on}} - V_{\text{plat}}} \tag{16}$$

$$t_{\text{off}} = \frac{Q_{\text{gd}}}{I_{g,\text{off}}} = \frac{R_{\text{off}} \cdot Q_{\text{gd}}}{V_{\text{plat}} - V_{\text{gs,off}}}. \tag{17}$$

Taking turn on loss as an example, it can be seen from (14) and (16) that v_{ds} is the dc-link voltage U_{dc} for the conventional totem-pole PFC. Because the same output power is assumed, the i_{ds} are the same input current i_s for the three topologies. A conventional totem-pole PFC has a total of four MOSFETs, two of which work at the grid frequency with low switching loss. Therefore, only the switching loss caused by the two MOSFETs operating at high frequency is considered here. To achieve the same switching frequency as cascaded topologies, conventional totem-pole PFC must work at $n \cdot f_s$. Total switching loss can be written as

$$P_{\text{sw,on,tot,conv}} = 1/2 \cdot U_{\text{dc}} \cdot i_s \cdot t_{\text{on,conv}} \cdot (n \cdot f_s) \cdot 2. \tag{18}$$

For a cascaded full-bridge PFC with n cells, the dc-link voltage of each cell is U_{dc}/n. The current of each cell is equal to the grid current i_s. Assuming bipolar modulation is adopted, the total switching loss of $4n$ MOSFETs can be expressed as (19). Compared with the conventional totem-pole PFC, the cascaded full-bridge can use low-voltage MOSFETs with lower gate-drain charge Q_{gd}, so overlapping time $t_{\text{on,cascfull}} < t_{\text{on,conv}}$. Since Q_{gd} varies with MOSFETs, quantitative comparison can be calculated by referring to MOSFET datasheets with (16) and (17). The qualitative comparison with conventional totem-pole PFC is provided as

$$\begin{aligned} P_{\text{sw,on,tot,cascfull}} &= \frac{1}{2} \cdot \frac{U_{\text{dc}}}{n} \cdot i_s \cdot t_{\text{on,cascfull}} \cdot f_s \cdot 4n \\ &< \frac{2P_{\text{sw,on,tot,conv}}}{n}. \end{aligned} \tag{19}$$

For the proposed PFC, there are n cascaded half-bridge cells on the upper arm, and another n cells in the lower arms. They work in the negative and positive half-cycles of the grid, respectively. Therefore, there are n half-bridges causing switching losses at any time, which are a total of $2n$ MOSFETs. Since there are $2n$ cells in total, the switching voltage of each cell is $U_{\text{dc}}/2n$, total switching loss is presented as

$$\begin{aligned} P_{\text{sw,on,tot,prop}} &= \frac{1}{2} \cdot \frac{U_{\text{dc}}}{2n} \cdot i_s \cdot t_{\text{on,prop}} \cdot f_s \cdot 2n \\ &< \frac{P_{\text{sw,on,tot,conv}}}{2n}. \end{aligned} \tag{20}$$

Upon analyzing (18)–(20), it becomes clear that the cascaded half-bridge PFC design results in reduced switching losses relative to both the cascaded full-bridge PFC and conventional totem-pole PFC topologies. As a result, the proposed PFC topology provides an efficiency advantage in the context of switching loss.

B. Conduction Loss

The conduction loss can be derived from the rms current and conduction resistance of MOSFETs as

$$P_{\text{condc}} = I_{\text{RMS}}^2 R_{\text{ds,on}} N_{\text{on,MOS}}. \tag{21}$$

For the proposed PFC design employing $2n$ cells, the count of conducted MOSFETs in the switching power loop, denoted as $N_{\text{on,MOS}}$, is $(n+1)$. In contrast, the cascaded full-bridge topology with n cells includes $2n$ MOSFETs within the conduction power loop. As such, the conduction loss for the cascaded full-bridge intensifies significantly with the growth of module quantity n. When the number of modules n is sufficiently large, cascaded full-bridges experience nearly twice the conduction losses compared with the proposed PFC topology with half-bridges. However, it is crucial to note that an increase in conduction loss with the module number n in these cascaded full- or half-bridge topologies does not necessarily imply that they are consistently inferior to the conventional totem-pole PFC in terms of conduction loss. This is attributable to the fact that cascaded topologies employ lower voltage MOSFETs characterized by lower $R_{\text{ds,on}}$. In conclusion, a comprehensive assessment of conduction loss demands careful consideration of all the parameters in (21).

C. Current Ripple and Required Inductance

One of the challenges to further improving the power density of PFC is still the large volume of inductors. In this section, the current ripple and requirements of inductance will be compared among the three topologies. Assuming the three topologies being compared use the same inductance, the relation between maximum peak-to-peak boost inductor current ripple $\Delta i_{\max}$ and inductance L can be given with equations for conventional totem-pole PFC, cascaded full-bridge PFC, and the proposed cascaded half-bridge PFC topologies as

$$\Delta i_{\max,\text{conv}} = \frac{U_{\text{dc}}}{4 \cdot (n \cdot f_s) L} \tag{22}$$

$$\Delta i_{\max,\text{cascfull}} = \frac{U_{\text{dc}}}{4n^2 f_s L} = \frac{\Delta i_{\max,\text{conv}}}{n} \tag{23}$$

$$\Delta i_{\max,\text{prop}} = \frac{U_{\text{dc}}}{8n^2 f_s L} = \frac{\Delta i_{\max,\text{conv}}}{2n}. \tag{24}$$

It can be found from (22)–(24) that the inductor current ripple is caused by the volt–seconds applied to it. For consistency of comparison, the switching frequency of conventional totem-pole PFC is still assumed to be equal to $n \cdot f_s$ to match cascaded topologies, although this will dramatically increase the switching loss of conventional totem-pole PFC as discussed previously. However, the current ripple is still $2n$ times higher than the proposed cascaded half-bridge PFC. As for the cascaded full-bridge PFC, the current ripple is two times higher than the proposed PFC. This is because the proposed PFC has lower voltage stress on the cell MOSFETs: the U_{dc} is divided by $2n$ cells, rather than n. The benefit of the proposed PFC is brought not only by the higher equivalent switching frequency but also by the reduction of volt–seconds on the inductor. Furthermore, considering that the current stress on MOSFETs is typically induced by the input current superimposed on the current ripple, the proposed PFC topology's characteristic of lower current ripple can also contribute toward alleviating the current stress exerted on the switching devices.

D. Power Factor and Total Harmonic Distortion (THD)

The power factor of a PFC converter is influenced by various factors, including converter topology, control strategy, load characteristics, switching frequency, and passive components. To achieve a high power factor, optimization of these factors is required. Although a well-designed conventional totem-pole PFC, cascaded full-bridges PFC, and the proposed PFC converter can all attain a power factor exceeding 0.95, the conventional totem-pole PFC experiences greater dv/dt on the boost inductor. Therefore, under conditions of equivalent boost inductance, the conventional totem-pole PFC presents a lower power factor and increased (THD) in the input current.

E. Voltage Stress of Cells

The voltage stress is contingent upon the number of cells sharing the dc-bus voltage. For the conventional totem- pole PFC, the MOSFETs function under the entirety of the dc-bus voltage, leading to high voltage stress. In contrast, the cascaded full-bridge PFC, with a total of $4n$ MOSFETs, distributes the dc-bus voltage across n cells, whereas the proposed cascaded half-bridge PFC manages to distribute it over $2n$ cells. Consequently, the proposed PFC exhibits the lowest voltage stress per cell, thus establishing its superiority in managing voltage stress.

To sum up, compared with conventional totem-pole PFC and cascaded full-bridge PFC, the proposed cascaded half-bridge PFC has advantages in switching losses, conduction losses, current ripple, and voltage and current stresses while providing more output ports. In the next section, the parameter mismatch will be analyzed, and the control strategy will be presented for the proposed cascaded half-bridge PFC.

IV. Control Strategy for the Proposed Cascaded Half-Bridge PFC

As a PFC with multidc out ports, the control target of stable operation is to distribute dc-link voltage among cells. Moreover, circulating current caused by cell parameter mismatch from rated values may also be a challenge for the multioutport converters. Therefore, in this section, the impact of parameter mismatch on the circulating current for the proposed PFC will be analyzed first, and then a control and modulation strategy will be presented.

A. Analysis of Parameter Mismatch

Due to manufacturing tolerances and the aging process, the capacitance of dc-link electrolytic capacitors varies from designed values. This parameter mismatch may lead to extra conduction loss due to circulating current among cells.

The proposed cascaded half-bridge multiport PFC working with input series output parallel (ISOP) dc/dc converter is

adopted as an example here. As shown in Fig. 6(a), the multiports of the proposed PFC are fed to multiple isolated dc/dc converters. In this ISOP system, it is vital that the total dc-link voltage is equitably distributed across each individual cell. Concurrently, the output current must also be uniformly allocated among the dc/dc converters. This distribution ensures that the device rating for each cell can remain identical. Furthermore, it also enables the active power to remain balanced between positive and negative half-grid cycles, thereby ensuring low input current THD for the proposed PFC topology.

However, there are three factors that may cause circulating current. The dc-link capacitors of the proposed PFC, the transformer ratio in the dc/dc stage, and the output filter (L_x and C_o) in the dc/dc stage. The analysis below will focus on the parameter mismatch of the dc-link capacitors of proposed PFC ($C_1 \sim C_{2n}$) while assuming that the transformer ratio and output LC filter of the dc/dc stage are the same ($Z_L = Z_{L1} = \cdots Z_{L2n}$). Therefore, the ac equivalent circuit of the proposed PFC in the ISOP application can be obtained in Fig. 6(b). Since the output voltage of the dc/dc stage will be regulated as constant, the output capacitor C_o can be ignored in Fig. 6(b) during the circulating current analysis. As discussed in Section II, the proposed cascaded half-bridge PFC can be modeled as current sources, as shown in Fig. 5. In the analysis below, we could assume that the ac components of the rectification current after half-bridge for the positive cycle cells are equal, which could be defined as $i_{\text{rec,ac},P}$. Similarly, $i_{\text{rec,ac},N}$ indicates ac components of the rectification current for the negative cycles cells, as shown in Fig. 6(b).

To simplify the analysis of circulating current, only the first cell's dc-link capacitance (Z_{C1}) is assumed to be different from other $(2n-1)$ cells ($Z_{C1} \neq Z_C = Z_{C2} = \cdots = Z_{C2n}$). By using the Norton Theorem for Cell(2) $\sim$ Cell($2n$) in Fig. 6(b), the simplified ac equivalent circuit for the negative grid cycle can be obtained, as shown in Fig. 6(c), the dc-link capacitors in half-bridge Cell(2) $\sim$ Cell($2n$) can be simplified as $Z_{C_{\text{Norton}}}$; the output inductor filters are combined as $Z_{L_{\text{Norton}}}$. Equations for $Z_{C_{\text{Norton}}}$ and $Z_{L_{\text{Norton}}}$ are

$$\begin{cases} Z_{C\,\text{Norton}} = \frac{Z_C}{2n-1} \\ Z_{L\,\text{Norton}} = \frac{Z_L}{2n-1} \end{cases} \tag{25}$$

where $Z_C = 1/(j2\omega_g C)$, $Z_L = j2\omega_g L$, and ω_g is the angular frequency of the grid.

During the negative grid cycle, the Norton equivalent circuit obtained from Fig. 6(b) can be shown in Fig. 6(c). As for $i_{\text{Norton},N}$ in Fig. 6(c), it could be determined with negative grid cycles, when the $i_{\text{rec,ac},P}$ is regarded as 0. Therefore, the $i_{\text{Norton},N}$ can be obtained by taking current sources for Cell(2) $\sim$ Cell(n) into consideration

$$i_{\text{Norton},N} = \frac{Z_C \cdot (n-1)}{Z_L + Z_C} \cdot i_{\text{rec,ac},N}. \tag{26}$$

Similarly, the Norton theorem's equivalent current during the positive grid cycle $i_{\text{Norton},P}$ can be derived by taking current

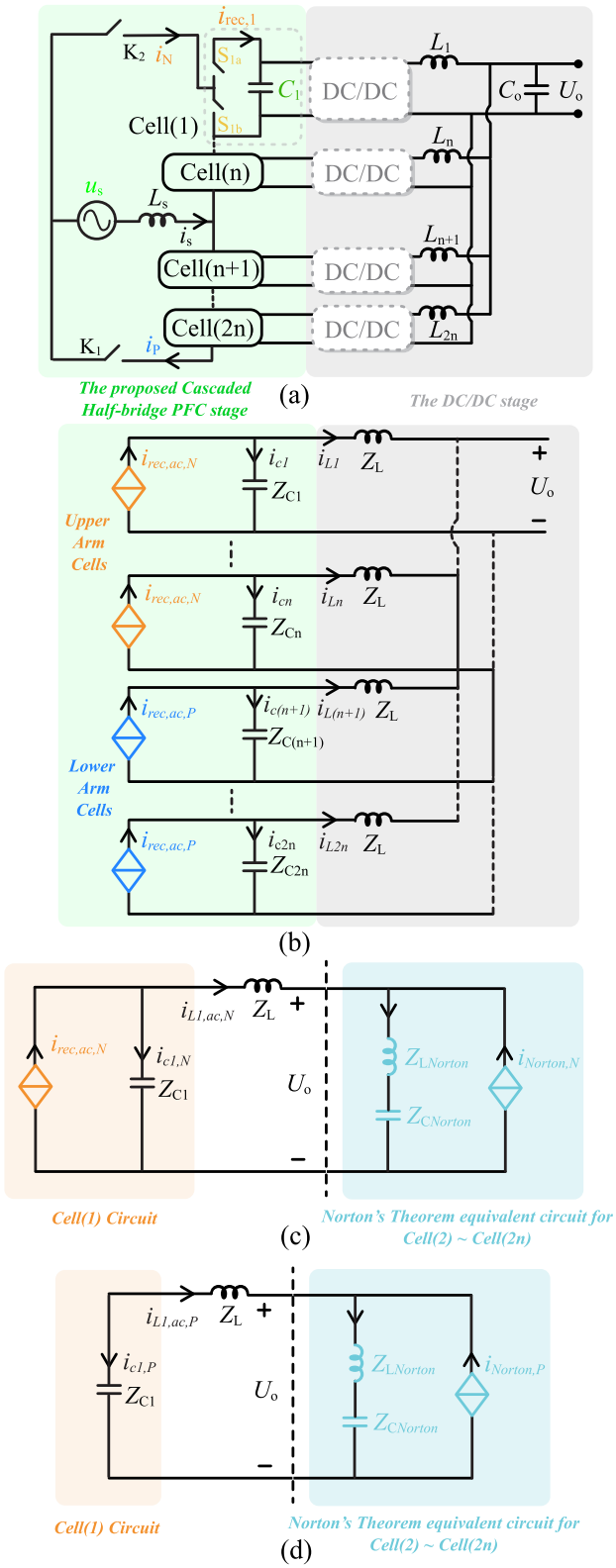


Fig. 6. Circulating current analysis of the proposed cascaded half-bridge-based multilevel multiport PFC. (a) Proposed PFC with $2n$ cells in ISOP application. (b) AC equivalent circuit of the proposed PFC in an ISOP application, where the cascaded half-bridges in proposed PFC can be modeled as controlled current sources. (c) Assuming only DC-link capacitor of the first cell (Z_{C1}) has parameter mismatch from other $(2n-1)$ cells (Z_C). By using Norton Theorem, the simplified equivalent circuit for the negative grid cycle can be obtained. (d) Norton equivalent circuit for the positive grid cycle.

sources for Cell$(n+1) \sim$ Cell$(2n)$ into consideration as

$$i_{\text{Norton},P} = \frac{Z_C \cdot n}{Z_L + Z_C} \cdot i_{\text{rec,ac},P}. \tag{27}$$

In (26) and (27), the $i_{\text{rec,ac},N}$ and $i_{\text{rec,ac},P}$ can be calculated based on the total power P_{tot}, and the total dc-link voltage U_{dc} of all the $2n$ cells as

$$i_{\text{rec,ac},N} = i_{\text{rec,ac},P} = \frac{P_{\text{tot}}}{U_{\text{dc}}}. \tag{28}$$

Therefore, with (26) and (27), Norton theorem's equivalent current can be written as

$$i_{\text{Norton}} = \begin{cases} i_{\text{Norton},N}, & u_s < 0 \\ i_{\text{Norton,P}}, & u_s \geq 0 \end{cases}. \tag{29}$$

By using the superposition law for two current sources ($i_{\text{rec,ac},N}$ and $i_{\text{Norton},N}$), as shown in Fig. 6(c), the capacitor current during the negative grid cycle $i_{C1,N}$ is obtained as

$$i_{C1,N} = i_{\text{Norton},N} \frac{Z_{C,\text{Norton}} + Z_{L,\text{Norton}}}{Z_{\text{tot}}} + i_{\text{rec,ac},N} \frac{Z_L + Z_{C,\text{Norton}} + Z_{L,\text{Norton}}}{Z_{\text{tot}}} \tag{30}$$

where $Z_{\text{tot}} = Z_L + Z_{C,\text{Norton}} + Z_{L,\text{Norton}} + Z_{C1}$.

For the positive grid cycle, the current $i_{\text{rec,ac},N}$ for Cell$(1) \sim$ Cell(n) is 0, so the Norton equivalent circuit considering $i_{\text{rec,ac},P}$ is obtained, as shown in Fig. 6(d). The capacitor current during the positive grid cycle $i_{C1,P}$ is

$$i_{C1,P} = i_{\text{Norton},P} \frac{Z_{C,\text{Norton}} + Z_{L,\text{Norton}}}{Z_{\text{tot}}}. \tag{31}$$

By combining (28)–(31), the circulating current amplitude going through the module 1 output filter inductors of the dc–dc stage (connected after the proposed PFC) during the negative grid cycle $i_{L1,\text{ac},N}$ and positive grid cycle $i_{L1,\text{ac},P}$ are

$$\hat{i}_{L1,\text{ac},N} = |i_{\text{rec,ac},N} - i_{C1,N}| = \frac{P_{\text{tot}}}{U_{\text{dc}}} \left| \frac{Z_{C1}(2n-1) - Z_C(n-1)}{Z_{C1}(2n-1) + 2n \cdot Z_L + Z_C} \right| \tag{32}$$

$$\hat{i}_{L1,\text{ac},P} = |-i_{C1,P}| = \frac{P_{\text{tot}}}{U_{\text{dc}}} \left| \frac{Z_C \cdot n}{Z_{C1}(2n-1) + 2n \cdot Z_L + Z_C} \right|. \tag{33}$$

As for the Cell$(2) \sim$ Cell$(2n)$ that are without parameter mismatch, their circulating current during negative and positive grid cycles can be given as

$$\hat{i}_{L2,\text{ac},N} = \cdots = \hat{i}_{L2\text{n},\text{ac},N} = \frac{\hat{i}_{L1,\text{ac},N}}{2n-1} \tag{34}$$

$$\hat{i}_{L2,\text{ac},P} = \cdots = \hat{i}_{L2\text{n},\text{ac},P} = \frac{\hat{i}_{L1,\text{ac},P}}{2n-1}. \tag{35}$$

It can be found from (32) and (33) that if the dc side capacitance for Cell(1) Z_{C1} is equal to the rest $(2n-1)$ cells capacitance Z_C, the circulating current amplitude during the negative cycle in (32) will be equal to the positive grid cycle circulating current in (33). The circulating current difference becomes larger as the difference between Z_c and Z_{C1} increases. Although the circulating current will not cause the runaway situation for the proposed cascaded half-bridge PFC, its increase could lead to a higher rms current for the MOSFETs and magnetic components, and might thereby cause extra losses.

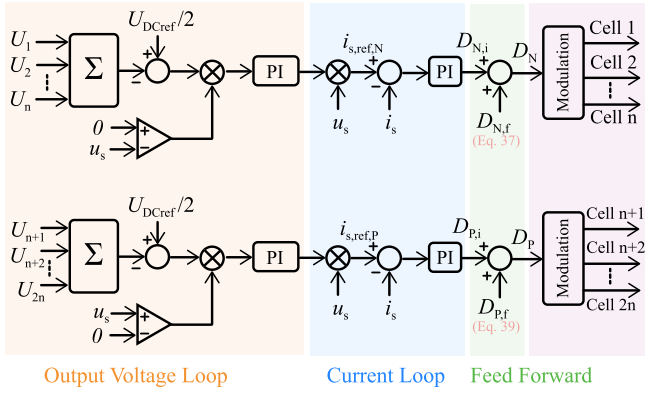


Fig. 7. Control diagram of the proposed cascaded half-bridge-based multilevel multiport PFC, which consists of four parts: output voltage loop, current loop, feed forward, and modulation. The DC-link voltages for upper and lower cells are controlled separately.

B. Control and Modulation Strategy for the Proposed Cascaded Half-Bridge PFC

The control and modulation strategy of the proposed cascaded half-bridge-based PFC will be presented in this section. Since the upper and lower arm cells are connected in series, the currents going through them are the same. Therefore, only the dc-link voltages of cells need to be controlled. The output current sharing is usually realized by dc/dc converters connecting to the proposed PFC converter. To maintain balanced capacitor voltage and equal voltage stress on all power switches, the common modulation index and the common duty cycle are applied to all power cells of the proposed PFC. This operation scheme is based on the natural balancing behavior inherent in multicell converter systems. There are also phase shift degrees applied to both upper and lower cells in the modulation strategy.

The control diagram for the proposed PFC is shown in Fig. 7. The dc-link voltage for the upper arm cells ($U_1, \ldots, U_n$) and lower arm cells ($U_{n+1}, \ldots, U_{2n}$) are controlled separately. There are voltage and current control loops and a feedforward in the controller. Taking the control during the negative grid cycle as an example, for the output voltage loop, the voltages of the upper arm cells ($U_1, \ldots, U_n$) are sampled by ADC and added up in DSP. The result of their summation is then subtracted from half of the dc-link voltage reference to obtain the voltage errors. To ensure that the proportional integral (PI) controller of the upper arm cells only accumulates voltage errors in the negative grid cycle, voltage errors are multiplied by the comparison of 0 V and the grid voltage. Afterward, the PI controller output is multiplied by the normalized grid voltage u_s to get the current loop reference $i_{s,\text{ref},N}$ in the negative half-cycle. Then, the duty ratio signal from current loop $D_{N,i}$ can be obtained by sending the difference between reference $i_{s,\text{ref},N}$ and the grid current i_s into the current inner loop PI controller. In this way, the current

follows a sinusoidal waveform with the grid voltage, thereby increasing the power factor.

To cope with the challenge of peak current at ac zero crossing and improve the transient response capability, duty cycle feedforward $D_{N,f}$ is added to the current (inner) control loop. Based on the volt–second balance principle and (12), volt–seconds applied to inductor L_s are the same when the cells are charged ($S_i = 1$) and bypassed ($S_i = 0$). During the positive grid cycle, the voltage on switch K_1 (u_{K1}) is 0, so the feed forward formula for common duty ratio $D_{N,f}$ with the help of (12) for cells on the upper arm can be written as

$$u_{\rm s} \cdot D_{N,f} = \left(\sum_{i=1}^{n} U_i - u_{\rm s}\right) \cdot (1 - D_{N,f}). \tag{36}$$

By solving (36), the feed forward formula during the negative cycle for common duty ratio $D_{N,f}$ is

$$D_{N,f} = 1 - \frac{u_{\rm s}}{\sum_{i=1}^{n} U_i} = 1 - \frac{2 \cdot u_{\rm s}}{U_{\rm dc}}. \tag{37}$$

The common duty ratio D_N for all the upper cells can be obtained by adding up the duty ratio from current loop output $D_{N,i}$ and feedforward $D_{N,f}$ as

$$D_N = D_{N,i} + D_{N,f}. \tag{38}$$

As for the positive grid cycle, the control strategy is similar except for the comparison of the grid voltage and 0 V. Moreover, with (10), the feed forward duty ratio equation for the positive grid cycles $D_{P,f}$ can be obtained for cells on the lower arm as

$$D_{P,f} = 1 - \frac{u_{\rm s}}{\sum_{j=n+1}^{2n} U_j} = 1 - \frac{2 \cdot u_{\rm s}}{U_{\rm dc}}. \tag{39}$$

The common duty ratio for lower arm cells

$$D_P = D_{P,i} + D_{P,f}. \tag{40}$$

D_N and D_P represent the required duty cycle for the upper and lower arms of the proposed PFC, which are sent to the modulation module. For the proposed PFC with $2n$ cells (n for the upper arm and n for the lower arm), the phase shift among cells on the upper arm is $360/n$ degrees. The same phase shift degrees are applied to lower arm n cells. In the positive half-cycle, Cell$(n+1)$ to Cell$(2n)$ are driven by PWMs modulated from common duty ratio D_P, whereas the upper arm Cell(1) to Cell(n) are in the bypass state (all Cells are set as $S_i = 0$) to reduce the voltage of switches K_2. Similarly, in the negative half-cycle of the grid, the lower Cell$(n+1)$ to Cell$(2n)$ are in the bypassed mode ($S_j = 0$) and the upper arm Cell(1) to Cell(n) are driven by PWMs modulated by duty ratio D_N to generate multilevel voltage.

The proposed PFC topology can operate properly with an odd number of output ports. Some control and design considerations must be given to ensure consistent operation during positive and negative grid cycles ($u_s > 0$ and $u_s < 0$). The power must be controlled equally during positive and negative cycles ($P_P = P_N$) to avoid high THD due to an unbalanced input current. Also, the total voltage of negative cycle cells should be the same as that of positive cycle cells, allowing both cycles to have the same modulation index. Finally, the phase shift of power cells needs to be adjusted based on cell number in positive and negative cycles.

In this section, the circulating current caused by the dc-link capacitor mismatch is analyzed in detail. Then, the control and modulation strategies are discussed for the proposed PFC converter. In the next section, the design method for the proposed PFC will be presented and the prototype with the designed parameters will be verified by experiments.

V. Design and Experimental Verifications

In this section, the proposed cascaded half-bridge-based multilevel multiport PFC will be designed, and a prototype will be built based on this design. Then, the proposed PFC will be verified by experiments with the prototype.

A. Design of Proposed PFC

1) DC-Link Capacitors: There are n half-bridge cells in series in the upper arm for the proposed PFC. The same number of n cells are in the lower arm as well. Although the grid current cannot charge the upper and lower half-bridge arm cells at the same time, this does not mean that the proposed PFC requires larger dc-link capacitance compared with conventional PFC. This is because the dc-link capacitors of the PFC are usually designed according to the hold-up time. This requires the PFC to be able to supply the same amount of power to load for the half-grid period after the grid outage. Designing the dc-link capacitor according to the hold-up time rule can just hold the cell voltage up for the proposed PFC when there is no corresponding charging current.

Considering hold-up time $t_{\rm hold}$ as 8.3 ms, and the maximum allowable drop of the dc-link voltage rate δ as 20%; for a $2n$ cells prototype with a total output power P_o of 500 W, the required dc-link capacitance of each cell can be calculated as

$$C_{\rm cell.dc} \geq \frac{2 \cdot P_o/(2n) \cdot t_{\rm hold}}{(U_{\rm dc}/(2n))^2 - (U_{\rm dc} \cdot (1-\delta)/(2n))^2}. \tag{41}$$

After calculation, 3465μF capacitance is required. Therefore, two 2200μF electrolytic capacitors are chosen in parallel for each half-bridge cell of the proposed PFC.

2) Boost Inductor L_s: The boost inductor is one of the most important components in a PFC, as it can determine the operating mode of the PFC. The smaller current ripple allows the PFC to operate in continuous conduction mode, but this means that the boost inductor must have a high inductance value. However, the higher the inductance value, the larger the size of the inductor. To optimize the overall performance of the proposed PFC, so that it can achieve an efficient balance between low-power operation and maximum power operation, the inductance value can be calculated as

$$L_s = \frac{U_{\rm dc}}{8n^2 f_s \Delta i_{\rm max,prop}}. \tag{42}$$

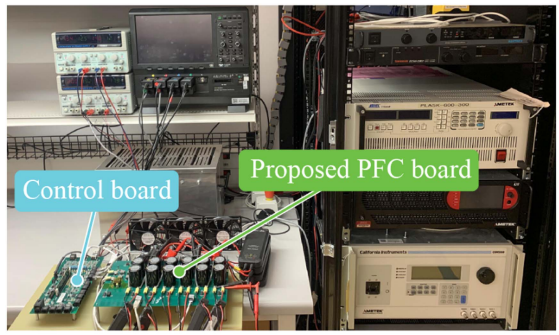
With (42), the required boost inductance can be calculated as 13μH. In the experimental prototype, four 3.3μH(19.6 A) inductors are in series for a total of 13.2μH inductance.

TABLE III
PARAMETERS OF THE PROPOSED PFC PROTOTYPE

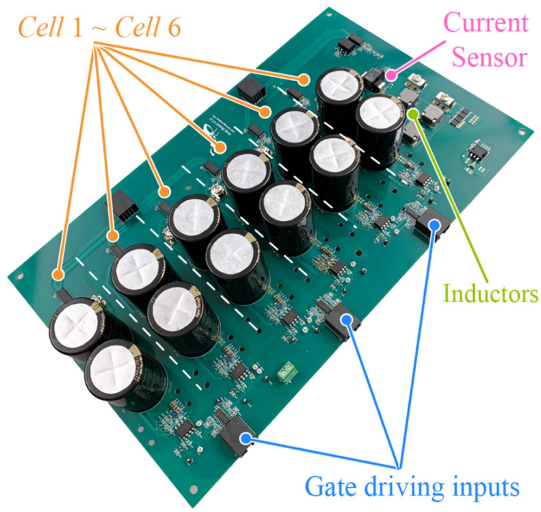
System parameters		
Parameters	Symbols	Values
Nominal Output Power	P_o	$500\ W$
DC Link Voltage	U_{dc}	$200\ V$
Number of Cells	$2n$	6
Cell Switching Frequency	f_s	$100\ kHz$
Hold-up Time	t_{hold}	$8.3\ ms, 20\%\ volt.\ drop$
Component Models		
MOSFETs	$6\times$EPC2152, $80\ V$, $8.5\ m\Omega$	
Diodes	$2\times$OnSemi, FES10G, $600\ V$, $V_F = 1.2\ V$	
Boost Inductors	$4\times$ETQ-P8M3R3JFA, $3.3\ \mu H$, $19.6\ A$	
Caps of Each Cell	$2\times$LKG2A222MESCCK, $2200\ \mu F$, $100\ V$	
Current Sensor	LEM, HLSR 32-P/SP33, $32\ A$	
Differential Driver	TI, AM26LV31EIDR, $3.3\ V$	
Differential Receiver	TI, AM26C32ID, $5\ V$	
Isolation Op Amp	Broadcom, ACNT-H790-000E, $5\ V/5\ V$	
Logic Optoisolator	Broadcom, HCPL-2430-500E, $5\ V/5\ V$	
DSP Controller	TI, TMS320F28335, $150\ MHz$	

3) MOSFETs and Diodes: There is a total of six half-bridge cells in the prototype. Therefore, the voltage stress on each GaN MOSFET is only $U_{\rm dc}/6$. Hence, the EPC2152 is chosen as the MOSFETs for all the half-bridge cells in the proposed PFC. It integrates the input logic interface, level shifting, bootstrap charging, and gate drive buffer circuits along with GaN output FETs configured as a half-bridge. There are several advantages of integrated GaN MOSFET IC. The integration of GaN MOSFETs with on-chip gate drivers could minimize the common source inductance and gate drive loop inductance. The power loop inductance is also reduced by the land grid array (LGA) pinouts, thereby facilitating the optimal layout. As for the power switches of K_1 and K_2, two diodes are adopted for them to switch at grid frequency. The model is FES10 G.

All the system parameters and component models used in the prototype are summarized in Table III. The picture of the assembled prototype is shown in Fig. 8.



(a)



(b)

Fig. 8. Prototype of the proposed cascaded half-bridge-based multilevel multiport PFC with six cells according to Table III. (a) Experimental setup consists of the proposed PFC board, control board, loads, and AC power source. (b) Close-up view of the proposed PFC board. The size of the boost inductor has been significantly reduced by the application of multilevel voltage.

B. Experimental Results

The measured experimental results are presented in this section. As shown in Fig. 9(a), boost inductor current i_{Ls} and switching node multilevel voltage $u_{\rm sw}$ are following the sinusoidal grid voltage u_s properly. The zoomed in waveforms are shown in Fig. 9(b). The maximum current ripple observed on the boost inductor was measured to be 2.1 A at 0.5 duty ratio. This represents a relatively low level of current ripple, particularly given the fact that only a 13.2μH inductance was utilized in this prototype. This is realized thanks to the reduced volt–second applied to the boost inductor from multilevel voltage $u_{\rm sw}$. First, the voltage change step of $u_{\rm sw}$ drops to $U_{\rm dc}/2n$ (33 V). This means a decrease of $2n$ times compared with conventional totem-pole PFC. Moreover, the equivalent frequency of i_{Ls} is n times higher than the switching frequency. Taking upper arm cells in the negative grid cycle as an example, the gate driving signals for low-side MOSFETs [S_{1b}, S_{2b}, and S_{3b}, shown in Fig. 9(b)] are 100 kHz, and are 120° phase shifted with each other, whereas the equivalent frequency on $u_{\rm sw}$ and i_{Ls} is 300 kHz. Therefore, the current ripple of the proposed multilevel PFC is low.

Figs. 9 and 10 present experimental comparison results of the current ripple in a conventional totem-pole PFC and the proposed PFC. For a fair comparison, the experimental results of the totem-pole PFC are presented with the same inductance as the proposed PFC. To match the equivalent switching frequency of the proposed PFC, the switching frequency for the totem-pole PFC is increased to 300 kHz instead of the cell switching frequency (100 kHz). Fig. 10(a) shows the measured results of the totem-pole PFC input voltage u_s, switching node voltage $u_{\rm sw}$, and boost inductor current i_{Ls}. Fig. 10(b) shows a zoomed in view of the totem-pole converter current ripple. It can be observed that the current has maximum ripple (12.7 A) when the input voltage (u_s) reaches its peak. Despite the switching frequency being increased to match that of the proposed PFC, the current ripple is still approximately six times higher than the ripple of the proposed PFC [2.1 A, as shown in Fig. 9(b)].

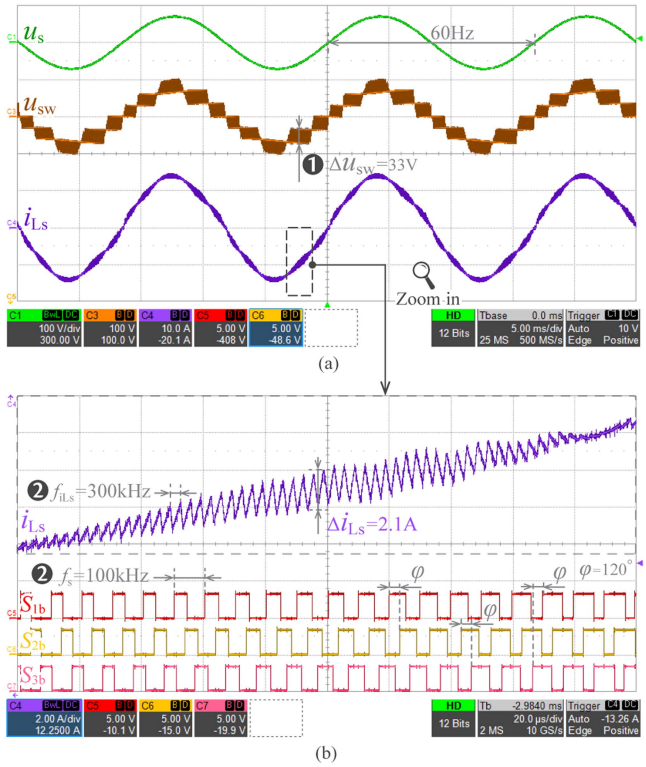


Fig. 9. Experimental captures of the proposed PFC. (a) Boost inductor current i_{Ls} and switching node multilevel voltage u_{sw} are following the sinusoidal grid voltage u_s. (b) Zoomed in view of i_{Ls} showing low current ripple (300 kHz, 2.1 A) at 0.5 duty ratio. This is because the reduced volt–second is applied to the boost inductor from u_{sw}. Due to the multi cell feature of the proposed PFC topology: ❶ u_{sw} voltage step is reduced to $U_{dc}/2n$ (33 V); ❷ i_{Ls} ripple frequency (300 kHz) is n times faster than cell gate driving signals (S_{1b}, S_{2b}, and S_{3b}, 100 kHz, 120° phase shifted).

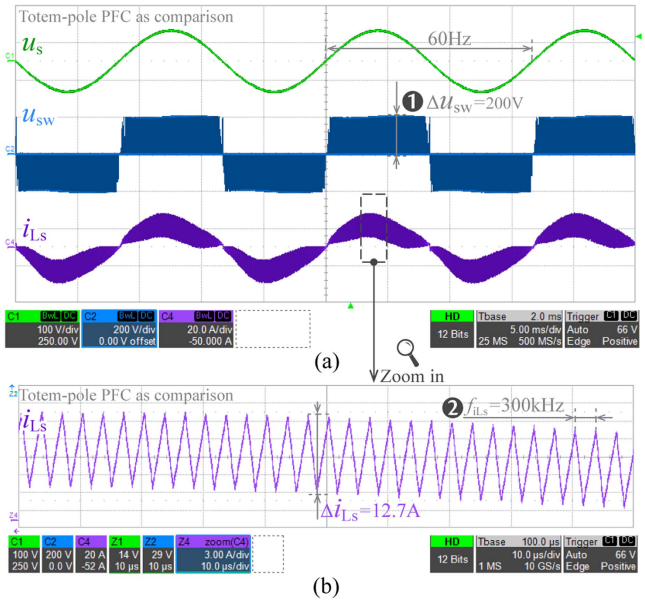


Fig. 10. Experimental results of the conventional totem-pole PFC with the same inductance as the proposed PFC. (a) Measured results of the converter input voltage u_s, switching node voltage u_{sw}, and the boost inductor current i_{Ls}. (b) Zoomed in view of the totem-pole converter current ripple. The current has maximum ripple when u_s reaches its peak. Although the switching frequency is increased to the same as the proposed PFC equivalent switching frequency (300 kHz)❷, the maximum current ripple is still as high as 12.7 A, which is around six times higher than the ripple of the proposed PFC shown in Fig. 9(b). This is a consequence of the six times higher Δu_{sw} for the totem-pole PFC ❶.

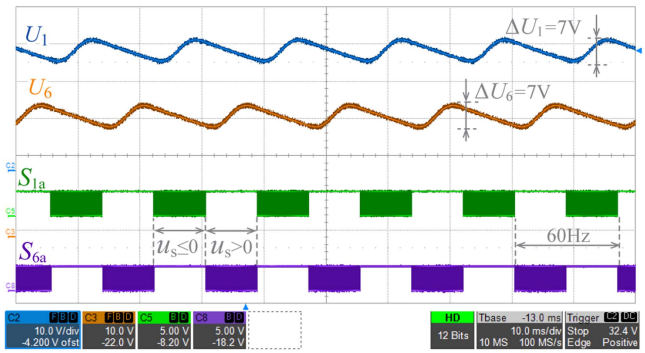


Fig. 11. Experimental capture showing the output DC voltage ripple of Cell(1) and Cell(6) in the positive ($u_s > 0$) and negative grid ($u_s \leq 0$) cycles. Gate driving signals are showing upper arm cells (Cell(1) to Cell(3)) and lower arm cells (Cell(4) to Cell(6)) are charged by i_{Ls} alternately. The cell voltage ripple during the full-grid cycle is 7 V.

This is because of the six times higher Δu_{sw} for the totem-pole PFC. Figs. 9 and 10 show the benefits of the proposed PFC in reducing current ripple and enhancing overall performance.

Considering cells in either the upper arm or the lower arm have similar voltage ripples, Cell(1) (from upper arm) and Cell(6) (from lower arm) are used as an example here to show the cell output dc voltage ripple in the positive ($u_s > 0$) and negative grid ($u_s \leq 0$) cycles. The experimental capture is shown in Fig. 11. Upper arm cells and lower arm cells are charged by i_{Ls} alternately at 60 Hz. When $u_s \leq 0$, cells in the upper arm are charged, whereas lower arm cells are held by the dc-link capacitors. The voltage ripple in the full-grid cycle is 7 V. Driving signal S_{1a} changes between high and low to control the duty ratio of Cell(1), while S_{6a} is always high to avoid potential overshoot during the u_s zero crossing. Therefore, the i_{Ls} follows the sinusoidal u_s. Similarly, when $u_s > 0$, Cell(6) in the lower arm is charged, and Cell(1) is held up by capacitors. S_{6a} outputs PWM waveforms, while S_{1a} is always high.

To demonstrate the ability of the dc output ports to equally distribute power despite mismatched system parameters, an experiment was conducted, as shown in Fig. 12. During the experiment, the output current and voltage of Cells (1), (2), (5), and (6) were measured. Cell (1) had a +20% mismatch in output capacitance and Cell (2) had the designed capacitance to serve as a comparison with Cell (1) in the upper arm. Similarly, Cell (5) had a -20% mismatch in output capacitance while Cell (6) had the designed capacitance to work as a reference to Cell (5) in the lower arm. As shown in Fig. 12, although there were some differences in the voltages and currents ripples of the cells, the proposed multilevel multiports PFC remained stable. The average current and voltage values were used to calculate the power for each cell, which resulted in 81.5, 80.5, 81, and 81.3 W, respectively. These results indicate that the power

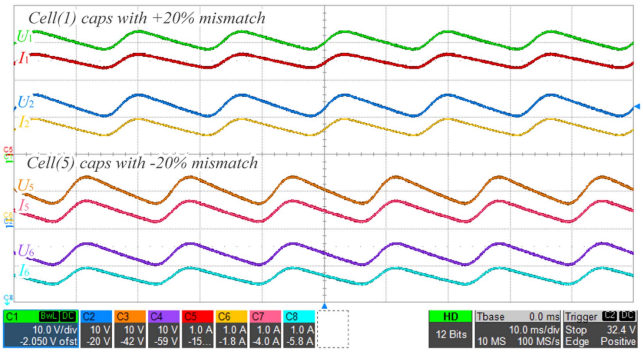


Fig. 12. Experimental results demonstrate the ability of multiple DC output ports to distribute output power evenly, despite ±20% mismatches in output capacitance parameters of Cells (1) and (5). The results show stable and evenly distributed power among Cells (1), (2), (5), and (6) with calculated values of 81.5, 80.5, 81, and 81.3 W, respectively, despite differences in voltage and current ripple amplitudes.

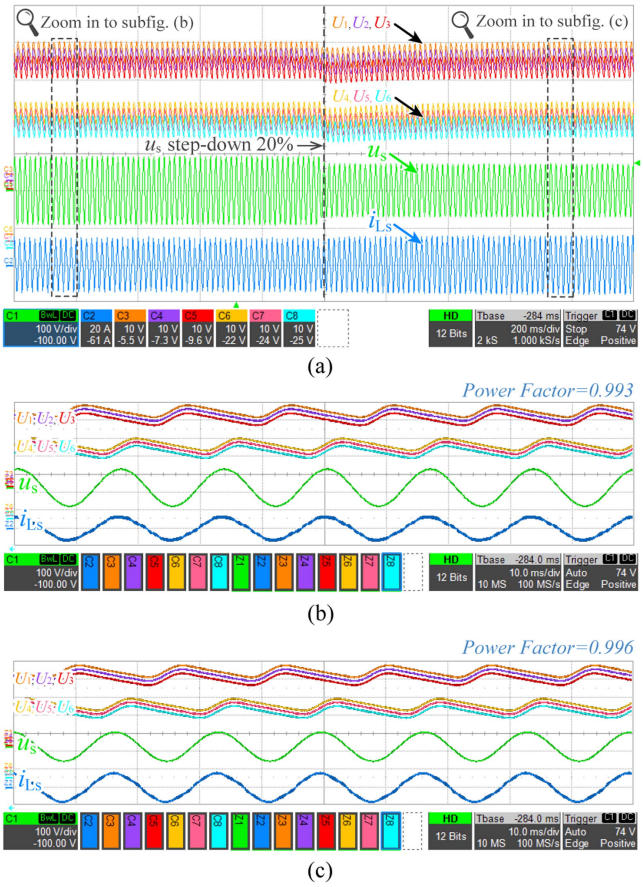


Fig. 13. Experimental results of proposed PFC converter for 20% input voltage (u_s) step down. (a) Overall waveforms demonstrating steady operation before and after the step-down transition. (b) Zoomed in view before the input voltage step down, with a power factor of 0.993. (c) Zoomed in view after the input voltage step down, with a power factor of 0.996.

was evenly distributed among the cells despite the mismatched system parameters.

To demonstrate the dynamic performance of the proposed PFC, the input voltage step-down and step-up experiments are conducted to emulate the grid voltage variations, and the corresponding results are shown in Figs. 13 and 14, respectively.

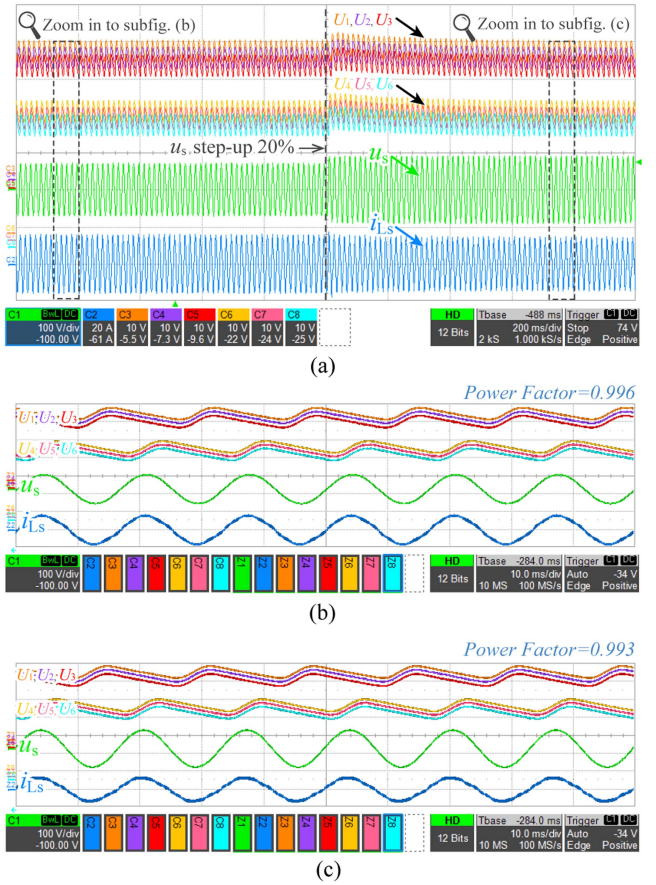


Fig. 14. Experimental results of proposed PFC converter for 20% input voltage (u_s) step up. (a) Overall waveforms demonstrating steady operation before and after the step-up transition. (b) Zoomed in view before the input voltage step up, with a power factor of 0.996. (c) Zoomed in view after the input voltage step up, with a power factor of 0.993.

In the step-down experiment of Fig. 13, the input voltage (u_s) was reduced by 20%, and the cell voltages (U_1 to U_6) returned to the set reference value of 33 V after a brief reduction. It is worth noting that the references of the six cells were intentionally staggered in the Fig. 13(b) and (c) to clearly show their respective voltages. The voltages of U_1 to U_6 were stabilized at the set values before and after the step-down experiment, and the control of the proposed PFC ensured voltage equalization for each cell. Moreover, the power factors are as high as 0.993 and 0.996 in Fig. 13(b) and (c), respectively, demonstrating that the proposed PFC effectively ensures power quality.

Fig. 14 shows the step-up experimental results of the proposed PFC topology, indicating that the voltages of Cells (1) to(6) returned to the set target value after a brief increase, and the voltages were uniformly distributed across the cells. The power factors were as high as 0.996 and 0.993 in Fig. 14(b) and (c), respectively. Overall, the results showed stable voltages and high power factor, demonstrating the proposed PFC's ability to ensure power quality and uniform voltage distribution in dynamic performance.

The measured and estimated conversion efficiency for the proposed half-bridge-based multilevel multiport PFC is shown in Fig. 15. The loss estimation relies on equations presented

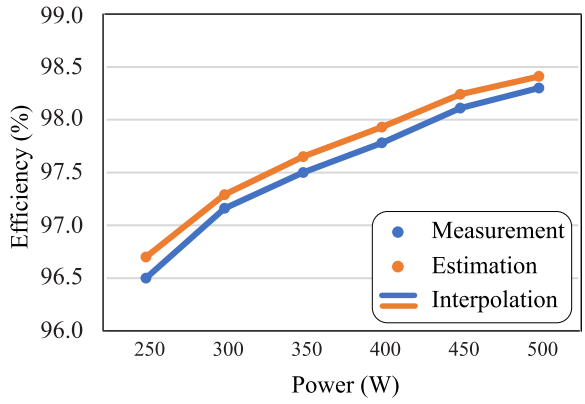


Fig. 15. Measured and estimated efficiency of the proposed half-bridge-based multilevel multiport PFC. The estimation of losses is based on equations presented in this article and simulations.

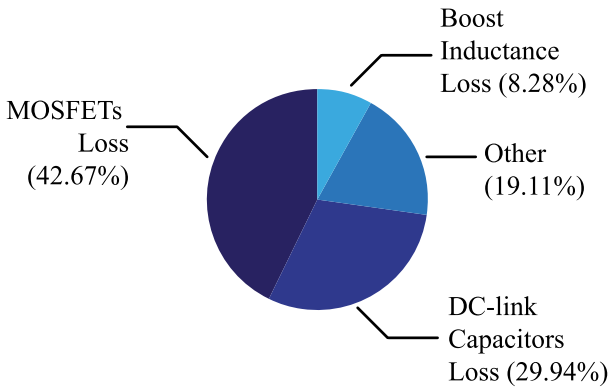


Fig. 16. Power loss breakdown of the proposed PFC topology based on experimental results at 500 W. MOSFETs switching and conduction losses account for 47.67% of the total loss, whereas the DC-link capacitors contribute to 29.94% of the total loss. The boost inductance and other factors account for 8.28% and 19.11% of the total loss, respectively.

in Section III and simulations. The measured efficiency of the converter is around 96.5% at 250 W. It increases with the rising of output power level. It goes up to 97.5% @350 W. Finally, it reaches the highest measured efficiency of 98.3% at 500 W. The breakdown of power loss analysis for the proposed PFC topology at 500 W based on experimental results is shown in Fig. 16. Four main factors contribute to the total loss in the system. The MOSFETs switching and conduction losses account for the largest portion of the total loss at 47.67%. The dc-link capacitors contribute to 29.94% of the total loss. The boost inductance and other factors account for 8.28% and 19.11% of the total loss, respectively. The figure provides important information on the sources of power loss in the proposed PFC topology and can be useful in optimizing the design for higher efficiency.

To sum up, the experimental results prove the stable operation of the proposed PFC under various conditions, while achieving high-efficiency power conversion, multidc output ports, and low-current ripples.

VI. Conclusion

In this article, a cascaded half-bridge-based bidirectional multilevel multiport bridgeless PFC has been proposed. Compared with cascaded full-bridge PFC, the number of power switches per cell is reduced by half while providing the same dc output ports, since the power cells are composed of half-bridges. Due to the multilevel voltage, the volt–second on the boost inductor drops, thereby reducing the current ripple compared to the conventional totem-pole PFC with the same inductance. Moreover, as the dc-link voltage $U_{\rm dc}$ is handled by $2n$ cells, the switching loss and conduction loss can also benefit from the use of lower voltage rating power switches. Finally, a prototype was built in the lab, and all the advantages of the proposed PFC topology were verified by experimental results.

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