Analysis and Evaluation of Modular Multilevel Converters for DC–DC Solid-State Transformer Based on Different Operating Conditions

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***Abstract*—In modular multilevel converter (MMC)-based solid-state transformer (SST), the MMC dominates total volume and power loss. The loss and volume of MMC are influenced by various factors, such as operating frequencies, waveforms of ac-link voltage, numbers of submodules, as well as modulation methods. Their impacts on loss and volume of MMC have not been comprehensively analyzed and evaluated. To investigate and evaluate the loss and volume of MMC based on various operating conditions, the computational model is developed for MMC-SST according to its operational principles. The developed model considered the parameter design of MMC to determine the capacitance and arm inductance based on various operating conditions, which are essential parameters to solve state variables. Then, with the developed computational model, the methodology is developed to comprehensively evaluate the losses and volume of MMC-SST under various operating conditions, and to investigate the impacts of the above-mentioned factors. The proposed analysis and methodology serve as a guidance and basis for the future optimal design of MMC-SST by providing insights into its performance. The proposed model and analysis are verified by experimental results.**

***Index Terms*—Computational model, parameter design, solid-state transformer (SST), modular multilevel converter (MMC).**

I. Introduction

SOLID-STATE transformers (SSTs) (also known as power electronic transformer or intelligent universal transformer) have been investigated for distribution systems to reduce the volume and weight of the power transformer [1], [2], [3], [4], [5]. However, the efficiency and power density are not competitive with the traditional power transformer, which limit the applications of SST. Generally, to improve the performance of SST, the efficiency and power density are mainly improved by modifying the control strategy, topology, hardware design, etc. Recently, the modular multilevel converter (MMC) has been employed in SST applications due to its salient features, such as modularity, scalability, high efficiency, and high reliability [6], [7], [8], [9], [10], [11], [12], [13]. For instance, the isolated modular multilevel dc–dc converter [13] is derived from the dual-active bridge (DAB) converter by employing MMCs into the isolated dc–dc converter, as shown in Fig. 1. The MMC can generate an arbitrary ac-link voltage to energize the medium-frequency transformer, which provides more flexibilities of controlling the SST while avoiding destructive *dv/dt* stress. However, there are

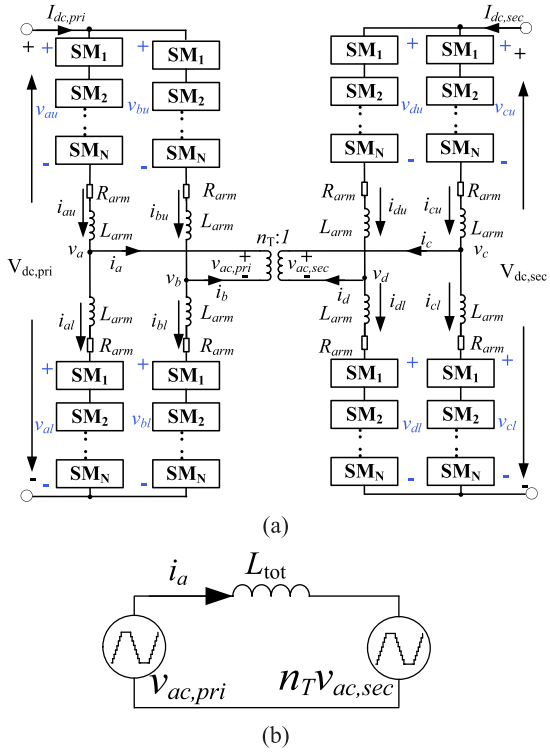

Fig. 1. Schematic of the MMC-SST. (a) Circuit diagram. (b) Equivalent circuit of ac link.

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many components in MMC, including capacitors, semiconductor devices, arm inductors, and heat sinks, which lead to high power loss and bulky volume. Therefore, the power loss and volume of MMC dominate the total loss and volume of the MMC-based SST (MMC-SST). To improve its efficiency and power density, the MMC should be optimized.

But, before optimizing the design of MMC-SST, its loss and volume should be investigated and evaluated by considering different operating conditions and circuit parameters, such as different operating frequencies, different ac-link voltage waveforms, number of cascaded submodules (N_{SM}), and modulation methods. This guides the optimal design of MMC-SST and helps to identify what can be done to improve efficiency and power density. In [14], the N_{SM} has been optimized for the cascaded H-bridge inverter, which mainly analyzed the impacts of N_{SM} on semiconductor loss, filter size, and reliability. In [15], an MMC based on full-bridge SMs has been optimized for low-frequency applications, which mainly analyzed the relationship between capacitor voltage ripple, semiconductor loss, as well as the inductor current ripple. In [16], the MMC has been optimized and compared with two-level inverters for low-voltage microgrids, which mainly analyzed the impacts of switching frequency on filter size. The authors in [17] proposed the multiobjective optimization procedure of an MMC based on full-bridge SMs for low-frequency applications, in which the analytical model did not consider the modulation methods and voltage-balancing algorithms. These papers only considered MMCs for fundamental-frequency applications, while they did not consider MMCs for medium/high-frequency applications. In addition, the operational principles of MMC-SST are not the same as MMCs for low-frequency applications. Thus, the existing analytical models cannot be directly applied to MMC-SST.

The loss and volume are greatly influenced by various factors, which have not been comprehensively analyzed and evaluated. Thus, in this article, the influences of these factors are analyzed and evaluated for MMC-SST to guide future optimal design. In addition, to investigate and evaluate the operational performance of MMC-SST under various conditions, another challenge is developing a computational model, which considers various parameters, various operating conditions, different modulation methods, etc. The switching model is time-consuming and inconvenient for studying various operating conditions and circuit parameters. The analytical model is inflexible and inconvenient to consider detailed switching states, switching currents, different modulation methods, and sorting algorithms. The circuit-based simplified models have been developed to accelerate the electromagnetic transient simulation, including average-value models and equivalent circuit models [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33]. For various operating conditions and parameters, these models are inflexible to sweep parameters and are not suitable for the optimal design of MMC-SST. In this way, in this article, a computational model is proposed for MMC-SST, which considers main-circuit parameter design, solves state variables, and is convenient to sweep parameters. The circuit parameter design serves as an inherent module of the developed computational model. Then, a methodology is proposed to facilitate the evaluation, analysis, and design of MMC-SST, which is based on the developed computational model.

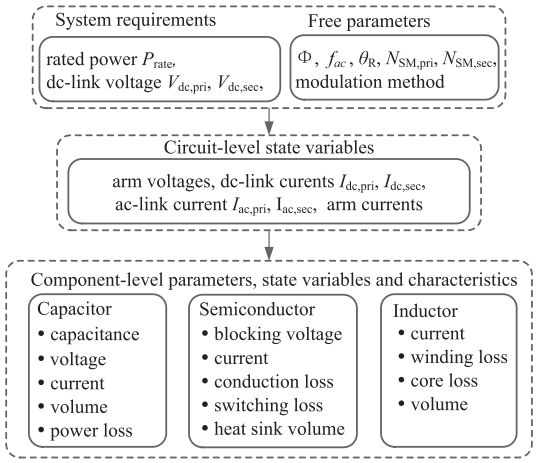


Fig. 2. Relationships among system requirements, circuit parameters, and state variables.

For the convenience of analysis, the parameters and state variables can be divided into three categories: system requirements and parameters, circuit-level parameters and state variables, as well as component-level parameters and state variables, as shown in Fig. 2. The system requirements mainly include rated power, primary-side and secondary-side dc-link voltages. The system-level free parameters include the phase-shift (PS) angle (Φ) between primary-side and secondary-side ac-link voltages, operating frequency (f_{ac}), modulation method, and ac-link voltage waveform. The system requirements and free parameters determine circuit-level state variables, which include dc-link currents, ac-link currents, as well as arm voltages and currents. Then, the rated voltages and currents of components are derived from circuit-level state variables, which greatly impact their operational characteristics.

This article mainly focuses on analyzing and evaluating the loss and volume of MMC rather than the entire MMC-SST. The rest of this article is organized as follows. Section II briefly summarizes the operational principles of MMC-SST and conceptually analyzes the impacts of the main factors. In Section III, a computational model is developed based on the abovementioned analysis. In Section IV, the methodology is proposed for evaluating the loss of MMC-SST based on the proposed computational model. The impacts of the main factors on the performances of MMCs are analyzed and evaluated in Section V. In Section VI, based on the parameters of the experimental prototype, the hardware is implemented according to the results of the developed model. The analysis and evaluations are verified by experimental results. Section VII analyzed and summarized the main findings and contributions of this article. Finally, Section VIII concludes this article.

II. Operational Principles of the MMC-SST

For the convenience of analysis, the operational principles of MMC-SST are briefly summarized in this section. The

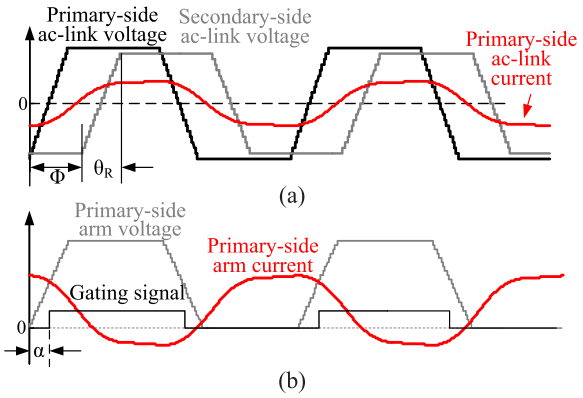


Fig. 3. Theoretical waveforms of the (a) primary-side and secondary-side AC-link voltages, and primary-side AC-link current, and (b) arm voltage, arm current, and SM gating signal.

MMC-SST has similar operational principles to the DAB converter, as shown in Fig. 1. The difference is that the MMC can generate a controllable multilevel voltage, which changes from a square waveform to a triangular waveform. The arbitrary ac-link voltage/current and arm voltage/current waveforms are shown in Fig. 3(a) and (b), respectively. Similar to the DAB converter, the ac-link currents and the transmitted power are determined by the PS angle (Φ) between the primary- and secondary-side ac-link voltages. The θ_{R} represents the ramping angle of ac-link voltage, which is used to define the ac-link voltage waveform. The α represents the PS angle of a gating signal relative to arm voltages. To generate the multilevel ac-link voltages, the PS and the nearest-level control (NLC) modulations are applicable for MMC-SST, which lead to different charging and discharging behaviors of SM capacitors [10], [12], [34].

A. Brief Summary of MMC-SST Operational Principles

1) Ac-Link Voltages and Current: The arbitrary nonsinusoidal ac-link voltage can be expressed as piecewise linear (1) and (2). The corresponding root-mean-square (rms) value of ac-link voltage is $V_{\mathrm{dc}}\sqrt{\frac{\theta_{\mathrm{R}}}{3\pi}+\frac{\pi-\theta_{\mathrm{R}}}{\pi}}$. Then, the ac-link current is solved by (3)

$$v_{\mathrm{ac,pri}}(\varphi)=\begin{cases}\dfrac{2V_{\mathrm{dc,pri}}}{\theta_{\mathrm{R}}}\varphi-V_{\mathrm{dc,pri}}, & 0<\varphi<\theta_{\mathrm{R}}\\ V_{\mathrm{dc,pri}}, & \theta_{\mathrm{R}}<\varphi<\pi\\ -v_{\mathrm{ac,pri}}(\varphi-\pi), & \pi<\varphi<2\pi\end{cases} \tag{1}$$

$$v_{\mathrm{ac,sec}}(\varphi)'=n_T v_{\mathrm{ac,sec}}(\varphi)=\frac{n_T V_{\mathrm{dc,sec}}}{V_{\mathrm{dc,pri}}}v_{\mathrm{ac,pri}}(\varphi-\Phi) \tag{2}$$

where $v_{\mathrm{ac,sec}}(\varphi)'$ is the reflected secondary-side voltage.

$$i_{\mathrm{ac}}(\varphi)=\frac{1}{\omega L_{\mathrm{tot}}}\int v_{\mathrm{ac,pri}}(\varphi)-v_{\mathrm{ac,sec}}(\varphi)'\mathrm{d}\varphi \tag{3}$$

where L_{tot} is the total ac-link inductance including the leakage inductance of transformer and arm inductances. The ω is determined by the operating frequency of the ac-link voltage, which equals switching frequency in this article.

2) Submodule Capacitance: The SM capacitance is determined by the limits of voltage ripple. The peak–peak ripple of capacitor voltage $\Delta V_{\mathrm{c,pp}}$ equals to $\frac{\Delta Q_{\mathrm{c,pp}}}{C}$, where $\Delta Q_{\mathrm{c,pp}}$ is the peak–peak ripple of capacitor charge. Generally, the capacitor charge (Q_c) is an integral of the capacitor current, which is determined by the arm current and the switching state of an SM. According to the analysis proposed in [34], the SM capacitor charging and discharging performance varies with different modulation methods and voltage-balancing algorithms.

3) Total Inductance and Arm Inductance: The dc-link current is derived from ac-link voltage and current, as expressed in (4), which is the function of the rated power, dc-link voltage, Φ, θ_{R}, and total inductance. In this way, when system parameters are given, the total inductance can be solved by (4), in which the rated power corresponds to $|\Phi|=\frac{\pi}{2}$

$$I_{\mathrm{dc,pri}}=\frac{\int_0^{2\pi}v_{\mathrm{ac,pri}}i_{\mathrm{a}}\mathrm{d}\varphi}{2\pi V_{\mathrm{dc,pri}}}. \tag{4}$$

The total inductance includes the leakage inductance of transformer and arm inductances of MMC. In this article, the arm inductance is only designed to limit the second-order ripple of circulating current. Similar to the analysis of SM capacitance, the inductor flux density is an integral of the inductor voltage. The peak–peak ripple of circulating current $\Delta i_{\mathrm{zx,pp}}$ equals to $\frac{\Delta B_{\mathrm{Larm,pp}}}{L_{\mathrm{arm}}}$, where $\Delta B_{\mathrm{Larm,pp}}$ is the peak–peak ripple of inductor flux density.

B. Analysis of Free-Parameters Impacts

As aforementioned, when designing or evaluating the MMC-SST, the main free parameters include frequency, N_{SM}, the ramping angle θ_{R} of ac-link voltage, and modulation methods. According to the abovementioned operational principles of MMC-SST, the impacts of the main free parameters are briefly analyzed.

1) Frequency of Ac-Link Voltage: According to (3) and (4), when the operating frequency is increased, to transfer the rated power, the total inductance and the arm inductances are reduced. The increased frequency also leads to reduced SM capacitance. In addition, the switching frequency greatly impacts the switching loss of semiconductor devices. Generally, the increased frequency leads to more switching loss. But, the frequency does not affect the rms value of current, and hence does not greatly affect the conduction losses of semiconductor devices.

Fig. 4(a) shows the influences of frequency on SM capacitance, the total inductance, arm inductance, and semiconductor loss. By increasing frequency, the volume of capacitor can be reduced due to the decreased capacitance. However, for the arm inductor, the frequency greatly affects core loss and winding loss. Although its volume can be reduced, its core loss and winding loss may not be decreased and could even be increased. A detailed evaluation is necessary to determine the tradeoff between loss and volume. For the semiconductor devices and the associated cooling system, the increased switching loss requires a larger heat sink to dissipate the generated heat.

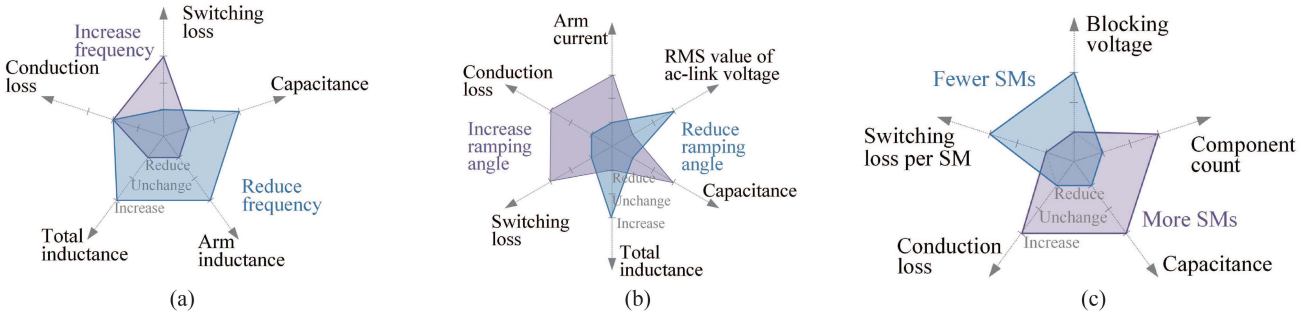


Fig. 4. Overview of tradeoffs affected by (a) operating frequency, (b) ramping angle of AC-link voltage, and (c) number of SMs.

2) Ramping Angle of Ac-Link Voltage: The rms value of ac-link voltage is determined by the ramping angle θ_{R}. By increasing θ_{R}, it avoids the high *dv/dt* of ac-link transformer, while reducing the rms value of ac-link voltage. Thus, to transfer the rated power, the ac-link current should be increased by reducing the total inductance L_{tot}, which greatly increases the requirements and challenges of designing and fabricating transformers to limit the leakage inductance. As shown in Fig. 4(b), the increased ac-link current greatly influences the state variables or parameters related to current and requires higher SM capacitance to limit capacitor voltage ripple, which potentially increasing capacitor loss and volume. The increased current also causes higher losses of semiconductor devices, which require larger heat sinks to dissipate the generated heat. For the arm inductor, the volume might be reduced due to the reduced inductance, while the winding loss might be increased. In addition, the increased current requires a larger cross-sectional area for the winding coil, which might require a larger core to optimize the window utilization.

3) Number of SMs: The N_{SM} directly determines the nominal capacitor voltage, the blocking voltages of semiconductor devices, and the components count. As analyzed in [14], the low-voltage semiconductor device has a better switching behavior, which reduces switching losses. Consequently, for each SM, when N_{SM} is increased, the switching loss and heat sink volume are reduced, while the conduction loss is not obviously influenced by blocking voltage. But, for MMC, the increased N_{SM} leads to increased component count, which increases the total conduction loss and heat sink volume. In addition, the increased N_{SM} requires higher SM capacitance to limit voltage ripple, which greatly increases the total volume of capacitors. Fig. 4(c) shows the effects of N_{SM}s.

III. Computational Model Considering Circuit Parameter Design of MMC-Based SST

To develop the computational model for evaluating MMC-SST, according to the aforementioned operational principles, it can be modeled as a group of differential equations. Then, the computational model is developed from the differential-equation model by considering the design of circuit parameters, which includes total inductance, arm inductance, and SM capacitance. The main circuit parameters are determined based on system-level requirements according to the analysis in Section II, which is incorporated into the computational model.

A. Mathematical Model of MMC-SST

The ac-link current is determined by ac-link voltages and Φ. When neglecting the voltage drop on the arm inductor, the ac-link voltages are mainly determined by arm voltages.

1) Arm Voltages and Currents: For each phase, based on Kirchhoff's voltage law, the relationship between arm voltage and arm current can be expressed as

$$\begin{cases} R_{\mathrm{arm}} i_{xu} + L_{\mathrm{arm}} \dfrac{\mathrm{d}i_{xu}}{\mathrm{d}t} & = \dfrac{V_{\mathrm{dc}}}{2} - v_{xu} - v_x \\ R_{\mathrm{arm}} i_{xl} + L_{\mathrm{arm}} \dfrac{\mathrm{d}i_{xl}}{\mathrm{d}t} & = \dfrac{V_{\mathrm{dc}}}{2} - v_{xl} + v_x \end{cases} \tag{5}$$

where the subscript x represents phase-leg a, b, c, and d. When $\{x = a, b\}$, the R_{arm} and L_{arm} denote the equivalent series resistance (ESR) and inductance of the primary-side arm inductor ($R_{\mathrm{arm,pri}}$ and $L_{\mathrm{arm,pri}}$). When $\{x = c, d\}$, the R_{arm} and L_{arm} represent the ESR and inductance of the secondary-side arm inductor ($R_{\mathrm{arm,sec}}$ and $L_{\mathrm{arm,sec}}$). Similarly, when $\{x = a, b\}$, the V_{dc} represents the primary-side dc-link voltage ($V_{\mathrm{dc,pri}}$). When $\{x = c, d\}$, the V_{dc} represents the secondary-side dc-link voltage ($V_{\mathrm{dc,sec}}$).

2) Ac-Link and Dc-Link Currents: The relationship among arm voltages, ac-link current, and circulating current can be described by

$$\begin{cases} R_{\mathrm{arm}} i_x + L_{\mathrm{arm}} \dfrac{\mathrm{d}i_x}{\mathrm{d}t} & = (v_{xl} - v_{xu}) - 2v_x \\ R_{\mathrm{arm}} i_{zx} + L_{\mathrm{arm}} \dfrac{\mathrm{d}i_{zx}}{\mathrm{d}t} & = \dfrac{V_{\mathrm{dc}} - v_{xu} - v_{xl}}{2}. \end{cases} \tag{6}$$

The primary-side and secondary-side dc-link currents are derived from corresponding circulating currents, as expressed in (7). By incorporating (6) of all phases, (8) expresses the relationship between arm voltages and ac-link current

$$\begin{cases} i_{\mathrm{dc,pri}} & = i_{za} + i_{zb} \\ i_{\mathrm{dc,sec}} & = i_{zc} + i_{zd} \end{cases} \tag{7}$$

$$\begin{aligned} &\frac{[(v_{al} - v_{au}) - (v_{bl} - v_{bu})] - n_T [(v_{cl} - v_{cu}) - (v_{dl} - v_{du})]}{2} \\ &= (R_T + R_{\mathrm{arm,pri}} + n_T^2 R_{\mathrm{arm,sec}}) i_a \\ &\quad + \left(L_T + L_{\mathrm{arm,pri}} + n_T^2 L_{\mathrm{arm,sec}}\right) \frac{\mathrm{d}i_a}{\mathrm{d}t} \end{aligned} \tag{8}$$

where R_{T} and L_{T} denote the winding resistance and leakage inductance of ac-link transformer. The $L_T + L_{\mathrm{arm,pri}} + n_T^2 L_{\mathrm{arm,sec}}$ is defined as the total inductance (L_{tot}) of MMC-SST.

3) Capacitor Voltage and Arm Voltage: Based on the abovementioned analysis, the arm currents, ac-link current, and dc-link current are regulated by arm voltages. The arm voltage is determined by summing the capacitor voltages of inserted SMs. In this way, to determine arm voltage, the capacitor voltage should be derived from the arm current, as expressed in (9). The S_{SMi} represents the switching function of the i^{th} SM. When $S_{\mathrm{SMi}}=1$, the SM is inserted. When $S_{\mathrm{SMi}}=0$, the SM is bypassed

$$\begin{cases} i_{\mathrm{ci}} = i_{\mathrm{arm}} S_{\mathrm{SMi}} \\ v_{\mathrm{ci}} = \frac{1}{C}\int i_{\mathrm{ci}}\mathrm{d}t \end{cases} \tag{9}$$

$$v_{\mathrm{arm}} = \sum_{i=1}^{N_{\mathrm{SM}}} v_{\mathrm{ci}} S_{\mathrm{SMi}} \tag{10}$$

where v_{ci} is the capacitor voltage of the ith SM in an arm, respectively.

4) Arm Inductance and Circulating Current: Theoretically, the circulating current contains half of the dc-link current and harmonics, as expressed in the following:

$$i_{zx} = \overline{i_{zx}} + \widetilde{i_{zx}} = \frac{I_{\mathrm{dc}}}{2} + \sum i_{zx,hn} \tag{11}$$

where I_{dc} represents primary/secondary-side dc-link current, $i_{zx,hn}$ represents the nth order harmonic of circulating current.

The arm voltage is divided into two terms: the ideal staircase voltage determined by average capacitor voltage, and the voltage ripple derived from capacitor voltage ripple, which are defined in the following:

$$v_{\mathrm{arm}} = \overline{v_{\mathrm{arm}}} + \widetilde{v_{\mathrm{arm}}} = \sum_{i=1}^{N_{\mathrm{SM}}} \overline{v_{\mathrm{ci}}} S_{\mathrm{SMi}} + \sum_{i=1}^{N_{\mathrm{SM}}} \widetilde{v_{\mathrm{ci}}} S_{\mathrm{SMi}} \tag{12}$$

where $\overline{v_{\mathrm{ci}}}$ denotes the average capacitor voltage of the ith SM, while $\widetilde{v_{\mathrm{ci}}}$ represents the capacitor voltage ripple of of the ith SM.

When substituting (11) and (12) into (6), it can be modified as

$$R_{\mathrm{arm}}\left(\overline{i_{zx}} + \widetilde{i_{zx}}\right) + L_{\mathrm{arm}}\frac{\mathrm{d}\widetilde{i_{zx}}}{\mathrm{d}t} = \frac{V_{\mathrm{dc}} - \overline{v_{xu}} - \overline{v_{xl}}}{2} - \frac{\widetilde{v_{xu}} + \widetilde{v_{xl}}}{2}. \tag{13}$$

In this way, the current ripple of circulating current results from capacitor voltage ripple. The voltage ripple crossing arm inductor can be estimated by $\dfrac{V_{\mathrm{dc}} - v_{xu} - v_{xl}}{2} - R_{\mathrm{arm}}\dfrac{I_{\mathrm{dc}}}{2}$. When neglecting R_{arm}, the current ripple of circulating current can be expressed as

$$\widetilde{i_{zx}} = \frac{B_{\mathrm{Larm}}}{L_{\mathrm{arm}}} = \frac{1}{L_{\mathrm{arm}}}\int \frac{V_{\mathrm{dc}} - v_{xu} - v_{xl}}{2} - R_{\mathrm{arm}}\frac{I_{\mathrm{dc}}}{2}\mathrm{d}t \tag{14}$$

where B_{Larm} is the flux density of the arm inductor. In this way, after determining the peak–peak ripple of flux density $\Delta B_{\mathrm{Larm,pp}}$, the arm inductance can be estimated as $\dfrac{\Delta B_{\mathrm{Larm,pp}}}{\Delta i_{zx,\mathrm{pp}}}$, where $\Delta i_{zx,\mathrm{pp}}$ is the peak–peak ripple of circulating current.

B. Implementation of Computational Model Considering Circuit Parameter Design

Based on the abovementioned analysis, the circuit parameters shall be determined in advance before solving the state variables. According to the analysis of Section II, when system-level parameters are given, the total inductance can be determined by (4). Then, assuming SM capacitor voltage has no ripple, the ac- and dc-link currents are solved to determine arm current and capacitor currents. The peak–peak ripple of capacitor charge $\Delta Q_{\mathrm{c,pp}}$ is solved to determine the SM capacitance. When the SM capacitance is determined, the capacitor voltages and arm voltages are recalculated by considering the capacitor voltage ripple. Then, the arm-inductor voltage is solved. The peak–peak ripple of $\Delta B_{\mathrm{Larm,pp}}$ is calculated from inductor voltage to determine arm inductor. Finally, all the state variables are updated. To be clear, in Table I, a pseudocode is developed to implement the computational model of an MMC-SST. The corresponding flowchart of the computational model is shown in Fig. 5, which is incorporated into the design methodology for evaluating the loss and volume.

IV. Methodology for Evaluating Loss and Volume of MMCs in MMC-SST

Since MMC contains many passive and active components, it dominate the total power loss and volume of MMC-SST. To evaluate its performance, the power loss and volume (efficiency and power density) are the main concerns. Based on the given system-level requirements and parameters, initially, the computational model determines the circuit parameters of MMC. Subsequently, the state variables of components are solved, including the switching states of semiconductor devices and the voltages and currents of all components. Then, the parameters of these components are selected from a preconstructed database.

The semiconductor devices are selected from a database to evaluate their power losses and volume, which collects data on insulated gate bipolar transistors (IGBTs) and metal-oxide-semiconductor field-effect transistors (MOSFETs) from Infineon, Rohm, Onsemi, IXYS, Wolfspeed, and ABB. Similarly, a database is employed to select the capacitors, which collected data on electrolytic and film capacitors from TDK, Nichicon, AVX, KEMET, and Vishay. The arm inductor is designed by the method proposed in [35], whose magnetic core is selected from datasheets for magnetic provided by Ferroxcube, Metglas, Hitachi, and TDK.

Finally, the overall power loss and volume of MMC are comprehensively evaluated. Fig. 5 shows the flowchart of the methodology to evaluate the loss and volume of MMC-SST.

A. Capacitor Selection

The electrolytic capacitors and film capacitors are selected to construct the SM capacitors. Generally, compared with electrolytic capacitors, film capacitors have higher voltage and current ratings, lower ESRs, and longer lifetime, while having lower capacitances. To estimate loss, the ESR is obtained from datasheet.

TABLE I
PSEUDOCODE OF COMPUTATIONAL MODEL FOR MMC-BASED SST CONSIDERING CIRCUIT PARAMETER DESIGN

STEP 1: Initialization
Set System Parameters: P_{rate}, $V_{\text{dc,pri}}$, $V_{\text{dc,sec}}$, f_{ac}, θ_{R}, Φ;
Set Circuit Parameters: N_{SM};
Set Limitations: $\Delta V_{\text{c,pp}}$, $\Delta i_{\text{zx,pp}}$;
Set Simulation parameters: number of simulation steps $k_{\max}$, simulation time step T_s;
Initialize Variables ($k = 1$): phase currents, arm currents, dc-link currents, arm voltages, capacitor voltages, gating signals;

STEP 2: Determine Circuit Parameters
Determine L_{tot} **by** (4) ;
Determine SM Capacitance
FOR k=2 to $N_{\text{SM}}N_{\text{samp}}$
% N_{samp} is number of sampling points per period $\frac{1}{f_{ac}T_s}$
solve $i_{\text{arm}}(k)$;
[$\text{S}_{SM}(k)$]=Balancing (Sorting options, $Q_c(k-1)$);
solve capacitor charge by $Q_c(k)=Q_c(k-1)+\frac{i_{\text{c}}(k)+i_{\text{c}}(k-1)}{2}T_s$;
ENDFOR
Determine SM capacitance C by $\frac{\Delta Q_{\text{c,pp}}}{\Delta V_{\text{c,pp}}}$;
Determine Arm Inductance
FOR k=2 to $N_{\text{SM}}N_{\text{samp}}$
[$\text{ID}_{xu}(k)$]=Voltage balancing (Sorting options, $v_{c,xu}(k-1)$);
[$\text{ID}_{xl}(k)$]=Voltage balancing (Sorting options, $v_{c,xl}(k-1)$);
[$\text{S}_{xu}(k)$,$\text{V}_{xu}(k)$]=Modulation (Modulation options, $v_{c,xu}(k-1)$);
[$\text{S}_{xl}(k)$,$\text{V}_{xl}(k)$]=Modulation (Modulation options, $v_{c,xl}(k-1)$);
solve flux density B_{Larm} by:
$B_{\text{Larm}}(k)=B_{\text{Larm}}(k-1)+\frac{V_{\text{dc}}-\text{V}_{xu}(k)-\text{V}_{xl}(k)}{2}T_s$;
solve $i_{\text{xu}}(k)$, $i_{\text{xl}}(k)$;
$[v_{c,xu}(k)]$=Solve Capacitor Voltage(C, $i_{xu}(k)$, $i_{xu}(k-1)$, $\text{S}_{xu}(k)$, T_s);
$[v_{c,xl}(k)]$=Solve Capacitor Voltage(C, $i_{xl}(k)$, $i_{xl}(k-1)$, $\text{S}_{xl}(k)$, T_s);
ENDFOR
Determine Arm Inductance L_{arm} by $\frac{\Delta B_{\text{Larm}}}{\Delta i_{\text{zx,pp}}}$;
Determine $L_{\text{T}} = L_{\text{tot}} - L_{\text{arm,pri}} - n_T^2 L_{\text{arm,sec}}$;

STEP 3: Solve All State Variables
Solve State Variables
FOR $k = 2$ to $k_{\max}$
Voltage Balancing
[$\text{ID}_{xu}(k)$]=Voltage balancing (Sorting options, $v_{c,xu}(k-1)$);
[$\text{ID}_{xl}(k)$]=Voltage balancing (Sorting options, $v_{c,xl}(k-1)$);
Modulation
[$\text{S}_{xu}(k)$,$\text{V}_{\text{arm},xu}(k)$]=Modulation (Modulation options, $v_{c,xu}(k-1)$);
[$\text{S}_{xl}(k)$,$\text{V}_{\text{arm},xl}(k)$]=Modulation (Modulation options, $v_{c,xl}(k-1)$);
Solve ac-link current and phase currents
$[i_a(k)]$=Solve ac-link current($V_{\text{arm},au}(k)\sim V_{\text{arm},du}(k)$, $V_{\text{arm},al}(k)\sim V_{\text{arm},dl}(k)$, $i_a(k-1)$, R_{T}, L_{T}, n_{T}, R_{arm}, L_{arm}, T_s);
$i_b(k) = -i_a(k)$, $i_c(k) = -n_{\text{T}} i_a(k)$, $i_d(k) = -n_{\text{T}} i_b(k)$;
Solve circulating currents
$[i_{zx}(k)]$=Solve circulating current($V_{\text{arm},xu}(k)$, $V_{\text{arm},xl}(k)$, $i_{zx}(k-1)$, R_{arm}, L_{arm}, T_s);
Solve arm currents
$i_{xu}(k)=0.5i_x(k)+0.5i_{zx}(k)$, $i_{xl}(k)=-0.5i_x(k)+0.5i_{zx}(k)$;
Update capacitor voltages
$[v_{c,xu}(k)]$=Solve Capacitor Voltage(C, $i_{xu}(k)$, $i_{xu}(k-1)$, $\text{S}_{xu}(k)$, T_s);
$[v_{c,xl}(k)]$=Solve Capacitor Voltage(C, $i_{xl}(k)$, $i_{xl}(k-1)$, $\text{S}_{xl}(k)$, T_s);
ENDFOR

In this article, the SM capacitor is constructed by combinations of n_{s} series-connected and n_{p} parallel-connected capacitors to reach the required capacitance, rated voltage, and rated current, while optimizing the volume and power losses (resulting from ESR). Then, some limits are set for the design, which can be modified according to the specific design requirements. In this article, the rated voltage ($n_{\text{s}}V_{\text{ci,rate}}$) is 1.1–1.5 times of the nominal SM capacitor voltage, while the current ($n_{\text{p}}I_{\text{ci,rate}}$) of the selected capacitor is 1.1–2 times of required rms current of SM capacitor, where $I_{\text{ci,rate}}$ is the rated current of an individual capacitor. The n_{s} is not greater than 4 since more series-connected capacitors lead to increased ESR and need voltage-balancing snubber [15].

B. Semiconductor Devices

Similarly, a switch of an SM is constructed by combinations of n_{p} parallel-connected IGBTs and MOSFETs to reach rated current and possibly reduce conduction loss, where n_{p} is no more than 4 [36].

When selecting IGBT and MOSFET from a database, the blocking voltage ($V_{\text{SW,blk}}$) ranges from 1.1 to 1.5 times of the nominal SM capacitor voltage, while the current rating ($n_p I_{\text{SW,rate}}$) is 1.1 to 2 times of required rms current of each switch ($I_{\text{SW,rms}}$).

When evaluating semiconductor devices, the power loss and heat sink volume are the main concerns. To estimate the power loss of IGBTs and MOSFETs, the analytical models are comprehensively proposed in existing papers and technical documents [37], [38], [39], which are briefly summarized in this article.

The power losses of the semiconductor devices include the conduction loss of IGBT (P_{conT}) and diode (P_{conD}), the switching loss (E_{on}, E_{off}) of IGBT, and the reverse recovery loss (E_{rec}) of diode. Based on [37], the power losses of IGBTs can be estimated based on the parameters provided by datasheets, which are expressed as

$$\begin{cases} P_{\text{conT}} = V_{\text{ce}}(i_c)\cdot i_c = \left(c_0 + c_1\cdot i_c + c_2\cdot i_c^2\right)\cdot i_c \\ P_{\text{conD}} = V_{\text{f}}(i_f)\cdot i_f = \left(d_0 + d_1\cdot i_f + d_2\cdot i_f^2\right)\cdot i_f \end{cases} \tag{15}$$

$$\begin{cases} E_{\text{on}} = \left(a_{\text{on0}} + a_{\text{on1}}\cdot i_c + a_{\text{on2}}\cdot i_c^2\right)\frac{V_{\text{C}}^{\text{nom}}}{V_{\text{CEN}}} \\ E_{\text{off}} = \left(a_{\text{off0}} + a_{\text{off1}}\cdot i_c + a_{\text{off2}}\cdot i_c^2\right)\frac{V_{\text{C}}^{\text{nom}}}{V_{\text{CEN}}} \\ E_{\text{rec}} = \left(a_{\text{rec0}} + a_{\text{rec1}}\cdot i_f + a_{\text{rec2}}\cdot i_f^2\right)\frac{V_{\text{C}}^{\text{nom}}}{V_{\text{CEN}}} \end{cases} \tag{16}$$

where V_{ce} is the ON-state collector–emitter voltage of IGBT; V_{f} is the forward voltage drop of the antiparalleled diode; the collector current (i_c) and free-wheeling diode current (i_f) are derived from the arm current and switching function; V_{CEN} is the rated V_{ce} under test condition; the coefficients $c_0 \sim c_2$, $d_0 \sim d_2$, $a_{\text{on0}} \sim a_{\text{on2}}$, $a_{\text{off0}} \sim a_{\text{off2}}$, and $a_{\text{rec0}} \sim a_{\text{rec2}}$ are extracted from datasheets using the curve fitting method. For MOSFET, (15) is still applicable for estimating the conduction losses of MOSFETs. However, most datasheets do not provide curves of E_{on}, E_{off}, and E_{rec}. Thus, the switching losses should be estimated from other parameters [38], [40], [41], which are not duplicated in this article.

Then, the maximum thermal resistance of the heat sink can be estimated from power loss [42], [43]. Based on the analysis proposed in [15], [44], the heat-sink volume can be estimated from its thermal resistance, as expressed in (17), where the cooling system performance index (CSPI) is assumed to be 3.0 for natural air cooling. In this article, an HB SM is assumed to

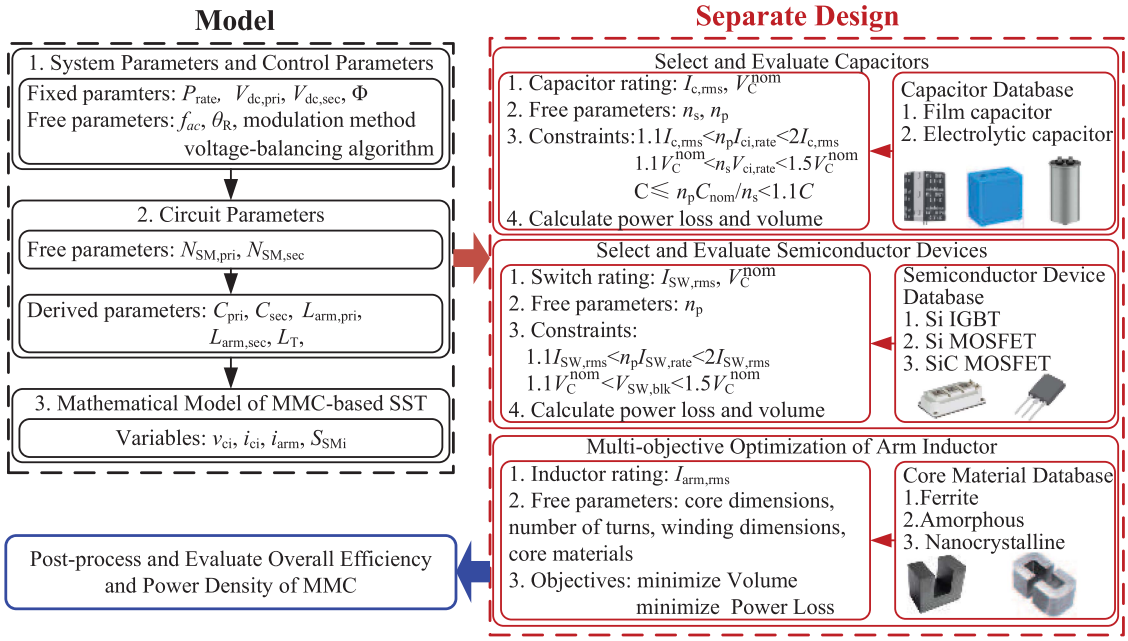


Fig. 5. Flowchart of methodology for evaluating performance of MMC-based SST.

be mounted on one heat sink. The total loss of an HB SM is calculated to estimate the thermal resistance of the heat sink. The ambient temperature is set as 40 °C

$$V_{\text{hs}}\,[\text{litre}] = \frac{1}{R_{hs}\left[\frac{\text{K}}{\text{W}}\right]\text{CSPI}\left[\frac{\text{W}}{\text{K·litre}}\right]} \tag{17}$$

where V_{hs} is the estimated volume of the heat sink.

C. Arm Inductor Design

The design procedure of the dc inductor has been comprehensively analyzed in [35], which applied the nondominated sorting genetic algorithm to the multiobjective optimization. This design methodology is also suitable for designing the arm inductor of MMC-SST in this article, which is briefly summarized in this section.

When constructing an arm inductor, the EE core is selected as the magnetic core, and the multistrand wire or litz wire is employed to construct arm inductor winding. The magnetic core materials and conductor materials in the database are considered as discrete selections. In the database, the magnetic materials include TDK N87 [45], Ferroxcube 3C90 [46], Metglas 2605-SA1 [47], and Hitachi FT-3M [48]. Information on other ferrite materials is available in [35]. For the winding coil design, only the copper material is considered. Then, the winding loss and core loss are analyzed separately. Finally, the total power loss and volume are estimated and evaluated.

To estimate core loss induced from nonsinusoidal excitations, the improved general Steinmetz equation (iGSE) is a popular method, which is expressed as (18). The coefficients K_c, α, and β are obtained from datasheets. The core loss P_{core} is calculated by $P_v\text{Vol}_{\text{core}}$, as expressed in (18) and (19)

$$P_v = \frac{1}{T}\int_0^T k_i|\Delta\text{B}|^{\beta-\alpha}\left|\frac{\text{dB(t)}}{\text{d}t}\right|^{\alpha}\text{d}t\ \frac{kW}{m^3} \tag{18}$$

where coefficient k_i is defined as

$$k_i = \frac{K_c}{2^{\beta-1}\pi^{\alpha-1}\int_0^{2\pi}|\cos(\theta)|^{\alpha}\text{d}\theta}. \tag{19}$$

To estimate the winding loss, the dc resistance of the winding coil is estimated by $\frac{l_w}{\sigma A_w}$, in which the l_w is the length of winding. σ denotes the conductivity of the material. A_w is the cross-sectional area of the winding coil. To estimate the ac resistance, the ratio of winding radius to skin depth determines the ac-resistance coefficient. The skin depth is estimated by $\frac{1}{\sqrt{\pi f\mu\sigma}}$, which is affected by frequency. μ is the permeability of conductor. Then, the coefficient of the ac resistance is estimated by (20). The ac resistance equals $k_{\text{ac}}R_{\text{dc}}$ [49]

$$k_{\text{ac}} = \begin{cases} 1+\dfrac{\left(\dfrac{r}{\delta_0}\right)^4}{48+0.8\left(\dfrac{r}{\delta_0}\right)^4}, & \left(\dfrac{r}{\delta_0}\right)<1.7 \\ 0.25+0.5\left(\dfrac{r}{\delta_0}\right)+\dfrac{3}{32}\left(\dfrac{r}{\delta_0}\right), & \left(\dfrac{r}{\delta_0}\right)>1.7. \end{cases} \tag{20}$$

D. Total Loss and Volume

The overall losses and volume of the MMC are assessed by considering those of capacitors, semiconductors, and arm inductors. Subsequently, the breakdowns of loss and volume are illustrated to determine the dominant loss and volume.

TABLE II
FIXED SYSTEM-LEVEL PARAMETERS OF COMPUTATIONAL MODEL

Rated power, P_{rate}	1 MW
Nominal dc-link voltage, $V_{\text{dc,pri}}$, $V_{\text{dc,sec}}$	10 kV
Transformer turns ratio	1:1
Number of phase legs per MMC	2
PS angle, Φ	0.5π

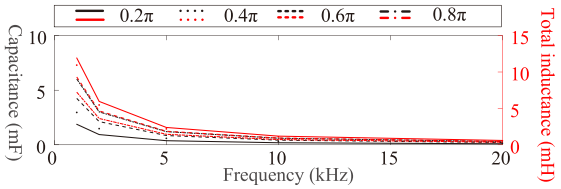


Fig. 6. Submodule capacitances and total inductances of MMC-SST based on different frequencies ($N_{\text{SM}} = 10$).

Based on the loss and volume, the impacts of various factors or parameters are evaluated, which helps to identify the main factors influencing the losses and volume of MMC.

V. LOSS AND VOLUME OF MMC BASED ON DIFFERENT OPERATING CONDITIONS

Based on the developed methodology, to evaluate the impacts of the aforementioned parameters, the fixed system-level parameters of the computational model are listed in Table II. The operating frequency is swept from 1 to 20 kHz, which equals the switching frequency. The N_{SM} changes from 2 to 25, and the ramping angle θ_{R} changes from 0.1π to π. Then, based on these parameters, the main circuit parameters are determined at first, which include SM capacitance, arm inductance, and total inductance. Then, the state variables are solved by the computational model. These variables are utilized to estimate the loss and volume of capacitors, arm inductors, semiconductor devices, and heat sinks.

A. Impacts of Operating Frequency

When the frequency changes from 1 to 20 kHz, the N_{SM} is fixed at 10. According to the analysis of Section II, the increased frequency leads to reduced SM capacitance and total inductance, as shown in Fig. 6. Then, based on various frequencies, the power losses and volume are evaluated for capacitors, semiconductors, and inductors as follows.

1) *Capacitor:* For each specific frequency, the nondominated solutions are shown in Fig. 7. As the frequency increases, the capacitor volume is greatly reduced due to the reduced SM capacitance, while the capacitor loss is not obviously influenced by frequency. Compared with electrolytic capacitors, film capacitors lead to smaller volume and lower power losses. In addition, for low-capacitance SMs, the SM capacitors are mainly constructed by film capacitors.
2) *Semiconductor devices and heat sink:* For each frequency, the average loss and volume of selected nondominated solutions are shown in Fig. 8. Conduction loss dominates the total loss of semiconductor devices, which is not greatly influenced by frequency. The higher frequency results in a higher switching loss. The SiC devices offer advantages over Si devices by reducing switching losses and reducing the required volume of the heat sink.
3) *Arm inductor:* For each frequency, the average loss and volume of nondominated solutions are shown in Fig. 9. By increasing frequency, the inductor loss and volume are reduced.
4) *Loss and volume breakdown:* To evaluate the impacts of frequency on the total loss and volume, for each simulation case, the nondominated solutions are selected based on the total loss and volume. Then, the average loss and volume of selected nondominated solutions are shown in Fig. 10, along with the breakdown of loss and volume. As shown in Fig. 10, the semiconductor loss dominates the total

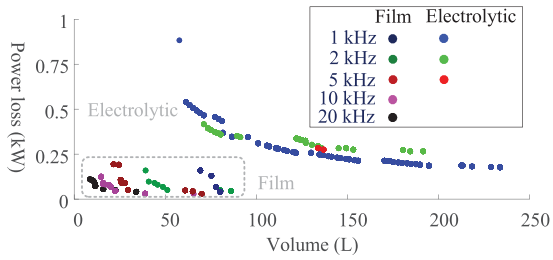


Fig. 7. Nondominated computational solutions of capacitor volume and power loss based on different frequencies.

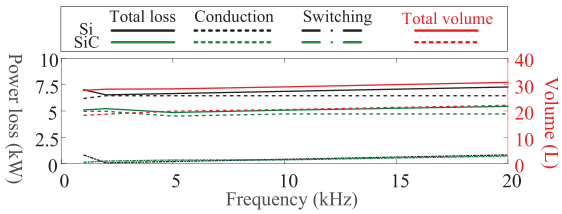


Fig. 8. Power loss breakdown of semiconductor devices and heat sink volume based on different frequencies ($N_{\text{SM}} = 10$).

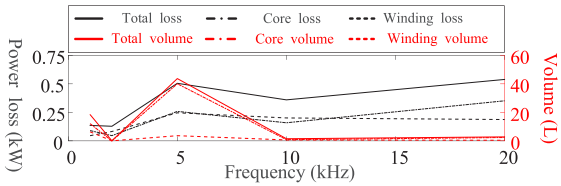


Fig. 9. Power loss and volume of arm inductors based on different frequencies ($N_{\text{SM}} = 10$).

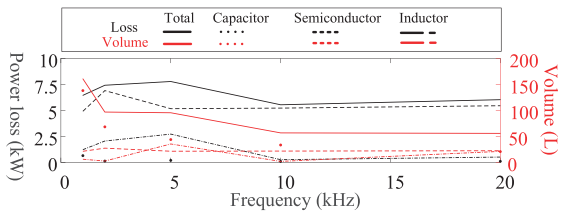


Fig. 10. Power loss and volume breakdown of MMC based on different frequencies ($N_{\text{SM}} = 10$).

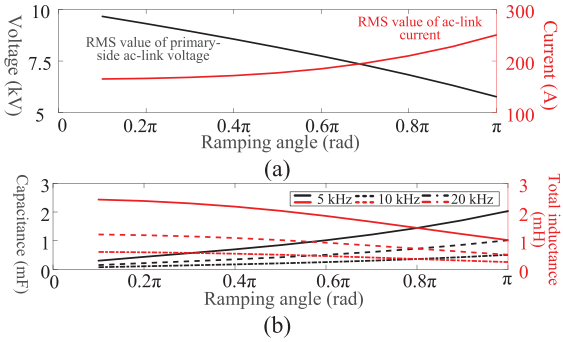


Fig. 11. Impacts of AC-link voltage ramping angle on (a) rms values of AC-link voltage and current and (b) total inductance and SM capacitance.

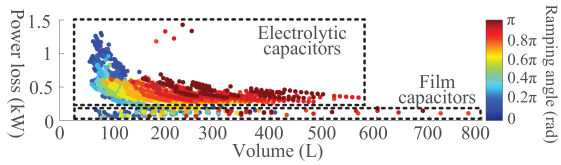


Fig. 12. Power loss and volume of SM capacitors based on various ramping angles (frequency is fixed at 10 kHz).

loss of MMC, while the volume of capacitors and heat sinks dominates the total volume. Initially, by increasing frequency, the loss and volume of the arm inductor and capacitor are reduced. By further increasing frequency, the switching loss and inductor loss are increased, which results in increased total loss.

B. Impacts of Ac-Link Voltage Waveform

To evaluate the impacts of the ac-link voltage waveform, the ramping angle θ_R varies from 0.1π to π, while the operating frequency is fixed at 10 kHz. According to the analysis of Section II, the rms value of ac-link voltage is related to θ_R. As the θ_R is increased, the rms value of ac-link voltage is reduced. To transmit the rate power, the total inductance is reduced, and the ac-link current is increased, as shown in Fig. 11.

1) *Capacitor:* Based on various ramping angles, the power loss and volume of SM capacitors are shown in Fig. 12. As the ramping angle is increased, the increased current results in a higher charging/discharging current of SM capacitor. Hence, the capacitor voltage ripple increases, which requires higher capacitance to suppress capacitor voltage ripple. The induced high SM capacitances and high currents lead to increased loss and volume. Film capacitors lead to lower losses than electrolytic capacitors.
2) *Semiconductor devices and heat sink:* The higher ramping angle results in greatly increased power loss of semiconductor devices due to the induced high current. Hence, it requires a larger heat sink to dissipate the generated heat, as shown in Fig. 13.
3) *Arm inductor:* For arm inductor design, based on the fixed frequency and various ramping angles, Fig. 14 shows the average loss and volume of nondominated solutions. The core loss almost equals the winding loss, which leads to

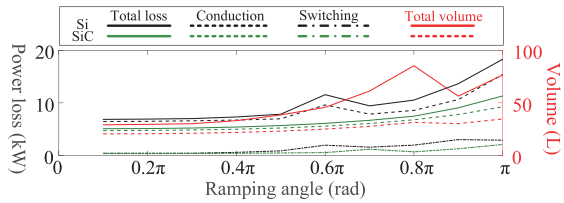


Fig. 13. Power loss of semiconductor devices and volume of heat sink based on various ramping angles (frequency is fixed at 10 kHz).

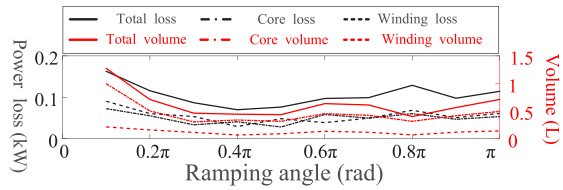


Fig. 14. Power loss and volume of arm inductor based on various ramping angles (frequency is fixed at 10 kHz).

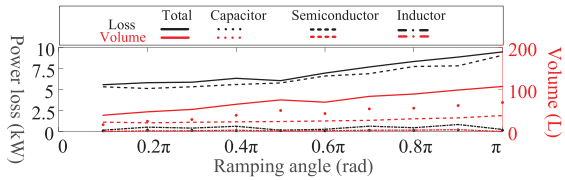


Fig. 15. Impacts of ac-link voltage ramping angle on total volume and power loss of MMC (frequency is fixed at 10 kHz).

the tradeoff between them. Initially, the increased ramping angle leads to reduced volume and power loss due to the induced low inductance. When the ramping angle is further increased, the high current requires a larger cross-sectional area of the winding coil. In this way, the larger core is selected to provide enough window area and to avoid saturation of the magnetic core. Consequently, the loss and volume are increased.

4) *Loss and volume breakdown:* Based on various ramping angles, the average loss and volume of nondominated solutions are shown in Fig. 15, which also shows the breakdown of loss and volume. The total loss and volume are greatly increased due to the increased ramping angle. Semiconductor loss still dominates the total power loss of MMC, while capacitor and heat sink volume dominate the total volume.

C. Impacts of Number of SMs

To evaluate the impacts of N_{SM}, the operating frequency is fixed at 10 kHz.

1) *Capacitor:* As analyzed in Section II, the SM capacitance is reversely proportional to the nominal capacitor voltage, which is reversely proportional to N_{SM}. Thus, the increased N_{SM} leads to increased capacitance, as shown in Fig. 16. The increased capacitance does not mean higher loss and volume. Initially, by increasing N_{SM}, the reduced blocking voltage requires fewer series-connected

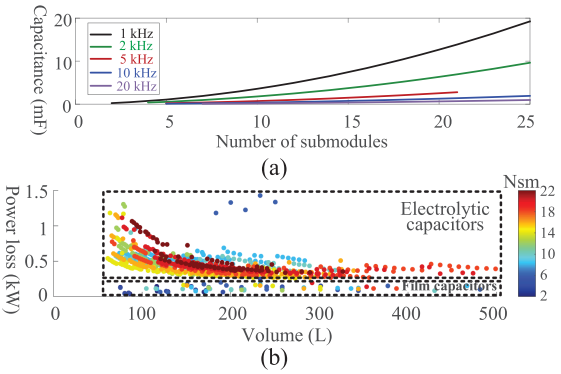


Fig. 16. Impacts of N_{SM} on (a) capacitance, and (b) loss and volume of SM capacitor (frequency is fixed at 10 kHz).

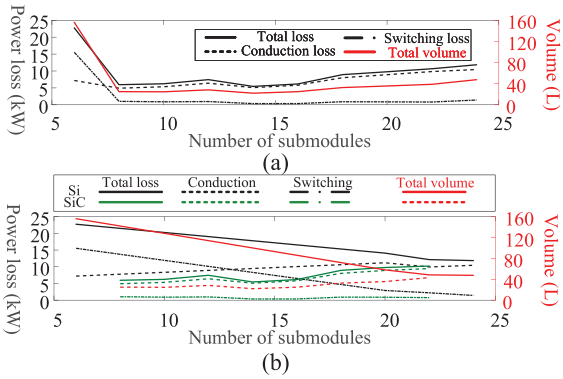


Fig. 17. Semiconductor loss and heat sink volume based on different N_{SM}s. (a) Average loss and volume of nondominated solutions. (b) Semiconductor loss and heat sink volume based on Si and SiC devices (frequency is fixed at 10 kHz).

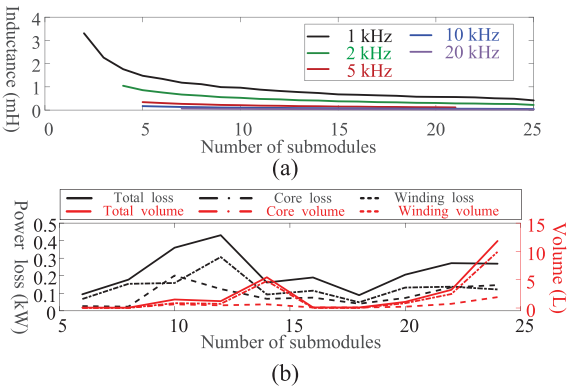


Fig. 18. Arm inductance, power loss, and volume of arm inductors based on different N_{SM}s. (a) Arm inductance. (b) Power loss and volume (frequency is fixed at 10 kHz).

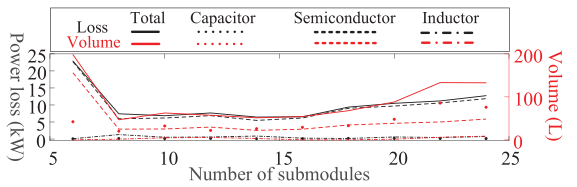


Fig. 19. Total loss and volume of MMC based on various numbers of submodules (frequency is fixed at 10 kHz).

capacitors, which reduces ESR and the induced loss. When further increasing N_{SM}, the increased capacitance requires more paralleled capacitors, which increases capacitor volume while reducing loss.

In addition, for low-voltage SMs, there are fewer film-capacitor solutions, as shown in Fig. 16(b). Compared with electrolytic capacitors, film capacitors have high voltage and current ratings with low capacitances. For low-voltage SMs, to reach the required SM capacitance, it needs more paralleled film capacitors than electrolytic capacitors, and the current rating of combined film capacitors is much higher than the nominal capacitor current, which is regarded as an overdesign. Thus, film capacitors are more suitable for high-voltage, low-capacitance SMs, while electrolytic capacitors are suitable for low-voltage, high-capacitance SMs.

2) *Semiconductor devices and heat sink:* For each N_{SM}, the nondominated solutions are selected, and their average power loss and volume are shown in Fig. 17(a). Initially, by increasing N_{SM}, the SM is constructed by low-voltage semiconductor devices with a better switching performance, which reduces switching loss and the required volume of the heat sink. When further increasing N_{SM}, the increased component count leads to greatly increased conduction loss and the total volume of heat sinks. Fig. 17(b) shows the power loss and volume of nondominated solutions corresponding to Si and SiC semiconductor devices. The SiC components have better switching performance than Si components. When N_{SM} increases, the switching losses of Si devices are reduced, while the switching losses of SiC devices remain low.

3) *Arm inductor:* As analyzed in Section III, the second-order circulating current ripple relates to the capacitor voltage ripple. When increasing N_{SM}, the increased SM capacitance reduces voltage ripple and the induced second-order circulating current. Thus, it requires lower arm inductance to suppress second-order circulating current. On the other hand, it can also be considered as that the increased capacitance lets SM capacitor absorb more second-order ripple of power, which reduces the requirements of arm inductors. However, there is no obvious relationship among inductor loss, volume, and N_{SM}, as shown in Fig. 18.

4) *Loss and volume breakdown:* Based on various N_{SM}s, the average loss and volume of nondominated solutions are shown in Fig. 19. Initially, by increasing N_{SM}, the semiconductor loss is reduced, which induces a smaller heat sink. By further increasing N_{SM}, the increased count of components leads to greatly increased total loss and volume due to increased semiconductor loss, heat sink volume, and capacitor volume. The design of the arm inductor is not obviously influenced by N_{SM}.

D. Impacts of Modulation Methods

The impacts of modulation methods and voltage-balancing algorithms have been analyzed in [34]. The detailed analysis

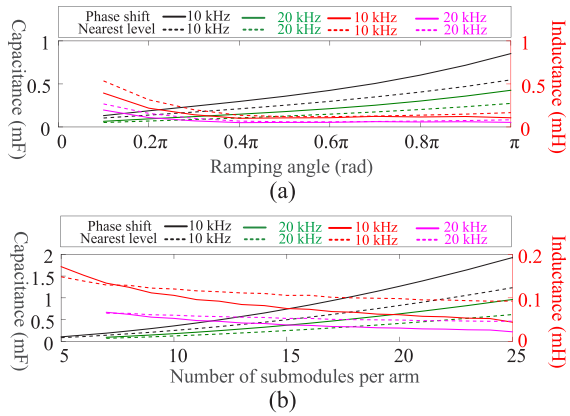


Fig. 20. Submodule capacitances and arm inductances based on different modulation methods. (a) Various ramping angles. (b) Various N_{SM}s.

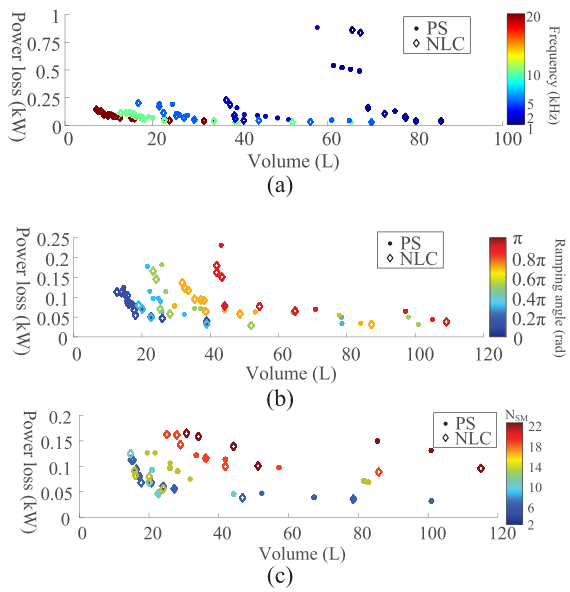


Fig. 21. Capacitor loss and volume based on different modulation methods. (a) Frequencies. (b) Various ramping angles. (c) Various N_{SM}s.

is not duplicated in this article. The modulation methods and voltage-balancing algorithms mainly influence the charging and discharging behaviors of SM capacitors, which lead to a low-frequency ripple of capacitor voltage. Based on the abovementioned analysis, different SM capacitances also impact the arm inductance.

Fig. 20 shows the SM capacitances and arm inductances based on PS modulation and NLC modulation. Compared with PS modulation, the NLC modulation leads to reduced capacitance. Due to reduced capacitance, the high-frequency ripple of capacitor voltage is increased, and results in increased second-order harmonics of arm current. Thus, based on NLC modulation, the arm inductance is increased. In addition, for low N_{SM}, different modulation methods result in implicit differences in SM capacitances and arm inductances.

Fig. 21 compares the total loss and volume of capacitors based on PS and NLC modulations. When employing NLC modulation, the reduced capacitance leads to lower losses and

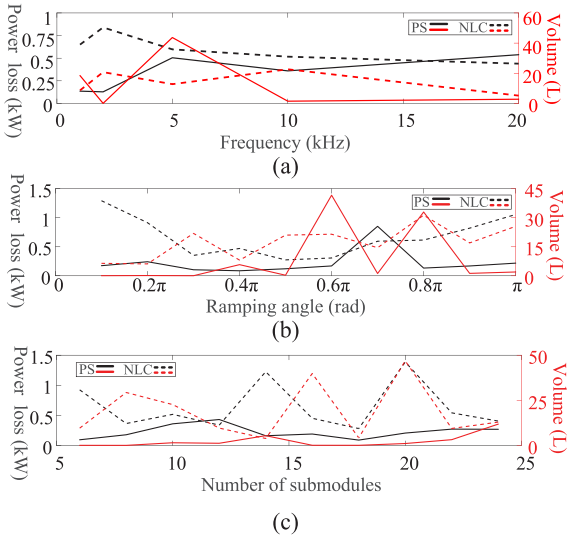


Fig. 22. Arm inductor loss and volume based on different modulation methods. (a) Frequencies. (b) Various ramping angles. (c) Various N_{SM}s.

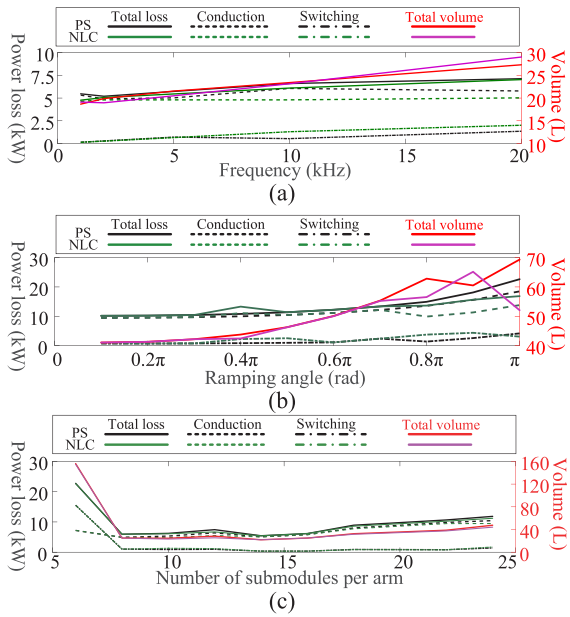


Fig. 23. Semiconductor loss and heat sink volume based on different modulation methods. (a) Frequencies. (b) Various ramping angles. (c) Various N_{SM}s.

smaller volumes. Fig. 22 compares the total losses and volume of arm inductors based on PS and NLC modulations. Based on NLC modulation, the increased inductance leads to increased loss and volume. Fig. 23 compares the heat sink volume and semiconductor loss. The modulation methods do not obviously impact semiconductor loss and heat sink volume.

Based on different modulation methods, the breakdown of loss and volume are shown in Figs. 24–26. The modulation methods do not obviously influence semiconductor loss. Compared with PS modulation, when employing the NLC modulation, the capacitor volume is greatly reduced due to the reduced SM capacitance, especially when θ_{R} is greater than 0.5π. Meanwhile,

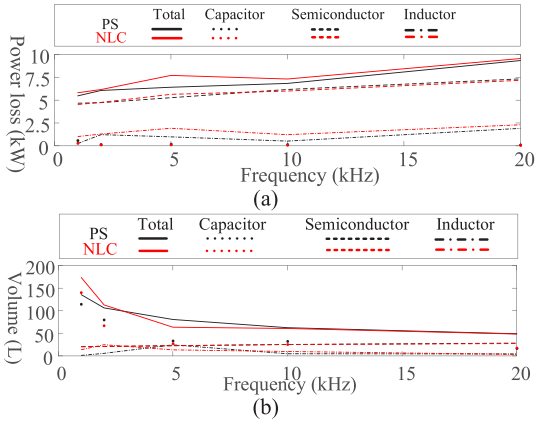


Fig. 24. Loss and volume breakdown of MMC based on different modulation methods and various frequencies. (a) Loss. (b) Volume.

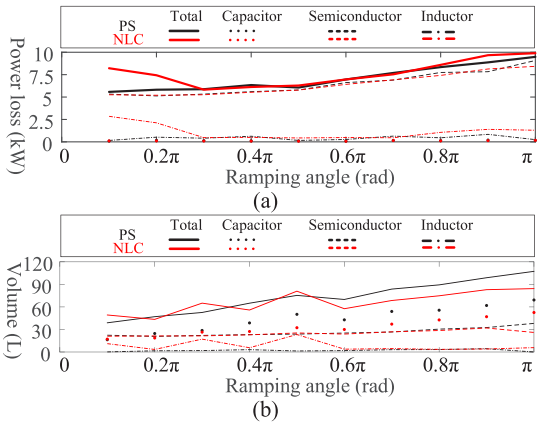


Fig. 25. Loss and volume breakdown of MMC based on different modulation methods and various ramping angles. (a) Loss. (b) Volume.

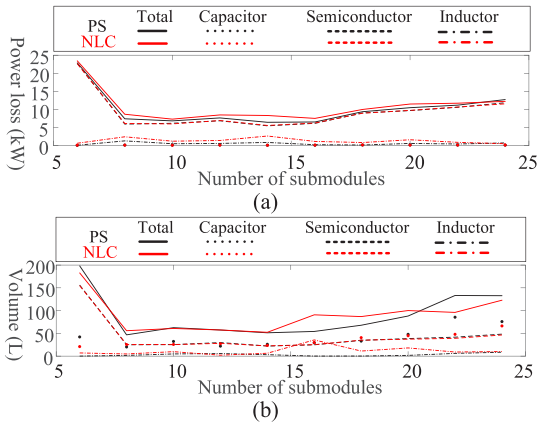
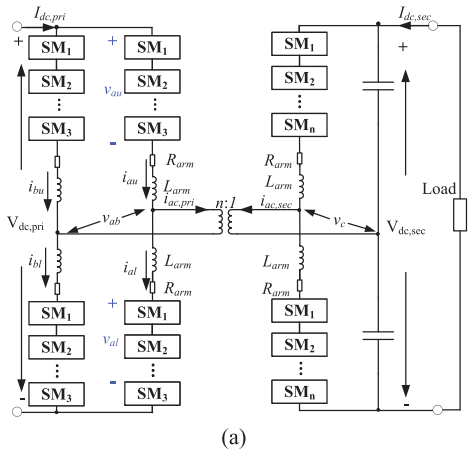


Fig. 26. Loss and volume breakdown of MMC based on different modulation methods and various N_{SM}s. (a) Loss. (b) Volume.

the inductance is increases, leading to increased arm inductor loss and volume.



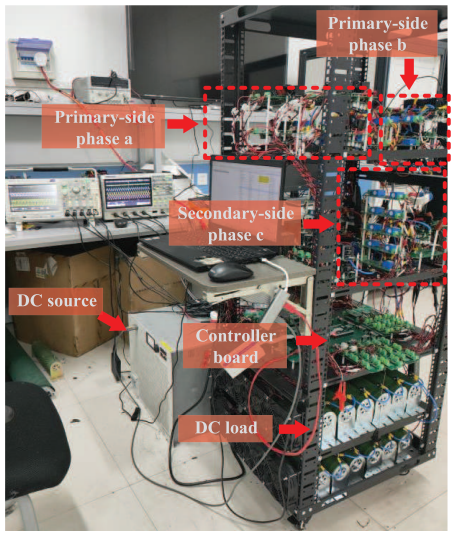


Fig. 27. Experimental prototype. (a) Schematic of the experiment prototype. (b) Photograph of the experiment prototype.

TABLE III
PARAMETERS OF THE EXPERIMENTAL PROTOTYPE

Rated load power, P	2.67 kW (400 V, 60 Ω)
Primary-side dc-link voltage, V_{dc}	200 V
Secondary-side dc-link voltage, V_{dc}	400 V
Primary-side number of SMs per arm	3
Secondary-side number of SMs per arm	3 to 5
Secondary-side dc-link capacitance	500 μF
Semiconductor device	FGH40T65UQDF

VI. Experimental Verification

A scale-down experimental prototype of MMC-SST is built to verify the effectiveness of the proposed computational model and evaluate the loss and volume of MMC under various operating conditions, as shown in Fig. 27. Its parameters are listed in Table III. The primary-side MMC contains two phases, and there are 3 SMs per arm. To increase the secondary-side dc-link voltage, the single-phase MMC is employed. In this way, the $N_{\mathrm{SM,sec}}$ can be changed from 3 to 5. In addition, under all conditions, the IGBT or MOSFET is mounted on Ohmite E3A-T220-25E heat sink to cool down the semiconductor device.

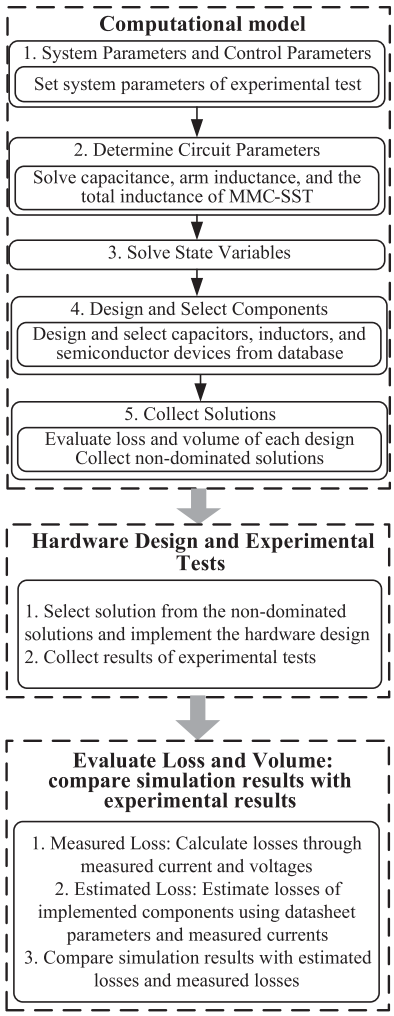


Fig. 28. Flowchart of experimental verifications.

TABLE IV
PARAMETERS OF TRANSFORMERS FOR MMC-SST BASED ON VARIOUS FREQUENCIES

Frequency (kHz)	n_{pri}	n_{sec}	Magnetic inductance (mH)	Leakage inductance (μH)
5	53	67	9.245	41.216
10	51	46	15.42	12.498
20	52	46	29.24	27.78
50	42	50	4.241	8.045

Thus, the heat-sink volume is identical for all experimental tests. Under all conditions, the PS angle between primary-side and secondary-side voltages (Φ) is fixed at $\pi/2$.

To verify the developed computational model and the analysis, the experimental tests are conducted under various operating conditions, which involve different frequencies, ac-link voltage waveforms, N_{SM}s, and modulation methods. The experimental verification procedure is illustrated in Fig. 28, which is briefly summarized as follows.

1) *Solve circuit parameters and state variables:* For each operating condition, the total inductance, SM capacitance, and arm inductance are determined. Then, the state variables are solved by the computational model.
2) *Design and select components:* Based on the developed design methodology proposed in Section IV, the capacitors, arm inductors, and semiconductor devices are selected from a preconstructed database. The loss and volume are estimated by the computational model to select the nondominated solutions. Subsequently, depending on available stock and quantity of components, one of the solutions is selected from these nondominated solutions.
3) *Hardware design and experimental test:* According to the selected solution, the SM capacitors and arm inductors are fabricated. The semiconductor devices are obtained from suppliers. Then, the experimental tests are conducted to collect measured currents and voltages of various components.
4) *Evaluate loss and volume:* Based on various operating conditions, the measured losses of SM capacitors, semiconductors devices, and arm inductors are calculated from measured voltages and currents. For SM capacitors, the ESRs are measured by an impedance analyzer. Then, the power losses are estimated by measured ESRs and capacitor currents. For semiconductor devices, the measured losses are also derived from the measured currents and voltages. The estimated losses are calculated from the measured currents, voltages, and the datasheet parameters. For arm inductors, to estimate the winding losses, the winding resistances are measured by an impedance analyzer. The core losses are estimated from the measured inductor currents and parameters provided by datasheets. Finally, the measured losses are compared with estimated losses and simulation results to evaluate the feasibility of the developed methodology. Since the components are designed or selected in accordance with the selected solutions, the volume should be identical.

The transformers are fabricated for various operating frequencies, whose parameters are listed in Table IV. Since the leakage inductances of fabricated transformers are unadjustable, for various operating conditions, to adjust the total inductance according to the computational model, an external inductor is connected in series with the primary-side winding of ac-link transformer.

Fig. 29 shows the ac-link voltages, ac-link current, arm voltages, and arm currents.

A. Experimental Results Based on Various Frequencies

To evaluate the loss and volume of MMC-SST based on various frequencies, the operating frequency varies from 10 to 50 kHz. The θ_{R} is fixed at 0.5π, and there are 3 SMs per arm. Based on various frequencies, Fig. 30 shows the arm inductances and SM capacitances of the experimental prototype.

1) Semiconductor Devices: By increasing operating frequency, the conduction loss of semiconductor devices is not obviously influenced, while the switching loss is greatly increased. Fig. 31 compares the semiconductor loss of the simulation model with the estimated loss and the measured loss. The

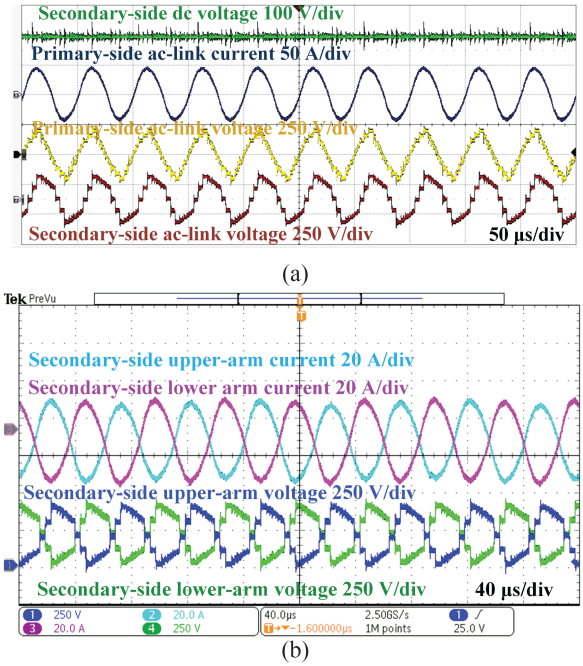


Fig. 29. Experimental results of the MMC-SST. (a) Primary- and secondary-side AC-link voltages, AC-link current, and secondary-side DC-link voltage. (b) Secondary-side arm voltages and current.

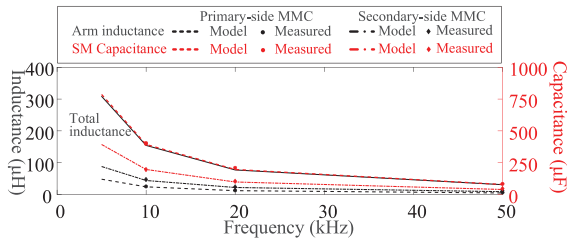


Fig. 30. Arm inductances and SM capacitances of experimental prototype based on various frequencies.

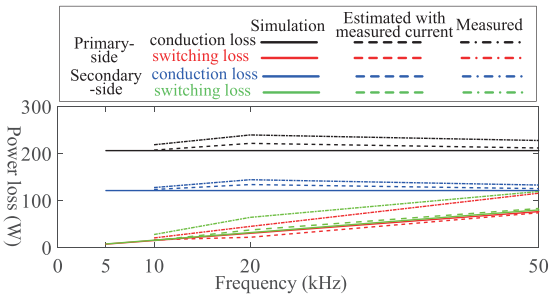


Fig. 31. Semiconductor losses of 650 V IGBTs based on various frequencies.

semiconductor loss is estimated from measured switching current and OnSemi FGH40T65UQDF parameters from datasheet. One of the reasons is that the circuit parameters and operating conditions of semiconductor devices are different from the standard testing condition provided by datasheets. In addition, due to the improper layout of SM dc-link power loop, the induced parasitic inductance leads to high ringing of collector–emitter voltage. To suppress the voltage ringing, the RC snubber is

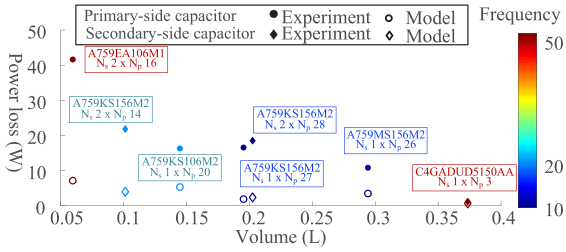


Fig. 32. Capacitor loss and volume of experimental prototype based on various frequencies.

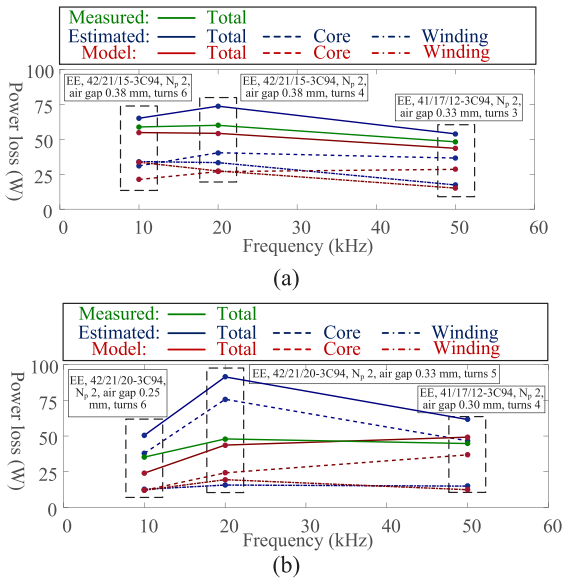


Fig. 33. Inductor loss of experimental prototype based on various frequencies. (a) Primary-side MMC. (b) Secondary-side MMC.

paralleled with IGBT, which leads to increased loss. But, the trend still agrees with the simulation results.

2) Capacitors: Fig. 32 shows the loss and volume of constructed SM capacitors based on various frequencies, which compares the estimated losses with those of the computational model. As aforementioned, for experimental tests, the power of SM capacitor is estimated from measured ESR and current. For the computational solution, the loss is estimated from the ESR that is provided by datasheet. The volume of experimental results and computational solutions are identical. Increased frequency reduces the number of paralleled capacitors due to reduced SM capacitance. Although it leads to reduced volume, the increased ESR results in higher loss.

For electrolytic capacitors, the measured loss is much higher than the loss of the computational solution. Because the computational model does not consider the resistances of PCB traces. However, in practice, the series-/parallel-connected capacitors are connected by PCB traces or wires, which leads to additional losses.

3) Arm Inductors: The arm inductors are constructed by EE cores from Ferroxcube, including 42/21/20-3C94, 42/21/15-3C94, and 41/17/12-3C94. To verify the effectiveness of the developed methodology, in Fig. 33, the measured losses of

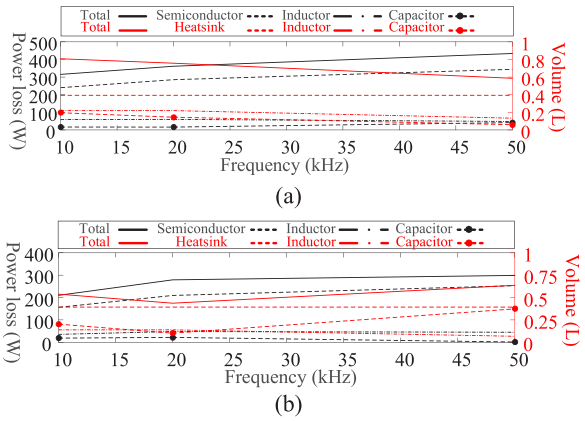


Fig. 34. Breakdown of volume and power loss of experimental prototype based on various frequencies. (a) Primary-side MMC. (b) Secondary-side MMC.

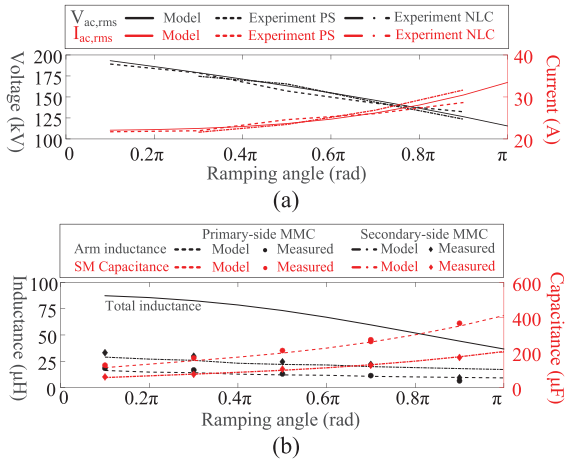


Fig. 35. Currents, voltages, and circuit parameters based on various ramping angles. (a) rms values of AC-link voltages and currents. (b) Arm inductance and SM capacitance.

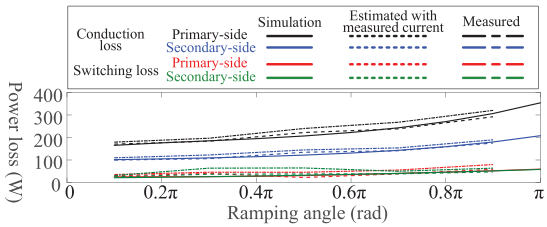


Fig. 36. Semiconductor losses based on different ramping angles: semiconductor losses of simulation model, experimental measurements, and estimation based on datasheet parameters and measured currents.

fabricated inductors are compared with estimated losses and simulation results. The measured loss is calculated from measured inductor current and voltage. The estimated core loss is obtained from the measured current and parameters from datasheets. Since the measured arm current contains noises, it results in high $|dB/dt|$, which greatly impacts the result of iGSE. Thus, the estimated core loss is much higher than the core loss from the simulation model. The estimated winding loss is calculated from measured winding resistance and arm current. As shown in Fig. 33, the measured losses are close to the simulation results, and the increased frequency reduces losses and volume of arm inductors due to the reduced arm inductance.

4) Loss and Volume Breakdown: The breakdowns of loss and volume are shown in Fig. 34. The semiconductor loss dominates the total loss of MMC, while the heat sink volume and capacitor volume dominate the total volume.

B. Experimental Results Based on Various Ramping Angles

To evaluate the impacts of ac-link voltage waveform, the ramping angle θ_R changes from 0.1π to 0.9π. The frequency is fixed at 20 kHz. For both primary-side and secondary-side MMCs, there are 3 SMs per arm. The PS modulation is employed to regulate arm voltage. Based on various ramping angles, the rms values of measured ac-link voltages and current, arm inductance, and SM capacitance are compared with theoretical values in Fig. 35. The experimental results coincide with theoretical values. However, in the experimental test, when θ_R is 0.9π, the theoretical total inductance is 46.4944 μH, and the leakage inductance of ac-link transformer is 27.78 μH. If fabricating the arm inductors according to theoretical values 9.57 μH (primary side) and 18.01 μH (secondary side), the actual total inductance exceeds the desired inductance. Thus, the actual arm inductance is lower than the theoretical arm inductance.

1) Semiconductor Devices: Fig. 36 compares the measured rms currents of semiconductor devices with those of the simulation model. The estimated loss is compared with the measured loss and simulation result, which are shown in Fig. 36. Based on the increased ramping angle, switching currents are increased, which increases semiconductor losses. The estimated loss coincides with the simulation results. The measured semiconductor losses are higher than the simulation results due to external RC snubber.

2) Capacitors: Fig. 37 shows the loss and volume of selected and implemented capacitors of the experimental prototype based on various ramping angles. The power losses are compared in Fig. 37.

For primary-side capacitors, when θ_R is 0.1π, the number of paralleled capacitors (n_p) is 12, and high ESR leads to high power loss. By increasing θ_R, initially, the n_p is increased to reach a high capacitance, which reduces ESR and the induced loss. By further increasing θ_R, although ESR is reduced, the greatly increased current causes increased loss, and the increased number of capacitors results in increased volume.

For secondary-side MMC, when θ_R is small, film capacitors are selected to construct the low-capacitance SM capacitors. However, although there are fewer series-connected and paralleled capacitors, the volume is still bulky. When increasing θ_R, the high-capacitance SM capacitors are constructed by electrolytic capacitors. The number of series-connected capacitors (n_s) is 2, which increases ESR and the induced loss.

3) Arm Inductors: Based on increased θ_R, although the arm current is increased, the reduced arm inductance requires fewer turns of winding coils and a smaller magnetic core. Hence, the loss of the arm inductor can still be reduced. But, in general, the loss and volume of the arm inductor are not monotonically

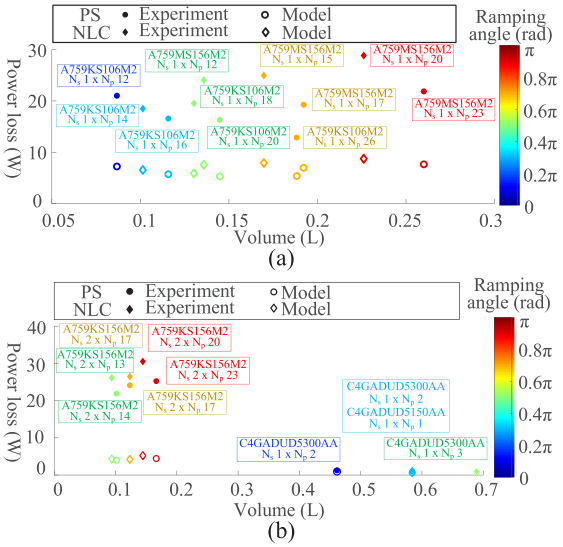


Fig. 37. Volume and power loss of electrolytic and film capacitors of experimental prototype based on various ramping angles. (a) Primary-side MMC. (b) Secondary-side MMC.

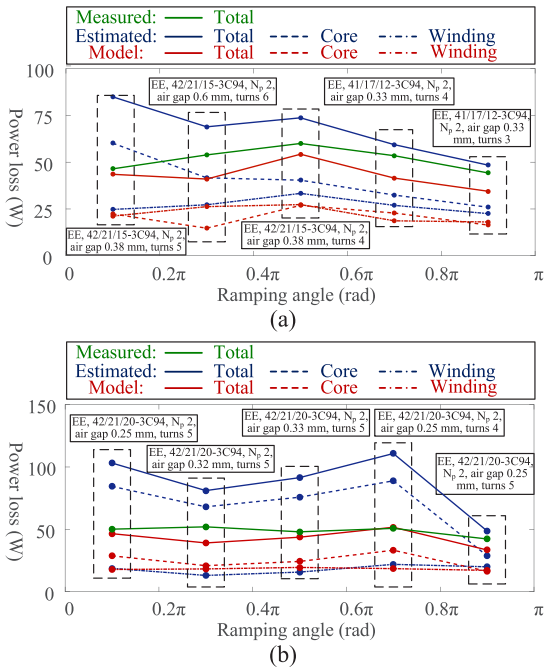


Fig. 38. Inductor volume and power loss of experimental prototype based on various ramping angles. (a) Primary-side MMC. (b) Secondary-side MMC.

influenced by the ramping angle. As shown in Fig. 38, the measured losses are close to the results of the simulation model.

4) Loss and Volume Breakdown: Based on various ramping angles, the loss and volume breakdowns are shown in Fig. 39. The semiconductor loss dominates the total loss, which is greatly increased due to the increased ramping angle. The capacitor volume and heat sink volume dominate the total volume. The capacitor loss is low, which can be neglected. The capacitor volume is increased by increasing ramping angle. The tradeoff between loss and volume can be obtained when θ_{R} is 0.5π.

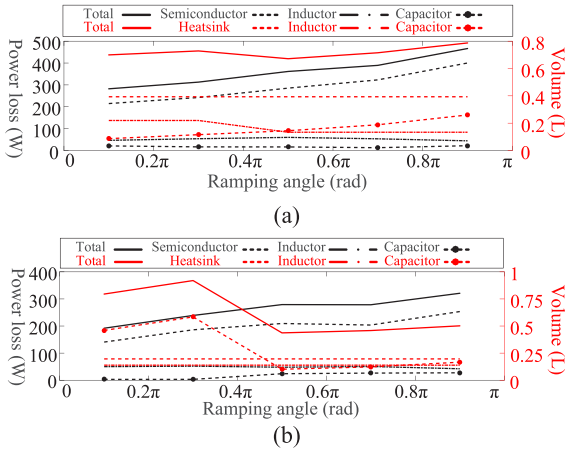


Fig. 39. Breakdown of volume and power loss of experimental prototype based on various ramping angles. (a) Primary-side MMC. (b) Secondary-side MMC.

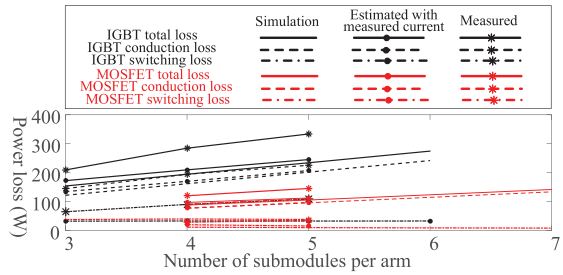


Fig. 40. Semiconductor losses of 650 V IGBTs and 250 V MOSFETs based on various $N_{\mathrm{SM,sec}}$s.

C. Experimental Results Based on Various N_{SM}s

To evaluate the impacts of various N_{SM}s, the θ_R is fixed at 0.5π, and the frequency is fixed at 20 kHz. The $N_{\mathrm{SM,sec}}$ changes from 3 to 5. When $N_{\mathrm{SM,sec}}$ equals 4 and 5, both Si 650 V IGBTs and 250 V MOSFETs are employed in MMC to evaluate semiconductor losses. The 650 V IGBT is FGH40T65UQDF from OnSemi. The 250 V MOSFET is IXFJ80N25X3 from IXYS. When further increases $N_{\mathrm{SM,sec}}$, the low-frequency ripple of capacitor voltage results in low-frequency arm current, which causes saturation of the arm inductor and ac-link transformer. To solve this problem, a bulky inductor should be employed to dc-side, which will definitely lead to higher loss and volume. Thus, the results are not posted in this article.

As show in Fig. 40, compare with 650 V IGBT, the 250 V MOSFET leads to lower loss. By increasing $N_{\mathrm{SM,sec}}$, although the switching loss is slightly reduced, the increased number of semiconductor devices causes higher conduction loss and total loss. In addition, due to the increased number of semiconductor devices, the volume of the associated heat sink is also greatly increased.

Although by increasing $N_{\mathrm{SM,sec}}$, the arm inductance is reduced, the loss and volume are not obviously reduced, as shown in Figs. 41 and 42.

At the same time, the SM capacitance is greatly increased, which increases the total volume of SM capacitors, as shown in Fig. 42. For SM capacitors, initially, when increasing $N_{\mathrm{SM,sec}}$,

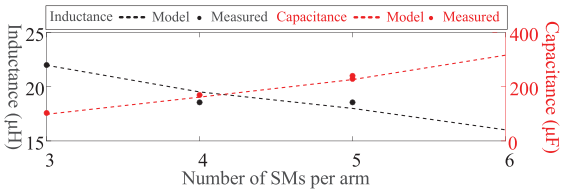


Fig. 41. Arm inductance and capacitance of secondary-side MMC based on various $N_{\mathrm{SM,sec}}$s.

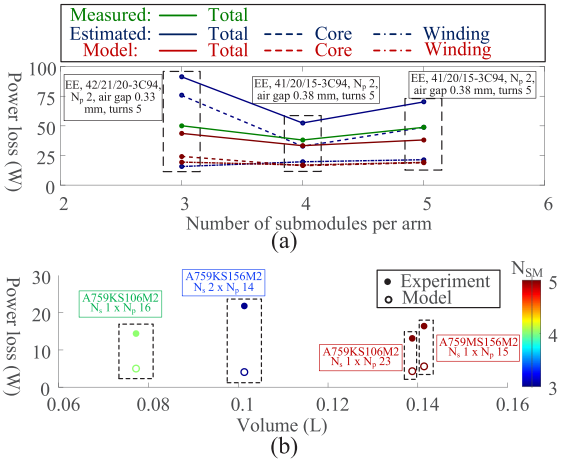


Fig. 42. Arm inductor and capacitors of secondary-side MMC based on various $N_{\mathrm{SM,sec}}$s. (a) Arm inductor loss. (b) Loss and volume.

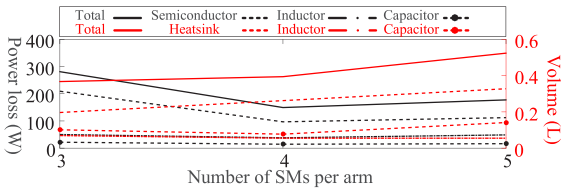


Fig. 43. Volume and loss breakdown of secondary-side MMC based on various $N_{\mathrm{SM,sec}}$s.

the reduced blocking voltage requires less series-connected electrolytic capacitors. Thus, the loss and volume are reduced due to the reduced number of capacitors and reduced ESR. When further increasing $N_{\mathrm{SM,sec}}$, the increased SM capacitance requires more parallel capacitors. Thus, although the reduced ESR leads to reduced loss, the total volume is greatly increased.

Fig. 43 shows the loss and volume breakdown of secondary-side MMC. The heat sink volume and capacitor volume dominate the total volume, which is increased by increasing $N_{\mathrm{SM,sec}}$. The semiconductor loss dominates the total loss of MMC. When $N_{\mathrm{SM,sec}}$ is increased from 3 to 4 and 5, the 650 V IGBTs are replaced by 250 V MOSFETs, which greatly reduces the semiconductor loss.

D. Experimental Results Based on Different Modulations

Different modulation methods are employed to 20 kHz MMC-SST based on various ramping angles. The $N_{\mathrm{SM,pri}}$ and $N_{\mathrm{SM,sec}}$ are fixed at 3. Fig. 44 shows the arm inductances and SM capacitances based on PS modulation and NLC modulation. The NLC

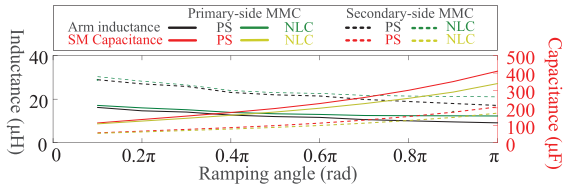


Fig. 44. Arm inductances and SM capacitances of experimental prototype based on different modulation methods.

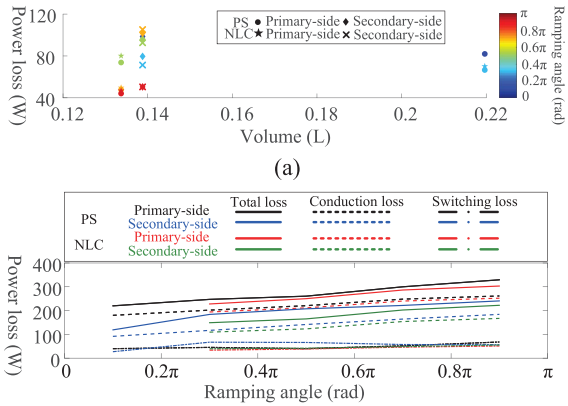


Fig. 45. Volume and loss of arm inductors and semiconductor devices of experimental prototype based on different modulation methods.

modulation results in reduced SM capacitance and increased arm inductance. Based on PS modulation and NLC modulation, the loss and volume of SM capacitors are compared in Fig. 37. Based on NLC modulation, due to the reduced capacitance, the reduced n_p leads to smaller volume while increasing ESR and power loss. The performances of arm inductor and semiconductor devices are not greatly influenced, as shown in Fig. 45.

VII. Discussion

According to the analysis and results of Sections V and VI, the semiconductor loss dominates the total loss of MMC. The capacitor volume and heat sink volume dominate the total volume. The following actions help to reduce the losses and volume of MMCs for SST applications.

A. Increase Operating Frequency

By increasing frequency, the capacitor volume and inductor volume are reduced. However, the increased switching losses of semiconductor devices require a larger heat sink. Thus, there is an optimal frequency, which leads to a tradeoff between losses and the volume of components. For a specific design, the operating frequency can be determined by the computational model.

1) *Capacitor:* The losses of SM capacitors can be neglected. To reduce the volume, the operating frequency should be increased. In this way, the reduced SM capacitance results in a reduced volume of SM capacitor. But, the operating frequency cannot be too high. Initially, when increasing

the operating frequency, the SM capacitor volume is decreased by replacing electrolytic capacitors with film capacitors. When further increasing the operating frequency, the capacitor volume does not obviously reduce.

2) *Semiconductor devices:* Although the increased frequency helps to reduce capacitor volume, the switching losses of semiconductor devices are greatly increased. Hence, the heat sink volume is increased.
3) *Arm inductor:* Although the increased frequency helps to reduce inductor volume, the core losses and winding losses are not greatly reduced or might even be increased.

B. Reduce Ramping Angle of Ac-Link Voltage

By decreasing the ramping angle of ac-link voltage, the ac-link current and arm currents are reduced, which benefits the reduction of semiconductor conduction losses, arm inductor winding losses, capacitor voltage ripple, etc. In this way, the total loss and volume can be reduced. But, the ramping angle cannot be too small to avoid the high *dv/dt* of ac-link voltage.

C. Optimize the Number of Submodules Per Arm

By increasing $N_{\mathrm{SM,sec}}$, the low-voltage semiconductor devices help to reduce switching losses and the required volume of the heat sink. However, the increased SM capacitance leads to increased volume. In addition, the greatly increased component count causes increased total losses and volume of MMC. For a specific design, the optimal $N_{\mathrm{SM,sec}}$ can be determined by the computational model to obtain the tradeoff between total loss and volume.

D. Other Concerns

Compared with the PS modulation, although the NLC modulation helps to reduce the capacitor losses and volume, the total losses and volume of MMC are not obviously affected. In this article, soft switching is not considered, which also helps to reduce the switching losses of semiconductor devices. This can be considered as a possible future work.

VIII. Conclusion

This article developed a methodology for evaluating the loss and volume of MMC-SST under various operating conditions, which is based on the proposed computational model. The developed computational model facilitates the circuit parameter design, components selection, and MMC design. Using the developed methodology, this article comprehensively evaluated the impacts of frequency, waveform of ac-link voltage, number of submodules, and modulation methods. Under various operational conditions, the semiconductor loss dominates the total loss of MMC. The heat sink volume and capacitor volume dominate the total volume. Although reducing frequency helps to reduce the switching loss of semiconductor devices, the total volume is increased due to increased capacitor volume. The tradeoff between total loss and volume should be determined based on various frequencies. Based on various ramping angles, the lower ramping angle leads to the lower loss and smaller volume. Based on various numbers of submodules, initially, the increased number of submodules leads to lower semiconductor loss and smaller heat sink volume. Thus, the total loss and volume is reduced. By further increasing the number of submodules, the increased component count leads to greatly increased total loss and volume. The experimental results also verified the feasibility and effectiveness of the proposed methodology and analysis.

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