An Expandable ZVZCS High Step-Down Interleaved DC–DC Converter

Amin Asghari

***Abstract*—This article introduces a new expandable multiphase interleaved converter. The presented idea can be applied to *K* phases, where *K* is an even number (2, 4, 6, …). In this converter, zero voltage zero current switching (ZVZCS) and zero voltage switching (ZVS) conditions are achieved for the main switches at turn-ON and turn-OFF instants, respectively. The synchronous rectifiers (SRs) and auxiliary switches operate under ZVS conditions. Moreover, the body diodes of SRs turn OFF under zero current switching (ZCS) conditions. This topology employs the series capacitors to improve the voltage gain and clamp the voltage stress of switches. Furthermore, ultrahigh step-down conversions can be achieved by adjusting the turns ratio of coupled windings. In the proposed converter, by utilizing one auxiliary four-quadrant switch for each pair of phases and a new switching algorithm, ZVS and phase interleaving are simultaneously provided, regardless of the number of phases. Although the leakage energy of coupled inductors is used to provide soft switching, the current ripple of the leakage inductor is not reflected in the output current, and uniform current sharing between modules is fully automatic. In addition, by increasing the number of phases, the duty cycle range in which the current sharing is uniform does not shrink. Continuous output current with low ripple and common input and output ground are other important strengths of this converter. The above-mentioned merits are achieved all together without using any extra magnetic core or current sharing control circuit. Also, the number of blocking capacitors is low and equal to the number of phases minus one. The operation principles of the introduced topology are presented and the theoretical analysis is confirmed by two laboratory prototypes.**

***Index Terms*—Automatic uniform current sharing, extended duty cycle, interleaved converters, zero current switching (ZCS), zero voltage switching (ZVS).**

I. Introduction

OVER the last couple of decades, the demand for high step-down converters with large output current has grown in various applications [1]. Some of these industrial applications are telecommunication power systems, electric vehicles, light-emitting diode drivers, and unidirectional chargers. Increasing the switching frequency is one of the main objectives in the design of dc–dc converters. This is a suitable method to achieve high power density and to improve the dynamic response. However, high switching frequency causes high switching loss and electromagnetic interference (EMI). Soft switching is an attractive solution to overcome the mentioned conflicts. Among the soft switching techniques, zero voltage switching (ZVS) is more efficient for metal–oxide–semiconductor field-effect transistors (MOSFETs). By providing zero voltage zero current switching (ZVZCS) condition at turn-ON instants, the voltage of the element decreases to zero just before its current increases. Furthermore, the rate of current change is restricted, and the current of the element gradually increases. As a result, the turn-ON switching loss and the capacitive turn-ON loss are eliminated. In addition, EMI decreases owing to the reduction of switching *dv/dt* and *di/dt*. In the *LLC* resonant converters, soft switching conditions can be achieved for the semiconductor elements. Nonetheless, a large turns ratio of the transformer is usually required to provide a high step-down conversion ratio. A higher peak and root-mean-square (RMS) value of sinusoidal current compared with square wave current is another difficulty with resonant converters [2], [3], [4], [5], [6], [7], [8], [9], [10]. The multiphase interleaved converters with extended duty cycle are appropriate candidates for step-down conversions. These converters can provide relatively high currents with low ripples as well as high step-down conversion ratios. The multiphase topologies proposed in [11], [12], and [13] employ the switched capacitor technique to increase the operating duty cycle. A two-phase series capacitor dual-path hybrid dc–dc converter with a step-down ratio of less than 1/6 is presented in [14]. Nevertheless, the switches of the mentioned topologies operate under hard switching conditions. In the converters introduced in [15] and [16], the step-down conversion ratio is improved, but the input and output grounds are separated. Moreover, the hard switching difficulty still remains. Two high step-down converters with soft switching are presented in [17] and [18]. In these converters, the voltage gain is a function of both duty cycle and the number of cells. Therefore, the number of cells must be increased in the ultrahigh step-down applications. A soft switching topology with dual coupled inductors is proposed in [19]. This converter provides high step-up conversions. Combining coupled inductor and series capacitor techniques is a viable option for improving the voltage gain [20], [21], [22], [23], [24], [25]. In [20] and [21], Two ultrahigh step-down converters are introduced. The switches of the mentioned topologies turn ON under zero current switching (ZCS) and turn OFF under hard switching conditions. The topologies introduced in [26] and [27] utilize energy-transferring capacitors and coupled inductors simultaneously. In [22], [23], [24], [25], [26], and [27], the ZVS condition is provided for the switches. However, in [22], [23],

Manuscript received 10 March 2023; revised 21 July 2023; accepted 2 September 2023. Date of publication 8 September 2023; date of current version 23 October 2023. Recommended for publication by Associate Editor D. Dong.

The author is with the Department of Electrical and Computer Engineering, Semnan University, Semnan 35131-19111, Iran (e-mail: a.asghari@semnan.ac.ir).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3313187.

Digital Object Identifier 10.1109/TPEL.2023.3313187

and [26], the currents of phases can be unbalanced owing to using the complementary pulses for the switches. The two-phase topology proposed in [25] requires four capacitors and five magnetic cores. An ultrahigh step-down converter based on coupled inductor and switched-capacitor methods is presented in [28]. Nonetheless, in [24] and [28], the output current ripple is medium. Two new converters with improved voltage conversion ratios are introduced in [29]. Hard switching and separated input and output grounds are the main drawbacks of these converters.

In this article, a new soft switching converter with ultrahigh step-down conversion ratio is presented. The proposed topology along with the applied switching algorithm overcomes all the aforementioned difficulties. In the proposed converter, coupled inductors and series capacitors are simultaneously employed to extend the operating duty cycle. The leakage energy of the coupled inductors is absorbed without imposing extra voltage stress on the switches. Owing to the charge balance principle of capacitors, uniform current sharing between interleaved modules is provided without an extra current sharing control circuit. The main switches are turned ON under ZVZCS condition and turned OFF under ZVS. Also, the ZVS condition is provided for the auxiliary switches and SRs. In addition, the body diodes of SRs turn OFF under ZCS condition. In this topology, the impact of each phase current ripple on the output current ripple is significantly reduced by the other phases. The input shares the ground with the output, and the number of phases can be changed. The duty cycle is extremely extended without using any extra magnetic core. The point is that the introduced converter provides above-mentioned merits all together. The operation of the proposed converter is explained in Section II. Section III focuses on the small-signal modeling. Section IV offers the design considerations and converter characteristics. The performance comparison and loss analysis are presented in Section V. Section VI focuses on the control scheme. Finally, the experimental results and drawn conclusions of this article are respectively provided in Sections VII and VIII.

II. Topology Description and Principles of Operation

The multiphase converter proposed in this article is shown in Fig. 1. The number of phases can be any even number (2, 4, 6, …). The proposed K-phase converter consists of main switches S_1, S_2, …, S_{K-1} and S_K, synchronous rectifiers SR_1, SR_2, …, SR_{K-1} and SR_K, auxiliary four-quadrant switches S_{a1}, …, $S_{aK/2}$, blocking capacitors C_1, C_2, …, C_{K-1}, snubber capacitors C_{S1}, …, $C_{SK/2}$, output capacitor C_o, and output inductors L_1, L_2, …, L_{K-1} and L_K. Inductors L_{a1}, L_{a2}, …, $L_{a(K-1)}$ and L_{aK} are, respectively, coupled with L_1, L_2, …, L_{K-1} and L_K. As shown in Fig. 1(b), each pair of coupled inductors can be modeled as an ideal transformer, a magnetizing inductance L_{mi}, and a leakage inductance L_{lki}. The turns ratio of coupled windings is equal to n. This converter operates in the continuous conduction mode. In order to simplify the analysis, the following assumptions are considered.

1) All the semiconductor and passive elements are ideal.

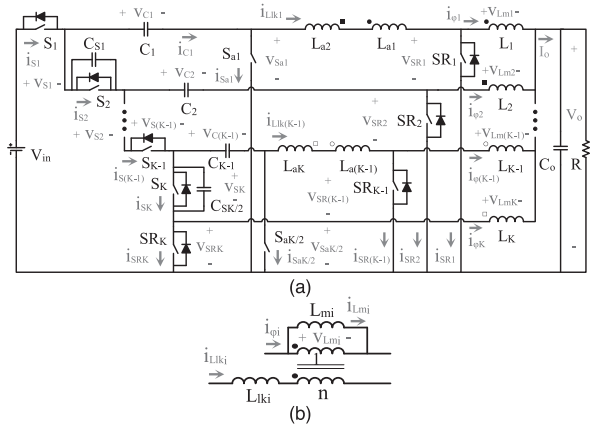

Fig. 1. Proposed K-phase dc–dc converter. (a) Circuit diagram. (b) Equivalent circuit of the coupled inductors in each phase.

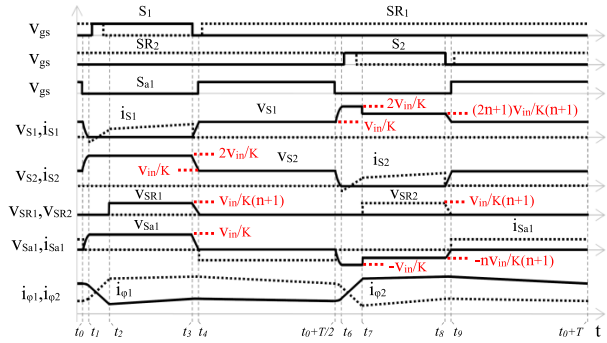

Fig. 2. Key theoretical waveforms over one switching period.

2) The drain–source capacitors of switches are ignored due to their negligible values compared with the values of snubber capacitors.
3) The input and output voltages are constant in a switching cycle.
4) The blocking capacitors are large enough and their voltages are almost constant.
5) The current ripple of magnetizing inductances is ignored.

In the proposed converter, the main switches are driven in the following order: S_1, S_3, …, S_{K-1}, S_2, S_4, …, S_K. If the drive signals of the main switches do not overlap, the maximum duty cycle is equal to $1/K$. In the applied switching algorithm, the drive signals of S_1, S_3, …, S_{K-1} can overlap. The drive signals of S_2, S_4, …, S_K can overlap too. In this case, the maximum duty cycle is 0.5. In this section, the operation of the first couple of phases is analyzed. The other phases operate in the similar way due to the symmetry between the phases. The theoretical waveforms are depicted in Fig. 2. Before the first interval, the main switches are OFF, and the other ones are ON. In this situation, the current of L_{lk1} and the voltage of S_1 are

$$i_{L_{lk1}}(t) = -\frac{I_{L_{m2}}}{n+1}, \quad v_{S_1}(t) = V_{in} - V_{C_1}. \tag{1}$$

Interval 1 ($t_0 < t \le t_1$) [see Fig. 3(a)]: The first interval begins by turning S_{a1} OFF. The capacitor C_{S1} charges through

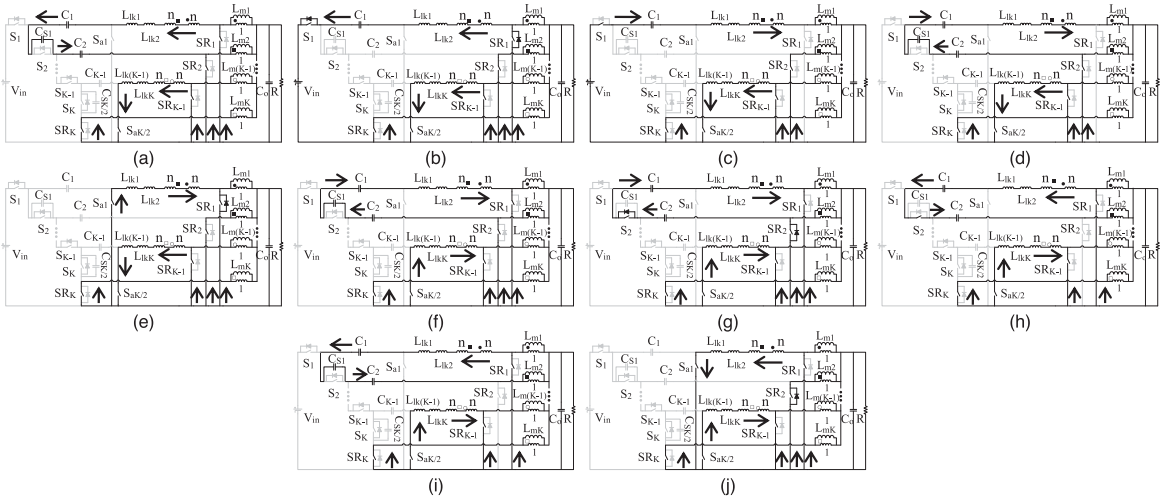

Fig. 3. Equivalent circuit of the proposed dc–dc converter during each operating interval. (a) $[t_0 - t_1]$. (b) $[t_1 - t_2]$. (c) $[t_2 - t_3]$. (d) $[t_3 - t_4]$. (e) $[t_4 - t_0 + T/2]$. (f) $[t_0 + T/2 - t_6]$. (g) $[t_6 - t_7]$. (h) $[t_7 - t_8]$. (i) $[t_8 - t_9]$. (j) $[t_9 - t_0 + T]$.

a resonance with $L_{\rm lk1}$ and $L_{\rm lk2}$, and its voltage increases to $V_{\rm in}$-V_{C2}. Simultaneously, the voltage of S_1 decreases to zero and the voltage across S_{a1} increases to $V_{\rm in}$-V_{C1}. Consequently, the auxiliary switch S_{a1} is turned OFF under ZVS. In this interval, the $L_{\rm lk1}$ current and S_1 voltage expressions are obtained as

$$i_{L_{\rm lk1}}(t) = -\frac{I_{L_{m2}}}{n+1}\cos\omega_0(t-t_0),\quad \omega_0 = \frac{1}{\sqrt{(L_{\rm lk1}+L_{\rm lk2})\,C_{\rm S1}}} \tag{2}$$

$$v_{\rm S_1}(t) = V_{\rm in} - V_{C_1} - \frac{\omega_0 I_{L_{m2}}\,(L_{\rm lk1}+L_{\rm lk2})}{n+1}\sin\omega_0(t-t_0). \tag{3}$$

Based on (3), the duration of this interval is

$$t_1 - t_0 = \frac{1}{\omega_0}\sin^{-1}\frac{(n+1)\,(V_{\rm in}-V_{C_1})}{\omega_0 I_{L_{m2}}\,(L_{\rm lk1}+L_{\rm lk2})}. \tag{4}$$

Interval 2 $(t_1 < t \le t_2)$ [see Fig. 3(b)]: The body diode of S_1 is turned ON at the beginning of the second interval. As a result, the ZVS condition is provided for turning S_1 ON. Also, SR_1 is turned OFF under ZVS because its body diode conducts after the turn-OFF instant. During this interval, the current of $L_{\rm lk1}$ is

$$i_{L_{\rm lk1}}(t) = \frac{V_{\rm in}-V_{C_1}}{L_{\rm lk1}+L_{\rm lk2}}\,(t-t_1) - \frac{G}{n+1} \tag{5}$$

where

$$G = \sqrt{I_{L_{m2}}^2 - \frac{(n+1)^2(V_{\rm in}-V_{C_1})^2 C_{\rm S1}}{L_{\rm lk1}+L_{\rm lk2}}}. \tag{6}$$

The second interval ends when the current of $L_{\rm lk1}$ reaches $I_{Lm1}/(n+1)$. From (5), the duration of this interval is

$$t_2 - t_1 = \frac{(L_{\rm lk1}+L_{\rm lk2})\,(I_{L_{m1}}+G)}{(n+1)\,(V_{\rm in}-V_{C_1})}. \tag{7}$$

Interval 3 $(t_2 < t \le t_3)$ [see Fig. 3(c)]: At t_2, the body diode of SR_1 is turned OFF under ZCS. During the third interval, S_1 is ON, L_{m1} and C_1 are charged, and the power is delivered to the load. From Fig. 3(c), by applying the KVL principle, the following voltage expressions are derived:

$$v_{\rm S_2}(t) = V_{\rm in} - V_{C_2},\ v_{\rm S_{a1}}(t) = V_{\rm in} - V_{C_1},\quad v_{L_{m2}}(t) = -V_o$$
$$v_{L_{m1}}(t) = \frac{V_{\rm in}-V_{C_1}}{n+1} - V_o,\quad v_{\rm SR_1}(t) = \frac{V_{\rm in}-V_{C_1}}{n+1}. \tag{8}$$

Interval 4 $(t_3 < t \le t_4)$ [see Fig. 3(d)]: The switch S_1 is turned OFF under ZVS at the beginning of the fourth interval. $C_{\rm S1}$ is discharged, and the voltages across SR_1 and S_{a1} decrease to zero. In this interval, the voltages of S_1 and S_{a1} are

$$v_{\rm S_1}(t) = \frac{I_{L_{m1}}}{(n+1)\,C_{\rm S1}}\,(t-t_3) \tag{9}$$

$$v_{\rm S_{a1}}(t) = V_{\rm in} - V_{C_1} - \frac{I_{L_{m1}}}{(n+1)\,C_{\rm S1}}\,(t-t_3). \tag{10}$$

Based on (10), the duration of this interval is

$$t_4 - t_3 = \frac{(n+1)\,C_{\rm S1}\,(V_{\rm in}-V_{C_1})}{I_{L_{m1}}}. \tag{11}$$

Interval 5 $(t_4 < t \le t_0 + T/2)$ [see Fig. 3(e)]: The voltages across SR_1 and S_{a1} reach zero at t_4. As a result, the ZVS condition is provided for turning ON SR_1 and S_{a1}. In the fifth interval, S_1 and S_2 are OFF, while S_{a1}, SR_1, and SR_2 are ON. The current of $L_{\rm lk1}$ is equal to $I_{Lm1}/(n+1)$. From Fig. 3(e), by applying the KVL principle, the following voltage expressions are derived:

$$v_{\rm S_1}(t) = V_{\rm in} - V_{C_1},\quad v_{\rm S_2}(t) = V_{C_1} - V_{C_2},$$
$$v_{L_{m1}}(t) = v_{L_{m2}}(t) = -V_o. \tag{12}$$

Interval 6 $(t_0 + T/2 < t \le t_6)$ [see Fig. 3(f)]: The sixth interval begins by turning S_{a1} OFF. The capacitor $C_{\rm S1}$ is discharged, and the voltages across S_1, S_2, and S_{a1} reach $V_{\rm in}$-V_{C2}, 0 and V_{C2}-V_{C1}, respectively. In this interval, $L_{\rm lk1}$ current and S_2 voltage expressions are obtained as

$$i_{L_{\rm lk1}}(t) = \frac{I_{L_{m1}}}{n+1}\cos\omega_0\left(t - t_0 - \frac{T}{2}\right) \tag{13}$$

$$v_{S_2}(t)=V_{C_1}-V_{C_2}-\frac{\omega_0 I_{L_{m1}}\left(L_{lk1}+L_{lk2}\right)}{n+1}\times \sin\omega_0\left(t-t_0-\frac{T}{2}\right). \quad (14)$$

From (14), the duration of this interval is

$$t_6-t_0-\frac{T}{2}=\frac{1}{\omega_0}\sin^{-1}\frac{(n+1)\left(V_{C_1}-V_{C_2}\right)}{\omega_0 I_{L_{m1}}\left(L_{lk1}+L_{lk2}\right)}. \quad (15)$$

Interval 7 ($t_6 < t \le t_7$) [see Fig. 3(g)]: The body diode of S_2 is turned ON at the beginning of the seventh interval. As a result, the ZVS condition is provided for turning S_2 ON. Also, SR_2 is turned OFF under ZVS because its body diode conducts after turn-OFF instants. During this interval, the current of L_{lk1} is

$$i_{L_{lk1}}(t)=-\frac{V_{C_1}-V_{C_2}}{L_{lk1}+L_{lk2}}(t-t_6)+\frac{H}{n+1} \quad (16)$$

where

$$H=\sqrt{I_{L_{m1}}^2-\frac{(n+1)^2(V_{C_1}-V_{C_2})^2 C_{S1}}{L_{lk1}+L_{lk2}}}. \quad (17)$$

The seventh interval ends when the current of L_{lk1} reaches $-I_{Lm2}/(n+1)$. Based on (16), the duration of this interval is

$$t_7-t_6=\frac{\left(L_{lk1}+L_{lk2}\right)\left(I_{L_{m2}}+H\right)}{(n+1)\left(V_{C_1}-V_{C_2}\right)}. \quad (18)$$

Interval 8 ($t_7 < t \le t_8$) [see Fig. 3(h)]: At t_7, the body diode of SR_2 is turned OFF under ZCS. During the eighth interval, S_2 is ON, C_1 is discharged, L_{m2} and C_2 are charged, and the power is delivered to the load. From Fig. 3(h), by applying the KVL principle, the following voltage expressions are derived:

$$v_{S_1}(t)=V_{in}-V_{C_2}-\frac{V_{C_1}-V_{C_2}}{n+1},\quad v_{S_{a1}}(t)=-n\frac{V_{C_1}-V_{C_2}}{n+1}$$
$$v_{L_{m2}}(t)=\frac{V_{C_1}-V_{C_2}}{n+1}-V_o,\quad v_{SR_2}(t)=\frac{V_{C_1}-V_{C_2}}{n+1}. \quad (19)$$

Interval 9 ($t_8 < t \le t_9$) [see Fig. 3(i)]: The switch S_2 is turned OFF under ZVS at the beginning of the ninth interval. C_{S1} is charged, and the voltage across S_{a1} decreases to zero. In this interval, the voltage expressions of S_2 and S_{a1} are obtained as

$$v_{S_2}(t)=\frac{I_{L_{m2}}}{(n+1)C_{S1}}(t-t_8) \quad (20)$$

$$v_{S_{a1}}(t)=n\frac{V_{C_2}-V_{C_1}}{n+1}+\frac{nI_{L_{m2}}}{(n+1)^2 C_{S1}}(t-t_8). \quad (21)$$

From (21), the duration of this interval is

$$t_9-t_8=\frac{(n+1)C_{S1}\left(V_{C_1}-V_{C_2}\right)}{I_{L_{m2}}}. \quad (22)$$

Interval 10 ($t_9 < t \le t_0+T$) [see Fig. 3(j)]: The voltages across SR_2 and S_{a1} reach zero at t_9. As a result, the ZVS condition is provided for turning ON SR_2 and S_{a1}. In the tenth interval, S_1 and S_2 are OFF, while S_{a1}, SR_1, and SR_2 are ON. The current of L_{lk1} is equal to $-I_{Lm2}/(n+1)$. From Fig. 3(j), by applying the KVL principle, the following voltage expressions are derived:

$$v_{S_1}(t)=V_{in}-V_{C_1},\quad v_{S_2}(t)=V_{C_1}-V_{C_2},$$
$$v_{L_{m1}}(t)=v_{L_{m2}}(t)=-V_o. \quad (23)$$

III. Small-Signal Modeling

In this section, the state-space averaging technique is employed to model the proposed converter. All components are assumed ideal, and the leakage inductances are ignored. The currents of inductors L_{m1}, L_{m2}, …, L_{mK} and the voltages of capacitors C_1, C_2, …, C_{K-1} and C_o are the state variables of the proposed converter. Therefore, the state vector x, input vector u, and output vector y are defined as follows:

$$x=\left[i_{L_{m1}}\quad i_{L_{m2}}\quad \dots\quad i_{L_{mK}}\quad v_{C_1}\quad v_{C_2}\quad \dots\quad v_{C_{K-1}}\quad v_{C_o}\right]^{\mathrm{T}},$$
$$u=\left[v_{in}\right],\quad y=\left[v_o\right] \quad (24)$$

where $(\blacksquare)^{\mathrm{T}}$ denotes transpose. The state equations are obtained from the equivalent circuits of operating intervals. By averaging the state equations over a switching cycle, the average state-space equations of the proposed converter can be expressed as

$$\begin{cases}\dot{x}=Ax+Bu\\ y=Ex+Fu\end{cases}. \quad (25)$$

In the above equations, matrix A is (26), as shown at the bottom of the next page. Also, matrices B, E, and F are

$$B=\left[\begin{array}{cccccccccc}\frac{d}{(n+1)L_{m1}} & 0 & \dots & 0 & 0 & 0 & \dots & 0 & 0\end{array}\right]^T,$$
$$E=\left[\begin{array}{cccccccccc}0 & 0 & \dots & 0 & 0 & 0 & \dots & 0 & 1\end{array}\right],\quad F=[0] \quad (27)$$

where d is the duty cycle of the main switches, and the dimensions of A, B, and E are $2K \times 2K$, $2K \times 1$, and $1 \times 2K$, respectively. In order to derive the small-signal model, small perturbations are superimposed onto the state variables, input voltage, output voltage, and duty cycle as follows: $x = X + \hat{x}$, $v_{in} = V_{in} + \hat{v}_{in}$, $v_o = V_o + \hat{v}_o$, and $d = D + \hat{d}$, where $\hat{x}$, $\hat{v}_{in}$, $\hat{v}_o$, and $\hat{d}$ are the corresponding small-signal values. Also, X, V_{in}, V_o, and D are the steady-state values. By substituting these into (25), and ignoring the steady-state terms and second-order small-signal terms, the small-signal state equations of the proposed converter are obtained as

$$\begin{cases}\dot{\hat{x}}=A'\hat{x}+B'\hat{u}+Q\hat{d}\\ \hat{y}=E\hat{x}+F\hat{u}\end{cases} \quad (28)$$

where (29), shown at the bottom of the next page.

The dimension of Q is $2K \times 1$. Also, by replacing variable d with D in matrices A and B, matrices A' and B' are obtained. Finally, by applying the Laplace transformation to (28), the control-to-output transfer function is calculated as

$$\left.\frac{\hat{v}_o(S)}{\hat{d}(S)}\right|_{\hat{u}(s)=o}=E(SI-A')^{-1}Q \quad (30)$$

where I is the $2K \times 2K$ identity matrix.

According to the specifications of 48-to-1.2 V laboratory prototype presented in Section VII, the control-to-output transfer function is obtained as follows:

$$\left.\frac{\hat{v}_o(S)}{\hat{d}(S)}\right|_{\hat{v}_{in}(s)=o}=\frac{6}{1+6.67\times10^{-5}S+2\times10^{-9}S^2}. \quad (31)$$

IV. Design Considerations and Converter Characteristics

A. Converter Voltage Gain

According to Section II, the main switch S_1 is turned ON at the beginning of interval 2, and turned OFF at the end of interval 3. Therefore, the duty cycle of S_1 is

$$D = \frac{t_3 - t_1}{T} \tag{32}$$

where T is the switching period. By ignoring the change of L_{lk1} current in the first interval due to its negligible value, based on (7) and (32), the duration of the third interval is

$$t_3 - t_2 = \frac{D}{f} - \frac{I_{L_{m1}}\left(L_{lk1} + L_{lk2}\right)}{(n+1)\left(V_{in} - V_{C_1}\right)} - \frac{I_{L_{m2}}\left(L_{lk1} + L_{lk2}\right)}{(n+1)\left(V_{in} - V_{C_1}\right)} \tag{33}$$

where f is the switching frequency. In the third interval, from (8), the voltage across L_{m1} is equal to $(V_{in} - V_{C1})/(n+1) - V_o$. The fourth interval is ignored due to its very small duration. The voltage of L_{m1} during other intervals is $-V_o$. As a result, by applying the principle of inductor volt-second balance to L_{m1}, the following equation is derived:

$$\left(D - \frac{f\left(L_{lk1}+L_{lk2}\right)\left(I_{L_{m1}}+I_{L_{m2}}\right)}{(n+1)\left(V_{in}-V_{C_1}\right)}\right)\left(\frac{V_{in}-V_{C_1}}{n+1}\right) - V_o = 0. \tag{34}$$

Similarly, the following equations are obtained by applying the principle of volt-second balance to L_{mi}.

$$\left(D - \frac{f\left(L_{lk(i-1)}+L_{lki}\right)\left(I_{L_{m(i-1)}}+I_{L_{mi}}\right)}{(n+1)\left(V_{C_{i-1}}-V_{C_i}\right)}\right)\left(\frac{V_{C_{i-1}}-V_{C_i}}{n+1}\right) - V_o = 0,$$
$$i = 2, 4, \ldots, K-2 \tag{35}$$

$$\left(D - \frac{f\left(L_{lki}+L_{lk(i+1)}\right)\left(I_{L_{mi}}+I_{L_{m(i+1)}}\right)}{(n+1)\left(V_{C_{i-1}}-V_{C_i}\right)}\right)\left(\frac{V_{C_{i-1}}-V_{C_i}}{n+1}\right) - V_o = 0,$$
$$i = 3, 5, \ldots, K-1 \tag{36}$$

$$\left(D - \frac{f\left(L_{lk(i-1)}+L_{lki}\right)\left(I_{L_{m(i-1)}}+I_{L_{mi}}\right)}{(n+1)V_{C_{i-1}}}\right)\left(\frac{V_{C_{i-1}}}{n+1}\right) - V_o = 0,$$
$$i = K. \tag{37}$$

In the two-phase structure of the proposed topology, K is 2, and thus, (37) is rewritten as

$$\left(D - \frac{f\left(L_{lk1}+L_{lk2}\right)\left(I_{L_{m1}}+I_{L_{m2}}\right)}{(n+1)V_{C_1}}\right)\left(\frac{V_{C_1}}{n+1}\right) - V_o = 0. \tag{38}$$

According to (34) and (38), the voltage of C_1 is

$$V_{C_1} = \frac{V_{in}}{2} = \frac{f\left(I_{L_{m1}}+I_{L_{m2}}\right)\left(L_{lk1}+L_{lk2}\right) + (n+1)^2 V_o}{(n+1)D}. \tag{39}$$

By substituting $I_o/2$ for I_{Lm1} and I_{Lm2} (which is discussed in Section IV-B), the above equation is rewritten as

$$V_{in} = \frac{2I_o f\left(L_{lk1}+L_{lk2}\right) + 2(n+1)^2 V_o}{(n+1)D}$$
$$\Rightarrow V_{in} = \frac{2V_o f\left(L_{lk1}+L_{lk2}\right) + 2(n+1)^2 R V_o}{(n+1)DR} \tag{40}$$

where R is the output impedance. Consequently, based on (40), the voltage gain of the two-phase structure of the proposed topology is

$$\frac{V_o}{V_{in}} = \frac{(n+1)DR}{2f\left(L_{lk1}+L_{lk2}\right) + 2(n+1)^2 R}. \tag{41}$$

If the values of leakage inductances are negligible, the voltage gain of the proposed two-phase converter can be expressed as

$$\frac{V_o}{V_{in}} = \frac{D}{2(n+1)}. \tag{42}$$

Likewise, from (34) to (37), the voltage gain of the K-phase converter proposed in this article is obtained as

$$\frac{V_o}{V_{in}} = \frac{D}{K(n+1)}. \tag{43}$$

B. Analysis of Uniform Current Sharing

The current waveform of the blocking capacitor C_1 is illustrated in Fig. 4(a). According to Fig. 3, in the fifth and tenth intervals, the C_1 current is 0. During other intervals, the current of C_1 is equal to the L_{lk1} current. Therefore, based on (2), (4), (5), (7), (11), (13), (15), (16), (18), and (22), the area under the C_1 current waveform is computed as

$$A = \begin{bmatrix}
0 & 0 & 0 & \cdots & 0 & 0 & \frac{-d}{(n+1)L_{m1}} & 0 & \cdots & 0 & \frac{-1}{L_{m1}} \\
0 & 0 & 0 & \cdots & 0 & 0 & \frac{d}{(n+1)L_{m2}} & \frac{-d}{(n+1)L_{m2}} & \cdots & 0 & \frac{-1}{L_{m2}} \\
\vdots & \vdots & \vdots & \cdots & \vdots & \vdots & \vdots & \vdots & \cdots & \vdots & \vdots \\
0 & 0 & 0 & \cdots & 0 & 0 & 0 & 0 & \cdots & \frac{d}{(n+1)L_{mK}} & \frac{-1}{L_{mK}} \\
\frac{d}{(n+1)C_1} & \frac{-d}{(n+1)C_1} & 0 & \cdots & 0 & 0 & 0 & 0 & \cdots & 0 & 0 \\
0 & \frac{d}{(n+1)C_2} & \frac{-d}{(n+1)C_2} & \cdots & 0 & 0 & 0 & 0 & \cdots & 0 & 0 \\
\vdots & \vdots & \vdots & \cdots & \vdots & \vdots & \vdots & \vdots & \cdots & \vdots & \vdots \\
0 & 0 & 0 & \cdots & \frac{d}{(n+1)C_{K-1}} & \frac{-d}{(n+1)C_{K-1}} & 0 & 0 & \cdots & 0 & 0 \\
\frac{1}{C_o} & \frac{1}{C_o} & \frac{1}{C_o} & \cdots & \frac{1}{C_o} & \frac{1}{C_o} & 0 & 0 & \cdots & 0 & \frac{-1}{RC_o}
\end{bmatrix} \tag{26}$$

$$Q = \begin{bmatrix} \frac{V_{in}-V_{C_1}}{(n+1)L_{m1}} & \frac{V_{C_1}-V_{C_2}}{(n+1)L_{m2}} & \cdots & \frac{V_{C_{K-1}}}{(n+1)L_{mK}} & \frac{I_{L_{m1}}-I_{L_{m2}}}{(n+1)C_1} & \frac{I_{L_{m2}}-I_{L_{m3}}}{(n+1)C_2} & \cdots & \frac{I_{L_{m(K-1)}}-I_{L_{mK}}}{(n+1)C_{K-1}} & 0 \end{bmatrix}^T. \tag{29}$$

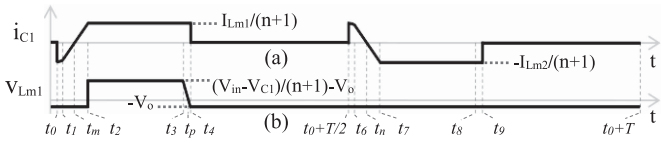

Fig. 4. (a) Current waveform of C_1. (b) Voltage waveform of L_{m1}.

follows:

$$\int_{t_0}^{t_0+T} i_{C_1}(t)dt = \frac{(L_{\rm lk1}+L_{\rm lk2})\left(I_{L_{m1}}^2-G^2\right)}{2(n+1)^2(V_{\rm in}-V_{C_1})} + \frac{I_{L_{m1}}DT}{n+1} - \frac{(L_{\rm lk1}+L_{\rm lk2})\left(I_{L_{m1}}^2+GI_{L_{m1}}\right)}{(n+1)^2(V_{\rm in}-V_{C_1})} + \frac{(L_{\rm lk1}+L_{\rm lk2})\left(H^2-I_{L_{m2}}^2\right)}{2(n+1)^2(V_{C_1}-V_{C_2})} + \frac{(L_{\rm lk1}+L_{\rm lk2})\left(I_{L_{m2}}^2+HI_{L_{m2}}\right)}{(n+1)^2(V_{C_1}-V_{C_2})} - \frac{I_{L_{m2}}DT}{n+1}. \quad (44)$$

By applying the principle of capacitor charge balance to C_1, according to (44), the following equation is derived:

$$\frac{I_{L_{m1}}DT}{n+1} + \frac{(L_{\rm lk1}+L_{\rm lk2})\left(I_{L_{m1}}^2+I_{L_{m2}}^2+2HI_{L_{m2}}\right)}{2(n+1)^2(V_{C_1}-V_{C_2})} + \frac{C_{\rm S1}(V_{\rm in}-V_{C_1})}{2} = \frac{I_{L_{m2}}DT}{n+1} + \frac{(L_{\rm lk1}+L_{\rm lk2})\left(I_{L_{m1}}^2+I_{L_{m2}}^2+2GI_{L_{m1}}\right)}{2(n+1)^2(V_{\rm in}-V_{C_1})} + \frac{C_{\rm S1}(V_{C_1}-V_{C_2})}{2}. \quad (45)$$

Based on (6), (17), (34), and (35), the above equation can be rewritten as

$$DT\left(I_{L_{m1}}-I_{L_{m2}}\right) + \frac{(L_{\rm lk1}+L_{\rm lk2})\left(I_{L_{m2}}\sqrt{I_{L_{m1}}^2-Z}-I_{L_{m1}}\sqrt{I_{L_{m2}}^2-Z}\right)}{(n+1)(V_{\rm in}-V_{C_1})} = 0 \quad (46)$$

where

$$Z = \frac{(n+1)^2(V_{\rm in}-V_{C_1})^2C_{\rm S1}}{L_{\rm lk1}+L_{\rm lk2}}. \quad (47)$$

Equation (46) is not valid unless $I_{Lm1} = I_{Lm2}$. Similarly, by applying the principle of charge balance to C_2, C_3, ..., $C_{K\text{-}1}$, it is derived that $I_{Lm2} = I_{Lm3}$, $I_{Lm3} = I_{Lm4}$, ..., $I_{Lm(K\text{-}1)} = I_{LmK}$. As it is explained in Section IV-F, the sum of the magnetizing inductances currents' is equal to the output current. Consequently, the current of magnetizing inductances is

$$I_{L_{m1}} = I_{L_{m2}} = I_{L_{m3}} = I_{L_{m4}} = \ldots = I_{L_{m(K-1)}} = I_{L_{mK}} = \frac{I_o}{K}. \quad (48)$$

As it is explained in Section II, in the proposed converter, the main switches are driven in the following order: S_1, S_3, ..., $S_{K\text{-}1}$, S_2, S_4, ..., S_K. By utilizing this switching algorithm, the length of time between turning ON the switches of each pair of phases is equal to $0.5T$. Therefore, the above analysis holds for $D<0.5$. As a result, the current sharing is uniform for $D<0.5$, regardless of the number of phases.

C. Calculation of Voltage Stresses

The values of $L_{\rm lk1}+L_{\rm lk2}$, $L_{\rm lk3}+L_{\rm lk4}$, ..., $L_{{\rm lk}(K\text{-}1)}+L_{{\rm lk}K}$ are equal in the symmetrical design of the proposed converter. Therefore, based on (34)–(37) and (48), the voltages of blocking capacitors are

$$V_{C_i} = \frac{(K-i)V_{\rm in}}{K}, \quad i = 1, 2, \ldots, K-1. \quad (49)$$

As shown in Fig. 2, the value of $V_{\rm S1}$ during the seventh interval is the maximum. From Fig. 3(g), by applying the KVL principle, the maximum voltage across S_1 is

$$V_{\rm S_{1max}} = V_{\rm in} - V_{C_2} = \frac{2V_{\rm in}}{K}. \quad (50)$$

Likewise, the maximum voltage across S_2, S_3, ..., S_K is obtained as

$$V_{\rm S_{2max}} = V_{\rm S_{3max}} = \ldots = V_{\rm S_{Kmax}} = \frac{2V_{\rm in}}{K}. \quad (51)$$

From Fig. 3(c), (g), and (h), by applying the KVL principle, the maximum voltages across SR_1, SR_2, and S_{a1} are

$$V_{\rm SR_{1max}} = V_{\rm SR_{2max}} = \frac{V_{\rm in}}{K(n+1)}, \quad V_{\rm S_{a1max}} = \pm\frac{V_{\rm in}}{K}. \quad (52)$$

Similarly, the maximum voltages of the other switches are obtained as

$$V_{\rm SR_{3max}} = \ldots = V_{\rm SR_{k_{max}}} = \frac{V_{\rm in}}{K(n+1)}, \quad V_{\rm S_{a2max}} = \ldots = V_{\rm S_{aK/2max}} = \pm\frac{V_{\rm in}}{K}. \quad (53)$$

From Fig. 3(e) and (j), by applying the KVL principle, the voltage across S_1 and S_2 before turn-ON instants and after turn-OFF instants is $V_{\rm in}/K$. Likewise, the voltage across S_3, S_4, ..., S_K before or after switching instants equals $V_{\rm in}/K$.

D. Calculation of Magnetizing Inductances

The voltage waveform of L_{m1} is illustrated in Fig. 4(b). The area under the L_{m1} voltage waveform from t_p to $T + t_2$ is computed as follows:

$$\int_{t_p}^{T+t_2} v_{L_{m1}}(t)dt = \int_{t_p}^{t_4}\left(\frac{V_{\rm in}-V_{C_1}}{n+1} - V_o - \frac{I_{L_{m1}}(t-t_3)}{(n+1)^2C_{S1}}\right)dt - \int_{t_4}^{T+t_2} V_o dt \Rightarrow \int_{t_p}^{T+t_2} v_{L_{m1}}(t)dt = \frac{(n+1)V_oC_{\rm S1}(V_{\rm in}-V_{C_1})}{I_{L_{m1}}} - \frac{(n+1)^2V_o^2C_{\rm S1}}{2I_{L_{m1}}} - \frac{V_o(1-D)}{f} - \frac{V_o(L_{\rm lk1}+L_{\rm lk2})\left(I_{L_{m1}}+G\right)}{(n+1)(V_{\rm in}-V_{C_1})}. \quad (54)$$

According to [30], to maintain continuous mode operation over the entire load range, L_{m1} can be calculated as

$$L_{m_1} \geq \frac{1}{2I_{L_{m1},\min}} \left(\frac{V_o\,(1-D)}{f} + \frac{(n+1)^2 V_o^2 C_{\mathrm{S1}}}{2I_{L_{m1},n}} + \frac{V_o\,(L_{\mathrm{lk1}}+L_{\mathrm{lk2}})\,(I_{L_{m1},n}+G)}{(n+1)\,(V_{\mathrm{in}}-V_{C_1})} - \frac{(n+1)\,V_o C_{\mathrm{S1}}\left(V_{\mathrm{in}}-V_{C_1}\right)}{I_{L_{m1},n}} \right) \tag{55}$$

where $I_{Lm1,n}$ is the nominal current of L_{m1}. The values of L_{m2}, L_{m3}, …, L_{mK} are computed in a similar way. In the symmetrical design, $L_{\mathrm{lk1}} + L_{\mathrm{lk2}}$, $L_{\mathrm{lk3}} + L_{\mathrm{lk4}}$, …, $L_{\mathrm{lk}(K\text{-}1)} + L_{\mathrm{lk}K}$ are the same. Also, the values of C_{S1}, …, $C_{\mathrm{S}K/2}$ are equal. Accordingly, based on (48) and (49), the magnetizing inductances are designed as

$$L_{m_i} \geq \frac{K}{2I_{o,\min}} \left(\frac{V_o\,(1-D)}{f} + \frac{V_o\,(L_{\mathrm{lk1}}+L_{\mathrm{lk2}})\,(I_{o,n}+KG)}{(n+1)\,V_{\mathrm{in}}} + \frac{(n+1)\,V_o C_{\mathrm{S1}}\,(K\,(n+1)\,V_o - 2V_{\mathrm{in}})}{2I_{o,n}} \right), \quad i = 1,2,\ldots,K \tag{56}$$

where $I_{o,n}$ is the nominal output current.

E. Blocking Capacitors

Based on Fig. 4(a), which is explained in Section IV-B, and (5), (11), (13), (15), (16), (34), and (35), the area under the C_1 current waveform from t_m to t_n is computed as

$$\int_{t_m}^{t_n} i_{C_1}(t)dt = \frac{I_{L_{m1}} D}{(n+1)\,f} + \frac{3C_{\mathrm{S1}}\,(V_{\mathrm{in}}-V_{C_1})}{2} - \frac{G I_{L_{m1}}\,(L_{\mathrm{lk1}}+L_{\mathrm{lk2}})}{(n+1)^2\,(V_{\mathrm{in}}-V_{C_1})}. \tag{57}$$

From the above equation, capacitor C_1 can be calculated as

$$C_1 \geq \frac{1}{\Delta V_{C_1}} \left(\frac{I_{L_{m1}} D}{(n+1)\,f} + \frac{3C_{\mathrm{S1}}\,(V_{\mathrm{in}}-V_{C_1})}{2} - \frac{G I_{L_{m1}}\,(L_{\mathrm{lk1}}+L_{\mathrm{lk2}})}{(n+1)^2\,(V_{\mathrm{in}}-V_{C_1})} \right). \tag{58}$$

The values of C_2, …, $C_{K\text{-}1}$ are computed likewise. In the symmetrical design, $L_{\mathrm{lk1}} + L_{\mathrm{lk2}}$, $L_{\mathrm{lk3}} + L_{\mathrm{lk4}}$, …, $L_{\mathrm{lk}(K\text{-}1)} + L_{\mathrm{lk}K}$ are the same. Also, the values of C_{S1}, …, $C_{\mathrm{S}K/2}$ are equal. Therefore, according to (48) and (49), the blocking capacitors are designed as

$$C_i \geq \frac{1}{\Delta V_{C_i}} \left(\frac{I_o D}{K\,(n+1)\,f} + \frac{3C_{\mathrm{S1}}V_{\mathrm{in}}}{2K} - \frac{G I_o\,(L_{\mathrm{lk1}}+L_{\mathrm{lk2}})}{(n+1)^2 V_{\mathrm{in}}} \right), \quad i = 1,2,\ldots,K-1 \tag{59}$$

where ΔV_{Ci} is the voltage ripple of C_i.

F. Output Current Ripple

From Fig. 1, by applying the KCL principle, the following equations are derived:

$$i_o(t) = i_{\varphi_1}(t) + i_{\varphi_2}(t) + \ldots + i_{\varphi_{K-1}}(t) + i_{\varphi_K}(t) \tag{60}$$

$$i_{\varphi_i}(t) = i_{L_{mi}}(t) - n i_{L_{lki}}(t), \quad i = 1,3,\ldots,K-1.$$

$$i_{\varphi_i}(t) = i_{L_{mi}}(t) + n i_{L_{lk(i-1)}}(t), \quad i = 2,4,\ldots,K. \tag{61}$$

By substituting (61) into (60), the output current is

$$i_o(t) = i_{L_{m1}}(t) + i_{L_{m2}}(t) + \ldots + i_{L_{m(K-1)}}(t) + i_{L_{mK}}(t). \tag{62}$$

According to [30], and based on (48) and (62), the output current ripple of the proposed converter can be calculated as follows:

$$\begin{aligned} |\Delta i_o| &= \left|\Delta i_{L_{m1}} + \Delta i_{L_{m2}} + \ldots + \Delta i_{L_{m(K-1)}} + \Delta i_{L_{mK}}\right| \\ &\Rightarrow |\Delta i_o| \leq \left| \frac{2I_{o,\min}}{K} - \frac{2\,(K-1)\,D I_{o,\min}}{K\,(1-D)} \right| \\ &\Rightarrow \Delta i_o \leq \left| \frac{2\,(1-KD)}{K\,(1-D)} I_{o,\min} \right|. \end{aligned} \tag{63}$$

G. ZVS Criteria for Switches

As it is explained in Section II, the ZVS condition is provided for the SRs owing to the conduction of their body diodes before turn-ON instants and after turn-OFF instants. C_{S1}, …, $C_{\mathrm{S}K/2}$ restrict the rate of voltage change at turn-OFF instant. As a result, the ZVS condition is achieved for the main and auxiliary switches. According to (10) and (21), the voltage of $\mathrm{S_{a1}}$ certainly reaches zero at the end of intervals 4 and 9. Therefore, the auxiliary switch $\mathrm{S_{a1}}$ can be turned ON under the ZVS condition at the beginning of intervals 5 and 10. Similarly, the other auxiliary switches can be turned ON under ZVS conditions. To provide the ZVS condition for turning ON $\mathrm{S_1}$ and $\mathrm{S_2}$, the voltages of $\mathrm{S_1}$ and $\mathrm{S_2}$ must reach zero at the end of the first and sixth intervals, respectively. Consequently, based on (3) and (14), the following inequalities must be satisfied:

$$\begin{aligned} V_{\mathrm{in}} - V_{C_1} &\leq \frac{\omega_0 I_{L_{m2}}\,(L_{\mathrm{lk1}}+L_{\mathrm{lk2}})}{n+1} \\ V_{C_1} - V_{C_2} &\leq \frac{\omega_0 I_{L_{m1}}\,(L_{\mathrm{lk1}}+L_{\mathrm{lk2}})}{n+1}. \end{aligned} \tag{64}$$

By substituting (2), (48), and (49), the above inequalities can be rewritten as

$$C_{\mathrm{S1}} \leq \frac{(L_{\mathrm{lk1}}+L_{\mathrm{lk2}})\,I_o^2}{(n+1)^2 V_{\mathrm{in}}^2}. \tag{65}$$

Likewise, to provide the ZVS condition for turning ON $\mathrm{S_3}$, $\mathrm{S_4}$, …, $\mathrm{S}_{K\text{-}1}$ and S_K, the following inequalities must be satisfied:

$$C_{Si} \leq \frac{\left(L_{\mathrm{lk}(2i-1)} + L_{\mathrm{lk}2i}\right) I_o^2}{(n+1)^2 V_{\mathrm{in}}^2}, \quad i = 2,3,\ldots,\frac{K}{2}. \tag{66}$$

TABLE I
PERFORMANCE COMPARISON BETWEEN THE PROPOSED TWO-PHASE CONVERTER AND ITS RECENT COUNTERPARTS

Characteristics	Proposed converter	[28]	[27]	[25]	[26]	[24]	[23]	[11]	[12]	[29]	[13]
Semiconductor element count	6*	7	4	6	6	6	5	5	5	6	8
No. of capacitors	2	5	4	4	4	4	5	3	4	3	4
No. of mag. cores	2	2	2	5	3	2	3	3	2	2	2
No. of windings	4	4	3	6	4	4	7	3	2	3	2
Voltage gain	$\frac{D}{2(1+n)}$	$\frac{D}{\beta^{**}}$	$\frac{D}{1+n}$	$\frac{D}{2(1+n)}$	$\frac{D(1-D)}{2(1+n)}$	$\frac{D}{2(1+n)}$	$\frac{D(1-D)}{\alpha^{***}}$	$\frac{D}{2-D}$	$\frac{D}{3}$	$\frac{nD}{\gamma^{****}}$	$\frac{D}{5}$
Voltage gain when D=0.2 and n=3	0.025	0.019	0.05	0.025	0.02	0.025	0.036	0.112	0.067	0.097	0.04
V_{in}(V), f_{sw}(KHz)	48, 100	48, 400	48, 50	400, 100	400, 100	48, 400	310, 100	20, 50	48, 500	155, 100	300, 100
V_{out}(V), I_{out}(A)	1.2, 40	1, 30	3.3, 10	12, 37.5	12, 20	3.3, 20	24, 8.34	5, 1.5	1.8, 33.34	24, 8.34	12, 8.34
Efficiency (%)	93.3	81.4	93.6	94.9	93.1	95.2	93.6	96.15	85	94.7	91.5
Inductors (μH)	–	–	24	250, 20	100	–	80	180	0.32	300	100
Magnetizing inductances	3 μH	6.6 μH	176 μH	1500 μH	100 μH	6.6 μH	150 μH	–	–	150 μH	–
Output capacitor (μF)	1000	40	1410	250	220	–	100	330	88	100	–
Blocking capacitors (μF)	100	18.8	60, 40	22	100, 10	20	100, 10	220	4	2	11
Voltage stress on switches (V)	48, 24, 6	32, 16, 9, 8	48, 12	200	200	48, 24, 16	212, 155	12.5	32, 16	135, 68	240, 180, 120, 60
Voltage stress on diodes (V)	–	–	–	100	32	–	90, 33	12.5	–	118, 68	120
Common ground	Yes	Yes	Yes	Yes	Yes	Yes	No	No	No	No	Yes
Automatic uniform current sharing	Yes	–	–	Yes	No	Yes	No	Yes	No	–	No
Output current ripple	Very low	Medium	Low	Very low	Very low	Medium	Very low	Very low	Very low	Low	Very low
Soft switching, turn-on/off	ZVZCS/ZVS	ZVS/No	ZVS/ZVS	ZVZCS/ZVS	ZVS/ZVS	ZVS/No	ZVS/No	No/No	No/No	No/No	No/No

* Two MOSFETs are required to implement the four-quadrant switch. ** $\beta=D(2-D)(2n+1)+2(n+1)$. *** $\alpha=n(D+1)+D(D-1)+1$. **** $\gamma=n(2-D)+1-D$

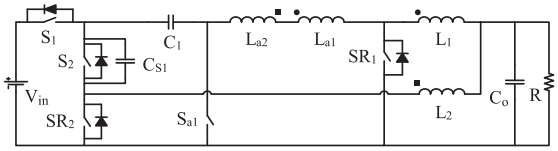

Fig. 5. Circuit diagram of the proposed two-phase dc–dc converter.

By considering the drain–source capacitors of switches, and recalculating the voltages of the main switches, the ZVS condition is provided for the main switches when

$$C_{Si} \le \frac{\left(L_{lk(2i-1)} + L_{lk2i}\right) I_o^2}{(n+1)^2 V_{in}^2} - C_{ds(2i-1)} - C_{ds2i} - C_{dsa_i},$$
$$i = 1, 2, \ldots, \frac{K}{2} \tag{67}$$

where C_{dsi} is the drain–source capacitor of S_i.

V. PERFORMANCE COMPARISON AND LOSS ANALYSIS

A. Performance Comparison

To show the features of the two-phase structure of the proposed topology, its circuit configuration is depicted in Fig. 5. A comparison between the proposed two-phase converter and its recent counterparts is presented in Table I. The converters presented in [11], [12], and [13] suffer from hard switching problems. In addition, the voltage gains of the mentioned converters depend only on the duty cycle. Therefore, the duty cycles of switches would be narrow in the extreme step-down conversions. In the topologies introduced in [11], [12], [23], and [29], there are separated grounds between the input and output ports. Moreover, in [12], [13], and [23], the currents of phases can be unbalanced. In [26], to handle the leakage energy and to provide the ZVS condition, complementary pulses must be applied to the main switches. The duty cycle of S_1 and S_3 is D, and the duty cycle of S_2 and S_4 is 1-D. The switches S_1 and S_3 are turned ON and turned OFF at the same time. The switches S_2 and S_4 are also driven simultaneously. In this topology, the currents of phases can be unbalanced owing to the complementary operation of the main switches. In [24] and [28], the output current ripple is high. The converter proposed in this article provides ZVZCS and ZVS conditions for the main switches at turn-ON and turn-OFF instants, respectively. Also, the auxiliary switches and SRs operate under ZVS conditions. Consequently, the turn-ON switching loss and the capacitive turn-ON loss are eliminated. Owing to ZVS, low voltage, and low current stresses, the turn-OFF switching loss is very low. In addition, the body diodes of SRs turn OFF under ZCS, and the reverse recovery losses are eliminated. In this converter, an ultrahigh step-down conversion can be achieved by a relatively low turns ratio of coupled windings. Therefore, the size and loss of coupled inductors are reduced. In the proposed topology, uniform current sharing between modules is fully automatic, and the output current ripple is low. Furthermore, the number of elements in the proposed two-phase converter is lower than the other ZVS ultrahigh step-down converters with automatic uniform current sharing and low output current ripple. A comparison of voltage gains in the proposed two-phase converter and its recent counterparts, when $n = 3$, is shown in Fig. 6.

By increasing the number of phases, the output current handling capability increases, and the output current ripple decreases. Compared to the conventional multiphase synchronous buck converter (SBC), the topology proposed in this article uses one auxiliary four-quadrant switch, one extra capacitor, and two extra windings for each couple of phases. Therefore, the proposed converter requires only one extra control signal for each pair of phases. Also, this topology does not utilize any extra magnetic core. As a result, the power density and cost of each phase are improved compared with the other ZVS ultrahigh step-down converters with automatic uniform current sharing. In many soft switching interleaved converters, it is not possible to increase the number of phases while maintaining

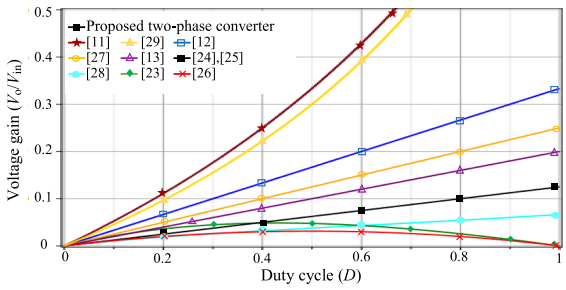

Fig. 6. Comparison of voltage gains in the proposed two-phase converter and its recent counterparts.

the soft switching and the phase interleaving. For instance, in the four-phase structure of the topologies presented in [1], [22], [25], and [26], either soft switching or phase interleaving will be missed. In the mentioned four-phase structures, to achieve the ZVS condition, two phases must simultaneously be in the power transfer mode. In comparison, in the multiphase converter proposed in this article, ZVS and phase interleaving are simultaneously provided, regardless of the number of phases. In this converter, each phase can be in the power transfer mode alone.

In the *LLC* resonant converters, a large turns ratio of the transformer is usually required to provide a high step-down conversion ratio. A higher peak and RMS value of sinusoidal current compared with square wave current is another difficulty with resonant converters. The pulse frequency modulation control is commonly employed in the *LLC* resonant converters [2], [3]. In [4], an *LLC* converter with frequency-adaptive phase-shift modulation control is presented. In [5], the fixed-frequency pulsewidth modulation (PWM) control is employed in a dual-bridge *LLC* resonant converter. The output voltage of the dual-transformer-based *LLC* converter introduced in [6] is regulated through a fixed-frequency phase-shift PWM control scheme. In order to increase the power rating and decrease the elements current stress, two input-parallel output-parallel *LLC* resonant converters are presented in [7] and [8]. Nevertheless, in high step-down applications, the topologies introduced in [2], [3], [4], [5], [6], [7], and [8] suffer from high output current ripple and large transformer turns ratio. In [9], a three-level *LLC* converter with pulsewidth and amplitude modulation control is presented. This topology can achieve a wide voltage gain range, but it has the output current ripple problem. A multiphase *LLC* converter with partial energy processing is introduced in [10]. It uses the phase interleaving technique to reduce current stress and current ripple on the secondary side. In this topology, even though the step-down conversion ratio is improved, a large transformer turns ratio is still required for high step-down applications. In comparison, the converter proposed in this article can provide high step-down conversions, although the turns ratio of coupled windings is low. In this converter, the PWM control strategy is employed, and the switching frequency is fixed. The output current is continuous, and the output current ripple is low. Moreover, the number of components in the two-phase structure of the proposed topology is lower than the converters presented in [2], [3], [4], [5], [6], and [9]. Also, the element count in the four-phase structure of the proposed topology is lower than the converters introduced in [7], [8], and [10].

B. Loss Analysis

In the converter proposed in this article, as discussed in Section V-A, the capacitive turn-ON loss and the switching loss are approximately eliminated. The core losses of inductors are negligible compared with the other losses. The conduction losses of blocking capacitors are computed as

$$P_{C_i} = R_{C_i} D \left(\left(\frac{I_{L_{mi}}}{n+1} \right)^2 + \left(\frac{I_{L_{m(i+1)}}}{n+1} \right)^2 \right) \tag{68}$$

where R_{Ci} is the equivalent series resistance (ESR) of C_i. The conduction losses of inductors are obtained as

$$P_{L_i} = \frac{R_{L_i}}{2} \left(\left(\frac{I_{L_{mi}}}{n+1} \right)^2 + \left(I_{L_{mi}} + \frac{n I_{L_{m(i+1)}}}{n+1} \right)^2 \right), \quad i = 1, 3, \ldots, K-1 \tag{69}$$

$$P_{L_i} = \frac{R_{L_i}}{2} \left(\left(\frac{I_{L_{mi}}}{n+1} \right)^2 + \left(I_{L_{mi}} + \frac{n I_{L_{m(i-1)}}}{n+1} \right)^2 \right), \quad i = 2, 4, \ldots, K \tag{70}$$

$$P_{L_{ai}} = \frac{R_{L_{ai}}}{2} \left(\left(\frac{I_{L_{mi}}}{n+1} \right)^2 + \left(\frac{I_{L_{m(i+1)}}}{n+1} \right)^2 \right), \quad i = 1, 3, \ldots, K-1 \tag{71}$$

$$P_{L_{ai}} = \frac{R_{L_{ai}}}{2} \left(\left(\frac{I_{L_{m(i-1)}}}{n+1} \right)^2 + \left(\frac{I_{L_{mi}}}{n+1} \right)^2 \right), \quad i = 2, 4, \ldots, K \tag{72}$$

where R_{Li} is the winding resistance of L_i. The conduction losses of switches are calculated as follows:

$$P_{S_i} = R_{ds_i} D \left(\frac{I_{L_{mi}}}{n+1} \right)^2 \tag{73}$$

$$P_{S_{ai}} = R_{ds_{ai}} \left(\frac{1}{2} - D \right) \left(\left(\frac{I_{L_{m(2i-1)}}}{n+1} \right)^2 + \left(\frac{I_{L_{m2i}}}{n+1} \right)^2 \right) \tag{74}$$

$$P_{\mathrm{SR}_i} = R_{ds_{\mathrm{SR}i}} \frac{\left(I_{L_{mi}} + I_{L_{m(i+1)}} \right)^2}{2}, \quad i = 1, 3, \ldots, K-1 \tag{75}$$

$$P_{\mathrm{SR}_i} = R_{ds_{\mathrm{SR}i}} \left(\frac{1}{2} - D \right) \left(\left(\frac{n I_{L_{m(i-1)}}}{n+1} + I_{L_{mi}} \right)^2 + \left(\frac{I_{L_{mi}}}{n+1} \right)^2 \right) + R_{ds_{\mathrm{SR}i}} D \left(\frac{n I_{L_{m(i-1)}}}{n+1} + I_{L_{mi}} + \frac{I_{L_{m(i+1)}}}{n+1} \right)^2, \quad i = 2, 4, \ldots, K-2 \tag{76}$$

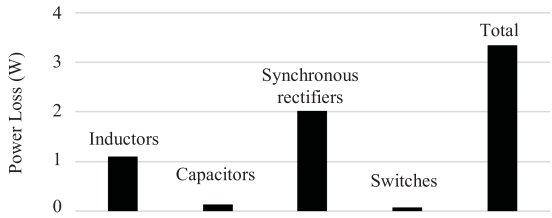

Fig. 7. Results of loss analysis at full load.

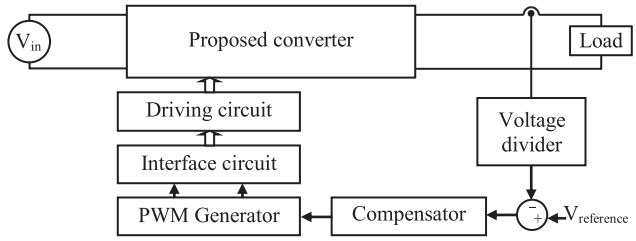

Fig. 8. Block diagram of the closed-loop system for the proposed converter.

$$P_{\mathrm{SR}_K} = R_{ds_{\mathrm{SR}K}} \left(\left(\frac{1}{2} - D \right) \left(\frac{I_{L_{mK}}}{n+1} \right)^2 + \frac{1}{2} \left(\frac{n I_{L_{m(K-1)}}}{n+1} + I_{L_{mK}} \right)^2 \right) \tag{77}$$

where R_{ds} is the drain–source resistance of the switches.

The result of loss analysis at full load, according to the specifications of the two-phase laboratory prototype presented in Section VII, is shown in Fig. 7.

As the number of phases increases, based on (50)–(53), the voltage stress of switches decreases. Also, from (43), the turns ratio of coupled windings can be reduced. In addition, according to (48), the currents of phases decrease. Since the conduction loss is related to the square of the current, the conduction loss is significantly reduced when the current decreases. Furthermore, semiconductor devices with lower ratings are required. Consequently, the loss of each element is considerably reduced. According to the aforementioned, based on the voltage gain, output current, and desirable output current ripple, the number of phases can be selected in such a way that the proper efficiency is achieved.

VI. Control Scheme

The block diagram of the control system for the proposed converter is presented in Fig. 8. According to the specifications of the two-phase laboratory prototype presented in Section VII, the compensator can be designed as follows. To optimize the design of the feedback loop in order to achieve stable overall operation of the system, the first step is to determine the control-to-output transfer function [see (31)]. The second step is to choose the crossover frequency (F_{co}) where the gain is unity. Theoretical limits set the crossover frequency at half of the switching frequency, but from practical experience, less than one-fifth of the switching frequency is used. For this analysis, we choose a crossover frequency of 20 kHz, which is one-fifth the switching frequency. Based on (31), at the chosen crossover frequency of 20 kHz, the loop gain without a compensator is -30.024 dB. Therefore, for an overall loop gain of zero, the compensator gain must be made $+30.024$ dB at 20 kHz. The switching power supply will be stable if the overall loop gain crosses over the 0-dB line at a -1 slope. Since the control-to-output gain of the converter is falling at a -2 slope, the compensator must supply a $+1$ slope at this point for a resulting slope of -1 (-20 dB per decade). The compensator must have sufficient gain at lower frequencies to reject line frequency input ripple. Thus, below the zero frequency (F_z), the compensator gain curve slope must be -1. This is done by providing two zeros at the same frequency (F_z) in the compensator transfer function. Below F_z, the gain falls at a -1 slope because of a pole at the origin which will be provided. At F_z, the first zero turns the gain slope horizontally; the second one turns it to a $+1$ slope. The gain cannot be permitted to continue upward at a $+1$ slope much beyond F_{co}. If it did, the gain would be high at high frequencies, and noise spikes would get through to the output. Thus, two poles are provided at frequency F_p. The first pole turns the $+1$ gain slope horizontally; the second pole turns it to a -1 slope. Locating F_z at too low, a frequency reduces low-frequency gain and prevents sufficient degeneration of line ripple. Placing F_p at too high, a frequency increases gain at high frequencies and permits high-frequency noise spikes to come through at greater amplitude. A K factor is introduced to define the locations of F_z and F_p. This factor is a ratio set to $K = F_{\mathrm{co}}/F_z = F_p/F_{\mathrm{co}}$. According to [30], a K factor of 4 yields the desired phase margin. For $F_{\mathrm{co}} = 20$ kHz and $K = 4$, F_z is 5 kHz, and F_p is 80 kHz. As a result, the transfer function of the employed compensator is

$$G_C(S) = \frac{-\left(1 + 33 \times 10^{-6} S\right)\left(1 + 33.79 \times 10^{-6} S\right)}{4.96 \times 10^{-6} S \left(1 + 1.84 \times 10^{-6} S\right)\left(1 + 1.75 \times 10^{-6} S\right)}. \tag{78}$$

Based on (31) and (78), the compensated closed-loop transfer function is obtained as

$$L(S) = \frac{1}{1 + 6.67 \times 10^{-5} S + 2 \times 10^{-9} S^2} \times \frac{-\left(1+33\times10^{-6}S\right)\left(1+33.79\times10^{-6}S\right)}{4.96\times10^{-6}S\left(1+1.84\times10^{-6}S\right)\left(1+1.75\times10^{-6}S\right)}. \tag{79}$$

The frequency response of the compensated closed-loop transfer function is shown in Fig. 9. In the proposed two-phase converter, S_1 and S_2 are the main switches, and SR_1 and SR_2 are the synchronous rectifiers. There are the mentioned switches in the conventional two-phase SBC too. The proposed topology utilizes one extra four-quadrant switch. As it is discussed in Section VII and shown in Fig. 11, each four-quadrant switch is controlled by one signal. Consequently, the proposed converter requires only one extra control signal. All the required pulses can be generated from the output pulses of one regular PWM controller.

According to Section II, the charging voltages of L_{m1} and L_{m2} are, respectively, equal to $(V_{\mathrm{in}}\text{-}V_{C1})/(n+1)\text{-}V_o$ and $V_{C1}/(n+1)\text{-}V_o$. The discharging voltage of both magnetizing inductances

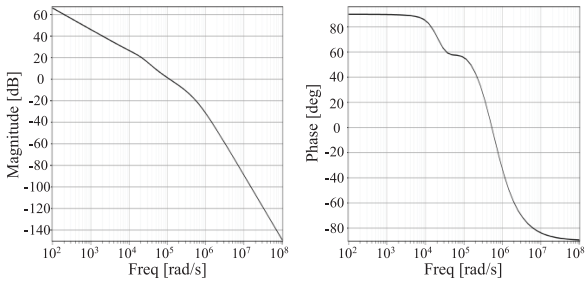

Fig. 9. Frequency response of the compensated closed-loop transfer function.

is $-V_o$. Moreover, the duty cycles of the main switches are equal. If the output voltage or duty cycle changes, the charging and discharging voltages or the charging and discharging durations of both magnetizing inductances change the same. Therefore, the currents of both phases change in the same way and remain balanced. On the other hand, if the phase's currents become unbalanced due to the input voltage change or any other reasons, the voltage of the series capacitor changes in order to balance these currents. For example, based on Fig. 4(a), if I_{Lm1} becomes larger than I_{Lm2}, the voltage of C_1 increases because its charging energy is larger than the discharging energy. In this situation, the charging voltage of L_{m1} decreases, but the charging voltage of L_{m2} increases. As a result, the imbalance between the currents of phases is removed automatically.

VII. Experimental Results

A 48-to-1.2 V laboratory prototype of the two-phase converter proposed in this article is implemented at 100 kHz operating frequency and 40 A output current. The design procedure is as follows. Based on the voltage gain equation and (63), to have a low output current ripple and low turns ratio, the duty cycle is set to 0.2 and n is calculated as 3. If the leakage inductances are ignored due to their negligible values, the magnetizing inductances are obtained from (56) as $L_{mi} \geq 2.4\ \mu$H. Therefore, the values of magnetizing inductances and coupling coefficients are, respectively, selected as 3 μH and 0.98. The ferrite cores of coupled inductors are E 42/21/20 (Series/Type: TDK B66329). The turns ratio of coupled windings is 3, and the turn number of the first winding is set to 3. According to (67), the snubber capacitor is designed as $C_{S1} = 11.2$ nF. Based on (49), the voltage across C_1 is equal to 24 V. By considering $\Delta V_{C1} = 0.24$ V, the blocking capacitor is calculated from (59) as $C_1 \geq 44\ \mu$F. Consequently, a 100 μF low ESR capacitor (radial lead type, series: FR, Type: A) is used as C_1. According to (50)–(52), the maximum voltages across the switches are equal to 48, 24, and 6 V. As a result, IRFP3206PbF with $R_{DS(\text{on})} = 2.4\ \text{m}\Omega$ is used for all the switches. The PWM control IC is UC3825, the data type flip-flop is CD4013BM, and the power MOSFET driver is TC4424. As shown in Fig. 10, each auxiliary four-quadrant switch is realized by connecting two MOSFETs. This four-quadrant switch is controlled by one signal. When this switch is ON, one of the MOSFETs operates in synchronous rectification mode. The specifications of the laboratory prototype are presented in Table II. A photograph of the two-phase

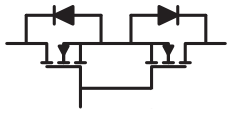

Fig. 10. Implementation of a four-quadrant switch.

TABLE II
Specifications of the Laboratory Prototype

Components	Symbol	Specifications
Input voltage	V_{in}	48 V
Output voltage	V_o	1.2 V
Output current	I_o	40 A
Number of phases	K	2
Switching frequency	f	100 KHz
Blocking capacitor	C_1	100 μF
Magnetizing Inductances	L_{m1}, L_{m2}	3 μH
Coupling Coefficients	K_1, K_2	0.98
Turns ratio	n	3
Snubber capacitor	C_{S1}	2*5.6 nF
Output capacitor	C_o	1000 μF

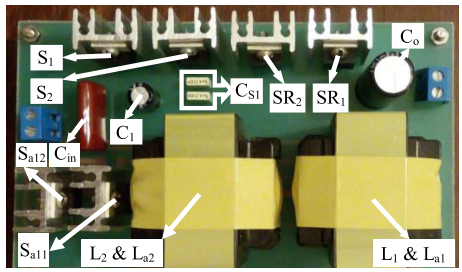

Fig. 11. Laboratory prototype of the proposed two-phase converter.

laboratory prototype is shown in Fig. 11. In this prototype, the auxiliary four-quadrant switch (S_{a1}) is implemented by S_{a11} and S_{a12}. The experimental results are depicted in Fig. 12. As it can be observed, the maximum voltages across the main switches, auxiliary switch, and SRs are, respectively, equal to 48 V, 24 V, and 6 V. The maximum current of all main and auxiliary switches is about 5 A. When the current of SR_1 reaches zero, the body diode of SR_1 turns OFF under ZCS. A resonance happens between L_{lk1}, L_{lk2} and the drain–source capacitor of SR_1. Consequently, as it can be seen in Fig. 12(b), the waveform of V_{SR1} has oscillations, which are damped to 6 V. When the current of SR_2 reaches zero, the body diode of SR_2 turns OFF under ZCS. A resonance happens between L_{lk1}, L_{lk2} and the drain–source capacitors of S_1, SR_2, and S_{a1}. As a result, the waveforms of V_{S1}, V_{SR2}, and V_{Sa1} have oscillations, which are, respectively, damped to 42, 6, and -18 V. From Fig. 12(d), the input voltage is 48 V, and the output voltage measures 1.2 V. The waveforms of i_{in}, i_{out}, $i_{\varphi 1}$, and $i_{\varphi 2}$ are shown in Fig. 12(e). Fig 12(f) illustrates the load-disturbance transition performance from light load (10% of full load) to full load and vice versa. The currents of phases during load transition are shown in Fig. 12(g). As can be observed, the currents of both phases change in the same way and remain balanced. The current and voltage waveforms of switches around switching instants are illustrated in Fig. 12(h)–(l). Fig. 12(h) and (i) shows that

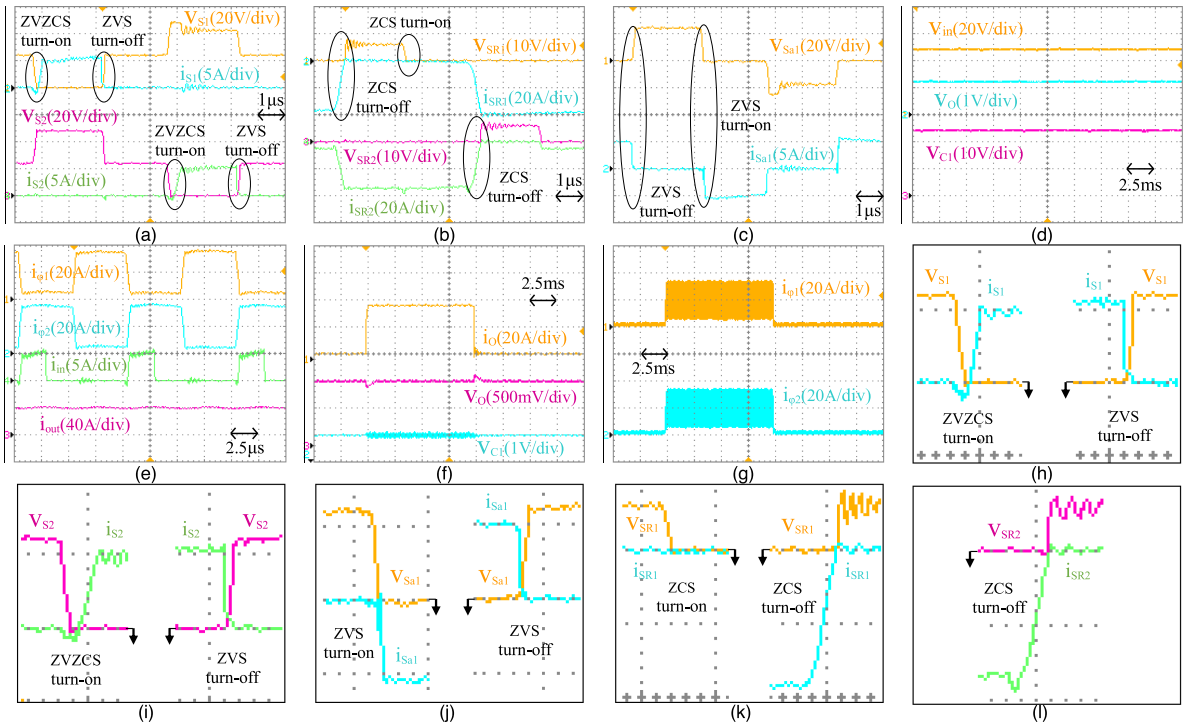

Fig. 12. Experimental waveforms of the implemented two-phase converter. (a) Currents and voltages of S_1 and S_2. (b) Currents and voltages of SR_1 and SR_2. (c) Current and voltage of S_{a1}. (d) Input voltage, output voltage, and voltage of C_1. (e) Input and output currents, and currents of phase 1 and phase 2. (f) Load-disturbance transition performance from light load (10% of full load) to full load and vice versa. (g) Currents of phase 1 and phase 2 during Load transition from light load to full load and vice versa. (h) Current and voltage of S_1 around switching instants. (i) Current and voltage of S_2 around switching instants. (j) Current and voltage of S_{a1} around switching instants. (k) Current and voltage of SR_1 around switching instants. (l) Current and voltage of SR_2 around switching instants.

the voltages of the main switches decrease to zero just before their currents increase. Furthermore, the rate of current change is restricted, and the currents of switches gradually increase. In the laboratory prototype, an external snubber capacitor is utilized. C_{S1} can adequately restrict the rate of voltage change at turn-OFF instant. Therefore, at turn-OFF instants, the voltages of switches rise slightly when their currents decrease significantly. As a result, the main switches are turned ON under ZVZCS and turned OFF under ZVS. Also, the auxiliary switch operates under ZVS. Fig. 12(k) and (l) shows that the currents of SRs decrease to zero just before their voltages increase. Moreover, the rate of current change is restricted, and the currents of switches gradually decrease. Consequently, the ZCS condition is provided for SRs. The efficiency of the two-phase converter proposed in this article versus the output current is depicted in Fig. 13. The efficiency has been measured for various loads when the input and output voltages are constant. The efficiency can be expressed as

$$\eta = \frac{P_o}{P_i} \times 100\% \tag{80}$$

where P_o is the output power and P_i is the input power. The efficiency has been measured for the output currents of 4, 12, 16, 20, 24, 32, and 40 A, when V_{in} and V_o are, respectively, fixed at 48 and 1.2 V. Then, the efficiency curve is drawn based on the measured efficiencies.

To show that the features of the introduced converter do not change by increasing the number of phases, and the proposed

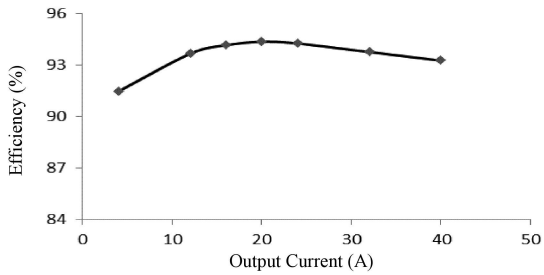

Fig. 13. Efficiency curve of the proposed two-phase dc–dc converter versus the output current.

topology can be expanded while retaining all the merits, a 400-W four-phase laboratory prototype of the introduced topology is implemented at 400 V input, 10 V output, and 100 kHz operating frequency. Based on the voltage gain equation and (63), to have a low output current ripple and low turns ratio, the duty cycle is set to 0.2 and n is calculated as 1. According to (56), the value of selected magnetizing inductances is 100 μH. The coupling coefficients are equal to 0.98, and two 5 nF capacitors are used as the snubber capacitances. The value of the output capacitor is equal to 220 μF. In addition, based on (59), three 10 μF capacitors are used as C_1, C_2, and C_3. The maximum voltages across the main switches, auxiliary switches, and SRs are, respectively, equal to 200 V, 100 V, and 80 V. Also, the maximum currents of the main switches, auxiliary switches, and SRs are, respectively, equal to 6 A, 6 A, and 20 A. As a

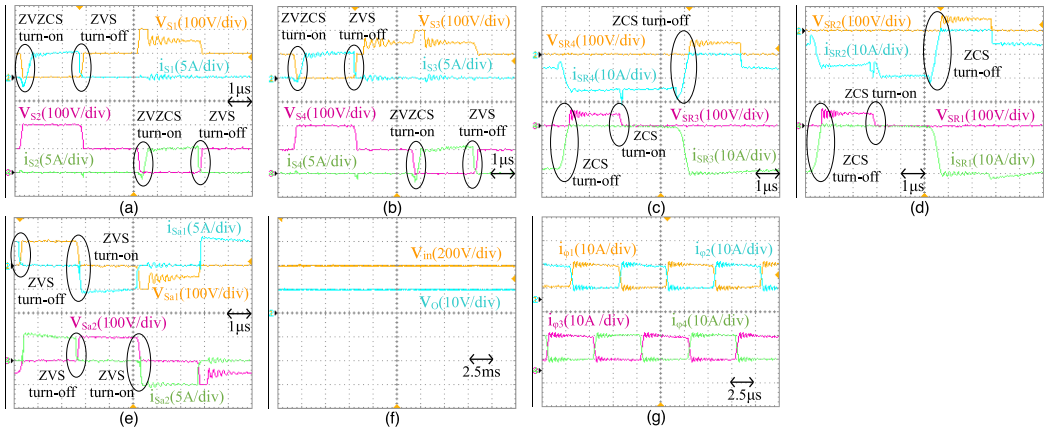

Fig. 14. Experimental waveforms of the implemented four-phase converter. (a) Currents and voltages of S_1 and S_2. (b) Currents and voltages of S_3 and S_4. (c) Currents and voltages of SR_3 and SR_4. (d) Currents and voltages of SR_1 and SR_2. (e) Currents and voltages of S_{a1} and S_{a2}. (f) Input voltage and output voltage. (g) Currents of phase 1, phase 2, phase 3, and phase 4.

result, IRF634 with $V_{DSS} = 250$ V and $I_D = 8$ A is used for the main switches. 2SK3152 with $V_{DSS} = 120$ V and $I_D = 10$ A is used for the auxiliary switches. 25N10 with $V_{DSS} = 100$ V and $I_D = 25$ A is used for the SRs. The experimental waveforms of the implemented four-phase converter are depicted in Fig. 14. The current and voltage waveforms of switches show that the main switches are turned ON under ZVZCS and turned OFF under ZVS. The auxiliary switches operate under ZVS. As can be seen in Fig. 14, the maximum voltages across the main switches, auxiliary switches, and SRs are, respectively, equal to 200 V, 100 V, and 80 V. The maximum current of all main and auxiliary switches is about 6 A. When the current of SR_1 reaches zero, the body diode of SR_1 turns OFF under ZCS. A resonance happens between L_{lk1}, L_{lk2}, and the drain–source capacitor of SR_1. Consequently, the waveform of V_{SR1} has oscillations that are damped to 50 V. When the current of SR_2 reaches zero, the body diode of SR_2 turns OFF under ZCS. A resonance happens between L_{lk1}, L_{lk2}, and the drain–source capacitors of S_1, S_3, SR_2, and S_{a1}. As a result, the waveforms of V_{S1}, V_{S3}, V_{SR2}, and V_{Sa1} have oscillations, which are, respectively, damped to 150 V, 150 V, 50 V, and −50 V. Likewise, some oscillations happen after turning OFF the body diodes of SR_3 and SR_4. From Fig. 14(f), the input voltage is 400 V, and the output voltage measures 10 V. The waveforms of $i_{\varphi 1}$, $i_{\varphi 2}$, $i_{\varphi 3}$, and $i_{\varphi 4}$ are shown in Fig. 14(g).

VIII. Conclusion

A new ZVZCS multiphase topology is proposed and analyzed in this article. In the K-phase structure, the voltage stresses across the main switches, auxiliary switches, and SRs are, respectively, equal to $2V_{in}/K$, V_{in}/K, and $V_{in}/K(n+1)$. Also, the number of blocking capacitors is equal to K-1. The proposed converter does not utilize any extra magnetic core. As discussed in Section IV, the duty cycle is extremely extended and the output current is continuous. In order to confirm the theoretical analysis, two laboratory prototypes are fabricated. The experimental waveforms show that the ZVS condition is achieved for all switches, and thus, the turn-ON switching loss and the capacitive turn-ON loss are eliminated. Also, the provided ZCS condition for the body diodes of SRs eliminates the reverse recovery losses of diodes. The proposed converter can be used for various applications, where ultrahigh step-down conversions and large output currents are required. Some of these industrial applications are telecommunication power systems, electric vehicles, light-emitting diode drivers, and unidirectional chargers. According to the application, input voltage, output voltage, output current, and desirable output current ripple, the number of phases is selected and the elements are designed.

References

[1] Y. Zheng, S. Li, and K. M. Smedley, "Non-isolated high step-down converter with ZVS and low current ripples," *IEEE Trans. Ind. Electron.*, vol. 66, no. 2, pp. 1068–1079, Feb. 2019, doi: 10.1109/TIE.2018.2833047.

[2] W. Sun, Y. Xing, H. Wu, and J. Ding, "Modified high-efficiency LLC converters with two split resonant branches for wide input-voltage range applications," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7867–7879, Sep. 2018, doi: 10.1109/TPEL.2017.2773484.

[3] L. A. D. Ta, N. D. Dao, and D. C. Lee, "High-efficiency hybrid LLC resonant converter for on-board chargers of plug-in electric vehicles," *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 8324–8334, Aug. 2020, doi: 10.1109/TPEL.2020.2968084.

[4] S. M. S. I. Shakib and S. Mekhilef, "A frequency adaptive phase shift modulation control based LLC series resonant converter for wide input voltage applications," *IEEE Trans. Power Electron.*, vol. 32, no. 11, pp. 8360–8370, Nov. 2017, doi: 10.1109/TPEL.2016.2643006.

[5] X. Sun, X. Li, Y. Shen, B. Wang, and X. Guo, "Dual-bridge LLC resonant converter with fixed-frequency PWM control for wide input applications," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 69–80, Jan. 2017, doi: 10.1109/TPEL.2016.2530748.

[6] S. Khan, D. Sha, X. Jia, and S. Wang, "Resonant LLC DC-DC converter employing fixed switching frequency based on dual-transformer with wide input voltage range," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 607–616, Jan. 2021, doi: 10.1109/TPEL.2020.3001161.

[7] C. Liu et al., "Magnetic-coupling current-balancing cells based input-parallel output-parallel LLC resonant converter modules for high-frequency isolation of DC distribution systems," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 6968–6979, Oct. 2016, doi: 10.1109/TPEL.2015.2507172.

[8] U. Ahmad, H. Cha, and N. Naseem, "Integrated current balancing transformer based input-parallel output-parallel LLC resonant converter modules," *IEEE Trans. Power Electron.*, vol. 36, no. 5, pp. 5278–5289, May 2021, doi: 10.1109/TPEL.2020.3026929.

[9] T. Jiang, J. Zhang, X. Wu, K. Sheng, and Y. Wang, "A bidirectional three-level LLC resonant converter with PWAM control," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 2213–2225, Mar. 2016, doi: 10.1109/TPEL.2015.2438072.

[10] H. Chen, X. Wu, and S. Shao, "A current sharing method for interleaved high frequency LLC converter with partial energy processing," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 1498–1507, Feb. 2020, doi: 10.1109/TIE.2019.2896102.

[11] M. Biswas, S. Majhi, and H. B. Nemade, "Two-phase high efficiency interleaved buck converter with improved step-down conversion ratio and low voltage stress," *IET Power Electron.*, vol. 12, no. 15, pp. 3942–3952, Dec. 2019, doi: 10.1049/iet-pel.2019.0547.

[12] L. Yu, L. Wang, C. Yang, and M. Wu, "Analysis and implementation of a single-stage transformer-less converter with high step-down voltage gain for voltage regulator modules," *IEEE Trans. Ind. Electron.*, vol. 68, no. 12, pp. 12239–12249, Dec. 2021, doi: 10.1109/TIE.2020.3045592.

[13] M. D. Vecchia, G. V. Broeck, S. Ravyts, J. Tant, and J. Driesen, "A family of DC–DC converters with high step-down voltage capability based on the valley-fill switched capacitor principle," *IEEE Trans. Ind. Electron.*, vol. 68, no. 7, pp. 5810–5820, Jul. 2021, doi: 10.1109/TIE.2020.2998760.

[14] Y. Wang, J. Zhang, Y. Guan, and D. Xu, "Analysis and design of a two-phase series capacitor dual-path hybrid DC-DC converter," *IEEE Trans. Power Electron.*, vol. 37, no. 8, pp. 9492–9502, Aug. 2022, doi: 10.1109/TPEL.2022.3158728.

[15] P. C. Heris, Z. Saadatizadeh, and N. Rostami, "Transformerless quadratic-based high step-down DC-DC converter with wide duty cycle range," *IET Power Electron.*, vol. 12, no. 3, pp. 368–382, Mar. 2019, doi: 10.1049/iet-pel.2018.5504.

[16] M. Biswas, S. Majhi, and H. B. Nemade, "A high step-down DC–DC converter with reduced inductor current ripple and low voltage stress," *IEEE Trans. Ind. Appl.*, vol. 57, no. 2, pp. 1559–1571, Mar./Apr. 2021, doi: 10.1109/TIA.2020.3046703.

[17] S. Khalili, M. Esteki, M. Packnezhad, H. Farzanehfard, and S. A. Khajehoddin, "Fully soft-switched non-isolated high step-down DC-DC converter with reduced voltage stress and expanding capability," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 11, no. 1, pp. 796–805, Feb. 2023, doi: 10.1109/JESTPE.2022.3180782.

[18] P. N. Truong, N. A. Dung, Y. C. Liu, and H. J. Chiu, "A nonisolated high step-down DC–DC converter with low voltage stress and zero voltage switching," *IEEE Trans. Power Electron.*, vol. 38, no. 3, pp. 3500–3512, Mar. 2023, doi: 10.1109/TPEL.2022.3222693.

[19] M. Forouzesh, Y. Shen, K. Yari, Y. P. Siwakoti, and F. Blaabjerg, "High-efficiency high step-up DC-DC converter with dual coupled inductors for grid-connected photovoltaic systems," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 5967–5982, Jul. 2018, doi: 10.1109/TPEL.2017.2746750.

[20] M. Amiri and H. Farzanehfard, "A high efficiency interleaved ultrahigh step down DC-DC converter with very low output current ripple," *IEEE Trans. Ind. Electron.*, vol. 66, no. 7, pp. 5177–5185, Jul. 2019, doi: 10.1109/TIE.2018.2869348.

[21] M. Amiri, H. Farzanehfard, A. Payman, B. Dakyo, and O. Aghabaghi, "Interleaved ultrahigh step-down converter with low component count," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 3, pp. 3322–3330, Jun. 2021, doi: 10.1109/JESTPE.2020.2997775.

[22] F. Marvi, E. Adib, and H. Farzanehfard, "Efficient ZVS synchronous buck converter with extended duty cycle and low current ripple," *IEEE Trans. Ind. Electron.*, vol. 63, no. 9, pp. 5403–5409, Sep. 2016, doi: 10.1109/TIE.2016.2558483.

[23] S. Khalili, N. Molavi, and H. Farzanehfard, "Soft-switched asymmetric interleaved WCCI high step-down converter with low-voltage stress," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 6, pp. 6692–6699, Dec. 2021, doi: 10.1109/JESTPE.2021.3069176.

[24] L. Zhang and S. Chakraborty, "An interleaved series-capacitor tapped buck converter for high step-down DC/DC application," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6565–6574, Jul. 2019, doi: 10.1109/TPEL.2018.2877309.

[25] M. Amiri and H. Farzanehfard, "An interleaved non-isolated ZVS ultra-high step down DC-DC converter with low voltage stress," *IEEE Trans. Ind. Electron.*, vol. 66, no. 10, pp. 7663–7671, Oct. 2019, doi: 10.1109/TIE.2018.2886794.

[26] A. Asghari, "A nonisolated soft switching interleaved converter with extended duty cycle and low output current ripple," *IEEE Trans. Ind. Electron.*, vol. 68, no. 10, pp. 9376–9385, Oct. 2021, doi: 10.1109/TIE.2020.3020023.

[27] C. Wei, Y. Zhao, Y. Zheng, L. Xie, and K. M. Smedley, "Analysis and design of a nonisolated high step-down converter with coupled inductor and ZVS operation," *IEEE Trans. Ind. Electron.*, vol. 69, no. 9, pp. 9007–9018, Sep. 2022, doi: 10.1109/TIE.2021.3114721.

[28] L. Yu, L. Wang, W. Mu, and C. Yang, "An ultrahigh step-down DC–DC converter based on switched-capacitor and coupled inductor techniques," *IEEE Trans. Ind. Electron.*, vol. 69, no. 11, pp. 11221–11230, Nov. 2022, doi: 10.1109/TIE.2021.3118368.

[29] S. Baharlou, M. R. Yazdani, and M. Delshad, "Nonisolated high-step-down DC-DC converters with low component count and voltage stress," *IEEE Trans. Ind. Electron.*, vol. 70, no. 8, pp. 7904–7912, Aug. 2023, doi: 10.1109/TIE.2023.3236092.

[30] A. I. Pressman, K. Billings, and T. Morey, *Switching Power Supply Design*, 3rd ed. New York, NY, USA: McGraw-Hill, Mar. 2009.

Amin Asghari received the B.S. degree from Shiraz University, Shiraz, Iran, in 2005, the M.S. degree from the Amirkabir University of Technology, Tehran, Iran, in 2008, and the Ph.D. degree from the Isfahan University of Technology, Isfahan, Iran, in 2015, all in electrical engineering.

He is currently a Faculty Member with the Department of Electrical and Computer Engineering, Semnan University, Semnan, Iran. His research interests include dc–dc converters, soft switching techniques, and gate drive circuits.