A Unified Frequency-Domain Model of Analog and Digital PWM DC–DC Converter Considering PWM Delay

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***Abstract*—In this article, the effect of the pulsewidth-modulation (PWM) delay on the stability of PWM dc–dc converters is analyzed. First, a unified frequency-domain model considering the PWM delay is proposed. Based on the proposed model, the physical mechanism of the PWM delay is the sampling characteristic of the modulation process rather than the digital controller. As the analog PWM (APWM) and digital PWM (DPWM) converters both have the modulation process, they both have the PWM delay. Then, the different stabilities of APWM and DPWM converters are compared, which are caused by the state feedback introduced by the output ripple in the APWM converter. As these differences are not caused by the additional time delay in the DPWM converter, when other parameters are the same, the DPWM converter is not always more unstable than the APWM converter. These influences are rarely reported in existing analyses of the modulation and can only be reflected by the proposed model. Finally, the stability of basic converters is analyzed by the proposed model. Compared with existing models, only the proposed model can reflect the different stabilities between the APWM and DPWM converters accurately, which is ensured by experiment results.**

***Index Terms*—Analog pulsewidth modulation (APWM), digital pulsewidth modulation (DPWM), frequency-domain model, pulsewidth-modulation (PWM) delay, stability.**

I. Introduction

THE pulsewidth-modulation (PWM) dc–dc converter plays an important role in the dc microgrid and distribution generation [1], [2], [3]. Generally, the PWM dc–dc converter has two main control methods: analog control and digital control. Compared with analog control, digital control has plenty of advantages such as good expansibility, complex computing ability, and low susceptibility to the environmental factor [4]. Thus, it was often predicted since the 1990s that digital control would soon become the new standard for all dc–dc switching converters [5]. However, although the cost of the digital controller has reduced dramatically in the last few decades, the basic analog controller of the dc–dc converter is still cheaper than the digital controller. Besides, the analog controller naturally has infinite bandwidth. However, the bandwidth of the digital controller is limited by the sampling process. Due to the above advantages, the analog controller still has a huge market share, which is continuously growing in recent years [6]. For the moment, the analog- and digital-controlled dc–dc converters are both important and indispensable components of the existing application, and it is important to research both of them.

To analyze the performance of these converters, the converter model is indispensable, which can be divided into the discrete-time model and frequency-domain model. The two models both have their advantages. The discrete-time model has good accuracy, which is the same as the simulation. Compared with the discrete-time model, the accuracy of the frequency-domain model is relatively low. However, the frequency-domain model has a compact structure and can provide the bode diagram of the converter, which is important for stability analysis and controller design. Therefore, in recent years, a large number of studies on stability analysis and controller design of the analog PWM (APWM) converter [7], [8], [9] and the digital PWM (DPWM) converter [10], [11], [12], [13], [14], [15] are based on frequency-domain models. Except for the discrete-time model, it is necessary to analyze the frequency-domain model of the converter as well.

The state-space average (SSA) model is a classical frequency-domain model [16], [17], [18]. In the SSA model, the state matrix and input matrix are the weighted averages of those in each mode. Based on the SSA model, plenty of nonlinear behaviors of the PWM dc–dc converter have been analyzed, such as the non-minimum phase phenomenon of the boost converter and the new method to avoid this issue [19], [20], [21]. However, the SSA model is not enough to represent all the nonlinear behaviors of the PWM dc–dc converter. In the SSA model, all terms related to the switching period and all effects of the ripple and modulation on the converter stability are ignored. Therefore, the SSA model is less accurate than the discrete-time model and it can only reflect the low-frequency dynamics of PWM converters [22], [23]. To increase the accuracy of the frequency-domain model

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TABLE I
DIFFERENCES BETWEEN THE PROPOSED MODEL AND EXISTING MODELS

Model	Consideration of the PWM Delay	Cause of the PWM Delay	Stabilities of DPWM and APWM Converters
SSA	Not considered	Not considered	Their stabilities are the same
DA	Not considered	Not considered	Their stabilities are the same
MFA	Not considered	Not considered	Their stabilities are the same
ZOH	Only in the DPWM converter	Digital controller	DPWM converters are always more unstable
DF	Only in the DPWM converter	Digital controller	DPWM converters are always more unstable
Proposed	In both APWM and DPWM converters	Modulation process	DPWM converters are not always more unstable

without destroying its compact structure, continuous efforts have been made.

For the APWM converter, the frequency-domain model is mainly corrected by considering the ripple more finely. In the discrete average (DA) model [24], [25], the effect of the equivalent series resistance (ESR) of the output capacitor is analyzed. Due to the ESR, the inductor current ripples in the output voltage, which equivalently introduces additional inductor current feedback and affects the stability of the converter. Following the DA model, the output ripple is analyzed more finely in the multifrequency average (MFA) model [26], [27], [28], [29]. In the MFA model, the output ripple is caused by both the ESR and discontinuous output current, and the output of the controller contains a significant switching ripple when the controller bandwidth is large. Based on the basic MFA model, the model of converters with different switching frequencies is further built in [30] and [31], and the beat frequency oscillator is analyzed.

For the DPWM converter, except for the time delay caused by the zero-order holder (ZOH) of the analog-to-digital converter (ADC) and the computational delay, another kind of time delay named the PWM delay is analyzed. In the ZOH model [32], [33], [34], [35], [36], the PWM delay is considered to be caused by the ZOH of controller output, which leads to a time delay of the half-sampling period. In the describing function (DF) model [37], [38], [39], the PWM delay is caused by the time delay between the update moment of the modulation signal and the moment when the modulation signal intersects the carrier. The value of this time delay varies for carriers. Based on these explanations, the PWM delay is caused by the digital controller, and the APWM converter has no PWM delay.

However, in the existing models, the PWM delay is not considered properly. For the SSA, DA, and MFA models, the PWM delays in the APWM and DPWM converters are both ignored. For the ZOH and DF models, the PWM delay in the APWM converter is ignored. The existing analyses are not enough to reflect the influence of PWM delay on the stability of APWM and DPWM converters accurately. Therefore, this article provides a detailed analysis of the PWM delay. To show the novelty of the proposed model, the differences between the proposed model and existing models are compared and listed in Table I, and the main contributions are summarized as follows.

1) A unified frequency-domain model considering the PWM delay is proposed. In existing models, the PWM delay is considered to be caused by the digital controller, which only occurs in the DPWM converter. However, in the proposed model, the PWM delay is caused by modulation. As the APWM and DPWM converters both have the modulation process, they both have the PWM delay as well.
2) Based on the proposed model, the different stabilities of APWM and DPWM converters are compared, which are caused by the state feedback introduced by the output ripple in the APWM converter. As these differences are not caused by the additional time delay in the DPWM converter, when other parameters are the same, the DPWM converter is not always more unstable than the APWM converter. These influences are rarely reported in existing analyses of the modulation and can only be reflected by the proposed model.
3) The effects of the above PWM delay and state feedback on the stability of basic converters are analyzed. Compared with existing models, only the proposed model can reflect the different effects of the PWM delay and state feedback in the APWM and DPWM converters. The proposed model is more accurate than the existing models.

The rest of this article is organized as follows. The proposed frequency-domain model is deduced in Section II. The stabilities of APWM and DPWM converters are compared in Section III. The experiments are shown in Section IV, whose results ensure the validity of theoretical analyses. Finally, Section V concludes this article.

II. PROPOSED MODEL

In this section, the principle of the proposed model is derived. First, an augmented time-variant model is obtained. Then, the time-variant model is transferred into the time-invariant model. Finally, a frequency-domain model is obtained from the time-invariant model, and the open-loop transfer functions are obtained.

A. Augmented Time-Variant Model

In the mode k, the PWM dc–dc converter can be represented by time-variant state-space equations

$$\begin{cases} \dot{\mathbf{x}}(t) = \mathbf{A}_k\mathbf{x}(t) + \mathbf{B}_k V_{\text{in}}(t) \\ v_{\text{o}}(t) = \mathbf{C}_k\mathbf{x}(t) \end{cases} \tag{1}$$

where $\mathbf{x}(t)$, $V_{\text{in}}(t)$, $v_{\text{o}}(t)$, $\mathbf{A}_k$, $\mathbf{B}_k$, and $\mathbf{C}_k$ are the state vector, input voltage, output voltage, state matrix, input matrix, and output matrix of the converter, respectively.

If the transfer function of the controller is $H(s)$, the controller can be expressed as following time-invariant state-space equations:

$$\begin{cases} \dot{\mathbf{x}}_{\text{C}}(t) = \mathbf{A}_{\text{C}}\mathbf{x}_{\text{C}}(t) + \mathbf{B}_{\text{C}}(V_{\text{ref}} - v_{\text{o}}(t)) \\ v_{\text{m}}(t) = \mathbf{C}_{\text{C}}\mathbf{x}_{\text{C}}(t) + \mathbf{D}_{\text{C}}(V_{\text{ref}} - v_{\text{o}}(t)) \end{cases} \tag{2}$$

where $\mathbf{x}_C(t)$, V_{ref}, $v_m(t)$, $\mathbf{A}_C$, $\mathbf{B}_C$, $\mathbf{C}_C$, and $\mathbf{D}_C$ are the state vector, reference output voltage, controller output, state matrix, input matrix, output matrix, and direct transfer matrix of the controller, respectively, and

$$H(s) = \mathbf{C}_C(s\mathbf{E} - \mathbf{A}_C)^{-1}\mathbf{B}_C + \mathbf{D}_C. \tag{3}$$

For the analog controller, the controller can be realized by the analog system described by (2) directly. For the digital controller, the controller is realized by iteration. To eliminate the time delay caused by the ADC, the parameter of this iteration is generally designed with the bilinear transformation. And (2) is just an equivalent representation of its dynamic properties.

To simplify the analysis process, a uniform equation is obtained by combining (1) with (2). With this transformation, the whole system is transferred into the form of unit positive feedback [40], which is expressed as

$$\begin{cases} \dot{\mathbf{x}}^*(t) = \mathbf{A}_k^*\mathbf{x}^*(t) + \mathbf{B}_k^*\mathbf{u}^*(t) \\ v_m(t) = \mathbf{C}_k^*\mathbf{x}^*(t) + \mathbf{D}_C V_{ref} \end{cases} \tag{4}$$

where $\mathbf{x}^*(t)$, $\mathbf{u}^*(t)$, $\mathbf{A}_k^*$, $\mathbf{B}_k^*$, and $\mathbf{C}_k^*$ are the augmented state vector, augmented input vector, augmented state matrix, augmented input matrix, and augmented output matrix, respectively, and

$$\begin{aligned} &\mathbf{x}^*(t) = \begin{bmatrix}\mathbf{x}(t)^T & \mathbf{x}_C(t)^T\end{bmatrix}^T, \quad \mathbf{u}^*(t) = \begin{bmatrix}V_{in}(t) & V_{ref}(t)\end{bmatrix}^T \\ &\mathbf{A}_k^* = \begin{bmatrix}\mathbf{A}_k & 0 \\ -\mathbf{B}_C\mathbf{C}_k & \mathbf{A}_C\end{bmatrix}, \quad \mathbf{B}_k^* = \begin{bmatrix}\mathbf{B}_k & 0 \\ 0 & \mathbf{B}_C\end{bmatrix} \\ &\mathbf{C}_k^* = \begin{bmatrix}-\mathbf{D}_C\mathbf{C}_k & \mathbf{C}_C\end{bmatrix}. \end{aligned} \tag{5}$$

B. Proposed Time-Invariant Model

Generally, the frequency-domain model is obtained by the small-signal analysis of a time-invariant model. To transfer (4) into a time-invariant equation, the equivalent state variable $\mathbf{x}_{eq}$ is used and

$$\begin{cases} \dot{\mathbf{x}}_{eq}(t) = \mathbf{A}_{eq}\mathbf{x}_{eq}(t) + \mathbf{B}_{eq}\mathbf{u}^*(t) \\ \mathbf{x}_{eq}(t_0) = \mathbf{x}^*(t_0) \end{cases} \tag{6}$$

where $\mathbf{A}_{eq}$ is the equivalent state matrix, $\mathbf{B}_{eq}$ is the equivalent input matrix, and t_0 is the initial time point.

If the relationship between $\mathbf{x}^*(t_0+T)$ and $\mathbf{x}^*(t_0)$ is the same as the relationship between $\mathbf{x}_{eq}(t_0+T)$ and $\mathbf{x}_{eq}(t_0)$, $\mathbf{x}_{eq}(t)$ has the same stability as $\mathbf{x}^*(t)$. For APWM converters with the trailing-edge carrier, the relationship between $\mathbf{x}^*(t_0+T)$ and $\mathbf{x}^*(t_0)$ is

$$\begin{cases} \mathbf{x}^*(t_0+T) = \mathbf{\Phi}\mathbf{x}^*(t_0) + \mathbf{\Gamma}\mathbf{u}^*(t_0) \\ \mathbf{\Phi} = e^{\mathbf{A}_2^*(1-d_n)T}e^{\mathbf{A}_1^* d_n T} \\ \mathbf{\Gamma} = \int_0^{(1-d_n)T} e^{-\mathbf{A}_2^*\tau}d\tau\mathbf{B}_2^* \\ \quad + e^{\mathbf{A}_2^*(1-d_n)T}\int_0^{d_n T} e^{-\mathbf{A}_1^*\tau}d\tau\mathbf{B}_1^* \end{cases} \tag{7}$$

where $\mathbf{\Phi}$ and $\mathbf{\Gamma}$ are iteration matrices, and d_n is the duty cycle of the nth period.

For DPWM converters with the trailing-edge carrier, due to the ADC, the input of the digital controller is constant in a switching period. Therefore, the relationship between $\mathbf{x}^*(t_0+T)$ and $\mathbf{x}^*(t_0)$ is different from that in APWM converters, which is

$$\begin{cases} \mathbf{x}^*(t_0+T) = \mathbf{\Phi}\mathbf{x}^*(t_0) + \mathbf{\Gamma}\mathbf{u}^*(t_0) \\ \mathbf{\Phi} = \begin{bmatrix} e^{\mathbf{A}_2(1-d_n)T}e^{\mathbf{A}_1 d_n T} & 0 \\ -\int_0^T e^{-\mathbf{A}_C\tau}d\tau\mathbf{B}_C\mathbf{C}_1 & e^{\mathbf{A}_C T}\end{bmatrix} \\ \mathbf{\Gamma} = \int_0^{(1-d_n)T} e^{-\mathbf{A}_2^*\tau}d\tau\mathbf{B}_2^* \\ \quad + e^{\mathbf{A}_2^*(1-d_n)T}\int_0^{d_n T} e^{-\mathbf{A}_1^*\tau}d\tau\mathbf{B}_1^*. \end{cases} \tag{8}$$

And the relationship between $\mathbf{x}_{eq}(t_0+T)$ and $\mathbf{x}_{eq}(t_0)$ is

$$\mathbf{x}_{eq}(t_0+T) = e^{\mathbf{A}_{eq}T}\mathbf{x}_{eq}(t_0) + \int_0^T e^{-\mathbf{A}_{eq}\tau}d\tau\mathbf{B}_{eq}\mathbf{u}^*(t_0). \tag{9}$$

Comparing (7)–(8) with (9), the relationship among $\mathbf{A}_{eq}$, $\mathbf{B}_{eq}$, $\mathbf{\Phi}$, and $\mathbf{\Gamma}$ is

$$\mathbf{\Phi} = e^{\mathbf{A}_{eq}T}, \quad \mathbf{\Gamma} = \int_0^T e^{-\mathbf{A}_{eq}\tau}d\tau\mathbf{B}_{eq}. \tag{10}$$

Making the Taylor expansion and ignoring the high-order terms of switching period T in (10), $\mathbf{A}_{eq}$ and $\mathbf{B}_{eq}$ are

$$\begin{cases} \mathbf{A}_{eq} = \mathbf{A}_1^* d_n + \mathbf{A}_2^*(1-d_n) + \mathbf{A}_{cor}d_n(1-d_n)T \\ \quad + O(T^2) \\ \mathbf{B}_{eq} = \mathbf{B}_1^* d_n + \mathbf{B}_2^*(1-d_n) + \mathbf{B}_{cor}d_n(1-d_n)T \\ \quad + O(T^2) \end{cases} \tag{11}$$

where $\mathbf{A}_{cor}$ and $\mathbf{B}_{cor}$ are one-order correction matrices.

For APWM converters, $\mathbf{A}_{cor}$ and $\mathbf{B}_{cor}$ are

$$\begin{cases} \mathbf{A}_{cor} = 0.5(\mathbf{A}_2^*\mathbf{A}_1^* - \mathbf{A}_1^*\mathbf{A}_2^*) \\ \mathbf{B}_{cor} = 0.5(\mathbf{A}_2^*\mathbf{B}_1^* - \mathbf{A}_1^*\mathbf{B}_2^*) \end{cases}. \tag{12}$$

And for DPWM converters, they are

$$\begin{cases} \mathbf{A}_{cor} = 0.5\begin{bmatrix}\mathbf{A}_2\mathbf{A}_1 - \mathbf{A}_1\mathbf{A}_2 & 0 \\ 0 & 0\end{bmatrix} \\ \mathbf{B}_{cor} = 0.5(\mathbf{A}_2^*\mathbf{B}_1^* - \mathbf{A}_1^*\mathbf{B}_2^*) \end{cases}. \tag{13}$$

The derivation of (11)–(13) is shown in the Appendix.

For converters with other carriers, $\mathbf{A}_{eq}$ and $\mathbf{B}_{eq}$ are obtained by similar methods, and the results can be expressed as the following unified form:

$$\begin{cases} \mathbf{A}_{eq} = \mathbf{A}_1^* d_n + \mathbf{A}_2^*(1-d_n) + \alpha\mathbf{A}_{cor}d_n(1-d_n)T \\ \quad + O(T^2) \\ \mathbf{B}_{eq} = \mathbf{B}_1^* d_n + \mathbf{B}_2^*(1-d_n) + \alpha\mathbf{B}_{cor}d_n(1-d_n)T \\ \quad + O(T^2) \end{cases} \tag{14}$$

where α is a coefficient, whose value is 1, 0, and -1 for converters with the trailing-edge, triangular, and leading-edge carriers, respectively.

C. Proposed Frequency-Domain Model

The proposed frequency-domain model is obtained in two steps. In the first step, the model of the converter and controller is obtained by the small signal analysis of (6) and (14)

$$\begin{cases} \hat{\mathbf{x}}_{eq}(s) = \mathbf{G}_{xd}(s)\hat{d}_n(s) \\ \mathbf{G}_{xd}(s) = (s\mathbf{E} - \bar{\mathbf{A}}_{eq})^{-1}[(\mathbf{A}_1^* - \mathbf{A}_2^*)\bar{\mathbf{x}}_{eq} + (\mathbf{B}_1^* - \mathbf{B}_2^*)\bar{\mathbf{u}}^*] \\ \quad + \alpha(s\mathbf{E} - \bar{\mathbf{A}}_{eq})^{-1}(\mathbf{A}_{cor}\bar{\mathbf{x}}_{eq} + \mathbf{B}_{cor}\bar{\mathbf{u}}^*)(1-2\bar{d}_n)T \end{cases} \tag{15}$$

where $\hat{\mathbf{x}}_{eq}(s)$ and $\hat{d}_n(s)$ are small disturbance values of corresponding variables, $\bar{\mathbf{x}}_{eq}$, $\bar{\mathbf{u}}^*$, $\bar{d}_n$, $\bar{\mathbf{A}}_{eq}$, and $\bar{\mathbf{B}}_{eq}$ are steady values

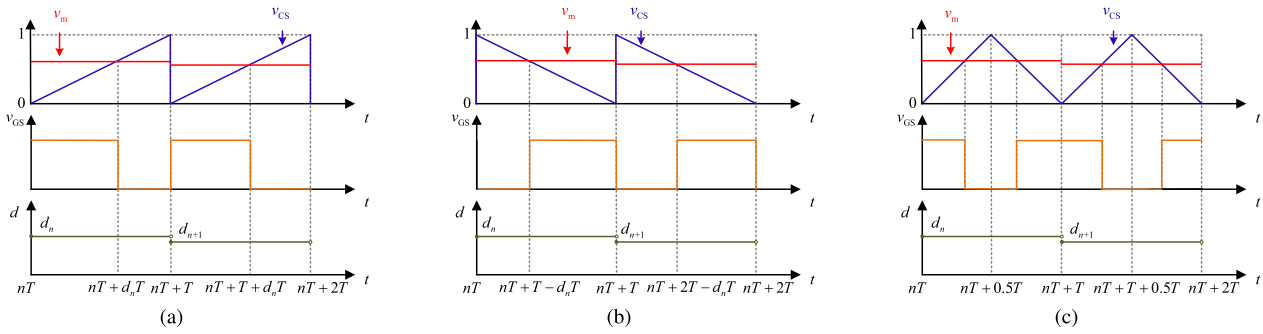

Fig. 1. Modulation process of the DPWM converter with different carriers. (a) Trailing-edge carrier. (b) Leading-edge carrier. (c) Triangular carrier.

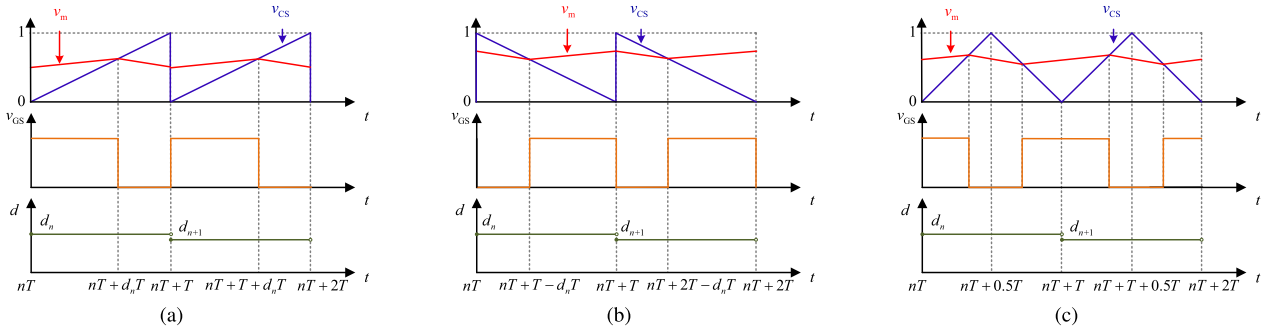

Fig. 2. Modulation process of the APWM converter with different carriers. (a) Trailing-edge carrier. (b) Leading-edge carrier. (c) Triangular carrier.

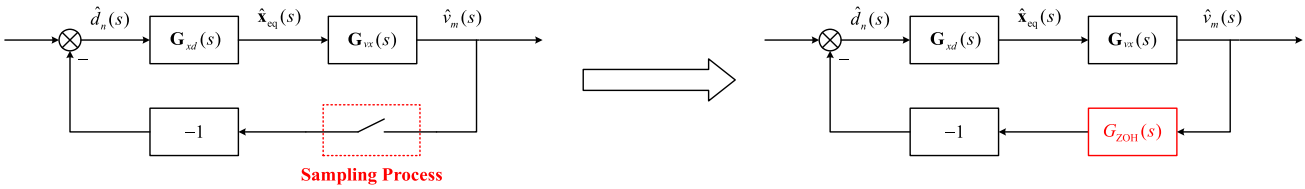

Fig. 3. Control block diagrams of the proposed model.

of corresponding variables, $\mathbf{G}_{xd}(s)$ is the transfer function between the state vector and duty cycle, and $\mathbf{E}$ is the unit matrix.

In the second step, the sampling process of the modulation is analyzed. The modulation processes of APWM and DPWM converters are shown in Figs. 1 and 2, where $v_{\rm CS}$ is the carrier, and $v_{\rm GS}$ is the switch signal. As shown in Figs. 1 and 2, due to the modulation, the value of the duty cycle d_n is only decided by the value of controller output $v_{\rm m}(t)$ at the intersection time point. This process is the same as the sampling process of the ADC, where the output of the ADC is only decided by the input at the sampling time point. Therefore, as shown in Fig. 3, the modulation in the APWM and DPWM converter naturally constitutes a sampling process.

The sampling process of modulation leads to two influences on the control block diagrams. On the one hand, as shown in Fig. 3, the same as the ADC, the modulation contains a ZOH element, which is expressed as

$$G_{\rm ZOH}(s) = \hat{d}_n(s)/\hat{v}_{\rm m}(s) = (1-e^{-sT})/sT \approx 1-0.5sT. \tag{16}$$

On the other hand, as shown in Figs. 1 and 2, for converters with different carriers and modulation methods, $v_{\rm m}(t)$ is sampled at different time points. Due to the influence of the ripple, the transfer function between $\hat{v}_{\rm m}(s)$ and $\hat{\mathbf{x}}_{\rm eq}(s)$ is varying, which is defined as

$$\mathbf{G}_{vx}(s) = \hat{v}_{\rm m}(s)/\hat{\mathbf{x}}_{\rm eq}(s). \tag{17}$$

The exact value of $\mathbf{G}_{vx}(s)$ is listed in Table II. The detailed derivation of $\mathbf{G}_{vx}(s)$ is shown in the Appendix.

As shown in Fig. 3, the open-loop transfer function $G_{\rm op}(s)$ of APWM and DPWM converters are both

$$G_{\rm op}(s) = -\mathbf{G}_{vx}(s)\mathbf{G}_{xd}(s)G_{\rm ZOH}(s). \tag{18}$$

Even if the ZOH of the ADC in the digital controller is eliminated by the bilinear transformation, the open-loop transfer function of the DPWM converter still contains a ZOH element, which is named the PWM delay. In the ZOH and DF models, it is considered to be caused by the digital controller. However, based on the proposed model, this PWM delay is caused by the modulation rather than the digital controller. As the APWM

TABLE II
TRANSFER FUNCTION BETWEEN STATE VECTOR AND CONTROLLER OUTPUT

Carrier	Value	
	APWM	DPWM
Trailing-edge	$\mathbf{G}_{vx}(s)=\frac{\mathbf{C}_1^* e^{\mathbf{A}_1^*\bar{d}_n T}}{1-G_{\text{ZOH}}(s)\mathbf{C}_1^* e^{\mathbf{A}_1^*\bar{d}_n T}(\mathbf{A}_1^*\bar{\mathbf{x}}_{\text{eq}}+\mathbf{B}_1^*\bar{\mathbf{u}}^*)T}$	$\mathbf{G}_{vx}(s)=\mathbf{C}_1^*$
Leading-edge	$\mathbf{G}_{vx}(s)=\frac{\mathbf{C}_2^* e^{\mathbf{A}_2^*(1-\bar{d}_n)T}}{1+G_{\text{ZOH}}(s)\mathbf{C}_2^* e^{\mathbf{A}_2^*(1-\bar{d}_n)T}(\mathbf{A}_2^*\bar{\mathbf{x}}_{\text{eq}}+\mathbf{B}_2^*\bar{\mathbf{u}}^*)T}$	$\mathbf{G}_{vx}(s)=\mathbf{C}_2^*$
Triangular	$\mathbf{G}_{vx}(s)=\frac{0.5(\mathbf{C}_1^* e^{0.5\mathbf{A}_1^*\bar{d}_n T}+\mathbf{C}_2^* e^{-0.5\mathbf{A}_1^*\bar{d}_n T}e^{sT})}{1-0.5G_{\text{ZOH}}(s)(\mathbf{C}_1^* e^{0.5\mathbf{A}_1^*\bar{d}_n T}-\mathbf{C}_2^* e^{-0.5\mathbf{A}_1^*\bar{d}_n T})(\mathbf{A}_1^*\bar{\mathbf{x}}_{\text{eq}}+\mathbf{B}_1^*\bar{\mathbf{u}}^*)T}$	$\mathbf{G}_{vx}(s)=\mathbf{C}_1^*$

and DPWM converters both have the modulation element, they both contain this ZOH element as well. The main difference between APWM and DPWM converters is the exact value of $\mathbf{G}_{vx}(s)$, which is introduced by the ripple.

III. DIFFERENT STABILITY OF APWM AND DPWM CONVERTERS

In the proposed model, the difference between APWM and DPWM converters mainly occurs on the exact value of $\mathbf{G}_{vx}(s)$. In this section, the influence of this difference on the stability of the converter is analyzed.

A. Triangular Carrier

In the APWM converter with the triangular carrier, due to the influence of the ripple, $\mathbf{G}_{vx}(s)$ can counteract the ZOH element in (18) approximately. Generally, the difference between $\mathbf{C}_1^*$ and $\mathbf{C}_2^*$ is caused by the ESR of the output capacitor, which is relatively small and

$$\mathbf{C}_1^* \approx \mathbf{C}_2^*. \tag{19}$$

Substituting (19) into $\mathbf{G}_{vx}(s)$ of the APWM converter with the triangular carrier and ignoring the high-order terms of switching period T, $\mathbf{G}_{vx}(s)$ can be simplified as

$$\begin{aligned}\mathbf{G}_{vx}(s) &\approx \mathbf{C}_1^*(1+e^{sT})/2+O(T^2)\\ &= \mathbf{C}_1^*/G_{\text{ZOH}}(s)+O(T^2).\end{aligned} \tag{20}$$

Substituting (20) into (18), for the converter with the triangular carrier, when other parameters are the same, the relationship between the APWM converter's open-loop transfer function $G_{\text{op\_A}}(s)$ and the DPWM converter's open-loop transfer function $G_{\text{op\_D}}(s)$ is

$$G_{\text{op\_A}}(s)=G_{\text{op\_D}}(s)/G_{\text{ZOH}}(s)+O(T^2). \tag{21}$$

As shown in (21), due to the influence of the ripple, the APWM converter with the triangular carrier always has a less ZOH element than the DPWM converter with the triangular carrier. When other parameters are the same, the APWM converter with the triangular carrier is always more stable than the DPWM converter with the triangular carrier.

In the existing analyses of the ZOH and DF models, the converter with the triangular carrier is mainly analyzed. According to their conclusion, the PWM delay is caused by the digital controller, which only occurs in the DPWM converter [32], [33], [34], [35], [36], [37], [38], [39]. This elimination phenomenon only occurs in the APWM converter with the triangular carrier, which is a probable reason for this misunderstanding.

B. Trailing-Edge and Leading-Edge Carriers

In converters with trailing-edge and leading-edge carriers, the ZOH is no more eliminated. Ignoring the high-order terms of switching period T, $\mathbf{G}_{vx}(s)$ of the APWM converter with the trailing-edge carrier can be expressed as

$$\mathbf{G}_{vx}(s)=\mathbf{C}_1^*+\mathbf{G}_{\text{add}}(s)T+O(T^2) \tag{22}$$

$$\mathbf{G}_{\text{add}}(s)=\mathbf{C}_1^*\frac{\mathbf{A}_1^*\bar{d}_n+\mathbf{C}_1^*(\mathbf{A}_1^*\bar{\mathbf{x}}_{\text{eq}}+\mathbf{B}_1^*\bar{\mathbf{u}}^*)\mathbf{E}}{1-\mathbf{C}_1^*(\mathbf{A}_1^*\bar{\mathbf{x}}_{\text{eq}}+\mathbf{B}_1^*\bar{\mathbf{u}}^*)T}. \tag{23}$$

And $\mathbf{G}_{vx}(s)$ of the APWM converter with the leading-edge carrier can be expressed as

$$\mathbf{G}_{vx}(s)=\mathbf{C}_2^*+\mathbf{G}_{\text{add}}(s)T+O(T^2) \tag{24}$$

$$\mathbf{G}_{\text{add}}(s)=\mathbf{C}_2^*\frac{\mathbf{A}_2^*(1-\bar{d}_n)+\mathbf{C}_2^*(\mathbf{A}_2^*\bar{\mathbf{x}}_{\text{eq}}+\mathbf{B}_2^*\bar{\mathbf{u}}^*)\mathbf{E}}{1-\mathbf{C}_2^*(\mathbf{A}_2^*\bar{\mathbf{x}}_{\text{eq}}+\mathbf{B}_2^*\bar{\mathbf{u}}^*)T}. \tag{25}$$

Substituting (22) and (24) into (18), for the converter with trailing-edge and leading-edge carriers, when other parameters are the same, the relationship between the open-loop transfer function of the APWM and DPWM converters is

$$\begin{aligned}G_{\text{op\_A}}(s)=&G_{\text{op\_D}}(s)-\mathbf{G}_{\text{add}}(s)\mathbf{G}_{xd}(s)G_{\text{ZOH}}(s)T\\ &+O(T^2).\end{aligned} \tag{26}$$

Compared with $G_{\text{op\_D}}(s)$, $G_{\text{op\_A}}(s)$ contains additional state feedback. As shown in (23) and (25), the value of $\mathbf{G}_{\text{add}}(s)$ is decided by the state matrix, input matrix, and output matrix of the converter and controller. Therefore, the influence of this state feedback on the stability varies for converters and carriers. When other parameters are the same, the stability of the APWM converter can be worse than the DPWM converter, which will be shown in the next section.

IV. VERIFICATION

A. Application Guideline of the Proposed Model

To make sure that the proposed model is not only suitable for special PWM dc–dc converters, the proposed model is derived by the matrix form and no specific parameter of the converter exists in the derivation. In this section, it is shown how to substitute the

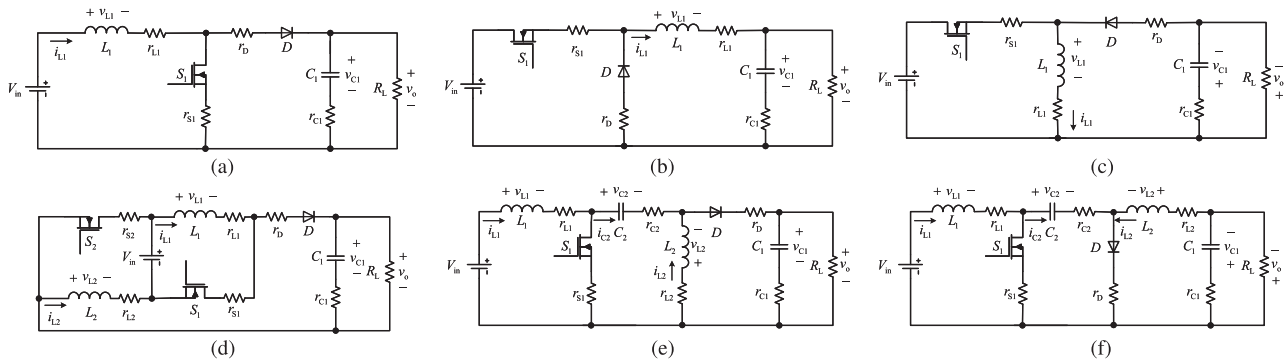

Fig. 4. Topologies of basic PWM dc–dc converters. (a) Boost converter. (b) Buck converter. (c) Buck–boost converter. (d) Double-boost converter. (e) SEPCI converter. (f) Cuk converter.

TABLE III
MATRIXES OF CONVERTERS

Item	Boost	Buck	Buck–boost	Double-boost	SEPIC	Cuk
$\mathbf{x}(t)$	$\begin{bmatrix} i_{L1} & v_{C1} \end{bmatrix}^{T}$	$\begin{bmatrix} i_{L1} & v_{C1} \end{bmatrix}^{T}$	$\begin{bmatrix} i_{L1} & v_{C1} \end{bmatrix}^{T}$	$\begin{bmatrix} i_{L1} & i_{L2} & v_{C1} \end{bmatrix}^{T}$	$\begin{bmatrix} i_{L1} & i_{L2} & v_{C2} & v_{C1} \end{bmatrix}^{T}$	$\begin{bmatrix} i_{L1} & i_{L2} & v_{C2} & v_{C1} \end{bmatrix}^{T}$
$\mathbf{A}_1$	$\begin{bmatrix} \frac{-r_{\Sigma 1}}{L_1} & 0 \\ 0 & \frac{-k_R}{C_1 R_L} \end{bmatrix}$	$\begin{bmatrix} \frac{-r_{\Sigma 1}}{L_1} & \frac{-k_R}{L_1} \\ \frac{k_R}{C_1} & \frac{-k_R}{C_1 R_L} \end{bmatrix}$	$\begin{bmatrix} \frac{-r_{\Sigma 1}}{L_1} & 0 \\ 0 & \frac{-k_R}{C_1 R_L} \end{bmatrix}$	$\begin{bmatrix} \frac{-r_{\Sigma 1}}{L_1} & 0 & 0 \\ 0 & \frac{-r_{\Sigma 1}}{L_2} & 0 \\ 0 & 0 & \frac{-k_R}{C_1 R_L} \end{bmatrix}$	$\begin{bmatrix} \frac{-r_{\Sigma 1}}{L_1} & \frac{-r_{S1}}{L_1} & 0 & 0 \\ \frac{-r_{S1}}{L_2} & \frac{-r_{\Sigma 4}}{L_2} & \frac{1}{L_2} & 0 \\ 0 & \frac{-1}{C_2} & 0 & 0 \\ 0 & 0 & 0 & \frac{-k_R}{C_1 R_L} \end{bmatrix}$	$\begin{bmatrix} \frac{-r_{\Sigma 1}}{L_1} & \frac{-r_{S1}}{L_1} & 0 & 0 \\ \frac{-r_{S1}}{L_2} & \frac{-r_{\Sigma 7}}{L_2} & \frac{1}{L_2} & \frac{-k_R}{L_2} \\ 0 & \frac{-1}{C_2} & 0 & 0 \\ 0 & \frac{k_R}{C_1} & 0 & \frac{-k_R}{C_1 R_L} \end{bmatrix}$
$\mathbf{A}_2$	$\begin{bmatrix} \frac{-r_{\Sigma 3}}{L_1} & \frac{-k_R}{L_1} \\ \frac{k_R}{C_1} & \frac{-k_R}{C_1 R_L} \end{bmatrix}$	$\begin{bmatrix} \frac{-r_{\Sigma 2}}{L_1} & \frac{-k_R}{L_1} \\ \frac{k_R}{C_1} & \frac{-k_R}{C_1 R_L} \end{bmatrix}$	$\begin{bmatrix} \frac{-r_{\Sigma 3}}{L_1} & \frac{-k_R}{L_1} \\ \frac{k_R}{C_1} & \frac{-k_R}{C_1 R_L} \end{bmatrix}$	$\begin{bmatrix} \frac{-r_{\Sigma 3}}{L_1} & 0 & \frac{-k_R}{2L_1} \\ 0 & \frac{-r_{\Sigma 3}}{L_2} & \frac{-k_R}{2L_2} \\ \frac{k_R}{2C_1} & \frac{k_R}{2C_1} & \frac{-k_R}{C_1 R_L} \end{bmatrix}$	$\begin{bmatrix} \frac{-r_{\Sigma 5}}{L_1} & \frac{-r_{\Sigma 6}}{L_1} & \frac{-1}{L_1} & \frac{-k_R}{L_1} \\ \frac{-r_{\Sigma 6}}{L_2} & \frac{-r_{\Sigma 3}}{L_2} & 0 & \frac{-k_R}{L_2} \\ \frac{1}{C_2} & 0 & 0 & 0 \\ \frac{k_R}{C_1} & \frac{k_R}{C_1} & 0 & \frac{-k_R}{C_1 R_L} \end{bmatrix}$	$\begin{bmatrix} \frac{-r_{\Sigma 5}}{L_1} & \frac{-r_D}{L_1} & \frac{-1}{L_1} & 0 \\ \frac{-r_D}{L_2} & \frac{-r_{\Sigma 3}}{L_2} & 0 & \frac{-k_R}{L_2} \\ \frac{1}{C_2} & 0 & 0 & 0 \\ 0 & \frac{k_R}{C_1} & 0 & \frac{-k_R}{C_1 R_L} \end{bmatrix}$
$\mathbf{B}_1$	$\begin{bmatrix} \frac{1}{L_1} & 0 \end{bmatrix}^{T}$	$\begin{bmatrix} \frac{1}{L_1} & 0 \end{bmatrix}^{T}$	$\begin{bmatrix} \frac{1}{L_1} & 0 \end{bmatrix}^{T}$	$\begin{bmatrix} \frac{1}{L_1} & \frac{1}{L_2} & 0 \end{bmatrix}^{T}$	$\begin{bmatrix} \frac{1}{L_1} & 0 & 0 & 0 \end{bmatrix}^{T}$	$\begin{bmatrix} \frac{1}{L_1} & 0 & 0 & 0 \end{bmatrix}^{T}$
$\mathbf{B}_2$	$\begin{bmatrix} \frac{1}{L_1} & 0 \end{bmatrix}^{T}$	$\begin{bmatrix} 0 & 0 \end{bmatrix}^{T}$	$\begin{bmatrix} 0 & 0 \end{bmatrix}^{T}$	$\begin{bmatrix} \frac{1}{2L_1} & \frac{1}{2L_2} & 0 \end{bmatrix}^{T}$	$\begin{bmatrix} \frac{1}{L_1} & 0 & 0 & 0 \end{bmatrix}^{T}$	$\begin{bmatrix} \frac{1}{L_1} & 0 & 0 & 0 \end{bmatrix}^{T}$
$\mathbf{C}_1$	$\begin{bmatrix} 0 & k_R \end{bmatrix}$	$\begin{bmatrix} k_R r_{C1} & k_R \end{bmatrix}$	$\begin{bmatrix} 0 & k_R \end{bmatrix}$	$\begin{bmatrix} 0 & 0 & k_R \end{bmatrix}$	$\begin{bmatrix} 0 & 0 & 0 & k_R \end{bmatrix}$	$\begin{bmatrix} 0 & k_R r_{C1} & 0 & k_R \end{bmatrix}$
$\mathbf{C}_2$	$\begin{bmatrix} k_R r_{C1} & k_R \end{bmatrix}$	$\begin{bmatrix} k_R r_{C1} & k_R \end{bmatrix}$	$\begin{bmatrix} k_R r_{C1} & k_R \end{bmatrix}$	$\begin{bmatrix} \frac{k_R r_{C1}}{2} & \frac{k_R r_{C1}}{2} & k_R \end{bmatrix}$	$\begin{bmatrix} k_R r_{C1} & k_R r_{C1} & 0 & k_R \end{bmatrix}$	$\begin{bmatrix} 0 & k_R r_{C1} & 0 & k_R \end{bmatrix}$

parameters of PWM dc–dc converters and controllers into the proposed model to analyze the stability. Several examples are provided, which include boost, buck, buck–boost, double-boost [41], SEPIC, and cuk converters.

The application of the proposed model can be divided into the following five steps.

In the first step, the state-space equations of the converter in (1) are obtained by the mode analysis of the PWM dc–dc converter. The detailed procedure for deriving state-space equations of the PWM dc–dc converter is available in [42, Sec. III], which is not repeated here. In this verification, the topologies of the six examples are shown in Fig. 4, and the matrixes in the state-space equations of converters are listed in Table III, where

$$\begin{aligned} k_R &= R_L/(R_L + r_{C1}), \quad r_{\Sigma 1} = r_{L1,2} + r_{S1,2} \\ r_{\Sigma 2} &= r_{L1,2} + r_D, \qquad r_{\Sigma 3} = r_{\Sigma 2} + k_R r_{C1} \\ r_{\Sigma 4} &= r_{\Sigma 1} + r_{C2}, \qquad r_{\Sigma 5} = r_{\Sigma 2} + r_{C2} \\ r_{\Sigma 6} &= r_D + k_R r_{C1}, \qquad r_{\Sigma 7} = r_{\Sigma 4} + k_R r_{C1}. \end{aligned} \tag{27}$$

And the parameters of the main circuit are listed in Table IV, whose design process is shown in the Appendix.

In the second step, the state-space equations of the controller in (2) are obtained by the transfer function of the controller. This is a general model transform in the modern control theory, whose detailed process can be found in [43, Sec. II] and is not repeated here as well. In this verification, the controller is constituted by the proportional–integral (PI) and lead-compensation controller, whose transfer function is

$$H(s) = \left(K_P + \frac{K_I}{s}\right) \frac{1 + s/\omega_B}{1 + s/(\beta\omega_B)}. \tag{28}$$

And matrixes in the state-space equations of the controller are

$$\begin{aligned} \mathbf{A}_C &= \begin{bmatrix} -\beta\omega_B & 0 \\ K_I & 0 \end{bmatrix}, \quad \mathbf{B}_C = \begin{bmatrix} \beta\omega_B(1-\beta) \\ \beta K_I \end{bmatrix} \\ \mathbf{C}_C &= \begin{bmatrix} K_P & 1 \end{bmatrix}, \qquad \mathbf{D}_C = \beta K_P. \end{aligned} \tag{29}$$

The parameters of the controller are listed in Table V, whose design process is shown in the Appendix. For converters with the leading-edge carrier, two experiments are made for each converter, which are signed by case 1 and case 2.

In the third step, the state-space equations of the augmented time-variant model in (4) are obtained. In this verification,

TABLE IV
PARAMETERS OF CONVERTERS

Parameter	Sign	Value					
		Boost	Buck	Buck–boost	Double-boost	SEPIC	Cuk
Input voltage	V_{in}	25V	50V	40V	25V	25V	20V
Switching frequency	f	10kHz	10kHz	10kHz	10kHz	10kHz	10kHz
Reference voltage	V_{ref}	50V	35V	30V	75V	30V	40V
Inductance	$L_{1,2}$	500μH	500μH	500μH	500μH	500μH	500μH
Capacitance	$C_{1,2}$	100μF	100μF	100μF	100μF	100μF	100μF
Load resistance	R_{L}	50Ω	20Ω	20Ω	50Ω	20Ω	30Ω
ESR of inductor	$r_{\text{L}1,2}$	200mΩ	200mΩ	200mΩ	200mΩ	200mΩ	200mΩ
ESR of capacitor	$r_{\text{C}1,2}$	10mΩ	10mΩ	10mΩ	10mΩ	10mΩ	10mΩ
ESR of MOSFET	$r_{\text{S}1,2}$	40mΩ	40mΩ	40mΩ	40mΩ	40mΩ	40mΩ
ESR of diode	r_{D}	45mΩ	45mΩ	45mΩ	45mΩ	45mΩ	45mΩ
MOSFET	$S_{1,2}$	IRFP260N	IRFP260N	IRFP260N	IRFP260N	IRFP260N	IRFP260N
Diode	D	MBR20200	MBR20200	MBR20200	MBR20200	MBR20200	MBR20200

TABLE V
PARAMETERS OF CONTROLLERS

Converter	Carrier	Case	K_{P}	K_{I}	ω_{B}	β
Boost	Trailing-Edge	____	0.05	5	10000	3
	Leading-Edge	1	0.05	5	10000	6
	Leading-Edge	2	0.05	5	10000	1
	Triangular	____	0.05	5	10000	1.5
Buck	Trailing-Edge	____	0.04	12	10000	2
	Leading-Edge	1	0.04	12	10000	1
	Leading-Edge	2	0.04	12	10000	1.5
	Triangular	____	0.04	12	10000	1.2
Buck-Boost	Trailing-Edge	____	0.06	3	10000	3
	Leading-Edge	1	0.04	2	10000	6
	Leading-Edge	2	0.06	3	10000	1
	Triangular	____	0.04	2	10000	1.5
Double-Boost	Trailing-Edge	____	0.03	3	10000	3
	Leading-Edge	1	0.03	3	10000	6
	Leading-Edge	2	0.025	2.5	10000	1
	Triangular	____	0.025	2.5	10000	1.5
SEPIC	Trailing-Edge	____	0.04	8	10000	3
	Leading-Edge	1	0.04	8	10000	6
	Leading-Edge	2	0.04	8	10000	1
	Triangular	____	0.04	8	10000	1.5
Cuk	Trailing-Edge	____	0.04	4	10000	2
	Leading-Edge	1	0.04	4	10000	1
	Leading-Edge	2	0.04	4	10000	1.5
	Triangular	____	0.04	4	10000	1.2

they can be obtained by substituting matrixes of converters and controllers in Table III and (29) into (5).

In the fourth step, the open-loop transfer function of the PWM dc–dc converter is obtained by (18). As shown in Section II, the open-loop transfer function is represented by the matrixes in the augmented time-variant model explicitly. Therefore, the open-loop transfer function can be obtained by substituting matrixes of the augmented time-variant model into the proposed model directly.

In the final step, the stability of the PWM dc–dc converter is analyzed by the open-loop transfer function obtained by the proposed model. In this verification, the stability of the converter is analyzed with the bode diagram, which will be shown in the next section.

The application and derivation of the proposed mode are both based on the state-space equations of the converter and controller. For different converters and controllers, the values of matrixes are different. However, the mathematical forms of the state-space equations are the same. Therefore, as far as the state-space equations of converters and controllers are obtained, stability analysis can be conducted by the proposed model with the aforementioned five steps uniformly. Furthermore, as demonstrated in textbooks [42] and [43], state-space equations are extensively utilized for analyzing PWM dc–dc converters and controllers, which can be obtained through definitive formulation. Therefore, the proposed model exhibits good adaptability in analyzing different PWM dc–dc converters.

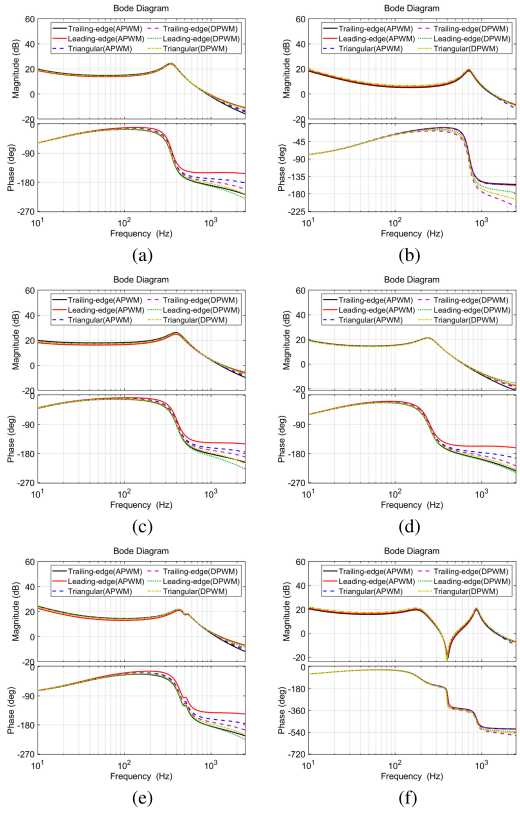

Fig. 5. Bode diagrams of converters with different carriers. (a) Boost converter. (b) Buck converter. (c) Buck–boost converter. (d) Double-boost converter. (e) SEPIC converter. (f) Cuk converter.

B. Results of the Verification

On the one hand, the bode diagrams of converters with different carriers are compared, which are shown in Fig. 5. As this

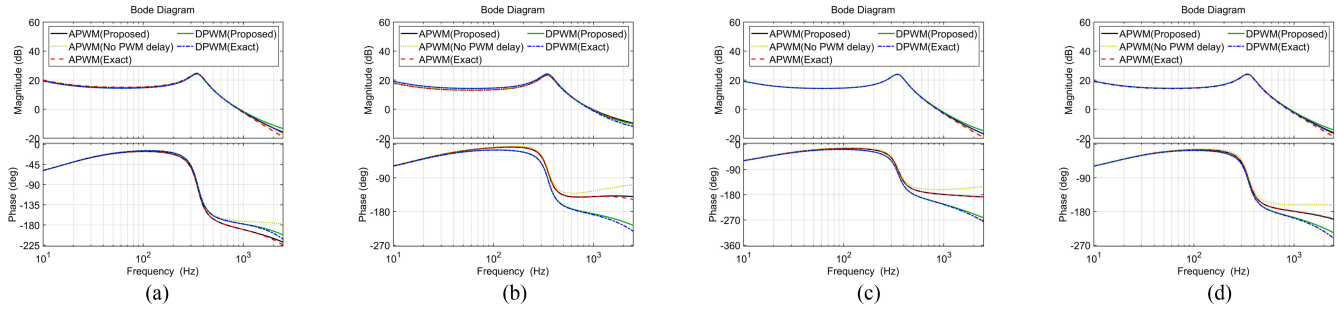

Fig. 6. Bode diagrams of the boost converter with different modulation methods. (a) Trailing-edge carrier. (b) Leading-edge carrier (case 1). (c) Leading-edge carrier (case 2). (d) Triangular carrier.

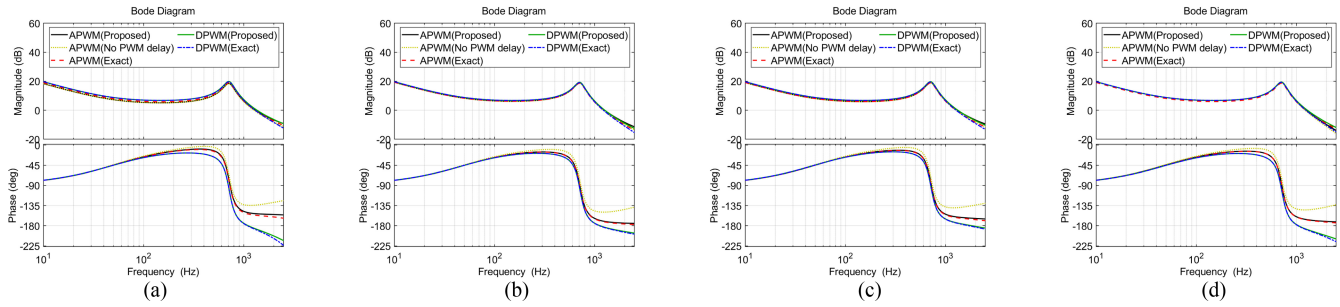

Fig. 7. Bode diagrams of the buck converter with different modulation methods. (a) Trailing-edge carrier. (b) Leading-edge carrier (case 1). (c) Leading-edge carrier (case 2). (d) Triangular carrier.

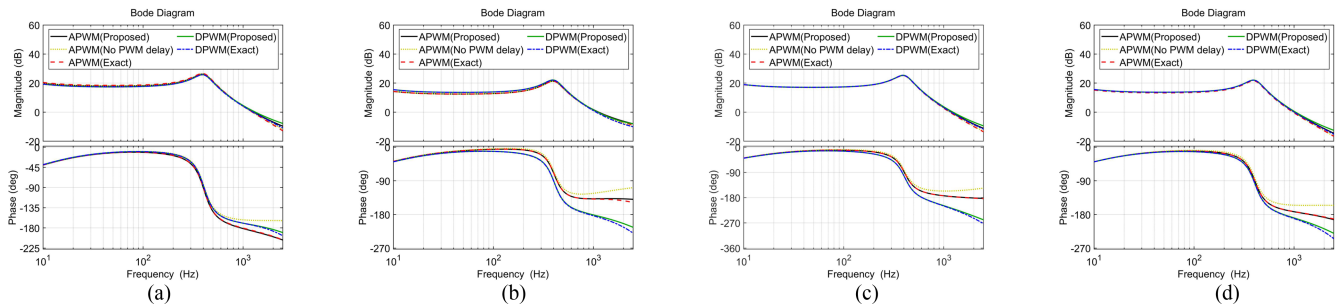

Fig. 8. Bode diagrams of the buck–boost converter with different modulation methods. (a) Trailing-edge carrier. (b) Leading-edge carrier (case 1). (c) Leading-edge carrier (case 2). (d) Triangular carrier.

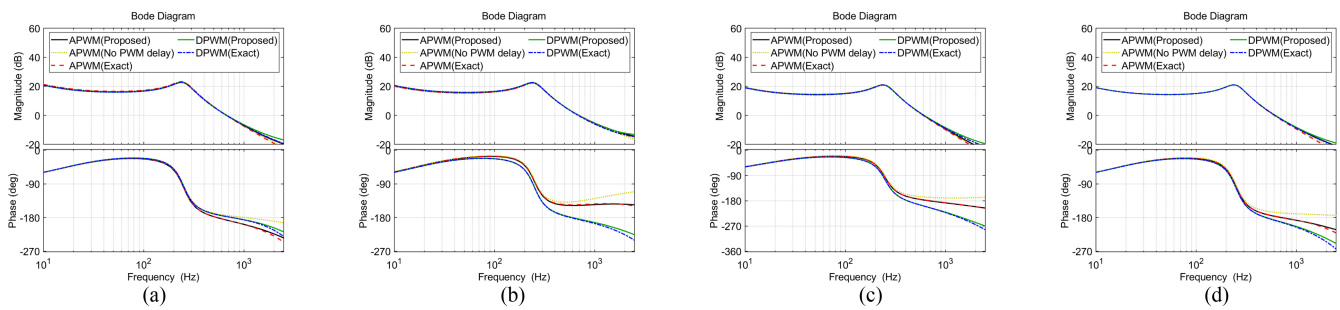

Fig. 9. Bode diagrams of the double-boost converter with different modulation methods. (a) Trailing-edge carrier. (b) Leading-edge carrier (case 1). (c) Leading-edge carrier (case 2). (d) Triangular carrier.

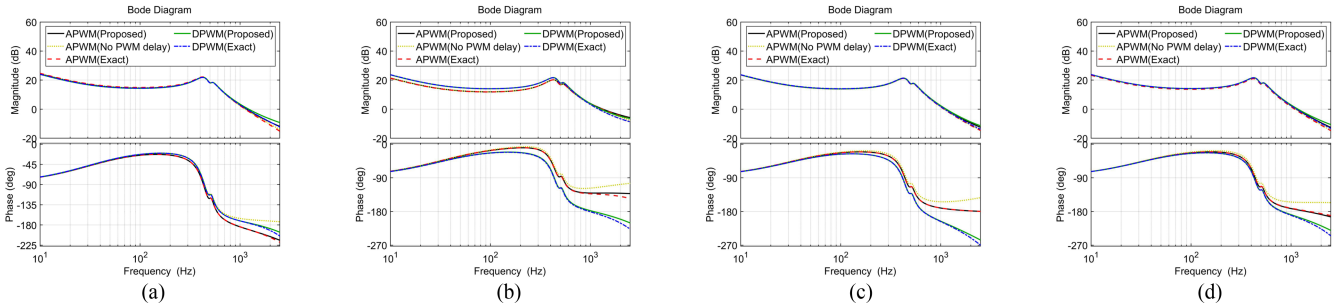

Fig. 10. Bode diagrams of the SEPIC converter with different modulation methods. (a) Trailing-edge carrier. (b) Leading-edge carrier (case 1). (c) Leading-edge carrier (case 2). (d) Triangular carrier.

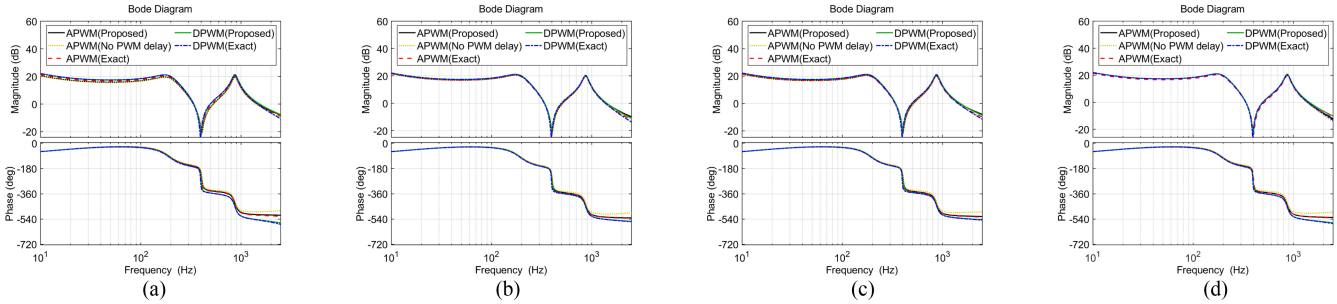

Fig. 11. Bode diagrams of the cuk converter with different modulation methods. (a) Trailing-edge carrier. (b) Leading-edge carrier (case 1). (c) Leading-edge carrier (case 2). (d) Triangular carrier.

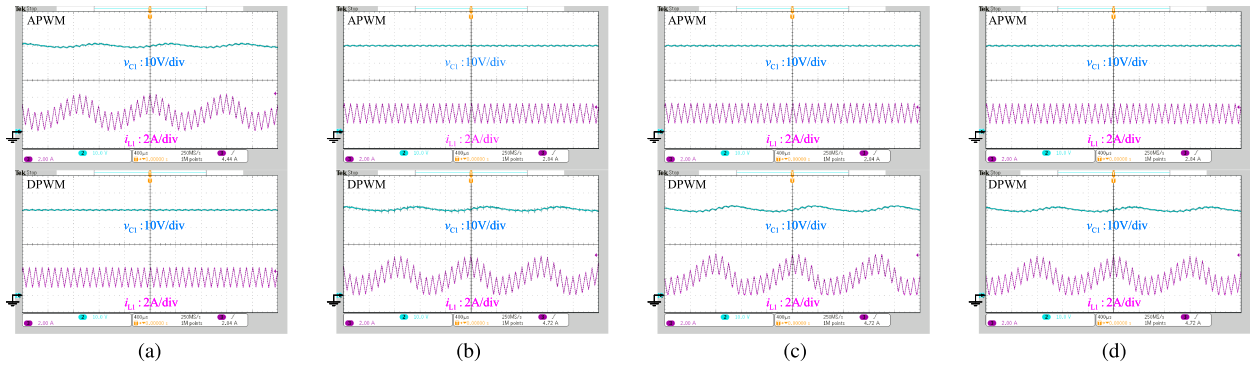

Fig. 12. Experiment waveforms of the boost converter. (a) Trailing-edge carrier. (b) Leading-edge carrier (case 1). (c) Leading-edge carrier (case 2). (d) Triangular carrier.

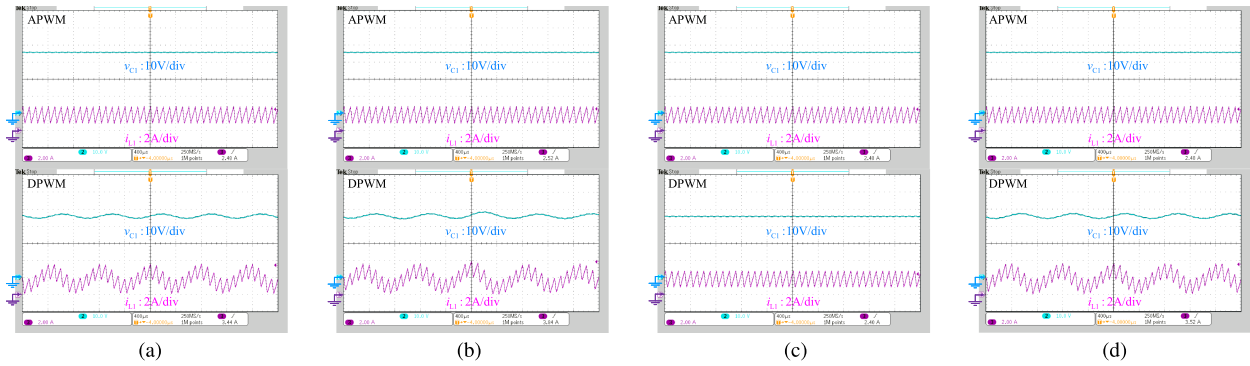

Fig. 13. Experiment waveforms of the buck converter. (a) Trailing-edge carrier. (b) Leading-edge carrier (case 1). (c) Leading-edge carrier (case 2). (d) Triangular carrier.

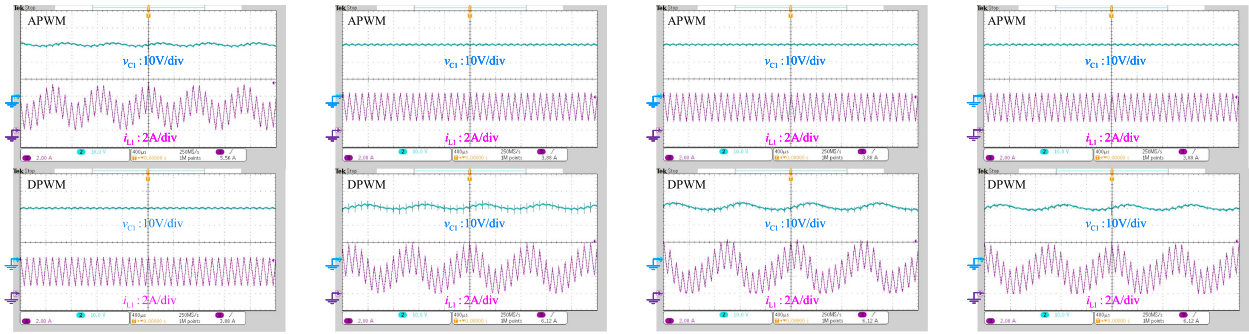

Fig. 14. Experiment waveforms of the buck–boost converter. (a) Trailing-edge carrier. (b) Leading-edge carrier (case 1). (c) Leading-edge carrier (case 2). (d) Triangular carrier.

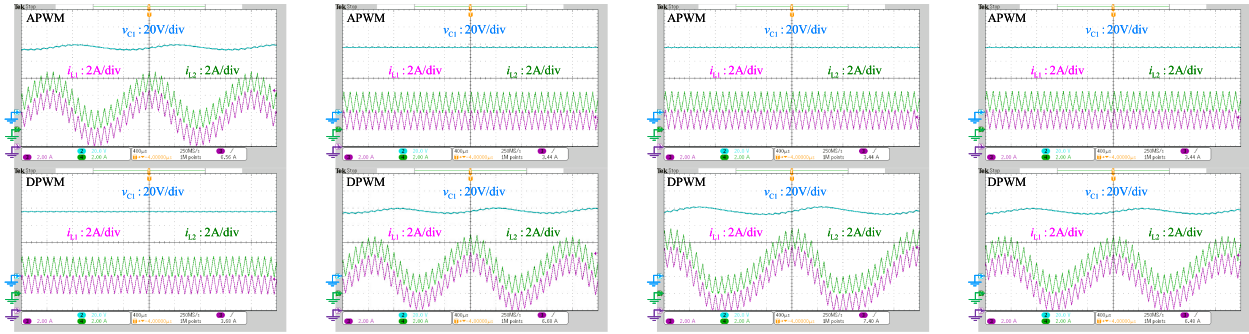

Fig. 15. Experiment waveforms of the double-boost converter. (a) Trailing-edge carrier. (b) Leading-edge carrier (case 1). (c) Leading-edge carrier (case 2). (d) Triangular carrier.

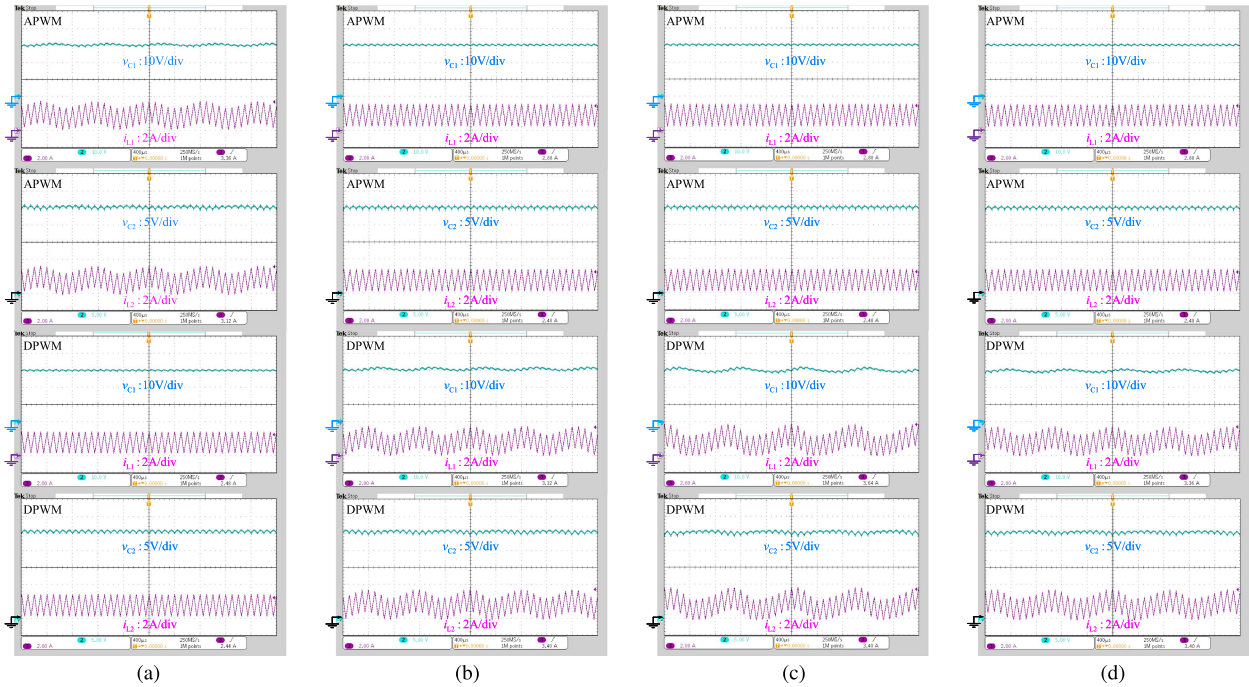

Fig. 16. Experiment waveforms of the SEPIC converter. (a) Trailing-edge carrier. (b) Leading-edge carrier (case 1). (c) Leading-edge carrier (case 2). (d) Triangular carrier.

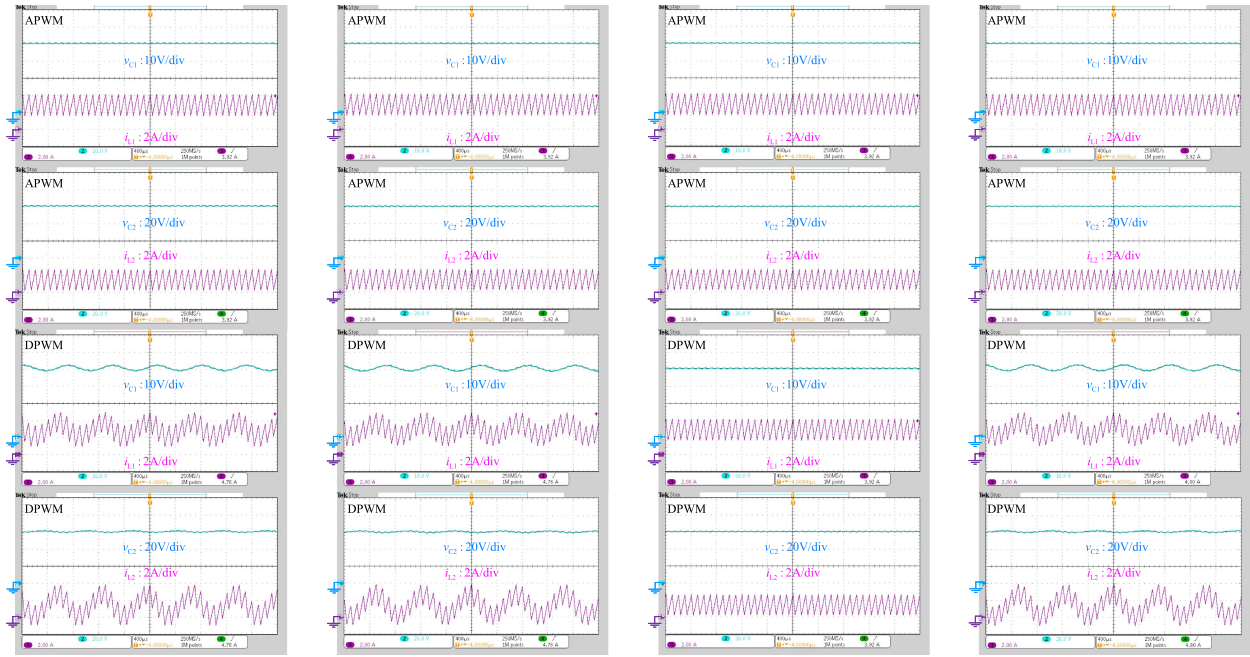

Fig. 17. Experiment waveforms of the cuk converter. (a) Trailing-edge carrier. (b) Leading-edge carrier (case 1). (c) Leading-edge carrier (case 2). (d) Triangular carrier.

comparison only makes sense when the controller parameters of converters with different carriers are the same, the controller parameter of converters with the leading-edge and triangular carriers are changed the same as converters with the trailing-edge carrier momentarily. The temporary changes mentioned here are limited to this particular comparison only and do not affect the controller parameters of converters used in other verifications.

As shown in Fig. 5, for the APWM boost, buck–boost, double-boost, and SEPIC converters, the $G_{\rm op}(s)$ of converters with the trailing-edge carrier have a phase lag than those of converters with the triangular carrier. $G_{\rm op}(s)$ of converters with the leading-edge carrier have a phase lead than those of converters with the triangular carrier. For the DPWM boost, buck–boost, double-boost, and SEPIC converters, the contrary is the case. For the APWM buck and cuk converters, $G_{\rm op}(s)$ of converters with different carriers are almost the same. For the DPWM buck and cuk converters, the $G_{\rm op}(s)$ of converters with different carriers have different phase-frequency characteristics. Therefore, for the APWM and DPWM converters with different carriers, the influences of PWM delay are different.

On the other hand, the bode diagrams of converters with different modulation methods are analyzed and compared with the experiment result. The results of the verification are summed and listed in Table VI. When the phase-frequency characteristic curve has no intersection with the -180° line, the magnitude margin is signed as $+\infty$. If the margins are positive, it means that based on this model, the converter is stable in this case. If the margins are negative, it means that based on this model, the converter is unstable in this case. Besides, for the six converters, the bode diagrams obtained by the proposed model and the exact time-variant model in the simulation are shown in Figs. 6–11. The experiment results of these converters with APWM and DPWM are shown in Figs. 12–17.

The experiment results verify the analyses of the proposed model. First, the APWM converter contains the PWM delay as well. As shown in Figs. 6–11, after considering the PWM delay, the transfer function of the proposed model fits well with the transfer function of the exact model. However, without considering the PWM delay, the transfer function has a phase advance than the transfer function of the exact model at the high-frequency band. Ignoring the PWM delay leads to error at the high-frequency band, and the modeling of the APWM converter should consider the PWM delay as well.

Then, the stabilities of APWM and DPWM converters vary for different converters and carriers. As listed in Table VI, for the boost, buck–boost, double-boost, and SEPIC converters with triangular and leading-edge carriers, the DPWM converter is more unstable than the APWM converter. The same phenomenon also arises in buck and cuk converters with all three types of carriers. However, for the boost, buck–boost, double-boost, and SEPIC converters with the trailing-edge carrier, the APWM converter is more unstable than the DPWM converter. The stability of the DPWM converter is not always worse than the APWM converter, which is the same as the analysis in Section III.

Finally, only the proposed model can reflect all cases accurately. As listed in Table VI, for the six basic converters with three kinds of carriers, among all 24 cases, the stabilities of APWM and DPWM converters are different in 22 cases. For the SSA model, as the PWM delay in the APWM and DPWM converters are both ignored, the margins of APWM and DPWM converters

TABLE VI
RESULTS OF VERIFICATION

Converter Type	Carrier Type	PWM Type	Magnitude margin				Phase margin				Experiment Result
			SSA	ZOH	DF	Proposed	SSA	ZOH	DF	Proposed	
Boost	Trailing-Edge	APWM	13.7dB	13.7dB	13.7dB	−5.69dB	12.7°	12.7°	12.7°	−7.45°	Unstable
		DPWM	13.7dB	−2.94dB	−3.17dB	3.71dB	12.7°	−3.97°	−4.32°	3.82°	Stable
	Leading-Edge (Case 1)	APWM	17.4dB	17.4dB	17.4dB	+∞dB	18.1°	18.1°	18.1°	39.8°	Stable
		DPWM	17.4dB	1.84dB	2.10dB	−3.39dB	18.1°	2.09°	2.38°	−4.70°	Unstable
	Leading-Edge (Case 2)	APWM	−4.13dB	−4.13dB	−4.13dB	3.96dB	−4.93°	−4.93°	−4.93°	2.84°	Stable
		DPWM	−4.13dB	−10.7dB	−10.6dB	−12.7dB	−4.93°	−20.3°	−20.0°	−28.3°	Unstable
	Triangular	APWM	3.33dB	3.33dB	3.33dB	2.81dB	3.10°	3.10°	3.10°	2.67°	Stable
		DPWM	3.33dB	−7.93dB	−7.93dB	−7.60dB	3.10°	−13.4°	−13.4°	−12.5°	Untable
Buck	Trailing-Edge	APWM	+∞dB	+∞dB	+∞dB	+∞dB	25.3°	25.3°	25.3°	27.0°	Stable
		DPWM	+∞dB	1.57dB	−4.21dB	−4.55dB	25.3°	2.13°	−6.92°	−8.10°	Unstable
	Leading-Edge (Case 1)	APWM	+∞dB	+∞dB	+∞dB	+∞dB	9.35°	9.35°	9.35°	9.72°	Stable
		DPWM	+∞dB	−7.13dB	−2.70dB	−2.74dB	9.35°	−12.7°	−3.58°	−3.48°	Unstable
	Leading-Edge (Case 2)	APWM	+∞dB	+∞dB	+∞dB	+∞dB	19.2°	19.2°	19.2°	19.4°	Stable
		DPWM	+∞dB	−2.47dB	5.23dB	5.89dB	19.2°	−3.67°	5.75°	5.96°	Stable
	Triangular	APWM	+∞dB	+∞dB	+∞dB	+∞dB	13.9°	13.9°	13.9°	13.9°	Stable
		DPWM	+∞dB	−5.24dB	−5.24dB	−5.24dB	13.9°	−8.56°	−8.56°	−8.56°	Unstable
Buck-Boost	Trailing-Edge	APWM	10.8dB	10.8dB	10.8dB	−5.34dB	15.7°	15.7°	15.7°	−7.58°	Unstable
		DPWM	10.8dB	−4.12dB	−2.72dB	3.68dB	15.7°	−7.85°	−4.95°	5.53°	Stable
	Leading-Edge (Case 1)	APWM	17.7dB	17.7dB	17.7dB	+∞dB	24.6°	24.6°	24.6°	42.0°	Stable
		DPWM	17.7dB	3.71dB	2.15dB	−2.20dB	24.6°	5.71°	3.41°	−4.08°	Unstable
	Leading-Edge (Case 2)	APWM	−4.02dB	−4.02dB	−4.02dB	5.98dB	−5.08°	−5.08°	−5.08°	4.02°	Stable
		DPWM	−4.02dB	−12.0dB	−12.6dB	−14.5dB	−5.08°	−26.5°	−29.1°	−39.3°	Unstable
	Triangular	APWM	6.28dB	6.28dB	6.28dB	6.20dB	7.21°	7.21°	7.21°	7.10°	Stable
		DPWM	6.28dB	−5.66dB	−5.66dB	−5.36dB	7.21°	−11.3°	−11.3°	−10.5°	Unstable
Double-Boost	Trailing-Edge	APWM	10.8dB	10.8dB	10.8dB	−4.41dB	9.08°	9.08°	9.08°	−6.76°	Unstable
		DPWM	10.8dB	−2.32dB	−2.51dB	1.98dB	9.08°	−3.44°	−3.75°	2.34°	Stable
	Leading-Edge (Case 1)	APWM	13.0dB	13.0dB	13.0dB	+∞dB	18.1°	18.1°	18.1°	32.6°	Stable
		DPWM	13.0dB	0.83dB	1.09dB	−2.52dB	18.1°	1.04°	1.35°	−3.82°	Unstable
	Leading-Edge (Case 2)	APWM	−1.83dB	−1.83dB	−1.83dB	2.31dB	−2.70°	−2.70°	−2.70°	2.63°	Stable
		DPWM	−1.83dB	−6.60dB	−6.50dB	−8.26dB	−2.70°	−13.5°	−13.2°	−19.1°	Unstable
	Triangular	APWM	2.98dB	2.98dB	2.98dB	2.67dB	3.49°	3.49°	3.49°	3.17°	Stable
		DPWM	2.98dB	−4.37dB	−4.37dB	−4.12dB	3.49°	−7.92°	−7.92°	−7.33°	Unstable
SEPIC	Trailing-Edge	APWM	12.2dB	12.2dB	12.2dB	−5.28dB	16.7°	16.7°	16.7°	−8.71°	Unstable
		DPWM	12.2dB	−2.59dB	−3.70dB	3.03dB	16.7°	−4.83°	−7.20°	4.62o	Stable
	Leading-Edge (Case 1)	APWM	15.8dB	15.8dB	15.8dB	+∞dB	24.4°	24.4°	24.4°	49.4°	Stable
		DPWM	15.8dB	1.72dB	3.18dB	−2.57dB	24.4°	2.95°	5.30°	−5.06°	Unstable
	Leading-Edge (Case 2)	APWM	−2.18dB	−2.18dB	−2.18dB	14.4dB	−2.92°	−2.92°	−2.92°	7.40°	Stable
		DPWM	−2.18dB	−9.81dB	−9.24dB	−11.7dB	−2.92°	−22.9°	−20.7°	−32.3°	Unstable
	Triangular	APWM	4.12dB	4.12dB	4.12dB	4.03dB	5.04°	5.04°	5.04°	4.93°	Stable
		DPWM	4.12dB	−7.33dB	−7.33dB	−6.95dB	5.04°	−15.9°	−15.9°	−14.7°	Unstable
Cuk	Trailing-Edge	APWM	14.1dB	14.1dB	14.1dB	11.2dB	19.4°	19.4°	19.4°	18.6°	Stable
		DPWM	14.1dB	1.87dB	−3.12dB	−3.59dB	19.4°	3.00°	−5.53°	−6.89°	Unstable
	Leading-Edge (Case 1)	APWM	11.0dB	11.0dB	11.0dB	8.12dB	13.7°	13.7°	13.7°	11.9°	Stable
		DPWM	11.0dB	−6.84dB	−2.48dB	−2.42dB	13.7°	−12.0°	−3.50°	−3.29°	Unstable
	Leading-Edge (Case 2)	APWM	13.2dB	13.2dB	13.2dB	9.47dB	17.5°	17.5°	17.5°	15.3°	Stable
		DPWM	13.2dB	−1.86dB	4.35dB	4.85dB	17.5°	−3.00°	5.86°	6.17°	Stable
	Triangular	APWM	12.1dB	12.1dB	12.1dB	12.1dB	17.1°	17.1°	17.1°	17.1°	Stable
		DPWM	12.1dB	−4.75dB	−4.75dB	−4.75dB	17.1°	−7.94°	−7.94°	−7.94°	Unstable

are the same, and the SSA model cannot reflect the stability of converters accurately. After considering the PWM delay in the DPWM converter, the ZOH and DF models are more accurate than the SSA model.

For converters with the triangular carrier, the ZOH and DF models have good accuracy. However, due to inaccurate physical interpretation and description of PWM delay in the ZOH and DF models, they still cannot achieve an accurate prediction of stability. For the APWM and DPWM boost, buck–boost, double-boost, and SEPIC converters with the trailing-edge carrier, the stability predicted by the ZOH and DF model is just opposite to the experiment results. For the APWM and DPWM boost, buck–boost, double-boost, and SEPIC converters with leading-edge carriers, the stabilities are different in the two cases of each converter. But their stabilities predicted by the ZOH and DF models are the same, which is different from the experiment results as well. Besides, the ZOH model cannot predict the stability of the buck and cuk converters with trailing-edge and leading-edge carriers.

Compared with the above three models, only the results of the proposed model fit well with the experiment results in all cases. After considering the PWM delay and state feedback caused by the ripple, the proposed model can reflect the stability of different converters, controllers, and carriers with a unified model, which is more accurate than other models.

V. CONCLUSION

In this article, the effect of PWM delay on the stability of PWM dc–dc converters is analyzed. A unified frequency-domain model considering the PWM delay is proposed. Based on the proposed model, the physical mechanism of the PWM delay is

the sampling characteristic of the modulation process rather than the digital controller. As the APWM and DPWM converters both have the modulation process, they both have the PWM delay. Besides, the different stabilities of APWM and DPWM converters are compared, which are caused by the state feedback introduced by the output ripple in the APWM converter. For converters with the triangular carrier, this state feedback eliminates the PWM delay, and the stability of the APWM converter is always better than the DPWM converter. However, for converters with other carriers, the PWM delay is no more eliminated and the effect of this state feedback varies for different converters and carriers. These influences are rarely reported in existing analyses of the modulation and can only be reflected by the proposed model.

To ensure the above analyses, the stability of basic converters is analyzed by the proposed model, whose results are compared with existing models and experiments. Compared with existing models, only the proposed model can reflect the different effects of PWM delay and state feedback in APWM and DPWM converters. The proposed model is more accurate than the existing models. Generally, the stability analysis and stabilization control of PWM dc–dc converters are based on these models. The proposed method is a potential alternative to these models when high precision is required.

APPENDIX

A. Derivations in the Proposed Model

First, the derivation of (11)–(13) is shown. The Taylor expansions of $\mathbf{\Phi}$ and $\mathbf{\Gamma}$ in (7) are

$$\begin{cases} \mathbf{\Phi} = \mathbf{E} + \mathbf{A}_1^* d_n T + \mathbf{A}_2^*(1-d_n)T + \frac{1}{2}\mathbf{A}_1^{*2} d_n^2 T^2 \\ \quad + \mathbf{A}_2^*\mathbf{A}_1^* d_n(1-d_n)T^2 + \frac{1}{2}\mathbf{A}_2^{*2}(1-d_n)^2 T^2 \\ \quad + O(T^3) \\ \mathbf{\Gamma} = \mathbf{B}_1^* d_n T + \mathbf{B}_2^*(1-d_n)T + \frac{1}{2}\mathbf{A}_1^*\mathbf{B}_1^* d_n^2 T^2 \\ \quad + \mathbf{A}_2^*\mathbf{B}_1^* d_n(1-d_n)T^2 + \frac{1}{2}\mathbf{A}_2^*\mathbf{B}_2^*(1-d_n)^2 T^2 \\ \quad + O(T^3) \end{cases} \tag{A1}$$

The Taylor expansions of $\mathbf{\Phi}$ and $\mathbf{\Gamma}$ in (8) are

$$\begin{cases} \mathbf{\Phi} = \mathbf{E} + \begin{bmatrix} \mathbf{A}_{\text{ave}} & 0 \\ -\mathbf{B}_{\text{C}}\mathbf{C}_1 & \mathbf{A}_{\text{C}} \end{bmatrix} T + \frac{1}{2}\begin{bmatrix} \mathbf{A}_{\text{ave}}^2 & 0 \\ -\mathbf{A}_{\text{C}}\mathbf{B}_{\text{C}}\mathbf{C}_1 & \mathbf{A}_{\text{C}}^2 \end{bmatrix} T^2 \\ \quad + \frac{1}{2}\begin{bmatrix} \mathbf{A}_2\mathbf{A}_1 - \mathbf{A}_1\mathbf{A}_2 & 0 \\ 0 & 0 \end{bmatrix} d_n(1-d_n)T^2 + O(T^3) \\ \mathbf{\Gamma} = \mathbf{B}_1^* d_n T + \mathbf{B}_2^*(1-d_n)T + \frac{1}{2}\mathbf{A}_2^*\mathbf{B}_2^*(1-d_n)^2 T^2 \\ \quad + \mathbf{A}_2^*\mathbf{B}_1^* d_n(1-d_n)T^2 + \frac{1}{2}\mathbf{A}_1^*\mathbf{B}_1^* d_n^2 T^2 + O(T^3) \end{cases} \tag{A2}$$

where

$$\mathbf{A}_{\text{ave}} = \mathbf{A}_1 d_n + \mathbf{A}_2(1-d_n). \tag{A3}$$

And the Taylor expansions of $\mathbf{\Phi}$ and $\mathbf{\Gamma}$ in (10) are

$$\begin{cases} \mathbf{\Phi} = \mathbf{E} + \mathbf{A}_{\text{eq}} T + \frac{1}{2}\mathbf{A}_{\text{eq}}^2 T^2 + O(T^3) \\ \mathbf{\Gamma} = \mathbf{B}_{\text{eq}} T + \frac{1}{2}\mathbf{A}_{\text{eq}}\mathbf{B}_{\text{eq}} T^2 + O(T^3) \end{cases}. \tag{A4}$$

Comparing (A1)–(A2) with (A4) and ignoring the difference between $\mathbf{C}_1$ and $\mathbf{C}_2$, (11)–(13) can be obtained.

Then, the exact value of $\mathbf{G}_{vx}(s)$ in Table II is derived. As shown in Fig. 1, for the DPWM converter, $v_{\text{m}}(t)$ is constant in a switching period. Therefore, as shown in Table II, $\mathbf{G}_{vx}(s)$ is equal to the output matrix directly.

As shown in Fig. 2, for the APWM converter, $v_{\text{m}}(t)$ is varying in a switching period. According to (4) and (6), $v_{\text{m}}(t)$ can be obtained by $\mathbf{x}_{\text{eq}}(t)$ and $\mathbf{u}^*(t)$. As shown in Fig. 2(a), for converters with the trailing-edge carrier, d_n is equal to $v_{\text{m}}(nT + d_n T)$

$$\begin{aligned} v_{\text{m}}(nT + d_n T) &= \mathbf{C}_1^* e^{\mathbf{A}_1^* d_n T}\mathbf{x}_{\text{eq}}(t) + \mathbf{D}_{\text{C}} V_{\text{ref}} \\ &\quad + \mathbf{C}_1^* \int_0^{d_n T} e^{-\mathbf{A}_1^* \tau} d\tau \mathbf{B}_1^* \mathbf{u}^*(t). \end{aligned} \tag{A5}$$

As shown in Fig. 2(b), for converters with the leading-edge carrier, d_n is equal to $v_{\text{m}}(nT + T - d_n T)$

$$\begin{aligned} v_{\text{m}}(nT + T - d_n T) &= \mathbf{C}_2^* e^{\mathbf{A}_2^*(1-d_n)T}\mathbf{x}_{\text{eq}}(t) + \mathbf{D}_{\text{C}} V_{\text{ref}} \\ &\quad + \mathbf{C}_2^* \int_0^{(1-d_n)T} e^{-\mathbf{A}_2^* \tau} d\tau \mathbf{B}_2^* \mathbf{u}^*(t). \end{aligned} \tag{A6}$$

As shown in Fig. 2(c), for converters with the triangular carrier, d_n is equal to the average value of $v_{\text{m}}(nT + 0.5 d_n T)$ and $v_{\text{m}}(nT + T - 0.5 d_n T)$

$$\begin{aligned} v_{\text{m}}(nT + 0.5 d_n T) &= \mathbf{C}_1^* e^{\mathbf{A}_1^* 0.5 d_n T}\mathbf{x}_{\text{eq}}(t) + \mathbf{D}_{\text{C}} V_{\text{ref}} \\ &\quad + \mathbf{C}_1^* \int_0^{0.5 d_n T} e^{-\mathbf{A}_1^* \tau} d\tau \mathbf{B}_1^* \mathbf{u}^*(t) \end{aligned} \tag{A7}$$

$$\begin{aligned} v_{\text{m}}(nT + T - 0.5 d_n T) &= \mathbf{C}_1^* e^{-\mathbf{A}_1^* 0.5 d_n T}\mathbf{x}_{\text{eq}}(t+T) + \mathbf{D}_{\text{C}} V_{\text{ref}} \\ &\quad + \mathbf{C}_1^* \int_0^{-0.5 d_n T} e^{-\mathbf{A}_1^* \tau} d\tau \mathbf{B}_1^* \mathbf{u}^*(t+T). \end{aligned} \tag{A8}$$

Considering the modulation process expressed by (16), the relationship between $\hat{v}_{\text{m}}(s)$ and $\hat{\mathbf{x}}_{\text{eq}}(s)$ can be obtained by the small-signal analysis of (A5)–(A8)

$$\begin{aligned} \hat{v}_{\text{m}}(s) &= \mathbf{G}_{vx}^*(s)\hat{\mathbf{x}}_{\text{eq}}(s) + G_{vd}(s)\hat{d}_n(s) \\ &= \frac{\mathbf{G}_{vx}^*(s)}{1 - G_{vd}(s)G_{\text{ZOH}}(s)}\hat{\mathbf{x}}_{\text{eq}}(s). \end{aligned} \tag{A9}$$

For converters with the trailing-edge carrier, transfer functions in (A9) are

$$\begin{cases} \mathbf{G}_{vx}^*(s) = \mathbf{C}_1^* e^{\mathbf{A}_1^* \bar{d}_n T} \\ G_{vd}(s) = \mathbf{C}_1^* e^{\mathbf{A}_1^* \bar{d}_n T}(\mathbf{A}_1^* \bar{\mathbf{x}}_{\text{eq}} + \mathbf{B}_1^* \bar{\mathbf{u}}^*) T \end{cases}. \tag{A10}$$

For converters with the leading-edge carrier, they are

$$\begin{cases} \mathbf{G}_{vx}^*(s) = \mathbf{C}_2^* e^{\mathbf{A}_2^*(1-\bar{d}_n)T} \\ G_{vd}(s) = -\mathbf{C}_2^* e^{\mathbf{A}_2^*(1-\bar{d}_n)T}(\mathbf{A}_2^* \bar{\mathbf{x}}_{\text{eq}} + \mathbf{B}_2^* \bar{\mathbf{u}}^*) T \end{cases}. \tag{A11}$$

For converters with the triangular carrier, they are

$$\begin{cases} \mathbf{G}_{vx}^*(s) = 0.5\left(\mathbf{C}_1^* e^{0.5\mathbf{A}_1^* \bar{d}_n T} + \mathbf{C}_2^* e^{-0.5\mathbf{A}_1^* \bar{d}_n T} e^{sT}\right) \\ G_{vd}(s) = 0.5\mathbf{C}_1^* e^{0.5\mathbf{A}_1^* \bar{d}_n T}(\mathbf{A}_1^* \bar{\mathbf{x}}_{\text{eq}} + \mathbf{B}_1^* \bar{\mathbf{u}}^*) T \\ \qquad - 0.5\mathbf{C}_2^* e^{-0.5\mathbf{A}_1^* \bar{d}_n T}(\mathbf{A}_1^* \bar{\mathbf{x}}_{\text{eq}} + \mathbf{B}_1^* \bar{\mathbf{u}}^*) T \end{cases}. \tag{A12}$$

Substituting (A10)–(A12) into (A9), $\mathbf{G}_{vx}(s)$ of the APWM converter in Table II can be obtained.

B. Parameter Design of the Verification

First, the parameter design process of the converter is shown. For the input voltage, output voltage, and load resistance, the voltage level and power level are similar to the previous modeling research of PWM dc–dc converter, which is common in the application [28], [29], [30], [31].

For the inductor, the inductance is chosen to make sure that the converter is in continuous conduction mode (CCM). Based on the mode analysis of basic converters [41], [44], the inductance L should satisfy the following equations:

$$L \geq \begin{cases} \frac{1}{2}\bar{d}_n(1-\bar{d}_n)^2 R_{\mathrm{L}} T, & \text{Boost} \\ \frac{1}{2}(1-\bar{d}_n) R_{\mathrm{L}} T, & \text{Buck} \\ \frac{1}{2}(1-\bar{d}_n)^2 R_{\mathrm{L}} T, & \text{Buck–boost} \\ \frac{1}{2}\bar{d}_n(1-\bar{d}_n)^2(1+\bar{d}_n)^{-1} R_{\mathrm{L}} T, & \text{Double-boost} \\ \frac{1}{2}\bar{d}_n^{-1}(1-\bar{d}_n)^2 R_{\mathrm{L}} T, & \text{Other.} \end{cases} \tag{A13}$$

As calculated by (A13), for the boost, buck, buck–boost, double-boost, SEPIC, and cuk converters, the inductance should be larger than 312.5 μH, 300 μH, 326.5 μH, 208.3 μH, 378.8 μH, and 250 μH, respectively. Therefore, the inductance is chosen as 500 μH.

For the capacitor, the capacitance is chosen to make sure that the peak-to-peak value of output voltage ripple ΔV_{o} is lower than 1 V. Based on the mode analysis of basic converters [41], [44], the capacitance C should satisfy the following equations:

$$C \geq \begin{cases} (1-\bar{d}_n) V_{\mathrm{o}} T^2/(8\Delta V_{\mathrm{o}} L), & \text{Buck and cuk} \\ \bar{d}_n I_{\mathrm{o}} T \Delta V_{\mathrm{o}}^{-1}, & \text{Other} \end{cases} \tag{A14}$$

where I_{o} is the output current.

As calculated by (A14), for the boost, buck, buck–boost, double-boost, SEPIC, and cuk converters, the capacitance should be larger than 50 μF, 26.3 μF, 64.2 μF, 75 μF, 81.8 μF, and 33.3 μF, respectively. Therefore, the capacitance is chosen as 100 μF.

For the MOSFET and diode, the maximum voltage stresses of the boost, buck, buck–boost, double-boost, SEPIC, and cuk converters are 50 V, 50 V, 70 V, 75 V, 55 V, and 60 V, respectively. Generally, the breakdown voltage of switch devices should be two to four times the voltage stress. Therefore, the IRFP260N and MBR20200 are used, whose breakdown voltage is 200 V.

Then, the parameter design process of the controller is shown. The main purpose of the verification is to show the different effects of APWM and DPWM on the converter. Therefore, to make a fair comparison, the same controller parameters should be used for the analog and digital controllers. Otherwise, the difference is caused by the different controller parameters rather than the different PWM delays. Besides, the controller parameters are designed to make the converter close to the critical point between stable and unstable operation. In this way, the different effects of APWM and DPWM can be observed by the stable and unstable operation of the converter directly, which can enhance the persuasion of the verification.

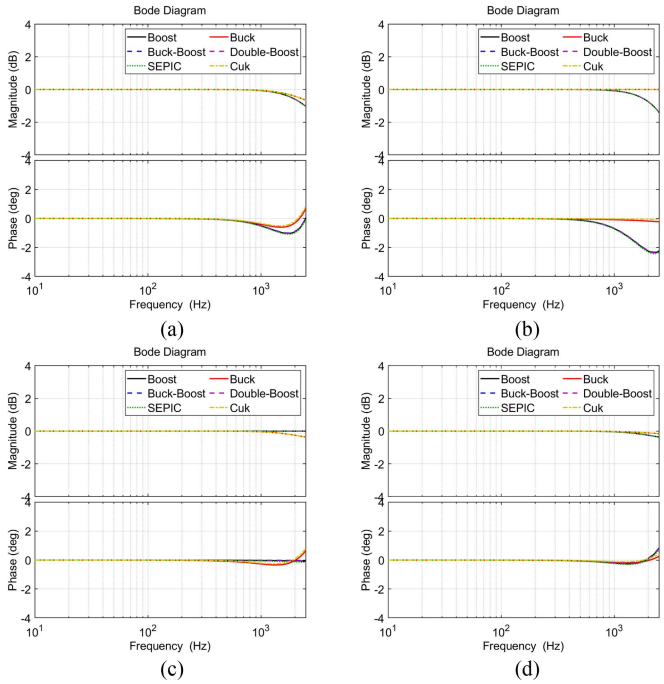

Fig. 18. Bode diagram of $H(s)/H(z)$. (a) Trailing-edge carrier. (b) Leading-edge carrier (case 1). (c) Leading-edge carrier (case 2). (d) Triangular carrier.

Besides, for the DPWM converter, the discrete controller $H(z)$ is obtained by the bilinear transformation of (28)

$$H(z) = \left(K_{\mathrm{P}} + K_{\mathrm{I}} \frac{T}{2} \frac{z+1}{z-1}\right) \frac{T(z+1) + 2(z-1)/\omega_{\mathrm{B}}}{T(z+1) + 2(z-1)/(\beta\omega_{\mathrm{B}})}. \tag{A15}$$

To make sure that the difference is not caused by the error of the bilinear transformation, the bode diagram of $H(s)/H(z)$ is shown in Fig. 18. As shown in Fig. 18, in the frequency band of the research, for the used controller, the maximum magnitude error is 1.42 dB, and the maximum phase error is 2.42°. These errors are much smaller than the difference between APWM and DPWM converters in the research, which can be ignored. The transfer function of the controller in the APWM and DPWM converters can be seen as the same.

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