A Two-Step Self-Startup Hybrid Structure Step-Up Converter Using Standard 5P0 MOSFETs Achieving 36 × Voltage Boosting With 50 mV Input Voltage and 84 × Input Voltage Range for Self-Powered IoT Applications

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***Abstract*—This article presents a hybrid structure step-up converter to achieve self-startup at ultralow input voltage and very wide input voltage range. To realize self-startup, a two-step self-startup strategy is designed, which involves three periods (charge pump self-startup period, hybrid mode period, and boost operating period). To further reduce the self-startup voltage and promote driving capability, a multistage multiphase charge pump with body-bias controlled ring oscillator is proposed. By optimizing design of the ring oscillator, the output ripple of the charge pump is reduced significantly. To solve the inherent contradiction between body-bias technique and operating voltage range, current limitation technique is adopted. The converter is fabricated by using standard 180 nm 5P0 CMOS process with 4.8 mm^2 chip area. Measurement results show that the converter can kick-start at 440 mV input voltage, and provide over 96.35 mW at 300 mV input voltage. The input voltage range is up to 84× (50 mV–4.2 V). The output voltage can be maintained at 1.8 V with the minimum input voltage of 50 mV, where 36× voltage step-up ratio is obtained. The maximum inductor current reaches 2 A, and the peak power conversion efficiency of 95.6% is achieved.**

***Index Terms*—Body-bias, charge pump, hybrid structure, multiphase, multistage, self-startup, step-up converter, voltage boosting.**

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I. INTRODUCTION

Wireless sensor networks (WSNs) and Internet of Things (IoTs) have developed rapidly in recent years. In order to achieve high system performance, most of the devices in WSN are scattered everywhere in the environment for sensing and detection [1], [2]. These devices are small in size and low in power consumption, but they are voluminous. Therefore, high integration, low maintenance cost, battery-less and self-powering solutions have become the focus of WSN devices. In the meantime, the increasing demand for IoTs application has brought great challenges to the power management system.

Under this background, energy harvesting technology as self-powering solution has been widely focused, which can harvest energy from the environment. Different energy sources, i.e., solar [3], [4], [5], vibration [6], [7], [8], radio frequency [9], [10], [11], acoustic [12], thermal [13], [14], triboelectric [15], electromagnetic [16], require different types of transducers and voltage range, therefore, a wide input voltage range is needed by the power management system [17], [18], [19]. As for low input voltage situation, the boost converter is widely used. For step-up converter, the minimum self-startup voltage and operating voltage with high performance are the essential features that needs to be considered carefully, especially when high breakdown voltage metal-oxide-semiconductor field-effect transistor (MOSFET) devices with high threshold voltage are employed in self-startup circuit to meet the requirement of wide input voltage range. Fig. 1 shows the research interests of step-up converter.

Employing auxiliary devices to precharge before starting up process as the prior startup techniques is widely used in boost converter. A low power boost converter for thermoelectric energy harvesting [20] reported that an external precharge capacitor is used to achieve 1 V output voltage with 20–250 mV input voltage range. The same method is mentioned in papers [21] and [22] to realize the similar function. External mechanical switches applied to control the charging period of the inductor by energy source is adopted to achieve self-startup [23]. A method of reusing off-chip transformers is presented to utilize *LC* autonomous oscillation by collecting external thermal

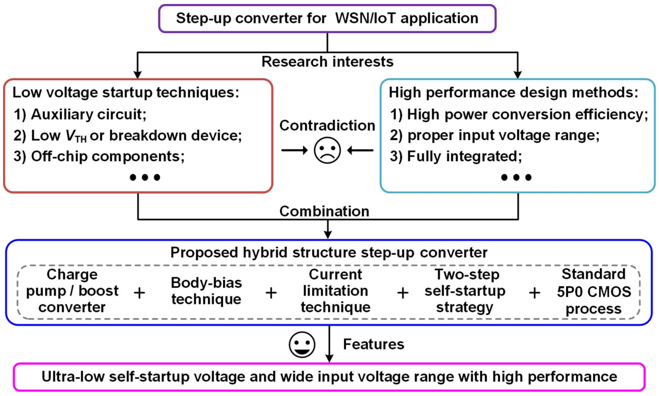


Fig. 1. Research interests of step-up converter.

noise to generate the internal supply voltage [24]. In addition, a boost converter with inductor peak current control method and zero current detection (ZCD) technique is reported, which can achieve 10 mV input self-startup [25].

Although the use of off-chip components can achieve lower self-startup voltage effectively, they are unbeneficial to system integration. Therefore, fully integrated self-startup techniques are widely studied. An on-chip switched-capacitor converter is proposed to realize directly charge the battery with 0.5 V input voltage [26]. A 95 mV startup voltage step-up converter is proposed by using V_{TH}-tuned technique [27], while it needs a high dc voltage (8.5 V) to bias the body of *p*-channel MOSFET (PMOS) to balance the V_{TH} of *n*-channel MOSFET (NMOS) and PMOS, the experimental result shows only 9X step-up voltage ratio. An integrated Dickson voltage-doubler is presented to achieve a 230 mV self-startup with 0.5 μH inductor by using 40 nm process [28], while negative-to-positive voltage converter structure determined the converter can only operate in sub-threshold. To further improve the startup features, special devices are employed in IC design, such as low-V_{TH} MOS [29] and native MOS [14], leading to more complex manufacture process, thus increasing the cost. Furthermore, due to the breakdown voltage and leakage current, the use of special devices is unpractical.

Based on the above discussions, a hybrid structure step-up converter combining with charge pump and boost converter is proposed in this work, where a two-step self-startup strategy and a multistage multiphase charge pump with body-effect technique are presented.

The rest of this article is organized as follows. In Section II, the system architecture and operating principle of the proposed converter is introduced. Subsequently, the design challenge and technical solution is analyzed in Section III. The circuit implementation is described in Section IV. Detailed description of the experimental results is presented in Section V. Finally, Section VI concludes this article.

II. SYSTEM ARCHITECTURE AND OPERATING PRINCIPLE OF HYBRID STRUCTURE STEP-UP CONVERTER

Fig. 2 shows the system architecture of the proposed hybrid structure step-up converter, including three parts: a low-voltage startup controller, a constant on-time (COT) control loop and a boost power stage.

The low-voltage startup controller contains five parts: a low-voltage ring oscillator, a multistage multiphase charge pump, an internal supply voltage generator, a bias&ref module, and an input voltage detect&logic control module. The low-voltage ring oscillator is designed to generate multiphase clock signals for the multistage multiphase charge pump, and then the output voltage V_{ST} of the charge pump is produced. Furthermore, the supply voltage V_{A} and V_{C} are generated by the internal supply voltage generator. The input voltage detect&logic control module monitors the input voltage V_{IN} and V_{A} to switch the operating states of the system alternately. The bias&ref module generates the reference voltage V_{REF} and bias current I_{B} for all other modules.

The COT control loop contains four parts: a hysteresis comparator, a ring oscillator, a COT generator, and a logic control&ZCD module. The hysteresis comparator compares the feedback voltage V_{FB} with V_{REF} to generate enable signal *EN*, which controls the ON/OFF states of the ring oscillator. When $V_{\mathrm{FB}} < V_{\mathrm{REF}}$, $EN = 1$, the ring oscillator operates to generate a frequency signal f_{C}. When $V_{\mathrm{FB}} > V_{\mathrm{REF}}$, $EN = 0$, the ring oscillator is disabled. The COT generator is designed to produce f_{COT} with constant ON-time for the logic control&ZCD module, where two nonoverlap signals V_{ND} and V_{PD} with ZCD control are further generated and used to control the boost power stage.

Furthermore, a COT controlled boost converter is designed to guarantee the steady output voltage with wide input range and various load condition. The power stage contains two power MOSFETs, in which the low-side transistor NM_1 is the main switch while the high-side transistor PM_1 adopts as synchronous rectification switch, both driven by V_{ND} and V_{PD}.

In order to achieve self-startup at ultra-low input voltage with high voltage conversion rate (VCR) and normal operating with high power conversion efficiency (PCE) at normal input voltage, a two-step three-periods (charge pump self-startup period, hybrid mode period, and boost operating period) self-startup strategy is designed. The detailed operating principle of the strategy is described as follows. Initially, when the input voltage reaches the kick-start voltage, the charge pump starts to work, and V_{ST} increases rapidly, the system enters the charge pump self-startup period. When V_{ST} exceeds a preset threshold voltage, which means the charge pump has enough driving capability, then the boost converter starts to operate, the system enters the hybrid mode period. When the internal supply voltage V_{A} is large enough to guarantee the V_{C} get into steady state, the charge pump is disabled after some delay time, the system shifts to the boost operating mode, and the output of the converter can be regulated efficiently.

III. DESIGN CHALLENGE AND TECHNIQUE SOLUTION

In order to realize as low as possible self-startup voltage and high VCR with high PCE of the step-up converter, the design challenge is studied first, and then, three main technique solutions are introduced in detail.

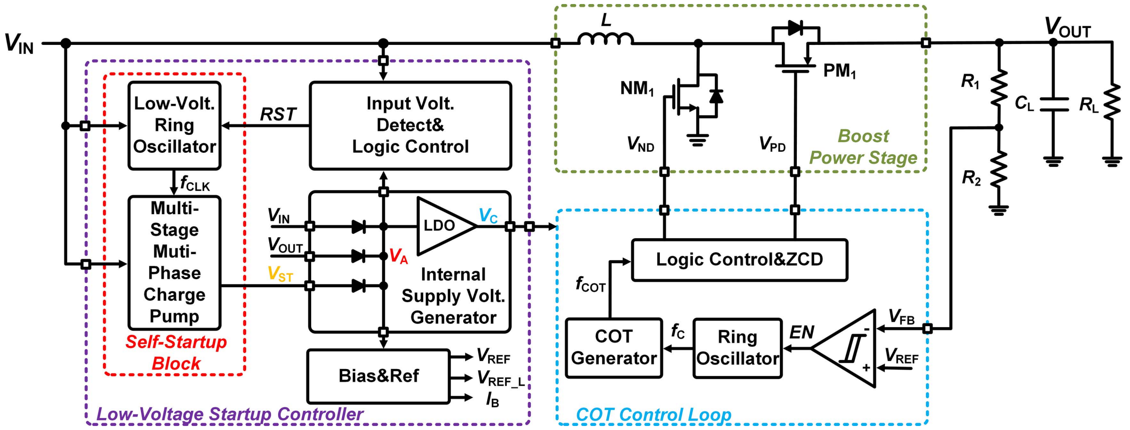


Fig. 2. System architecture.

A. Design Challenge

For low-voltage start-up technology, two challenges are involved in design process. First, raising up the ultralow input voltage to the sufficient level to power the converter. Second, being able to kick-start the system without external supply or auxiliary mechanical switches. To solve these, there are three key issues need to be addressed, which are as follows.

1) The most important key issue is to raise up the ultralow input voltage to the normal operating voltage that can be supplied to the system, which means the high VCR and enough driving capability at ultralow input voltage need to be achieved. Conventional methods by using boost converter or charge pump with special device are difficult to meet the requirements. Therefore, carefully designing and optimizing the system architecture is essential, then a multiphase multistage cross coupled charge pump structure is adopted.
2) Besides, another key issue is to kick-start the converter at ultralow input voltage. Conventional methods by using external supply or auxiliary mechanical switches can realize high performance, but these will seriously limit its application, especially not applicable for self-powered sensor nodes. In addition, to meet the requirement of wide input/output voltage range, the use of high breakdown voltage MOSFETs (high V_{th}) in circuit are inevitable, which makes it hard to work when the input voltage is lower than a threshold voltage. Therefore, the minimum supply voltage of ring oscillator should be considered, where the body-bias controlled inverter is adopted in this article to reduce the threshold voltage of MOS transistors used in low-voltage ring oscillator.
3) In addition, the establishing process of internal supply voltage should be further considered. It is necessary to reasonably design the self-startup strategy at different operating condition to arrange the internal power supply strategy. After the output voltage of the converter reaches steady state, the system enters boost operating period, the internal supply voltage is switched to V_{OUT} and the self-startup circuit is then disabled to save energy.

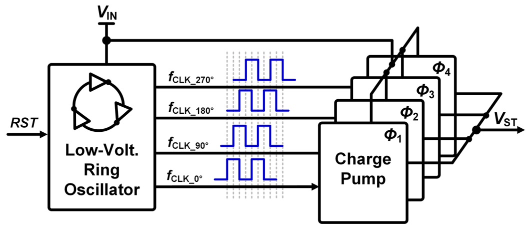


Fig. 3. Proposed self-startup block.

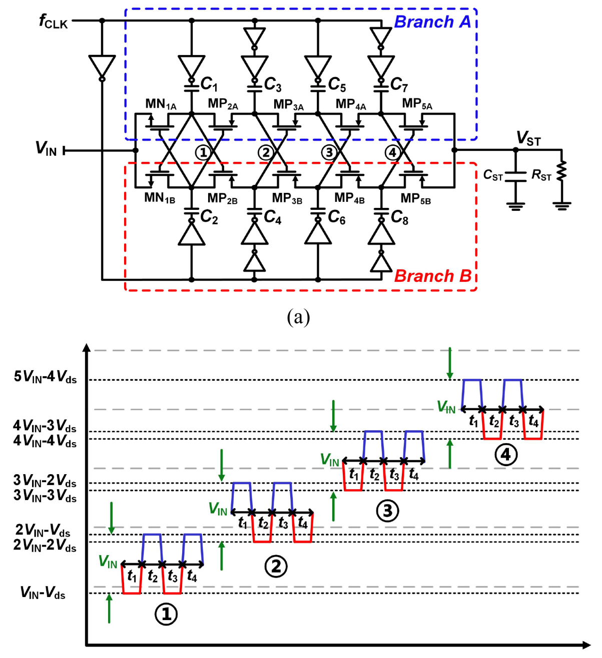
B. Self-Startup Block

Fig. 3 shows the proposed self-startup block, it contains a low-voltage ring oscillator and a 4-phase charge pump. The 4-phase clock signals are generated by the low-voltage ring oscillator, and then used to drive the 4-phase charge pump. In order to improve the VCR and driving capability under ultra-low input voltage, 5-stage with cross coupled charge pump structure is adopted.

The schematic of single-phase charge pump and corresponding waveforms are shown in Fig. 4(a) and (b), respectively. NMOS transistors are used in 1st-stage to obtain better conduction characteristics at low V_{IN}, and PMOS transistors are used in all other stages to avoid the body-effect.

Fig. 5 shows the operating state of the charge pump during the negative/positive half cycle of the f_{CLK}. During the time interval t_1 in Fig. 4(b), $f_{\mathrm{CLK}} = 1$, the charge pump operates in positive half cycle, as shown in Fig. 5(a). During the time interval t_2, $f_{\mathrm{CLK}} = 0$, the charge pump operates in negative half cycle, as shown in Fig. 5(b). Because the switches in branch A and branch B are intertwined, for a 5-stage charge pump, the output voltage V_{ST} can be up to $5V_{\mathrm{IN}}$.

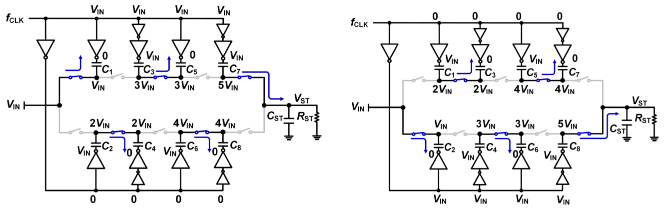
In ideal case, the voltage drop on MOSFETs can be ignored, $V_{\mathrm{ST}} = 5V_{\mathrm{IN}}$ is achieved in steady state. However, there is insufficient time for full charge-sharing across the capacitors between interstage in half cycle because of the high frequency of f_{CLK}. Therefore, as shown in Fig. 4(b), considering the voltage drop on MOSFETs of the charge pump, V_{ST} will be lower than the ideal value. Especially in ultralow V_{IN}, the conduction



(a)

(b)

Fig. 4. (a) Schematic, and (b) corresponding voltage waveforms of 5-stage cross coupled charge pump.



(a)

(b)

Fig. 5. Operating states of 5-stage cross coupled charge pump. (a) Positive half cycle. (b) Negative half cycle.

characteristic of the MOSFETs with high withstand voltage will worsen, thus the charge pump needs to be optimized carefully.

As the operating states shown in Fig. 5(a) and (b), when in positive half cycle, capacitor C_1, C_4, C_5, and C_8 are charged, C_2, C_3, C_6, and C_7 are discharged. The dc voltage on C_7 at steady state can be expressed by the following:

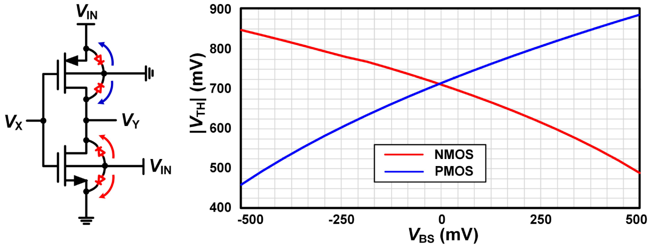
$$V_{7\_DC} = 5V_{IN} - \Delta V_{ds\_total} \tag{1}$$

where $\Delta V_{\text{ds\_total}} = I_1 r_{\text{ds}} + I_4 r_{\text{ds}} + I_5 r_{\text{ds}} + I_8 r_{\text{ds}}$, and I_1–I_8 are the charge/discharge current of capacitors, and r_{ds} is the ON-resistance of the MOSFETs.

When the output voltage of charge pump is in steady state, the energy consumed by the load in half cycle is almost the same as the energy discharged on capacitor C_7. Thus, the decrease voltage ΔV_7 of C_7 in half cycle can be written as follows:

$$\Delta V_7 = I_{ST} T / 2C_7 \tag{2}$$

where I_{ST} is the load current of charge pump, and ΔV_7 can be defined as the output voltage ripple.



(a)

(b)

Fig. 6. Inverter with body-bias control. (a) Schematic. (b) Simulated waveforms of $|V_{\text{TH}}|$ versus V_{BS}.

Thus, the output voltage V_{ST} can be expressed by

$$V_{ST} = V_{ST\_DC} \pm V_{ST\_AC} = V_{7\_DC} - I_{ST} r_{ds} \pm \Delta V_7/2. \tag{3}$$

Substituting (1) and (2) into (3), V_{ST} can be obtained by the following:

$$V_{ST} = 5V_{IN} - \Delta V_{ds\_\text{total}} - I_{ST} r_{ds} \pm I_{ST} T/4C_7. \tag{4}$$

It can be seen from (4) that when the load current I_{ST} increases, more energy is required in each charging cycle, which results in lower dc voltage and larger ripple of V_{ST}.

C. Body-Bias Controlled Low-Voltage Ring Oscillator

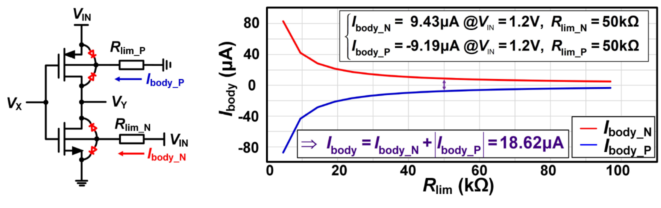
Due to the wide input voltage range of the proposed converter, 5P0 MOSFETs (5 V withstand voltage and 710 mV normal threshold voltage) are used in circuit design, especially in low-voltage ring oscillator. therefore, to further reduce the startup voltage and the power dissipation at normal operating voltage, body-bias control method and current limitation technique are adopted. The threshold voltage of NMOS $V_{\text{TH,n}}$ can be expressed as follows [30]:

$$V_{TH,n} = V_{TH0} + \gamma \left(\sqrt{2\Phi_F - V_{BS}} - \sqrt{2\Phi_F} \right) \tag{5}$$

where V_{TH0} is the initial threshold voltage, γ is the body-effect coefficient which lies in the range of 0.3 to 0.4 $\text{V}^{1/2}$, Φ_{F} is the surface potential, and V_{BS} is the bulk-source potential difference.

It can be seen from (5) that $V_{\text{TH},n}$ can be decreased due to the positive bias voltage between substrate and source, which makes the self-startup circuit easier to operate in lower supply voltage. In the same way, when $V_{\text{BS}} < 0$ for PMOS, its threshold voltage will similarly decrease. As example, the schematic of inverter with body-bias control is shown in Fig. 6(a), and the simulated $|V_{\text{TH}}|$ of PMOS and NMOS versus their V_{BS} is shown in Fig. 6(b). When $V_{\text{BS}} = 500$ mV, $V_{\text{TH,n}}$ can be reduced from 710 to about 490 mV.

However, due to the body diode, when the input voltage is higher than the forward voltage V_{F} of diode, the body diode will conduct, and the substrate current will increase rapidly with the increase of input voltage, which leads to the dramatic increase in power consumption. To solve this problem, current limitation technique is adopted, where a large resistor is used to limit the diode forward current, the schematic is shown in Fig. 7(a), that



(a) (b)

Fig. 7. Inverter with body-bias control and current limitation techniques. (a) Schematic. (b) Simulated results of $I_{\rm body}$ versus $R_{\rm lim}$.

is, all NMOS substrates are connected to $V_{\rm IN}$ through resistor $R_{\rm lim\_N}$, and all PMOS substrates are connected to *gnd* through $R_{\rm lim\_P}$ with the same value. Take NMOS for example, when $V_{\rm IN} < V_{\rm F}$, the body diode will not conduct, and the current $I_{\rm body\_N}$ flowing through the resistor is very small. When $V_{\rm IN} > V_{\rm F}$, $I_{\rm body\_N} = (V_{\rm IN} - V_{\rm F}) / R_{\rm lim\_N}$, where $V_{\rm F} = V_{\rm PN\_junction} + \Sigma I_{\rm F} \times r = V_{\rm PN\_junction} + I_{\rm body\_N} \times r$, and r is the ON-resistance of the body diode. Fig. 7(b) shows the simulated results of $I_{\rm body}$ versus $R_{\rm lim}$ at $V_{\rm IN} = 1.2$ V, $I_{\rm body}$ decreases with the increase of $R_{\rm lim}$. By trade-off the input voltage, power consumption and PCE, $R_{\rm lim} = 50$ kΩ (rhrp_3k model with L/W = 74 μm/5 μm) is chosen to guarantee the maximum $I_{\rm body}$ is only 18.62 μA when $V_{\rm IN} = 1.2$ V.

To realize body-bias control of complementary MOSFET (CMOS), p-substrate with deep n-well (DNW) process is needed. Fig. 8 shows the cross-section view of CMOS inverter and its equivalent device structure and schematic, where the NMOS transistor is fabricated in DNW to make the body p-well independent from p-substrate, thus the body terminal can be biased freely.

While, a P^+NPNPN^+ (6-layer with 5-junction) structure is made up from *start* to *end* in Fig. 8, where two *PNPN* structure silicon-controlled-rectifier (layers ①②③④ and layers ③④⑤⑥) devices are produced. Here, $R_{\rm lim\_N}$ and $R_{\rm lim\_P}$ are the current limitation resistance of CMOS inverter. $R_{\rm p\_sub}$ (in p-substrate) and $R_{\rm DNW}$ (in DNW) are the base parasitic resistance of NPN$_1$ and PNP$_2$. Therefore, it is necessary to analyze the latch-up effect. As shown in the bottom part of Fig. 8, due to the body-bias control, when $V_{\rm IN} > V_{\rm F}$, the BE junction of PNP$_1$ and NPN$_2$ are both positively biased, and the BC junction are both nearly zero biased, which means these two transistors are working in linear amplification region. Fortunately, the voltage level of layers ①④ and ③⑥ are the same, and the BE junction of NPN$_1$ and PNP$_2$ are both negatively biased. Therefore, no latch-up is appeared. However, due to the operating region of PNP$_1$ and NPN$_2$, the power consumption needs to be analyzed.

Take cascade inverters for example, as shown in Fig. 9(a), which is adopted in low-voltage ring oscillator design. The layout implementation is shown in Fig. 9(b), and the entire equivalent circuit is shown in Fig. 9(c), where, the PNP$_1$ and NPN$_2$ are the same transistors as in Fig. 8, and both are the vertical bipolar transistors, the PNP$_3$ and NPN$_3$ are the lateral bipolar transistors.

For PNP$_1$ and NPN$_2$, because the doping density of p-sub, n-well, p-well, and DNW are very low and no buried layer is used, the parasitic resistance of base and collector are very large. Besides, the resistance value of $R_{\rm lim\_N}$ and $R_{\rm lim\_P}$ are also very large. Even $V_{\rm IN}$ is high enough, the voltage of BE junction is still weakly positively biased, thus the base current $I_{\rm b}$ and collector current $I_{\rm c}$ are both very small, and the amplification factor β are much less than 1. For the lateral bipolar transistors of PNP$_3$ and NPN$_3$, they have the same base as PNP$_1$ and NPN$_2$, thus $I_{\rm b}$ is also the same. However, because of the low doping density, very wide base width and serious surface recombination of carrier, the $I_{\rm c}$ and β of PNP$_3$ and NPN$_3$ are even much smaller than that of PNP$_1$ and NPN$_2$.

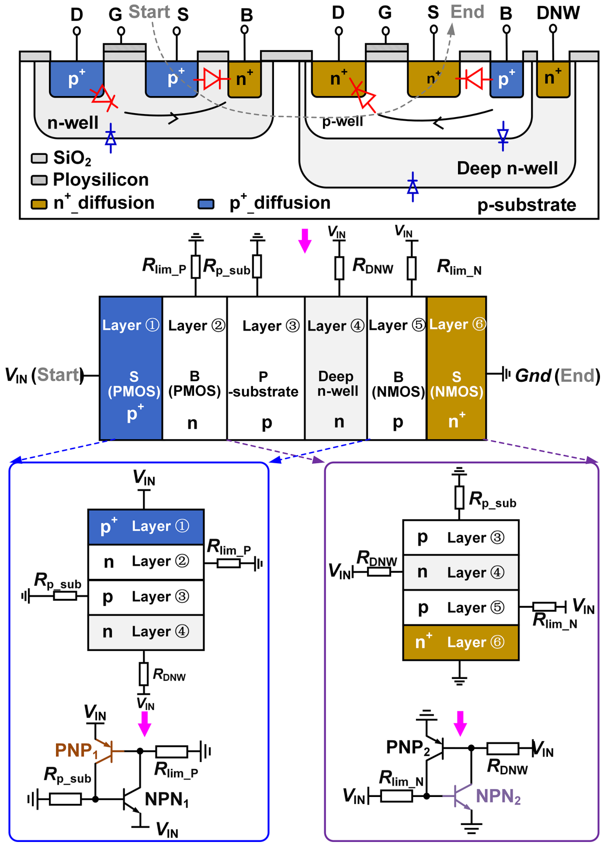


Fig. 8. Cross-section view of CMOS inverter and its equivalent device structure and schematic.

D. Internal Supply Voltage Generator

The detailed circuit implementation of the proposed internal supply voltage generator is shown in Fig. 10, where $V_{\rm A}$ is the main power supply node, which is supplied by the maximum voltage value of $V_{\rm ST}$, $V_{\rm IN}$, and $V_{\rm OUT}$. The output voltage of charge pump $V_{\rm ST}$ is connected to $V_{\rm A}$ by a diode. $V_{\rm IN}$ and $V_{\rm OUT}$ are also connected to $V_{\rm A}$ by two active diodes, which are controlled by $V_{\rm C\_stable}$. The internal supply voltage $V_{\rm C}$ is generated by $V_{\rm A}$ through an LDO regulator.

Voltage establish process of the system including $V_{\rm A}$ and $V_{\rm C}$ can be divided into three periods: charge pump self-startup period, hybrid mode period, and boost operating period, which is shown in Fig. 11. The voltage startup transient diagram when $V_{\rm IN} < 1.2$ V is shown in Fig. 12.

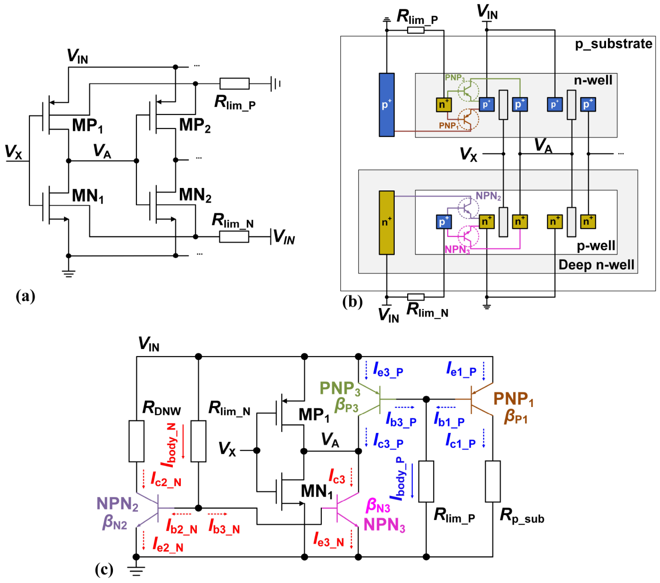


Fig. 9. Cascade inverters. (a) Schematic. (b) Layout implementation. (c) Entire equivalent circuit.

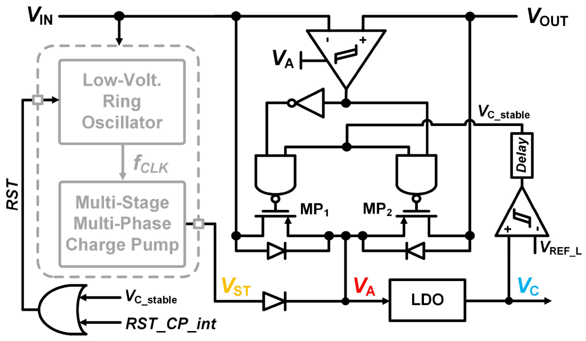


Fig. 10. Circuit implementation of internal supply voltage generator.

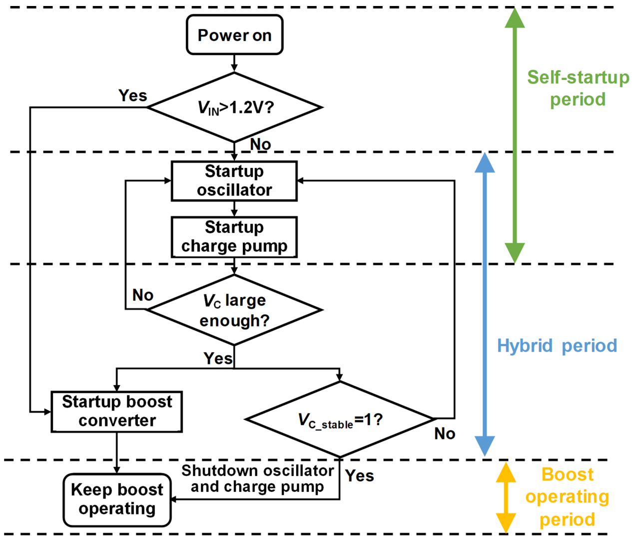


Fig. 11. Flowchart of the voltage establish process.

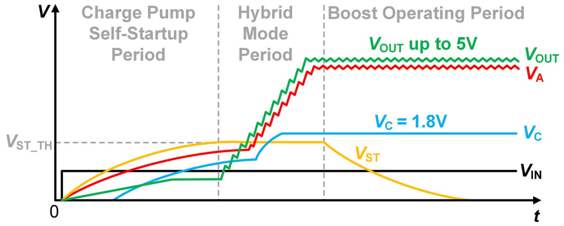


Fig. 12. Voltage startup transient diagram when $V_{\text{IN}} < 1.2$ V.

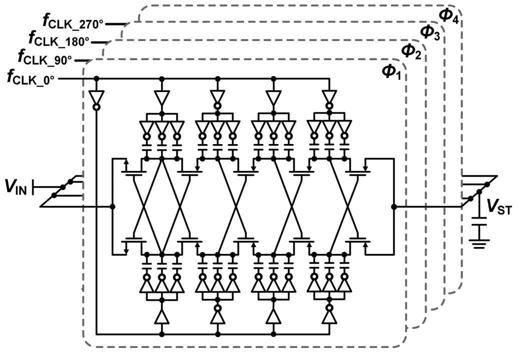


Fig. 13. Schematic implementation of multi stage multiphase charge pump.

As the main power supply node in internal supply voltage generator, the V_{A} always has the highest voltage all the time to guarantee all other modules work well. The *RST* signal is produced by the $V_{\text{C\_stable}}$ and *RST_CP*_int through a *OR* logic, where the *RST_CP*_int signal is generated by the input voltage detect&logic control module.

IV. CIRCUIT IMPLEMENTATION

To further illustrate the design difficulties of the hybrid step-up converter, the circuit implementation of multistage multiphase charge pump, low-voltage oscillator, input voltage detect&logic control module, and COT controlled boost converter are introduced detailly.

A. *Multistage Multiphase Charge Pump Design*

A fully integrated multistage multiphase charge pump is designed to decrease the self-startup voltage, promote driving capability and reduce output ripple of V_{ST} as much as possible. To realize the voltage step-up without off-chip components, and as well as considering the compromise between output power and layout area, finally a 5-stage 4-phase cross coupled charge pump is designed, as shown in Fig. 13.

Usually, single large flying capacitor is used in interstage, resulting in the large time constant τ and slow frequency response with the large chip area and complex interconnection. In order to solve this problem, distributed design concepts are adopted, where the single large flying capacitor is divided into N equal piece and driven by the same size inverter.

Fig. 14 shows the equivalent charging/discharging model of flying capacitors in an inter-stage. In Fig. 14(a), assuming the

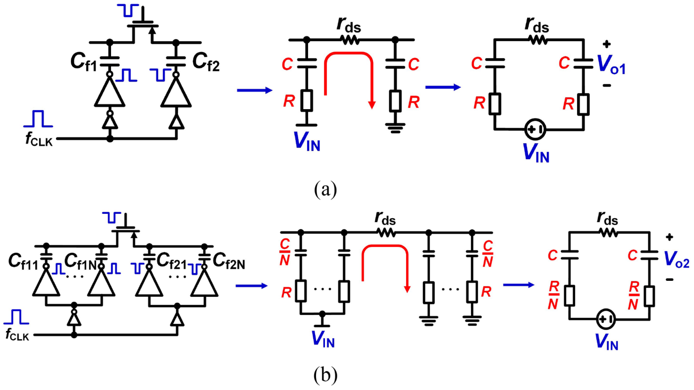


Fig. 14. Equivalent charging/discharging model of flying capacitors in interstage. (a) Without capacitor division. (b) With *N* equal pieces division.

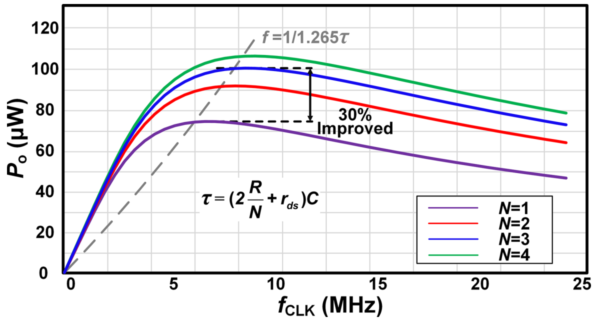


Fig. 15. Numerical simulation of output power P_o versus f_{CLK} at $V_{IN} = 700$ mV with different *N*.

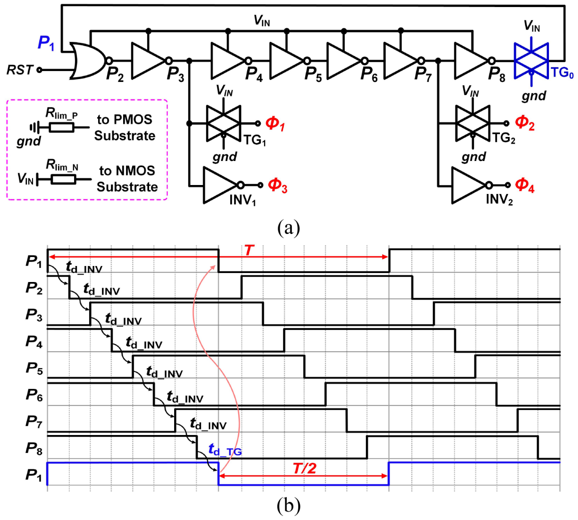


Fig. 16. Low-voltage ring oscillator. (a) Circuit. (b) Time diagram.

value of flying capacitor C_f is *C*, the equivalent resistance of the driving circuit is *R*, and the channel resistance of the switch transistor is r_{ds}. Thus, the charging voltage V_{o1} and power P_{o1} in each charge cycle (1/2f_{CLK}) can be obtained as follows:

$$\begin{cases} V_{o1} = \frac{V_{IN}}{2}\left(1-e^{-\frac{1}{2(2R+r_{ds})Cf_{CLK}}}\right) \\ P_{o1} = CV_{o1}^2 f_{CLK} \end{cases} . \tag{6}$$

If the C_f is divided into *N* equal pieces, it means that each small capacitor is *C/N*, while the equivalent resistance of the same driving circuit and switch transistor are still *R* and r_{ds}, respectively, as shown in Fig. 14(b). The V_{o2} and P_{o2} in each charge cycle (1/2f_{CLK}) can be written as follows:

$$\begin{cases} V_{o2} = \frac{V_{IN}}{2}\left(1-e^{-\frac{1}{2(2\frac{R}{N}+r_{ds})Cf_{CLK}}}\right) \\ P_{o2} = CV_{o2}^2 f_{CLK} \end{cases} \tag{7}$$

Fig. 15 shows the numerical simulation of output power P_o versus f_{CLK} at $V_{IN} = 700$ mV with different *N*. It can be seen that with the increase of *N*, P_o increases, especially at the maximum power point, and the optimal frequency range of around $f = 1/(1.256\tau)$ can be obtained. To balance the power improvement and design complexity, $N = 3$ is finally chosen to achieve as much as 30% power increasing.

For 1-phase charge pump, the output ripple can be equivalent to the discharge voltage of the flying capacitor in last-stage, and its formula is shown in (2). While in 4-phase charge pump, there always has two current paths in each *T*/4 cycle to charge the load, thus the output ripple can be expressed as follows:

$$\Delta V = I_{ST}T/8C_7. \tag{8}$$

It can be seen that if the time cycle is constant, the output ripple of 4-phase charge pump can be reduced by about 1/4 compared with that of 1-phase charge pump.

B. Low-Voltage Ring Oscillator Design

Fig. 16(a) shows the circuit implementation of the low-voltage ring oscillator, which is composed of an NOR logic, six inverters, and a transmission gate in cascade, and is powered by V_{IN}, to produce 4-phase with 90° phase shift clock signals for the 4-phase charge pump. *RST* signal can set/reset the ring oscillator through the NOR logic. There are two key design points to keep correct results. One is positive feedback loop design, the transmission gate TG_0 is carefully designed and used here to guarantee the same delay for chain $P_3 \rightarrow P_4 \rightarrow P_5 \rightarrow P_6 \rightarrow P_7$ and chain $P_7 \rightarrow P_8 \rightarrow P_1 \rightarrow P_2 \rightarrow P_3$. Another is the output node design, in order to keep the same delay time with 180° phase difference, the TG_1, TG_2, INV_1, and INV_2 are all optimal designed. By combining these key design points, precisely 4-phase clock signals Φ_1, Φ_2, Φ_3, and Φ_4 can be produced.

The time diagram of the low-voltage ring oscillator is shown in Fig. 16(b), where the delay of inverter and transmission gate are defined as t_{d_INV} and t_{d_TG}, respectively, and assuming that each logic has the same propagation delay.

According to Barkhausen's criterion, the frequency of the ring oscillator f_{CLK} is as follows:

$$f_{CLK} = 1/\left(7t_{d\_\mathrm{INV}} + t_{d\_TG} + T/2\right). \tag{9}$$

If $t_{d\_INV} = t_{d\_TG}$, a phase difference of $\pi/2$ can be generated between any four logics. In order to keep the same delay time, an approach to calculate the propagation delay by integrating the charging (discharging) current of total capacitance is studied

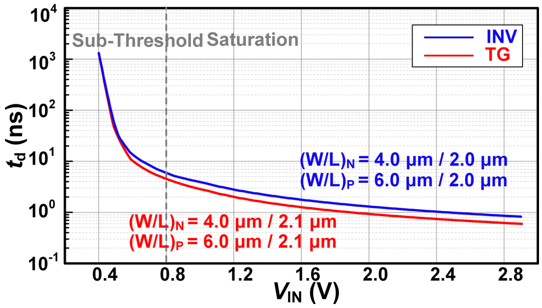


Fig. 17. Simulation results of t_{d} versus V_{IN} for INV and TG.

[31]. Thus, the delay of INV and TG can be written as follows:

$$\begin{cases} t_{d\_INV} = \left(t_{dLH\_INV} + t_{dHL\_INV}\right)/2 \\ \quad = C_{T\_INV}\left(R_{eqn} + R_{eqp}\right)/\sqrt{2} \\ t_{d\_TG} = \left(t_{dLH\_TG} + t_{dHL\_TG}\right)/2 \\ \quad = R_{eq}\left(C_{LH\_TG} + C_{HL\_TG}\right)/\sqrt{2} \end{cases} \tag{10}$$

Where $C_{\mathrm{T\_INV}}$ is the total output capacitance, including the drain diffusion capacitors of PMOS and NMOS and the gate capacitors of the next stage. R_{eqn} and R_{eqp} are the equivalent resistance of NMOS discharges cycle and PMOS charging cycle, respectively. $C_{\mathrm{LH\_TG}}$ and $C_{\mathrm{HL\_TG}}$ are the capacitance of channel-to-gate and channel-to-body of PMOS and NMOS, respectively. R_{eq} is the equivalent ON-resistance of PMOS and NMOS as parallel connection in TG. The relevant equations can be obtained as follows:

$$R_{\mathrm{eqn}} = \begin{cases} \frac{3}{4}\frac{V_{IN}}{\kappa_n V_T^2} exp\left(-\frac{V_{IN} - V_{\mathrm{TH},n}}{nV_T}\right), & V_{TH,n} < V_{IN} < 2V_{TH,n} \\ \frac{3}{2}\frac{V_{IN}}{\kappa_n\left(V_{IN} - V_{TH,n}\right)^2}, & V_{IN} > 2V_{TH,n} \end{cases} \tag{11}$$

$$R_{eqp} = \begin{cases} \frac{1}{4}\frac{V_{IN}}{\kappa_p V_T^2} exp\left(-\frac{V_{IN} - \left|V_{TH,p}\right|}{nV_T}\right), \\ \quad \left|V_{TH,p}\right| < V_{IN} < 2\left|V_{TH,p}\right| \\ \frac{1}{2}\frac{V_{IN}}{\kappa_p\left(V_{IN} - \left|V_{TH,p}\right|\right)^2}, V_{IN} > 2\left|V_{TH,p}\right| \end{cases} \tag{12}$$

$$R_{eq} = \frac{1}{1/R_{eqn} + 1/R_{eqp}} \tag{13}$$

where κ_{n} and κ_{p} are the gain factor of NMOS and PMOS, respectively, V_{T} is the thermal voltage, and V_{TH} is the threshold voltage.

According to (10), since $C_{\mathrm{T\_INV}}$ are approximately equal to the total of C_{TG}, the $R_{\mathrm{eqn}}+R_{\mathrm{eqp}}$ is designed to be equal to R_{eq}, then $t_{\mathrm{d\_INV}} = t_{\mathrm{d\_TG}}$ can be achieved.

Fig. 17 shows the simulation results of t_{d} versus V_{IN} for INV and TG. With the decrease of V_{IN}, the operating state of the INV and TG shifts from saturation region to subthreshold region. It can be seen that the delay is insensitive to the change of power supply voltage at high input voltage, but when V_{IN} is close to $2V_{\mathrm{TH}}$, the delay begins to increase rapidly. When the length of CMOS in TG is designed to be about 1.05 times the size of INV, the propagation delays are approximately coincident, which is a good proof for the above conclusion.

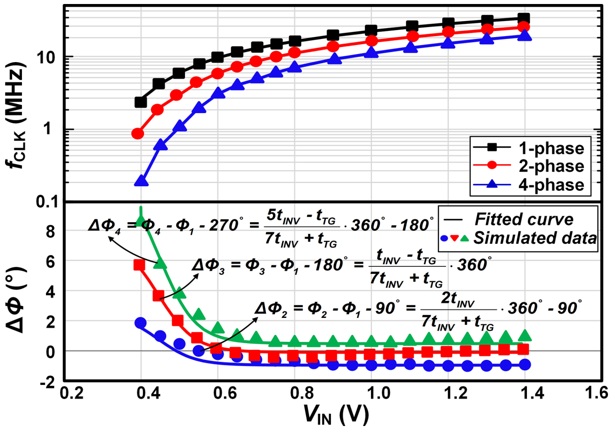


Fig. 18. Simulation results of f_{CLK} and $\Delta\Phi$ versus V_{IN} with different phase.

Fig. 18 shows the simulation results of the frequency f_{CLK} and phase deviation $\Delta\Phi$ versus V_{IN} with different phase of the low-voltage ring oscillator. As the load capacitance of the ring oscillator becomes larger with the increase of phases, f_{CLK} will decrease. According to the optimal operating frequency shown in Fig. 15, excessive clock frequency will affect the PCE of the charge pump. Therefore, the low-voltage ring oscillator should be turned off when the input voltage V_{IN} is higher than 1.2 V to ensure the frequency can be limited within 15 MHz.

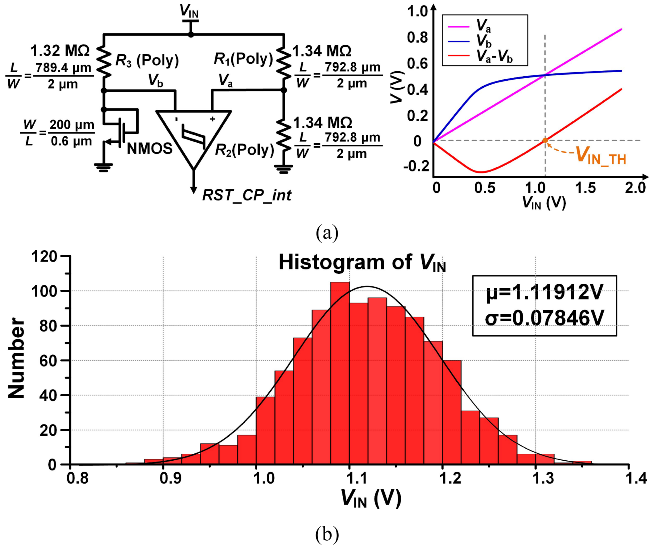
The phase stability between two phases is the key to reduce the output voltage ripple of the charge pump. Fig. 18 also shows that a small phase error is achieved, and with the increase of V_{IN}, the ring oscillator gradually enters the saturation region, and $\Delta\Phi$ is almost keep unchanged. The simulation results are in good agreement with the theoretical analysis, indicating that the ring oscillator can achieve high performance with large input voltage range.

C. Input Voltage Detect&Logic Control Module Design

Circuit implementation and voltage diagram of the input voltage detect&logic control module is shown in Fig. 19(a). It is composed of three resistors, a diode-connected NMOS and a hysteresis comparator. At beginning when power-on, with the increase of V_{IN}, V_{a} and V_{b} are both increase. Because of the diode-connected NMOS, V_{b} increases rapidly, while V_{a} increases linearly, thus $V_{\mathrm{a}}–V_{\mathrm{b}} < 0$, and *RST_CP*_int = 0. When V_{IN} is higher than a threshold value $V_{\mathrm{IN\_TH}}$, $V_{\mathrm{a}} – V_{\mathrm{b}} > 0$, and then *RST_CP*_int changes from 0 to 1, which is used to disable the low-voltage ring oscillator. Carefully design the resistors and NMOS, $V_{\mathrm{IN\_TH}}$ can be changed. Combining with the design discussion in Fig. 10, $V_{\mathrm{IN\_TH}} = 1.12$ V is finally chosen. Fig. 19(b) shows the statistical distribution of V_{IN} corresponding to $V_{\mathrm{IN\_TH}}$ in 1000 times Monte Carlo simulation (include process and mismatch). The results prove that the designed module has very good characteristics.

D. COT Controlled Boost Converter Design

To reduce the power consumption of the system, a COT controlled boost converter including a hysteresis comparator, a



(a)

(b)

Fig. 19. (a) Circuit implementation and voltage diagram of input voltage detect&logic control module. (b) Statistical distribution of V_{IN} corresponding to $V_{\mathrm{IN\_TH}}$ in 1000 times Montes-Carlo simulation (process and mismatch).

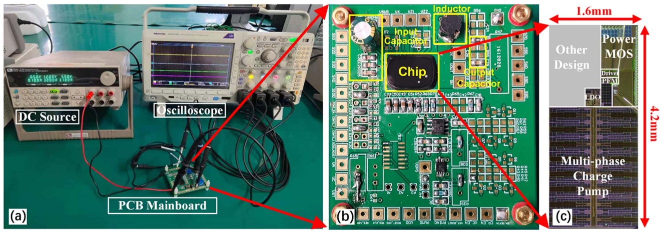


Fig. 20. Experimental testing apparatus. (a) Test platform. (b) PCB mainboard photo. (c) Chip photo.

ring oscillator, a COT generator, a logic control&ZCD module, and a boost power stage is designed, as shown in Fig. 2, which enables the output of the converter to be regulated in wide input voltage and load range.

V. MEASUREMENT RESULTS AND ANALYSIS

Finally, the hybrid structure step-up converter has been fabricated by using standard 0.18 μm CMOS process with 5P0 MOSFETs. Fig. 20(a) shows the actual test platform, including dc source, oscilloscope, and PCB mainboard with the designed ASIC chip. The PCB mainboard photo is shown in Fig. 20(b) and the chip photo is shown in Fig. 20(c). The active area is about 4.8 mm^2. The inductor and capacitor of the boost converter are 4.7 μH and 2.2 μF, respectively. The input voltage range is 50 mV–4.2 V, and the output voltage range is 0.6 (V_{REF})–5 V.

To verify the benefit of the designed charge pump, the output voltage and ripple at different phases with the same input voltage are measured, as shown in Fig. 21. When $V_{\mathrm{IN}} = 700$ mV, on-chip load capacitor $C_{\mathrm{ST}} = 100$ pF, the load resistances are all 10 kΩ. The measured f_{CLK} and V_{ST} are 13 MHz and 1.55 V with 44 mV ripple at 1-phase, 8 MHz and 1.7 V with 40 mV ripple at 2-phase, 3 MHz and 1.8 V with 26 mV ripple at 4-phase, respectively.

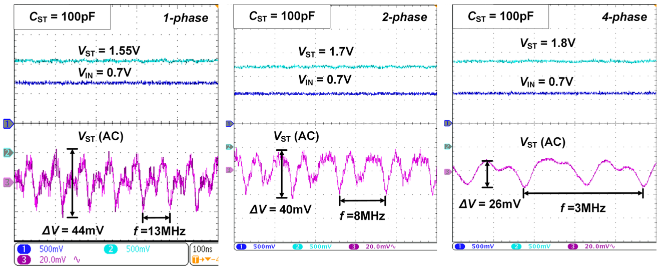
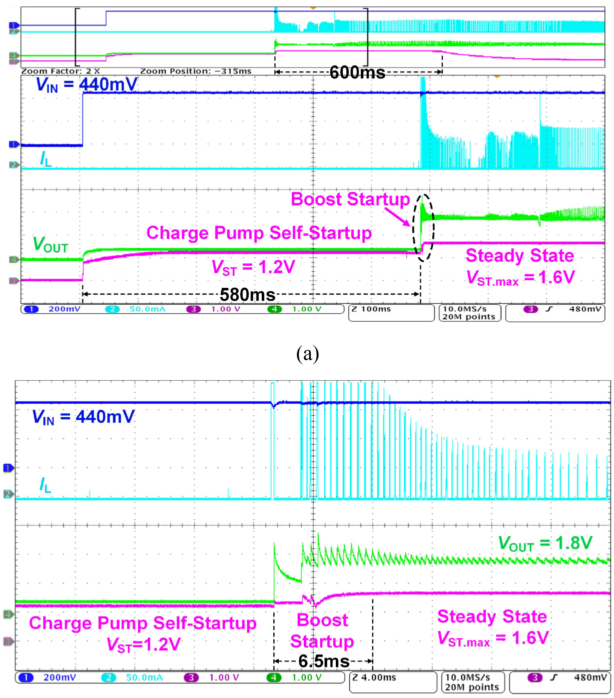


Fig. 21. Measured waveforms of charge pump operating at different phase.



(a)

(b)

Fig. 22. Measured waveforms. (a) Low-voltage self-startup process at light load condition. (b) Detailed transient response of boost startup period.

The measured waveforms of two-step self-startup process at light load condition is shown in Fig. 22(a), which include V_{IN}, inductor current I_{L}, output voltage of the boost converter V_{OUT}, and output voltage of charge pump V_{ST}. It demonstrates that the proposed step-up converter can kick-start with the minimum of 440 mV input voltage at load current of 30 μA with 580 ms charge pump self-startup time. V_{ST} is up to 1.2 V in the self-startup period and increases to 1.6 V in steady period due to the shifting of internal supply voltage from V_{ST} to V_{OUT}. Then, after delay about 600 ms when V_{OUT} is in steady state, then the charge pump is disabled, and V_{ST} decreases to zero. The detailed transient response of boost startup period is shown in Fig. 22(b). It can be seen that V_{OUT} steps up in 6.5 ms during boost startup period.

Fig. 23 shows the measured waveforms of V_{C} in setup process when $V_{\mathrm{IN}} = 500$ mV, demonstrating that V_{C} can maintain to 1.8 V in steady state when $V_{\mathrm{OUT}} > 1.8$ V.

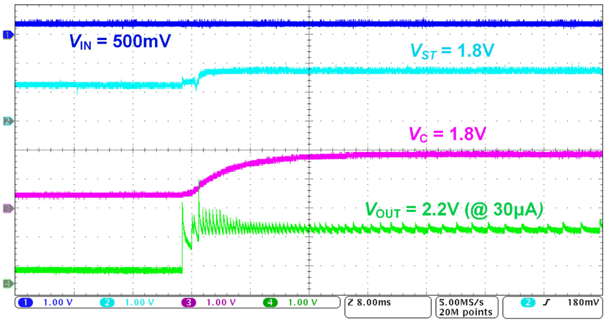
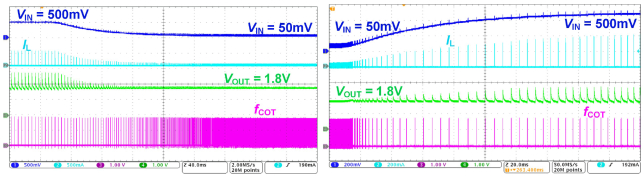
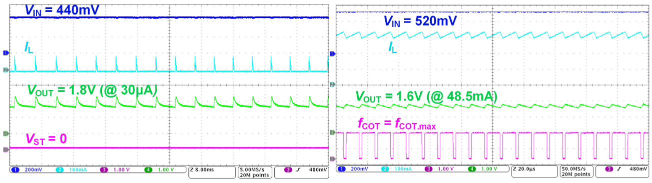


Fig. 23. Measured waveforms of V_{C} in setup process when $V_{\mathrm{IN}} = 500$ mV.



(a) (b)

Fig. 24. Measured transient response. (a) V_{IN} changes from 500 to 50 mV. (b) V_{IN} changes from 50 to 500 mV.



(a) (b)

Fig. 25. Measured waveforms in steady state. (a) When $V_{\mathrm{IN}} = 440$ mV and $V_{\mathrm{OUT}} = 1.8$ V at 30 μA load current. (b) When $V_{\mathrm{IN}} = 520$ mV and $V_{\mathrm{OUT}} = 1.6$ V at 48.5 mA load current.

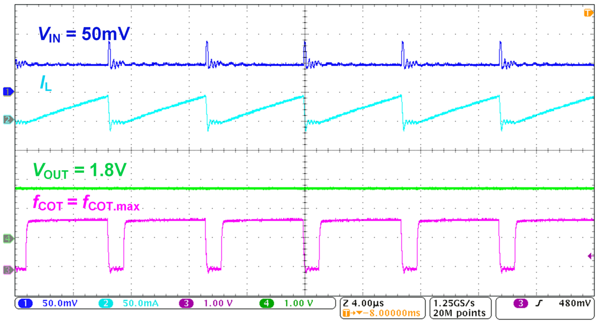
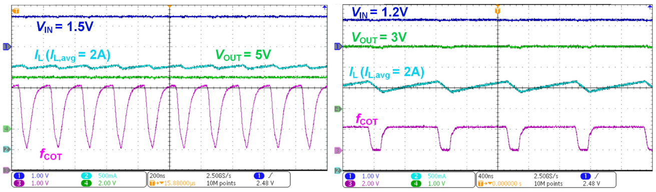
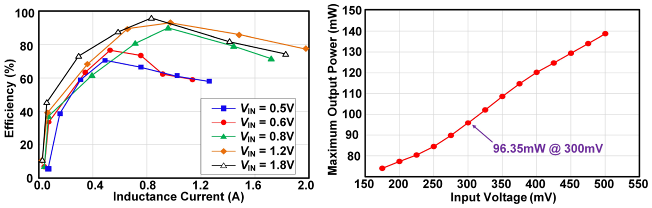


Fig. 26. Measure waveforms in steady state when $V_{\mathrm{IN}} = 50$ mV and $V_{\mathrm{OUT}} = 1.8$ V at light load condition.



(a) (b)

Fig. 27. Measured waveforms in steady state with 2 A average inductor current. (a) When V_{OUT} is 5 V under 1.5 V input voltage. (b) When V_{OUT} is 3 V under 1.2 V input voltage.



(a) (b)

Fig. 28. Measurement results. (a) PCE versus average inductance current with different input voltage. (b) Maximum output power versus input voltage.

Furthermore, the measured transient response of V_{IN} changes from 500 to 50 mV and from 50 to 500 mV at load resistance of 60 kΩ are shown in Fig. 24(a) and (b), respectively. It can be evidently seen that f_{COT} changes between 200 Hz and 150 kHz with V_{IN} decreasing from 500 to 50 mV, which makes V_{OUT} maintain up to 1.8 V continuously, and vice versa.

Fig. 25(a) shows the measured waveforms in steady state when $V_{\mathrm{IN}} = 440$ mV and $V_{\mathrm{OUT}} = 1.8$ V at 30 μA load current, which presents that the COT control loop works well and the low-voltage startup controller can be disabled normally. Fig. 25(b) shows the measured waveforms in steady state when $V_{\mathrm{IN}} = 520$ mV and $V_{\mathrm{OUT}} = 1.6$ V at 48.5 mA load current. It can be seen that $f_{\mathrm{COT}} = f_{\mathrm{COT,max}} = 150$ kHz and the boost converter operating at continuous conduction mode (CCM).

Fig. 26 shows the measured waveforms in steady state when $V_{\mathrm{IN}} = 50$ mV, indicating that the COT control loop works well even under ultralow input voltage condition, where V_{OUT} can be maintained to 1.8 V, and as much as 36× voltage step-up is achieved.

To verify the maximum output voltage and average inductor current, the measured waveforms in steady state at heavy load condition is shown in Fig. 27. The proposed hybrid structure step-up converter can maintain V_{OUT} up to 5 V when $V_{\mathrm{IN}} = 1.5$ V and V_{OUT} up to 3 V when $V_{\mathrm{IN}} = 1.2$ V with 2 A average inductor current, as shown in Fig. 27(a) and (b), respectively, which verify that the designed converter works well even in heavy load condition.

The measured PCE versus average inductance current with different input voltage is shown in Fig. 28(a). The peak PCE is up to 81.8% at $V_{\mathrm{IN}} = 500$ mV and is up to 95.6% at $V_{\mathrm{IN}} = 1.8$ V, respectively. It can be seen that the PCE can maintain high value with wide inductance current and input voltage. Fig. 28(b) shows the measured maximum output power versus V_{IN} within the range of 150–500 mV, and the converter can provide over 96.35 mW output power at 300 mV input voltage. Fig. 29 shows the loss breakdown at the nominal power. The power loss mainly comes from five dominant sources: Power MOS

TABLE I
PERFORMANCE COMPARISON WITH PREVIOUSLY PUBLISHED WORKS

	[17] TCAS-I'18	[18] TCAS-II'17	[26] JSSC'16	[32] JSSC'21	[33] TPE'23	[32] TPE'18	**This work**
Process	0.18 μm Std. CMOS	65 nm SOTB* CMOS	0.18 μm HV CMOS	0.18 μm BCD	0.13 μm CMOS-SOI	0.5 μm 5P0 Std. CMOS	**0.18 μm 5P0 Std. CMOS**
Special Device /Source	Off-Chip *RF* & *Clock* Source	Off-Chip *LC* Resonant	Low Power 1.8 /5 V CMOS	None	GaN	None	**None**
Chip Area	0.48 mm^2	2.13 mm^2	2.42 mm^2	2.76 mm^2	9 mm^2	1.2 mm^2	**4.8 mm^2**
System Architecture	RF Charge Pump + Boost	*LC* Osc. + Charge Pump	Charge Pump	Switched-Capacitor +Boost	Resonant Boost	Rectifier + Buck-Boost	**Charge Pump + Boost**
Inductor	47 μH	41 nH	47 μH	10 μH	8.1 nH	820 μH	**4.7 μH**
Output Capacitor	N/A	100 pF	N/A	20 μF	10 nF	10 μF	**2.2 μF**
Input Volt. Range (Ratio)	0.012-0.38 V (31.7X)	0.1-0.14 V (1.4X)	0.14-0.62 V (4.4X)	2.3-5 V	6 V	1.8-5 V AC (2.7X)	**0.05-4.2 V (84X)**
Self-Startup Volt.	0.26 V	0.1 V	0.3 V	–	–	1.8 V	**0.44 V**
Min. Sustainable Volt.	0.012 V	0.1 V	0.14 V	–	–	1.8 V	**0.05 V**
Output Volt. Range	0.9-1.4 V	0.76-1.2 V	2.9-4.1 V	10-35 V	14-20 V	3.0 V	**0.6 (V_{REF})-5.0 V**
Max. Step-up Ratio	75X	9.2X	N/A	8.1X	3.3X	–	**36X**
Max. Output Power	6.48 mW	0.015 mW	0.001 mW	1 W	4.194 W	330 μW	**3 W@I_L= 2 A**
Peak Power Conversion Efficiency	90.8% @ V_{IN}=0.18 V, V_{OUT} = 0.9 V, I_{load} = 1.67 μA	33% @ V_{IN}=0.1 V, V_{OUT} = 0.76 V, I_{load} = 8.68 μA	87% @ V_{IN}=3 V, V_{OUT} = 1 V, I_{load} = 1 μA	91.15% @ V_{IN}=3.7 V, V_{OUT} = 30 V, I_{load} = 30 mA	58% @ V_{IN} = 6 V	–	**95.6% @ V_{IN} = 1.8 V, V_{OUT} = 4.4 V, I_{load} = 400 mA**

Note: *: Silicon-on-Thin-Buried-Oxide.

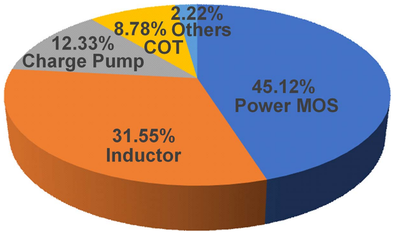


Fig. 29. Loss breakdown at nominal power of each part.

(45.12%, including NMOS and PMOS), inductor (31.55%), charge pump (12.33%), COT control (8.78%), and other circuits (2.22%).

The measurement results confirm the excellent performance of the proposed converter. Finally, Table I summarizes the performance comparison of this work with previously published works. The merits of low self-startup and sustainable voltage, wide input voltage range and high PCE without using any special process and device of the step-up converter demonstrate clear suitability and potential for self-powered IoT applications.

VI. CONCLUSION

In summary, a two-step self-startup hybrid structure step-up converter was developed and fabricated. A two-step self-startup strategy combining with fully integrated multi-stage multi-phase charge pump and body-bias controlled low-voltage ring oscillator was designed to kick start the converter at ultralow input voltage with high VCR and driving capability. In addition, current limitation technique is adopted to solve the inherent contradiction between body-bias technique and operating voltage range, which achieves an extremely wide input voltage range. Finally, measurement results demonstrate excellent performance of the designed system.

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