A Three-Phase Synergetically Controlled Buck–Boost Current DC-Link EV Charger

Daifei Zhang, *Member, IEEE*, Jonas Huber, *Senior Member, IEEE*, and Johann W. Kolar, *Fellow, IEEE*

***Abstract*—With the ever-increasing share of electric vehicles (EVs) comes a need for highly efficient and compact EV chargers. EV charger modules should provide a wide-output-voltage range (200–1000 V) to ensure compatibility with various EV battery voltages. Thus, buck–boost functionality is needed, which can advantageously be realized by a current DC-link topology; a buck-type current-source rectifier (CSR)-stage and a downstream three-level boost-type DC/DC-stage share the main magnetic component (the DC-link inductor). Furthermore, the two stages can operate collaboratively; for low output voltages, the CSR-stage controls the output voltage and the DC/DC-stage is clamped to avoid switching losses; for high output voltages, the DC/DC-stage shapes the DC-link current such that the CSR-stage operates with 2/3-PWM (switching limited to two out of the three phases) and, hence, with reduced switching losses. This article, thus, introduces a simplified synergetic control concept that ensures this loss-optimum operation of the two-stage system for any output voltage. A compact 10-kW hardware demonstrator with a power density of 6.4 kW/dm^3 (107.5 W/in^3) is then used to verify the control concept and the seamless transitions between operating modes. For the first time, a system-level experimental demonstration of the loss savings achieved by 2/3-PWM is provided, and the precompliance conducted EMI test results meet CISPR 11 Class A. Moreover, a detailed experimental characterization of losses/efficiency over the full range of output voltage and power confirms the loss models and the design procedure presented earlier. Finally, the demonstrator shows quite a flat efficiency characteristic (higher than 98% for most operating points with output voltages above 400 V and more than 25% of rated load) with a peak efficiency of 98.8% at 520 V output voltage and 5 kW. All in all, the presented current DC-link buck–boost PFC rectifier system features a promising solution for future isolated or nonisolated EV charger modules.**

***Index Terms*—Electric vehicle (EV) chargers, synergetic control, three-phase (3-Φ) buck–boost (bB) current DC-link PFC rectifier, 2/3-pulse-width modulation (2/3-PWM).**

I. Introduction

THE International Energy Agency (IEA) estimates that there will be 220 million electric vehicles (EVs) on the road by 2030, with China, Europe, and North America accounting for the majority of this growth according to the "Global EV Outlook 2021" report [1]. Obviously, EV batteries must be recharged or might even serve as energy storage complementing fluctuating renewable generation in future energy systems [2]. Hence, EV charging technology is vital to the widespread adoption of EVs and to shaping the future of low-carbon-emission road transport.

A typical battery charging profile comprises two charging modes, i.e., constant current (CC) mode and constant voltage (CV) mode [3], [4]. Starting with a discharged battery, first, a high charging current is applied in the CC charging mode until the battery voltage reaches a certain threshold voltage, and then above this threshold voltage, the charger is switched to CV charging mode, completing the charging process with a decreasing current at an almost constant battery voltage to avoid thermal runaway of the battery [5]. Hence, EV chargers do not operate at full load most of the time: in the CC mode, although the charger provides rated current, the battery voltage only gradually increases starting typically from about 80% of the rated voltage for a lithium-ion battery [3]; in the CV mode, only a small charging current is allowed if the battery voltage is close to the rated value. Various nominal battery voltages, such as 400 or 800 V, are in use, and hence, standards, such as CHAdeMO [6], define wide-output-voltage ranges of 150–1000 V for universal EV chargers. Thus, high-efficiency operation over wide-output-power and output-voltage ranges, i.e., a flat high-efficiency characteristic, is a desirable feature of the power converters used for EV charging.

EV chargers interface the ac mains to the dc terminals of EV batteries and are typically realized with two converter stages [7]: a grid-side ac/dc PFC rectifier and a subsequent, typically isolated, DC/DC-stage. Such isolated converter stages can be implemented, for example, as a dual active bridge converter [8], [9], [10], [11] or as an LLC resonant converter [12], which both provide an adjustable voltage gain. Even though, in this case, the required ultrawide-output-voltage regulation capability can be collaboratively provided by both the DC/DC converter and the three-phase (3-Φ) PFC rectifier front end; loss-optimal operating modes of the whole system depend on the specific loss characteristics of the PFC rectifier and the DC/DC-stage. In other words, these loss-optimal operating modes are different for each specific realization of these converter stages. Thus, optimal designs of such a cascaded system have to take the front end and the isolation stage into account at the same time instead of optimizing them separately. To avoid such design and control issues, and to achieve high efficiency, often series-resonant DC/DC-stages with limited voltage control range, i.e., dc transformers (DCXs) [13], [14], [15], are used [16]. Then,

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The authors are with the Power Electronic Systems Laboratory, ETH Zurich, 8092 Zurich, Switzerland (e-mail: zhang@lem.ee.ethz.ch; huber@lem.ee.ethz.ch; kolar@lem.ee.ethz.ch).

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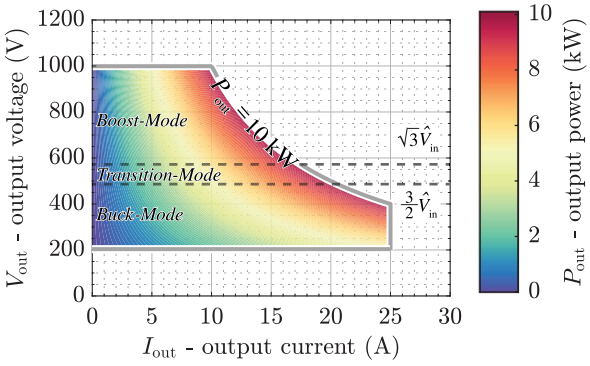

Fig. 1. Typical operating range of a 10 kW EV charger module covering an output voltage from 200 to 1000 V with an output-current limit of $I_{out} = 25$ A. Such a wide-output-voltage range is covered by three main operating modes, i.e., buck mode, transition mode, and boost mode.

the ac/dc PFC rectifier stage must provide buck–boost (bB) functionality to cover the wide-output-voltage range (typically 200–1000 V, see Fig. 1). This is especially also the case in future nonisolated EV chargers [17], [18].

Today, most EV chargers employ topologies with a voltage DC-link [19] (i.e., a DC-link capacitor is placed between a boost-type PFC rectifier and a buck-type dc/dc converter, realizing boost–buck (Bb) functionality). Alternatively, however, topologies with a current DC-link (i.e., a DC-link inductor connects a buck-type PFC rectifier and a boost-type dc/dc converter) can also be applied.

Current DC-link topologies have first been employed in thyristor-based line-commutated medium-voltage drives in the 1970s [20]. Later, with the availability of gate-turn-OFF thyristors or gate-commutated thyristors, pulsewidth modulation (PWM) operation and, thus, motor-friendly waveforms and reliable short-circuit protection could be realized [21], [22], [23], [24], [25]. Applications with lower voltages and power levels have also been considered due to the advent of wide-bandgap power semiconductors, which facilitate higher switching frequencies and, thus, a reduction of the, otherwise, potentially large DC-link inductor volume [26], such as variable speed drives [27], [28], [29], [30], data center power supplies [31], [32], [33], solid-state transformers [34], electric springs [35], grid interfaces for renewable energy sources [36], and also recently EV chargers [37], [38], [39], [40]. Furthermore, extensive research has been conducted on the duality between the comparative analyses of voltage DC-link and current DC-link converters [41], [42], [43], [44], [45], [46].

However, current DC-link systems require switching devices with the capability to block both voltage polarities and to conduct at least one or possibly (for bidirectional ac/dc conversion) both current directions. These switching devices were commonly realized by series connection of diodes with unipolar devices, e.g., normally-on SiC JFETs [27], [47], for unidirectional operations. However, recently, the development of monolithic bidirectional power transistors has gained traction [48], [49], [50]; these devices provide the required functionality with only about one-fourth of the chip area required for today's realizations based on antiseries connections of unipolar devices [51]; hence, in contrast to voltage DC-link topologies, current DC-link topologies feature a significant potential for future performance improvements and/or cost reductions.

Therefore, targeting a universal[1] EV charger ac/dc module covering the wide operating range, as shown in Fig. 1, the 3-Φ bidirectional bB current DC-link PFC rectifier system, as shown in Fig. 2, is considered in this article. So far, a similar topology has commonly been realized by a 3-Φ buck-type current-source rectifier (CSR) stage and a subsequent two-level (2-L) boost-type DC/DC-stage [52], [53], [54]. However, in this article, a 3-L boost-type DC/DC-stage is preferably employed to avoid considerable hard-switching losses occurring at high output voltages for EV battery charger applications. Compared with a conventional realization with a 3-Φ Bb voltage DC-link PFC rectifier [55], advantageously, only one shared main magnetic component, i.e., the DC-link inductor connecting the CSR-stage and the DC/DC-stage, is needed instead of three ac-side boost inductors plus at least one dc-side inductor of the needed buck-type DC/DC-stage, which facilitates a compact converter realization.

The conventional loss-optimal operation and the corresponding control of such two-stage 3-Φ bB current DC-link PFC rectifiers, considering 2-L DC/DC-stage, have been analyzed, e.g., in [53] and [54], where a robust controller enabling operation with heavily unbalanced mains is presented in [53], and Nussbaumer et al. [54] derive a detailed control-oriented small-signal model. In both cases, the implemented control methods can achieve a state-of-the-art loss-optimal operation: if the output voltage is relatively low (buck mode, see Fig. 1), the DC/DC-stage is clamped without generating switching losses but the CSR-stage solely regulates the output voltage; advantageously, the DC/DC-stage is only activated if the output voltage is high[2] (boost mode, see Fig. 1).

However, if the DC/DC-stage has to operate, it can advantageously be used to shape the DC-link current to follow the maximum of the absolute values of the three mains currents, which allows advanced 2/3-PWM operation of the CSR-stage, i.e., only active switching states are needed but not the zero (freewheeling) switching states [49], [53], [56], [57]. Thus, the advanced 2/3-PWM only needs to switch two instead of three phases of the CSR-stage within one switching period, resulting in a significant reduction in switching losses because there are fewer switching instants and these happen at lower voltages (see Section II-B for further details). Taking advantage of this, a synergetic control concept that operates the converter, as shown in Fig. 2, in the loss-optimal mode for any output voltage (i.e., employs 2/3-PWM whenever possible and clamps the DC/DC-stage if the output voltage is sufficiently low) has been introduced in [40]. However, the controller structure presented in [40] is quite complex regarding its implementation, and the concept

[1]Note that Zhang et al. [18] discuss a control method for the proposed topology, which regulates the low-frequency ground leakage current to zero and allows a direct connection of the dc output midpoint to protective earth, hence facilitating nonisolated charger applications.

[2]Output voltage is higher than $3/2 \cdot \hat{V}_{in}$ with $\hat{V}_{in}$ denoting the phase voltage amplitude, i.e., the maximum output voltage that a buck-type CSR-stage can generate.

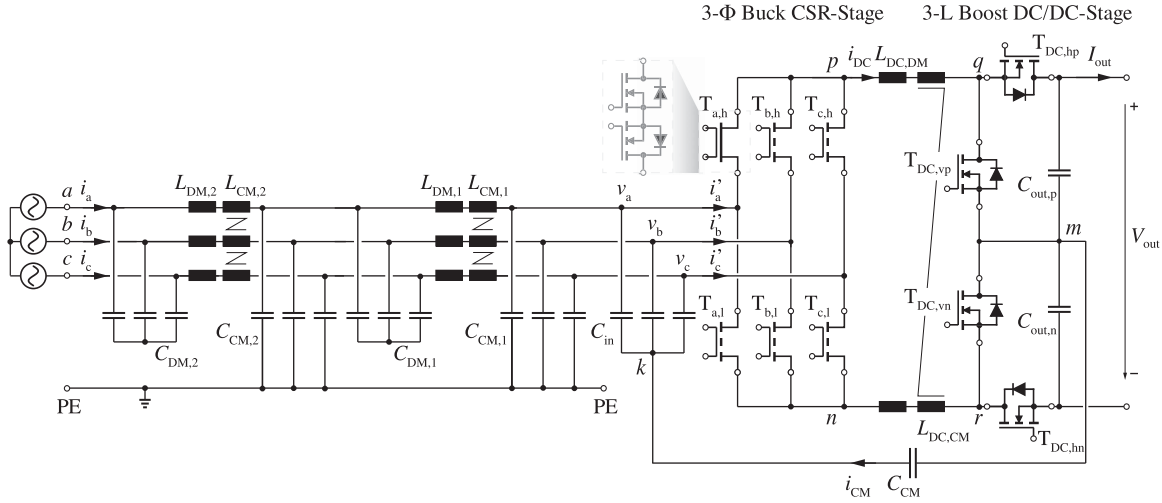

Fig. 2. Power circuit of the considered 10 kW 3-Φ bB current DC-link PFC rectifier system, including CM/DM EMI filters, which employs a 3-Φ buck-type CSR-stage cascaded by a 3-L boost-type DC/DC-stage via a shared DC-link inductor. To filter the HF CM noise at the DC output port, an integrated CM filter consisting of a shared CM inductor $L_{\mathrm{DC,CM}}$ in the DC-link and a capacitor C_{CM} that ties the DC output midpoint to the artificial mains neutral point k, formed by input capacitors, is applied. Table I lists the key specifications and components.

TABLE I
SYSTEM SPECIFICATIONS AND KEY COMPONENTS OF THE DEMONSTRATOR INTRODUCED IN SECTION V

	Description	Value
V_{in}	RMS phase volt.	230 V
V_{out}	DC output-volt. range	200 V∼1000 V
P_{out}	Rated output power	10 kW
$I_{\mathrm{out,max}}$	Output-curr. limit	25 A ($V_{\mathrm{out}} < 400$ V)
$\mathrm{T}_{\mathrm{CSR}}$	CSR-stage semi.	C3M0021120K, 1200 V, 21 mΩ
f_{CSR}	CSR-stage sw. freq.	100 kHz
$\mathrm{T}_{\mathrm{DC/DC}}$	DC/DC-stage semi.	C3M0010090K, 900 V, 10 mΩ
$f_{\mathrm{DC/DC}}$	DC/DC-stage sw. freq.	100 kHz
$2\times L_{\mathrm{DC,DM}}$	DC-link DM ind.	2×125 µH (3×N87 ELP 43/10/28, 14 turns)
$2\times L_{\mathrm{DC,CM}}$	DC-link CM ind.	2×5.5 mH (VAC 500F 40/25/15, 10 turns)
C_{in}	Input filter cap.	3×6 µF
$C_{\mathrm{out},p} = C_{\mathrm{out},n}$	Output filter cap.	2×11.2 µF
C_{CM}	Integrated filter cap.	88 nF
$L_{\mathrm{DM},1} = L_{\mathrm{DM},2}$	EMI DM ind.	15 µH
$C_{\mathrm{DM},1} = C_{\mathrm{DM},2}$	EMI DM cap.	3 µF
$L_{\mathrm{CM},1} = L_{\mathrm{CM},2}$	EMI CM ind.	1.2 mH (VAC 20/12.5/8, 11 turns)
$C_{\mathrm{CM},1} = C_{\mathrm{CM},2}$	EMI CM cap.	18.8 nF

has further never been experimentally verified, especially over a wide-output-voltage range where different modulation schemes and operating modes have to be covered.

Furthermore, Guacci et al. [49] report significant calculated performance improvements achieved by using advanced 2/3-PWM instead of conventional 3/3-PWM (with a constant DC-link current that is at least as high as the peak value of the phase currents) but consider only the CSR-stage. Thus, Zhang et al. [38], [39] have addressed the system-level losses (i.e., the CSR-stage and the DC/DC-stage) and provide a detailed loss modeling analysis and electromagnetic interference (EMI) filter and use Pareto optimization to select a final converter design. However, there is again a lack of a comprehensive experimental evaluation of the system-level loss reduction as well as a possible impact on the EMI emission signature of using 2/3-PWM.

Therefore, this article addresses the research gaps mentioned earlier by introducing a simplified and intuitive implementation of the synergetic control concept retaining all the advantageous features, e.g., achieving loss-optimal operation with advanced 2/3-PWM and ensuring seamless transitions between different operating modes democratically. The proposed control strategy is then verified on a realized 10-kW hardware demonstrator to, importantly, provide extensive experimental verification of the proposed design and the synergetic control method, e.g., efficiency characteristics over a wide operating range, efficiency improvement achievable with 2/3-PWM, and conducted EMI noise emissions.

The rest of this article is organized as follows. Section II derives and explains the advanced 2/3-PWM concept for current DC-link systems with the comparison of conventional 3/3-PWM. Section III discusses the loss-optimal operating modes for the three regions of the wide-output-voltage range (200–1000 V), as indicated in Fig. 1. Section IV then presents the new simplified synergetic control structure that ensures operation in the respective loss-optimal mode and seamless transitions between these modes. Section V introduces a 10-kW hardware demonstrator and provides extensive experimental results. The detailed efficiency measurements in the full operating range demonstrate a flat efficiency characteristic and a peak efficiency of 98.8%. EMI precompliance test results meeting CISPR 11 Class A limits are also provided. Finally, Section VI concludes this article.

II. CURRENT DC-LINK PWM

The CSR-stage (see Fig. 2) consists of two commutation cells, each comprising three bidirectional switches (e.g., the high-side commutation cell consists of $T_{\mathrm{a,h}}$, $T_{\mathrm{b,h}}$, and $T_{\mathrm{c,h}}$). At any given

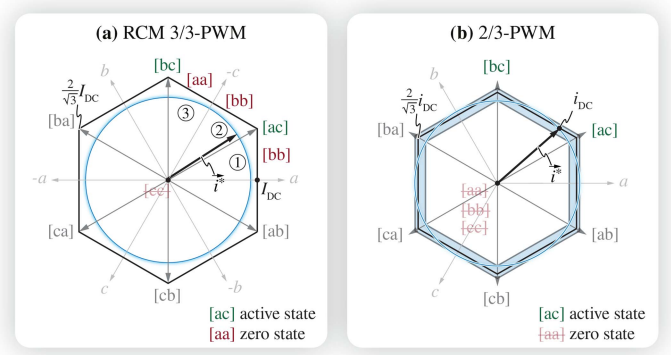

Fig. 3. Space-vector diagrams of (a) RCM 3/3-PWM where the hexagon size is fixed by a constant I_{DC}, i.e., the active space-vectors' magnitude is $2/\sqrt{3}\, I_{DC}$ and (b) 2/3-PWM where the hexagon size is pulsating (over the shaded area) according to a time-varying i_{DC}, i.e., the active space-vectors' magnitude is $2/\sqrt{3}\, i_{DC}$. The switching state of the CSR-stage is expressed by the turned-ON switches of the high-side and low-side commutation cells as, for example, [ac], which indicates that the DC-link current flows through $T_{a,h}$ and $T_{c,l}$.

be short circuited) switch per commutation cell is turned ON and connects the DC-link current to one of the 3-Φ terminals. Therefore, the switching state of the CSR-stage can be described in the form [ab] (see Fig. 3), where this specific example indicates that the high-side commutation cell connects phase a to the DC-link and the low-side commutation cell connects phase b to the DC-link. Freewheeling states are possible too, e.g., [bb] indicates that the DC-link current freewheels through the two commutation cells' switches connected to phase b. In each switching period, a sequence of switching states must be applied to realize sinusoidal local-average values of the phase currents i'_a, i'_b, and i'_c. Two conceptually different PWM schemes, i.e., conventional 3/3-PWM and advanced 2/3-PWM [53], [56], can be applied and are discussed in the following.

A. Conventional 3/3-PWM

Conventionally, current DC-link rectifiers operate with a constant DC-link current I_{DC} that must be at least as high as the peak value of the phase currents. A constant DC-link current and the available switching states define six active space vectors with a magnitude of $2/\sqrt{3}\, I_{DC}$ and three zero vectors (freewheeling states), as indicated in Fig. 3(a). To realize a desired input current space vector $\vec{i}^*$, each switching period is composed of the two closest active states and one zero state. Therefore, all three phases are switching with PWM ["3/3-PWM," see Fig. 4(a)] within one switching period.

In the example shown in Fig. 3(a), which considers a vector $\vec{i}^*$ in sector ②, the active states [ac] and [bc] are needed, whereas the selection of the zero state ([aa] or [bb] or [cc]) is a degree of freedom to optimize, e.g., the overall switching losses [26] or the resulting low-frequency common-mode (CM) voltage [58]. If the zero state corresponding to the phase with the minimum phase voltage, i.e., phase b and, hence, state [bb] in sector ②, is selected, a reduced common-mode (RCM) 3/3-PWM[3] results

[3]Unless, otherwise, noted, 3/3-PWM indicates RCM 3/3-PWM in the rest of the article.

TABLE II
MODULATION SEQUENCES, I.E., SWITCHING STATE SEQUENCES, WITHIN ONE SWITCHING PERIOD CONSIDERING THREE EXEMPLARY SECTORS (SEE FIG. 3)

Sector	RCM 3/3-PWM	2/3-PWM
①	[bb]⇒[ab]→[ac]→[ab]→[bb]	[ab]→[ac]→[ab]
②	[bb]→[bc]⇒[ac]→[bc]→[bb]	[bc]⇒[ac]→[bc]
③	[aa]→[ac]→[bc]→[ac]→[aa]	[ac]→[bc]→[ac]

The hard turn-ON switching transitions of the two switches connected to phase a are indicated by the ⇒ symbol, whereas the soft turn-ON and all turn-OFF switching transitions are indicated by the → symbol.

without sacrificing switching losses [58], which advantageously features a continuous low-frequency CM voltage without any voltage step at the sector boundaries [39]. This facilitates the integrated CM filter composed of $L_{DC,CM}$ and C_{CM} (see Fig. 2). Table II lists the resulting RCM 3/3-PWM switching sequences for $\vec{i}^*$ in three exemplary sectors. Note that the sequences are symmetric with respect to the center of a switching period, which facilitates synchronous sampling of the local-average (over one switching period) DC-link current and further ensures that only one commutation cell switches (instead of two commutation cells) during each transition [26], [27], [39], [44], [58].

Note that the modulation index of the CSR-stage is

$$M = \frac{\hat{I}_{in}}{i_{DC}} = \frac{\bar{v}_{pn}}{\frac{3}{2}\hat{V}_{in}} \leq 1 \tag{1}$$

and, hence, a maximum dc output voltage of voltage $\bar{v}_{pn} = V_{out} \leq 3/2\hat{V}_{in} = 488\,\mathrm{V}$ (the numerical value refers to a $400\,\mathrm{V}$ mains) can be realized without a downstream DC/DC-stage (or with that DC/DC-stage not operating, as shown in Fig. 2).

B. Advanced 2/3-PWM

Differently, if such a DC/DC-stage is present (see Fig. 2), the DC/DC-stage can be utilized to realize 2/3-PWM of the CSR-stage [49], [53], [56], [57], which requires a time-varying DC-link current i_{DC}. This time-varying DC-link current i_{DC} follows the upper envelope of the 3-Φ current absolute values (see Fig. 4(b)), i.e., shows the typical six-pulse shape. In the space-vector diagram (see Fig. 3(b)), such a six-pulse-shaped DC-link current is translated into a correspondingly pulsating size of the hexagon spanned by the six active vectors (whose length, after all, is given by the instantaneous value of the DC-link current) [49]. Zero states are not needed to modify the length of the synthesized vector; actually, any point on the hexagon can be reached by only applying active vectors. Because now the hexagon's size is pulsating, it becomes possible to synthesize the circular trajectory of $\vec{i}^*$ without any zero states, which is clearly visible from the exemplary switching sequences, as given in Table II. Consequently, each switching period is only composed of two active switching states but no zero state such that only two out of three phases are switching with PWM ("2/3-PWM") over one switching period. The switching sequence is implemented to minimize the voltage–time area of the

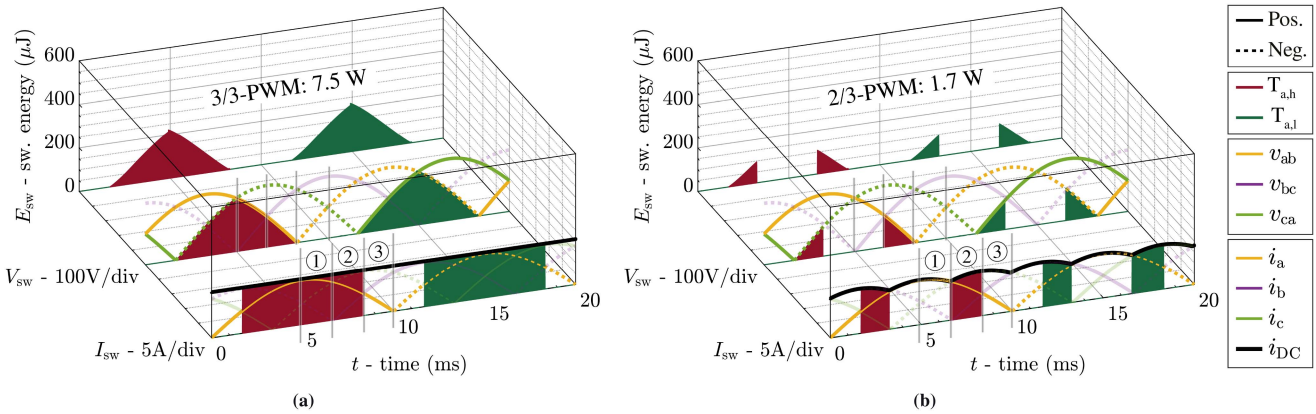

Fig. 4. Calculated hard-switching energy dissipated in the switches $T_{a,h}$ (red) and $T_{a,l}$ (green) connected to phase a over one mains period, and the corresponding switched voltages and currents when (a) 3/3-PWM and (b) 2/3-PWM are applied. In both cases, $V_{out} = 800\,V$ and $P_{out} = 10\,kW$. In average, 1.7 W instead of 7.5 W, i.e., a 77% reduction of switching losses, results if 2/3-PWM instead of 3/3-PWM is employed since the switches switch less frequently and with reduced voltages and currents (details in the text). Note that soft-switching transitions and their losses are neglected.

DC-link inductor, i.e., the corresponding switching-frequency DC-link current ripple, by centering the switching state with a larger v_{pn} within one switching period, e.g., in sector ②, $v_{ac} > v_{bc}$ such that the switching state [ac] is centered, and vice-versa in sector ③ [39], [49].[4]

Importantly, an additional converter stage, e.g., a boost DC/DC-stage as shown in Fig. 2, is always needed to implement 2/3-PWM because the six-pulse-shaped DC-link current has to be regulated by this additional converter stage; and 2/3-PWM can only rectify 3-Φ mains' voltages into six-pulse shaped $\bar{v}_{pn}$ at the output of the CSR-stage so that this converter stage is required to regulate $\bar{v}_{pn}$ into a constant dc output voltage.

C. Switching Loss Comparison

The potential switching loss savings of operating the CSR-stage with 2/3-PWM instead of with 3/3-PWM are analyzed in the following. Focusing on the CSR-stage, a high output voltage ($V_{out} = 800\,V$) that requires operating the boost-type DC/DC-stage in both cases is considered. Fig. 4 compares the hard-switching losses E_{sw} generated in the two bidirectional switches connected to phase a (i.e., $T_{a,h}$ and $T_{a,l}$) considering the 3/3-PWM[5] and the 2/3-PWM for $V_{out} = 800\,V$ and $P_{out} = 10\,kW$.

Before further exploring these results, it is important to briefly discuss the physical realization of these switches, which is indicated in Fig. 2 and shown in detail in Fig. 5, and the nature of the commutations. In general, commutations occur between two switches of one commutation cell in a current DC-link rectifier, e.g., changing the state from [bb] to [ab] implies that the DC-link current commutates from $T_{b,h}$ to $T_{a,h}$, as indicated in Fig. 5; the involved commutation voltage is the line-to-line voltage v_{ab}. As the line-to-line voltage attains both polarities, each switch

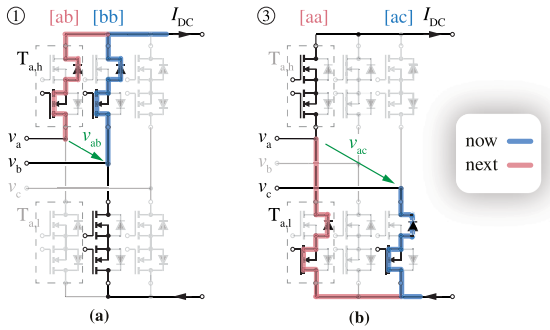

Fig. 5. Two exemplary switching states before and after actual commutations occurring in sectors (a) ① and (b) ③ (see Fig. 3), which directly involve $T_{a,h}$ or $T_{a,l}$, respectively. In sector ①, switching from [bb] to [ab] is a hard-switching transition since the switched voltage $v_{ab} > 0$ and the switched current flow out of the switching node (see Fig. 2). In sector ③, the switched voltage $v_{ac} > 0$ but the switched current flows into the switching node. Thus, switching from [ac] to [aa] is a soft transition. A more detailed explanation is given in the main text.

must be realized by an antiseries connection of two MOSFETs to block these bipolar voltages. Note that, different from the voltage DC-link PFC rectifier where the commutation loop closes over the dc-side commutation capacitors (in parallel with the DC-link capacitors), the commutation loop of the current DC-link rectifier includes ac-side commutation capacitors (in parallel with the ac-side filter capacitors C_{in} in Fig. 2).

For a given polarity of a line-to-line voltage, e.g., v_{ab}, two of the four involved MOSFETs can either be turned ON or turned OFF without affecting the switching state because their antiparallel diodes are forward biased by the line-to-line voltage. While it is generally advantageous to keep these MOSFETs ON (to reduce conduction losses), the current-direction-dependent four-step commutation sequences [59] are needed in practice to ensure that there is always a path for the DC-link current and the ac-side capacitors are never short circuited, resulting in the (intermediate) circuit configurations just prior and after the actual current commutation, as shown in Fig. 5. It is clearly recognizable that the actual commutations are identical to those known from half-bridge arrangements with the voltage DC-link;

[4]Note that the switched voltage of the 3-L boost DC/DC-stage is also aligned at the center of one switching period such that the voltage-time area of the DC-link inductor, i.e., the time integral of the voltage difference $v_{pn} - v_{qr}$ (see Fig. 2), is minimized.

[5]3/3-PWM uses $i_{DC} = \hat{i}_{DC,2/3} = \hat{I}_{in}$, which is the minimum constant DC-link current required to generate 3-Φ sinusoidal mains' currents without modulation saturation.

however, the assignment of turn-ON and turn-OFF losses to the individual MOSFETs changes with the polarity of the involved line-to-line voltage. As here the focus is on system-level loss behavior, losses are assigned to the bidirectional switches, e.g., $T_{\mathrm{a,h}}$ or $T_{\mathrm{a,l}}$, without considering the individual MOSFETs for simplicity. Thus, considering the example occurring in ① when implementing 3/3-PWM (see Fig. 5(a)), the transition from [bb] to [ab] results in a hard switching with $T_{\mathrm{a,h}}$ subject to a hard turn-ON.[6] The other exemplary transition in the low-side commutation cell from [ac] to [aa] occurs in ③ when implementing 3/3-PWM (see Fig. 5(b)), which results in a soft switched with $T_{\mathrm{a,l}}$. Soft-switching transitions are assumed to be lossless.

The hard-switching losses E_{sw} of a given transition can be modeled as

$$E_{\mathrm{sw}} = \left(k_1 I_{\mathrm{sw}}^2 + k_2 I_{\mathrm{sw}} + k_3\right) V_{\mathrm{sw}} + \left(C_{\mathrm{oss,Q}} + C_{\mathrm{par}}\right) V_{\mathrm{sw}}^2 \quad (2)$$

where V_{sw} and I_{sw} indicate the switched voltage and current, respectively. The losses contain two main contributions, i.e., losses introduced by the overlap of the switched voltage and current waveforms, and capacitive losses resulting from the charging and discharging of the semiconductor (charge equivalent) output capacitance $C_{\mathrm{oss,Q}}$ and the parasitic (PCB, etc.) capacitance C_{par} [38].

The hard-switching losses dissipated in $T_{\mathrm{a,h}}$ and $T_{\mathrm{a,l}}$ are indicated in Fig. 4, assuming PFC operation with unity power factor over one mains period. Furthermore, the modulation sequences, i.e., the switching state sequences, of three exemplary sectors are listed in Table II. In sector ①, the switching transition from [bb] to [ab] contributes to significant switching losses because of a comparably large switched line-to-line voltage v_{ab}. However, such a hard-switching transition only exists for 3/3-PMW since the zero state [bb] is not needed for 2/3-PWM; note that the significantly longer intervals without hard-switching losses are achieved when using 2/3-PWM. In sector ②, hard-switching losses are generated when switching from [bc] to [ac] for both 3/3-PWM and 2/3-PWM. However, importantly, in sector ②, the switched line-to-line voltage v_{ab} (see Fig. 4) is lower, leading to relatively small switching losses compared to the one generated in sector ① with 3/3-PWM. In sector ③, $T_{\mathrm{a,h}}$ and $T_{\mathrm{a,l}}$ are not subjected to hard turn-ON transitions and, hence, almost no switching losses are generated for both 3/3-PWM and 2/3-PWM.

Thus, advantageously, 2/3-PWM does not need those hard-switched transitions that in 3/3-PWM result in the largest contributions to the overall switching losses because of the high switched voltages. Considering, e.g., the applied SiC MOSFET *C3M0021120 K* and its detailed switching loss models based on calorimetric measurements [38], averaging the hard-switching energy dissipation over one mains period results in switching losses of 1.7 W for 2/3-PWM instead of 7.5 W for 3/3-PWM, i.e., a 77% reduction of switching losses (for PFC operation with unity power factor). Note that, furthermore, also the lower conduction losses (reduced by 8% [49]) are expected since 2/3-PWM employs the minimum possible time-varying DC-link current.

[6] All hard-switching losses are assigned to the turning-ON switch for simplicity [38].

III. Loss-Optimal Operation

While 2/3-PWM reduced the CSR-stage switching losses, it requires the DC/DC-stage to operate; on the other hand, the CSR-stage alone can control low output voltages but then needs to operate with 3/3-PWM. It is, therefore, interesting to consider the loss-optimal operating modes of the 3-Φ bB current DC-link PFC rectifier system (see Fig. 2), whose key specifications and circuit parameters are listed in Table I.

The wide-output-voltage range (200–1000 V) is covered by three operating modes [39], i.e., buck mode ($V_{\mathrm{out}} < {}^3\!/_2\hat{V}_{\mathrm{in}} = 488\,\mathrm{V}$), boost mode ($V_{\mathrm{out}} > \sqrt{3}\hat{V}_{\mathrm{in}} = 563\,\mathrm{V}$), and, in between, transition mode (${}^3\!/_2\hat{V}_{\mathrm{in}} < V_{\mathrm{out}} < \sqrt{3}\hat{V}_{\mathrm{in}}$), by collaboratively operating the CSR-stage and the DC/DC-stage; see also the simulated key waveforms in Fig. 6. The semiconductor losses, as the main contribution to the total converter, are minimized if the following two criteria are met.

1) The minimum possible DC-link current should be used, which results in minimum conduction losses of the whole system as the DC-link current flows through the turned-ON semiconductors of the CSR-stage and the DC/DC-stage, and in the DC-link inductor. The CSR-stage forms the 3-Φ mains' currents (see Section II), and likewise, the DC/DC-stage forms the output dc current by pulsewidth modulating the DC-link current. Thus
$$i_{\mathrm{DC}} \geq \max\left(|i_{\mathrm{a}}|, |i_{\mathrm{b}}|, |i_{\mathrm{c}}|, I_{\mathrm{out}}\right) \quad (3)$$
must be guaranteed at any moment; equality results in the (potentially time varying) minimum possible DC-link current.
2) The number of switching instants and/or the switched voltages/currents should be minimized. Thus, 2/3-PWM of the CSR-stage should be used whenever the DC/DC-stage must operate anyhow because of a high output voltage, or alternatively, the DC/DC-stage should be clamped (i.e., $T_{\mathrm{DC,hp}}$ and $T_{\mathrm{DC,hn}}$ are permanently ON).

These three main operating modes are then explained in detail as follows.

A. Buck Mode

If the output voltage is low, i.e., $V_{\mathrm{out}} < {}^3\!/_2\hat{V}_{\mathrm{in}} = 488\,\mathrm{V}$, the converter operates in the buck mode (see Fig. 6(a)). The output voltage can be obtained by the CSR-stage directly stepping down the 3-Φ mains' voltages, and no boost functionality is needed, i.e., the switching losses of the DC/DC-stage can be avoided by permanently turning ON $T_{\mathrm{DC,hp}}$ and $T_{\mathrm{DC,hn}}$ [note that constant $v_{\mathrm{qr}} = V_{\mathrm{out}}$ in Fig. 6(a)]. Furthermore, clamping the DC/DC-stage automatically results in

$$i_{\mathrm{DC}} = I_{\mathrm{DC,3/3}} = I_{\mathrm{out}} > \max\left(|i_{\mathrm{a}}^*|, |i_{\mathrm{b}}^*|, |i_{\mathrm{c}}^*|\right) \quad (4)$$

such that the minimum possible DC-link current is applied according to (3). Sinusoidal 3-Φ mains' currents are realized

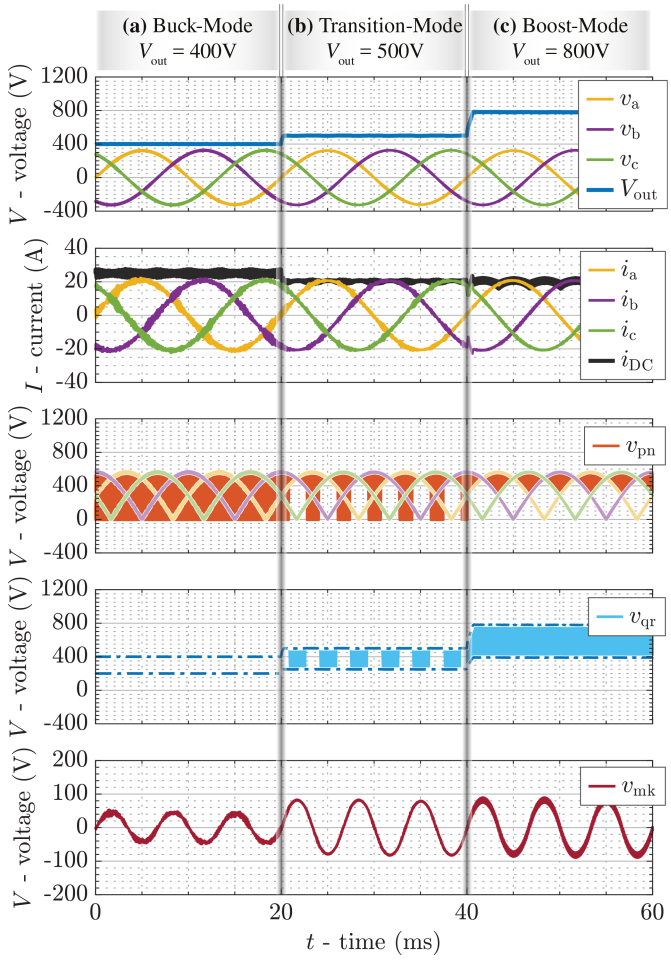

Fig. 6. Simulated key waveforms of the 3-Φ bB current DC-link PFC rectifier system, as shown in Fig. 2, when operating in (a) buck mode, (b) transition mode, and (c) boost mode when supplying constant power at different output voltages. The switched DC-side voltage of the CSR-stage, v_{pn}, and the switched input voltage of the DC/DC-stage, v_{qr}, indicate the CSR-stage modulation method (with 2/3-PWM, v_{pn} never attains zero as no zero states are employed) and/or the clamping of the DC/DC-stage. The voltage v_{mk} across the integrated CM filter capacitor C_{CM} verifies that mainly an LF CM voltage appears at the output terminals. Note that v_{qr} is a 3-L switched voltage with the levels of 0, $V_{out}/2$, and V_{out} if the DC/DC-stage is actively switching.

by 3/3-PWM of the CSR-stage, i.e., v_{pn} also attains zero (corresponding to the zero switching states) in Fig. 6(a).

B. Boost Mode

If the output voltage is high, i.e., $V_{out} > \sqrt{3}\hat{V}_{in} = 563\,V$, the converter operates in the boost mode (see Fig. 6(c)). The DC/DC-stage *must* operate to step-up the output voltage of the CSR-stage to higher output voltages. Thus, advantageously, the two converter stages should be operated synergetically/collaboratively; as the DC/DC-stage is needed anyways, it can control the DC-link current to the six-pulse shape defined by

$$i_{DC} = i_{DC,2/3} = \max(|i_a|, |i_b|, |i_c|) > I_{out} \tag{5}$$

which allows implementing 2/3-PWM of the CSR-stage with significantly reduced switching losses (see Section II). Note that, in Fig. 6(c), the input voltage of the DC/DC-stage v_{qr} is now a high-frequency (HF) switched voltage, and on the other hand, the DC-side voltage of the CSR-stage v_{pn} never attains zero, corresponding to the absence of zero states in 2/3-PWM. The time-varying DC-link current $i_{DC,2/3}$ is also the minimum possible DC-link current according to (3) and, hence, minimizes the overall conduction losses.

C. Transition Mode

If the output voltage is in the range of $^3/_2\hat{V}_{in} < V_{out} < \sqrt{3}\hat{V}_{in}$, i.e., higher than the buck-mode boundary but lower than the boost-mode boundary, the boost functionality provided by the DC/DC-stage is not needed continuously, but only during parts of the mains period. By selecting the DC-link current as in (3), essentially

$$i_{DC} = \max\left(I_{DC,3/3}, i_{DC,2/3}\right) \tag{6}$$

results and, hence, the CSR-stage operation alternates between 3/3-PWM and 2/3-PWM accordingly, and the DC/DC-stage is activated only when the boost functionality is required. This is clearly visible in the simulated v_{pn} and v_{qr} waveforms, as shown in Fig. 6(b).

IV. Synergetic Control Strategy

A synergetic control strategy of the 3-Φ bB current DC-link PFC rectifier system (see Fig. 2), which ensures that two converter stages always operate collaboratively in loss-optimum modes and transitions seamlessly between these modes if the output voltage changes, is presented in this section. While a control method in [40] has been introduced earlier, we present here a simplified and intuitive version (without modulation indices of two stages) that, however, does not sacrifice any functionality. Fig. 7 shows the corresponding block diagram and highlights the three main functional blocks, i.e., *output voltage control*, *DC-link current reference generation*, and *DC-link current control*, which are explained in detail in the following sections.

A. Output Voltage Control

The outermost control loop (see Fig. 7(a)) tracks the output-voltage reference V_{out}^* by providing the corresponding power reference P^*. From that, the CSR-stage input reference conductance G^* is given as follows:

$$G^* = \frac{P^*}{\frac{3}{2}\hat{V}_{in,meas}^2}. \tag{7}$$

The 3-Φ sinusoidal mains current references i_a^*, i_b^*, and i_c^* are then selected proportional to the corresponding measured 3-Φ input voltages v_a, v_b, and v_c such that purely ohmic operation of the 3-Φ mains results. The output-current reference I_{out}^* is calculated by dividing P^* by V_{out}^*.

B. DC-Link Current Reference Generation

The selection of the appropriate DC-link current reference (see Fig. 7(b)) is at the core of the proposed synergetic control structure and vital to achieving seamless and automatic transitions between the different operating modes and modulation

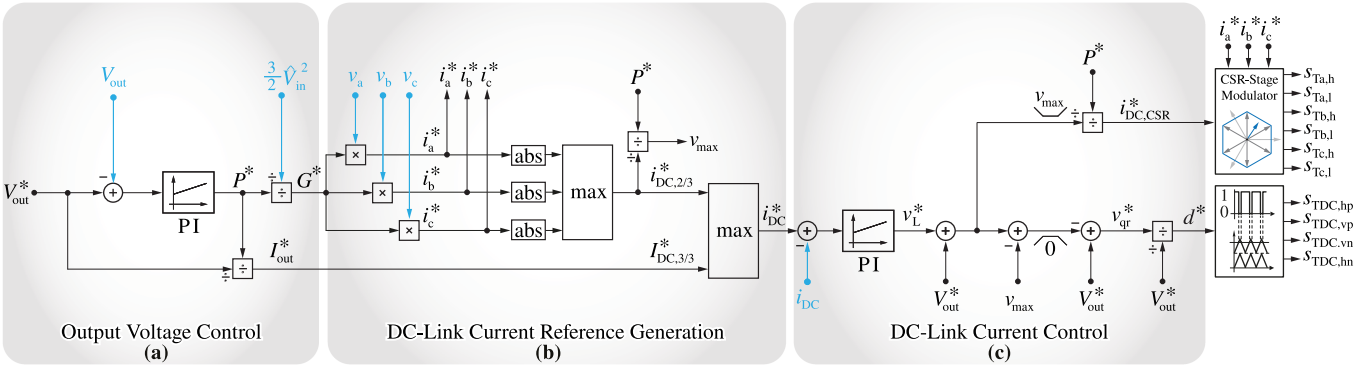

Fig. 7. Block diagram of the proposed synergetic control strategy 3-Φ bB current DC-link PFC rectifier system (see Fig. 2). The three main functional blocks enable collaborative operation of the 3-Φ CSR-stage and of the boost-type DC/DC-stage, and seamless transitions between the buck and boost modes needed to cover the wide-output-voltage range. Note that the regular sampling is employed to sense only local-average (over one switching period) quantities.

schemes. As discussed above in Section III, in the buck mode, $i_{\mathrm{DC}} = I^*_{\mathrm{DC},3/3} = I^*_{\mathrm{out}}$ is used, which results in 3/3-PWM of the CSR-stage while the DC/DC-stage is clamped. In the boost mode, $i_{\mathrm{DC}} = i^*_{\mathrm{DC},2/3} = \max(|i^*_a|, |i^*_b|, |i^*_c|)$ is needed to realize 2/3-PWM of the CSR-stage. Thus, the overall DC-link current reference is

$$i^*_{\mathrm{DC}} = \max\left(I^*_{\mathrm{DC},3/3}, i^*_{\mathrm{DC},2/3}\right) \tag{8}$$

i.e., the DC-link current reference always corresponds to the minimum possible DC-link current leading to reduced switching losses and conduction losses.

C. DC-Link Current Control

Finally, the DC-link current is closed-loop controlled (see Fig. 7(c)) by comparing the DC-link current reference i^*_{DC} with the measured DC-link current i_{DC}. The deviation is processed by a PI controller that then defines the voltage v^*_{L} across the DC-link inductor L_{DC} needed to counteract the control error. It is material to highlight that v^*_{L} can be realized by either the CSR-stage *and/or* the DC/DC-stage, e.g., a positive v^*_{L} can be generated by either an increased output voltage v_{pn} of the CSR-stage or a decreased input voltage v_{qr} of the DC/DC-stage (see Fig. 2 for the definition of these voltages). Thus, the second part of the DC-link current control structure is designed to democratically assign v^*_L to the CSR-stage or the DC/DC-stage according to the loss-optimal operating modes, as discussed in Section III.

To do so, it is useful to define $v_{\max} = P^*/i^*_{\mathrm{DC},2/3}$, i.e., $v_{\max}$ is the local-average value of the CSR-stage DC-side voltage v_{pn} that would result if $i_{\mathrm{DC}} = i^*_{\mathrm{DC},2/3}$ as needed for 2/3-PWM. Note that $v_{\max}$ is, thus, time varying, too, to deliver constant power.

If $V^*_{\mathrm{out}} < v_{\max}$, the CSR-stage alone can regulate the DC-link current and the DC/DC-stage should be clamped, i.e., permanently gating $\mathrm{T}_{\mathrm{DC,hp}}$ and $\mathrm{T}_{\mathrm{DC,hn}}$ ON. A positive v^*_{L} can, thus, be realized by increasing the CSR-stage DC-side voltage v_{pn}, i.e., a shortening of the zero states used in 3/3-PWM of the CSR-stage. Thus, a positive v^*_{L} should result in a reduced reference DC-link current $i^*_{\mathrm{DC,CSR}}$ fed to the space-vector pulsewidth modulator of the CSR-stage. Following the control diagram and assuming that v^*_{L} is comparably small, we have

$$i^*_{\mathrm{DC,CSR}} = \frac{P^*_{\mathrm{out}}}{\min\left(V^*_{\mathrm{out}} + v^*_{\mathrm{L}}, v_{\max}\right)} = \frac{P^*_{\mathrm{out}}}{V^*_{\mathrm{out}} + v^*_{\mathrm{L}}} \tag{9}$$

which results in the desired behavior. Likewise, a negative v^*_{L} results in an increase of $i^*_{\mathrm{DC,CSR}}$ and, hence, in an elongation of the zero vector dwell times. The DC/DC-stage modulation index d^* is calculated as follows:

$$d^* = \frac{-\max\left(v^*_{\mathrm{L}} + V^*_{\mathrm{out}} - v_{\max}, 0\right) + V^*_{\mathrm{out}}}{V^*_{\mathrm{out}}} = \frac{0 + V^*_{\mathrm{out}}}{V^*_{\mathrm{out}}} = 1 \tag{10}$$

so that d^* is not affected by v^*_{L} and ensures that $T_{\mathrm{DC,hp}}$ and $T_{\mathrm{DC,hn}}$ are turned ON continuously.

If, conversely, $V^*_{\mathrm{out}} > v_{\max}$, only the DC/DC-stage can regulate the DC-link current since the CSR-stage operates with 2/3-PWM, i.e., no zero switching states and, thus, no voltage regulation capability. A positive v^*_{L} can then be realized by decreasing the input voltage v_{qr} of the DC/DC-stage. Therefore, the DC/DC-stage modulation index d^* is modified by v^*_{L} (which, again, is assumed to be comparably small) as

$$d^* = \frac{-\max\left(v^*_{\mathrm{L}} + V^*_{\mathrm{out}} - v_{\max}, 0\right) + V^*_{\mathrm{out}}}{V^*_{\mathrm{out}}} = \frac{v_{\max} - v^*_{\mathrm{L}}}{V^*_{\mathrm{out}}}. \tag{11}$$

On the other hand

$$i^*_{\mathrm{DC,CSR}} = \frac{P^*_{\mathrm{out}}}{\min\left(V^*_{\mathrm{out}} + v^*_{\mathrm{L}}, v_{\max}\right)} = \frac{P^*_{\mathrm{out}}}{v_{\max}} = i^*_{\mathrm{DC},2/3} \tag{12}$$

results, which ensures 2/3-PWM operation of the CSR-stage.

Note that in the transition mode, therefore, i_{DC} is regulated alternatively by the CSR-stage or by the DC/DC-stage, i.e., v^*_{L} is realized by either (modified) 3/3-PWM of the CSR-stage as in (9) or by (modified) DC/DC-stage duty cycles as in (11). Importantly, there are no abrupt changes in v^*_{L} but only different converter stages realize the required v^*_{L} depending on the (instantaneous) relation of V^*_{out} and $v_{\max}$. Advantageously, the loop gain of the DC-link current control is not affected, and seamless transitions between different operating points are achieved.

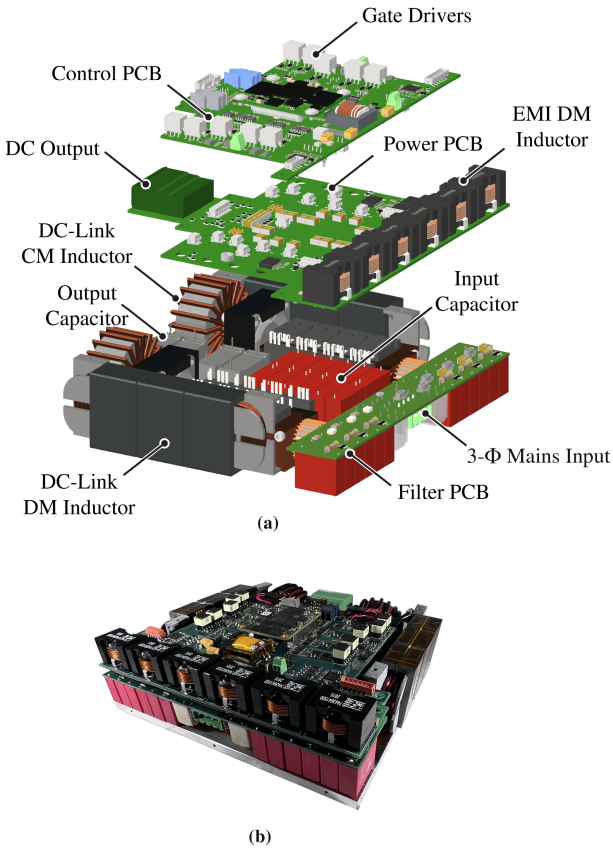

Fig. 8. (a) Exploded view of the 10 kW 3-Φ bB current DC-link PFC rectifier hardware demonstrator (see Fig. 2 for the schematics and Table I for key components). (b) Photograph of the realized prototype. The dimensions are $184 \times 172 \times 49\,\mathrm{mm}^3$ ($9.8 \times 5.1 \times 1.9\,\mathrm{in}^3$), resulting in a power density of $6.4\,\mathrm{kW/dm}^3$ ($107.5\,\mathrm{W/in}^3$). Operating from the 400 V 3-Φ mains and employing 1200 V SiC (CSR-stage) and 900 V SiC (DC/DC-stage) MOSFETs, a wide-output-voltage range of 200–1000 V is covered.

V. Experimental Verification

A 10-kW hardware demonstrator (see Fig. 8) has been built to experimentally verify the proposed synergetic control structure and to comprehensively characterize the conducted EMI performance and efficiency behavior over the wide-output-voltage and power ranges. Detailed modeling of component losses and volumes, a corresponding Pareto optimization (considering efficiency and power density), and finally, a selected design have been presented earlier in [38] and [39], considering a compact two-stage EMI filter providing sufficient attenuation, i.e., the maximum required attenuation over the wide-output-voltage range, to meet the requirements of CISPR 11 class A. Thus, design details are not reiterated here for the sake of brevity. Table I summarizes the key components of the realized demonstrator.[7]

Fig. 8 shows an exploded-view three-dimensional (3-D) CAD rendering and a photograph of the 10-kW hardware demonstrator with outer dimensions of $184 \times 172 \times 49\,\mathrm{mm}^3$ ($9.8 \times 5.1 \times 1.9\,\mathrm{in}^3$) and, thus, a power density of $6.4\,\mathrm{kW/dm}^3$ ($107.5\,\mathrm{W/in}^3$). The CSR-stage employs antiseries connections of 1200 V SiC MOSFETs for each bidirectional switch and the 3-L DC/DC-stage uses 900 V SiC MOSFETs. The realized demonstrator is composed of three separate PCBs: the control PCB (Zynq 7000 SoC, gate drivers, measurement data acquisition, etc.), the power PCB (carrying the power transistors, ac-side and DC-side capacitors, etc.), and a dedicated EMI filter PCB.

A. Experimental Waveforms

Characteristic waveforms of the10-kW hardware demonstrator are presented in Fig. 9 for operation in (a) buck mode, (b) transition mode, and (c) boost mode. The phase a voltage v_a, the phase a current i_a, the DC-link current i_DC, and the output voltage V_out illustrate the desired behavior at the ac input and the dc output. Furthermore, the switched voltage v_pn at the output of the CSR-stage clearly indicates the CSR-stage operation with 2/3-PWM or 3/3-PWM. Similarly, the switched voltages v_qm and v_mr indicate whether the DC/DC-stage operates or is clamped. The measured CM capacitor voltage v_mk, mainly consisting of LF components, verifies the function of the integrated CM filter, i.e., suppressing the HF CM noise at the dc output. Note that the close similarity of the measured waveforms to the simulation results is shown in Fig. 6.

Specifically, Fig. 9(a) presents the buck-mode operation with $V_\mathrm{out} = 400\,\mathrm{V}$ and $P_\mathrm{out} = 10\,\mathrm{kW}$, where the CSR-stage operates with 3/3-PWM and the DC/DC-stage clamps, i.e., $T_\mathrm{DC,hp}$ and $T_\mathrm{DC,hn}$ are permanently ON as visible from v_qm and v_mr. Fig. 9(c) shows the boost-mode operation with $V_\mathrm{out} = 1000\,\mathrm{V}$ and $P_\mathrm{out} = 10\,\mathrm{kW}$, where the DC-link current i_DC is regulated into the six-pulse shape, i.e., the envelope of the phase current absolute values needed for 2/3-PWM of the CSR-stage, i.e., v_pn never attains 0 V (freewheeling states are not employed), resulting in reduced switching losses of the CSR-stage. However, the DC/DC-stage has to regulate the DC-link current in the boost mode and control the output voltage at the same time. In the transition-mode operation, the CSR-stage alternatively operates with 2/3-PWM and 3/3-PWM and the DC/DC-stage is democratically activated to shape the DC-link current if needed; this ensures loss-optimal operation.

The proposed control strategy is thoroughly verified by the measurements, as shown in Fig. 10, where the output voltage steps up from 0 to 800 V with a load resistance of $80\,\Omega$. Automatic and smooth transitions between different operating modes, i.e., buck mode, transition mode, and boost mode, are achieved, and the loss-optimum modulation (i.e., 2/3-PWM of the CSR-stage if possible; clamped DC/DC-stage otherwise) is employed. Note further the smooth startup, which the current DC-link topology achieves without the need for precharging a DC-link capacitor (via precharge resistors) as is the case for voltage DC-link converters.

B. Efficiency Measurements

The efficiency of the 10-kW hardware demonstrator, as shown in Fig. 8, is measured (Yokogawa WT3000) over the full wide-output-voltage (from 200 to 1000 V) and output-power

[7]Minor differences with respect to the selected design from [38] are due to mechanical/availability considerations. The loss calculations shown in the following employ the loss models from [38] but, of course, consider the actual components' data.

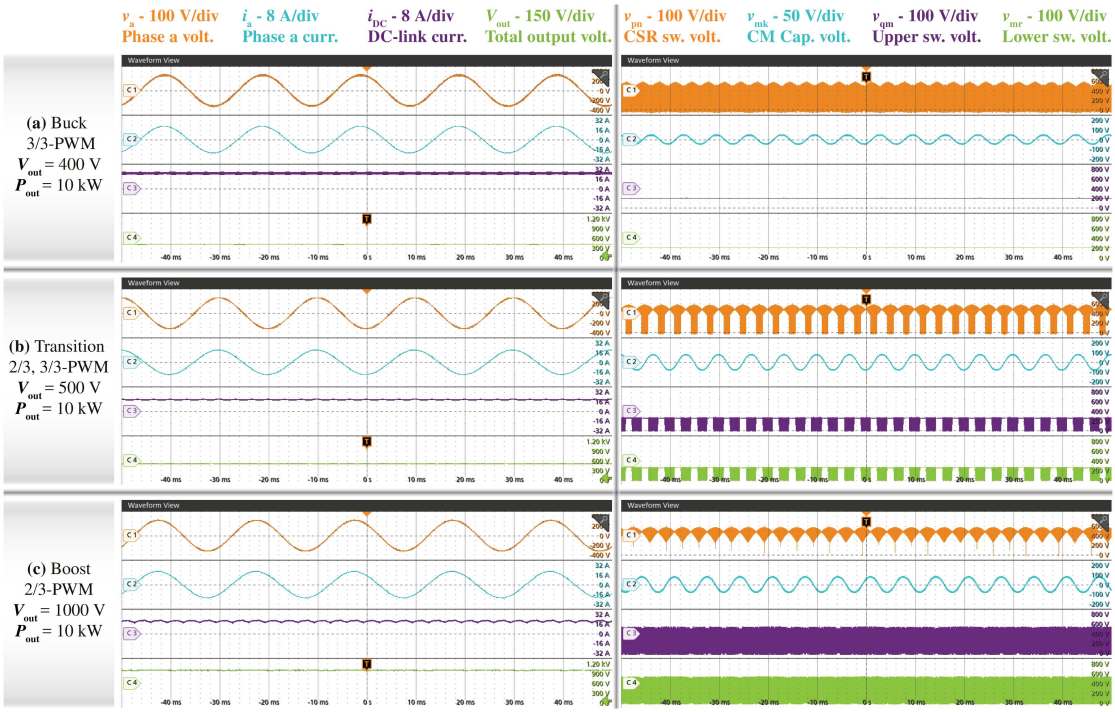

Fig. 9. Experimental waveforms of the converter shown in Fig. 8, operating with the proposed synergetic control strategy. (a) Buck mode, where the CSR-stage uses 3/3-PWM to step down the mains voltage to the low output voltage and the DC/DC-stage is clamped (note that v_{qm} and v_{mr} are constant). (b) Transition mode, where the CSR-stage changes between 3/3-PWM and 2/3-PWM, and the DC/DC-stage is democratically activated only when the boost functionality is required. (c) Boost mode, where the DC/DC-stage regulates the DC-link current i_{DC} to the six-pulse shape needed for 2/3-PWM of the CSR-stage (note the absence of the zero level in v_{pn}).

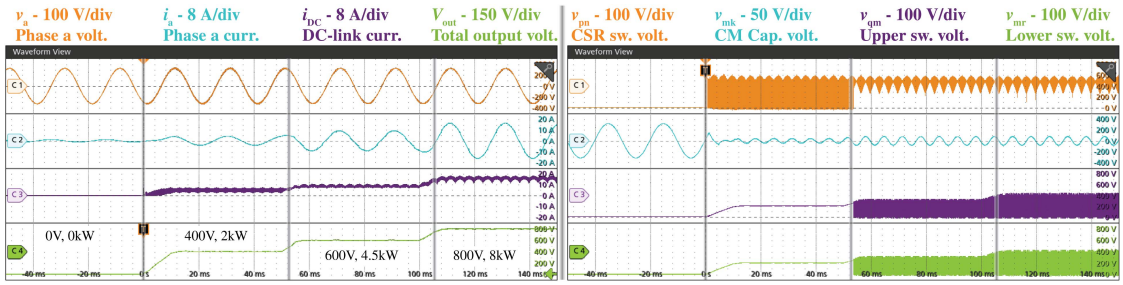

Fig. 10. Experimental waveforms of the converter shown in Fig. 8 when supplying a resistive load of 80 Ω and the output voltage set point is changed from 0 to 800 V, i.e., covering a wide-output-voltage range. Automatic and seamless transitions from buck mode to boost mode are achieved by the proposed synergetic control strategy (see Fig. 7). Also note the very smooth startup.

(from full load down to 25% load) ranges. Thus, Fig. 11(a) shows the measured efficiency results in dependence of the output voltage and the load, considering the loss-optimum operating mode for each operating point; Fig. 11(b) shows the same information in a 2-D contour plot, where, in addition, the operating points at which the efficiency measurements have been taken are indicated (linear interpolation is used in-between). Clearly, the converter features a relatively flat characteristic over the full operating area. High efficiencies, i.e., above 98%, are achieved for a large part of the operating range, i.e., in most of the operating ranges, where output voltages are above 400 V and more than 25% of the rated load. To further illustrate this, Fig. 12(a) shows efficiency versus output voltage at rated power, and Fig. 12(b) shows efficiency versus output power for different output voltages. A peak efficiency of 98.8% at 520 V and 5 kW can be observed.

It is further worthwhile, for the first time, to experimentally quantify the system-level efficiency improvement when using 2/3-PWM instead of 3/3-PWM in the boost mode and the transition mode (note that the boost-type DC/DC-stage sensibly *must* be clamped in the buck mode). Fig. 11(c) shows the measured efficiency when operating with 3/3-PWM in those parts of the operating range where the loss-optimal operation would employ 2/3-PWM. Fig. 11(d) then shows the efficiency improvements between the proposed loss-optimum operation (using 2/3-PWM whenever possible) and the conventional approach that does

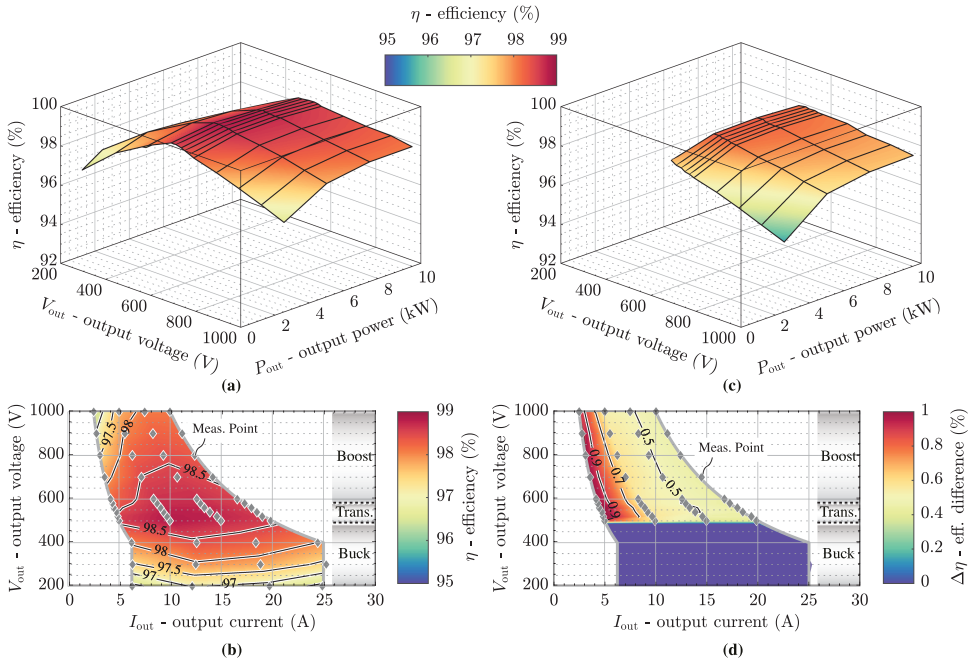

Fig. 11. Measured (Yokogawa WT3000) efficiencies of the realized 10-kW hardware demonstrator, as shown in Fig. 8, when operating over a wide-output-voltage (200–1000 V) and output-power (from full load to 25 % load) ranges, using the (a) proposed loss-optimal modulation scheme with 2/3-PWM of the CSR-stage whenever possible; (b) shows the corresponding efficiency contours and indicates the measured operating points (linear interpolation in-between). (c) shows the measured efficiency of the conventional operation using 3/3-PWM instead of 2/3-PWM where applicable (i.e., in the boost mode and the transition mode). (d) quantifies the efficiency difference between the (a) proposed and (c) state-of-the-art methods, highlighting up to 1% efficiency improvement in the transition mode and the boost mode. Note that no efficiency difference is expected in the buck mode, where 3/3-PWM must be used in all cases. Thus, (c) does not show efficiencies for buck-mode operating points; the efficiency difference in that operating range is always zero (see (d)).

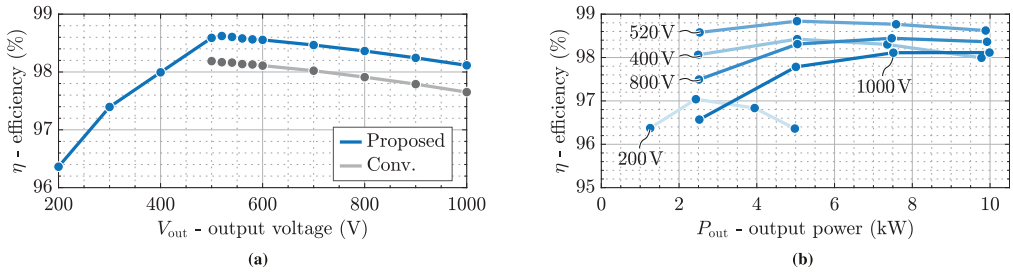

Fig. 12. Measured (Yokogawa WT3000) efficiency curves of the realized 10-kW hardware demonstrator, as shown in Fig. 8. (a) Efficiency versus output voltage V_{out} at rated power (or rated output current below 400 V, see Fig. 1). (b) Efficiency versus output power P_{out} (using the proposed loss-optimal modulation scheme). A peak efficiency of 98.8% when $V_{\text{out}} = 520\,\text{V}$ and $P_{\text{out}} = 5\,\text{kW}$ is achieved.

never employ 2/3-PWM, indicating improvements of up to 1% in the transition mode and the boost mode (again, no difference is expected in the buck mode).

Finally, Fig. 13 provides the calculated loss breakdowns versus (a) output voltage at rated power, (b) output power at 400 V (buck mode), and (c) output power at 800 V (boost mode). The loss modeling has been presented earlier [38], but the calculation results shown here have been updated to reflect the components actually used in the demonstrator (see Table I). Moreover, the loss breakdowns provide the following observations.

1) Conduction losses account for a significant proportion of the total losses. As these reduce with the square of the current (and accordingly with the power), a relatively flat efficiency characteristic of the converter results.
2) In buck mode, the CSR-stage operating with 3/3-PWM contributes considerable switching losses, whereas the DC/DC-stage only generates conduction losses and zero switching losses due to clamping.
3) In boost mode, 2/3-PWM is used for the CSR-stage and leads to almost negligible switching losses. On the other hand, the DC/DC-stage generates comparably high switching losses because of the high switched voltage (boost mode).

Fig. 13 also indicates the measured (Yokogawa WT3000) losses, and a very close match between calculation and measurement can be observed.

C. EMI Measurement

Conducted EMI precompliance tests have been carried out to assess the compliance of the realized 10-kW hardware demonstrator (see Fig. 8) with the limits set forth in CISPR 11 Class A

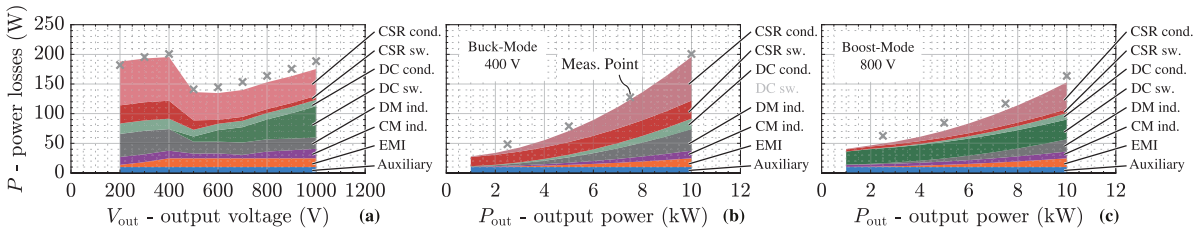

Fig. 13. Calculated loss breakdowns of the converter shown in Fig. 8 and loss-optimal operation in (a) for different output voltages V_{out} and rated power (or rated output current below 400 V), in (b) for buck-mode operation ($V_{\text{out}} = 400\,\text{V}$) and varying power P_{out}, and in (c) for boost-mode operation ($V_{\text{out}} = 800\,\text{V}$) and varying power. The measured (Yokogawa WT3000) total losses are in excellent agreement with the calculations.

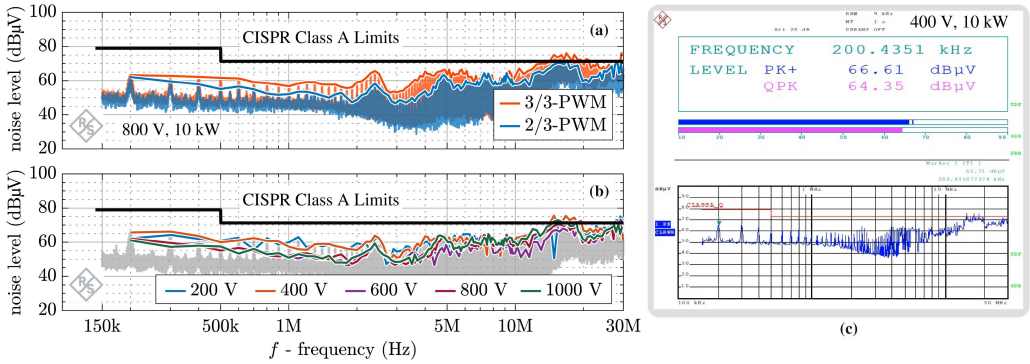

Fig. 14. Measured conducted EMI noise emission spectra of the realized 10-kW hardware demonstrator, as shown in Fig. 8. The Rhode & Schwarz ESPI3 test receiver uses the CISPR 11 peak (PK) detector with a resolution bandwidth of 9 kHz, 4 kHz step size, and 1 ms measurement time. The local peak values are connected by colored envelopes for easier comparisons between different operating points. (a) Comparison of the EMI noise emissions between 2/3-PWM and 3/3-PWM when operating in the boost mode, i.e., $V_{\text{out}} = 800\,\text{V}$ and $P_{\text{out}} = 10\,\text{kW}$, indicating a maximum reduction of 9.7 dBμV at 2.4 MHz when using 2/3-PWM instead of 3/3-PWM. (b) Final conducted EMI precompliance test results of the demonstrator using the loss-optimum operating modes for each operating point (different output voltages, rated power); note that the minor violations of the CISPR 11 Class A limit above 10 MHz could likely be defined by placing the converter in a grounded housing. (c) Screenshot directly taken from the EMI test receiver at the worst-case operating point ($V_{\text{out}} = 400\,\text{V}$and $P_{\text{out}} = 10\,\text{kW}$), indicating the QP value of 64.4 dBμV at 200 kHz.

for the frequency range of 150 kHz–30 MHz. The test setup consists of a Rhode & Schwarz ESH2-Z5 3-Φ LISN and a Rhode & Schwarz ESPI3 EMI test receiver.

First, the differences in the conducted EMI emission characteristics when operating with 2/3-PWM or, conventionally, 3/3-PWM for boost-mode operating points are compared. Fig. 14(a) presents EMI measurement results when operating in the boost mode ($V_{\text{out}} = 800\,\text{V}$ and $P_{\text{out}} = 10\,\text{kW}$) with the two different modulation schemes used in the CSR-stage. In general, 2/3-PWM results in lower noise levels, with a maximum reduction of 9.7 dBμV at 2.4 MHz. This can be explained by the difference between DM/CM noise sources. Fig. 15 first presents the HF DM/CM noise source waveforms generated by 2/3-PWM and 3/3-PWM, i.e., the switched current $i_{\text{a}'}$ (see Fig. 2) and the CSR-stage CM voltage $v_{\text{CM,CSR}} = (v_{\text{pk}} + v_{\text{nk}})/2$ (see [38] for a detailed analysis; note that the CM noise generated by the DC/DC-stage is neglected here since the focus is on comparing the EMI performances of different CSR-stage modulation schemes). To compare the required EMI filter efforts, the DM and CM voltage spectra that would be measured by a LISN in the absence of an EMI filter are provided. The DM noise source can, thus, be represented by the voltage that would appear at the LISN's 50 Ω measurement resistor if $i_{\text{a}'}$ would directly flow in this resistor. On the other hand, the CM voltage defined above is directly the relevant noise source if a comparably large parasitic capacitance of the converter's output to PE is assumed as a worst case. Thus, the calculated noise spectra (see Fig. 15) indicate that 2/3-PWM results in a reduction of the DM noise of up to 6 dBμV (at 500 kHz). Regarding the CM noise, the maximum reduction is similar, i.e., 6 dBμV ∼ 8 dBμV, but observed for (almost) all frequency components. Hence, it can be assumed that mainly the lower CM noise, which is a direct consequence of the CSR-stage not using zero states with 2/3-PWM [39], contributes to the overall lower noise emissions of the converter operating with 2/3-PWM compared with 3/3-PWM. This implies further that a converter originally designed without considering 2/3-PWM can advantageously be operated with 2/3-PWM (by, essentially, only changing the control method) without the need for a redesign of the EMI filter.

Moreover, considering the loss-optimum operation, Fig. 14(b) shows conducted EMI noise emission measurements of the 10-kW demonstrator over the full output-voltage range at rated power (note that the output-current limit restricts the power to $P_{\text{out}} = 5\,\text{kW}$ for the operating point at $V_{\text{out}} = 200\,\text{V}$). Because the designed EMI filter (see Table I) achieves a similar DM and CM attenuation, e.g., roughly 110 dBμV at 200 kHz according to the detailed discussion in [38], and because of the higher DM noise emission levels for the exemplary operating point discussed in the context of Fig. 15, it is likely that the DM noise

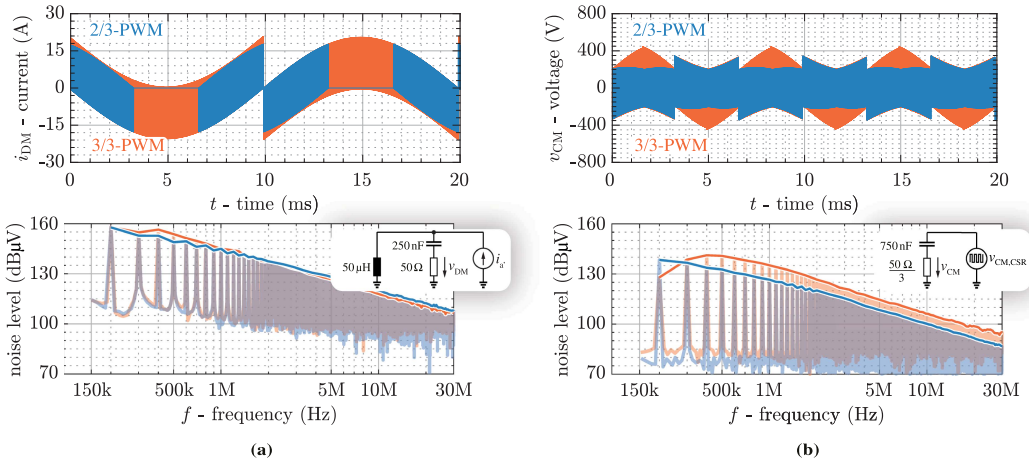

Fig. 15. Comparison of calculated HF (a) DM and (b) CM EMI noise waveforms and spectra (as they would appear at the LISN without an EMI filter present) for operation with 2/3-PWM *(blue)* or 3/3-PWM *(orange)* in the boost mode at $V_{out} = 800\,\mathrm{V}$ and $P_{out} = 10\,\mathrm{kW}$.

dominates in the measurement results, especially when the CSR-stage operates with high modulation indices. Thus, focusing on the measured noise at 200 kHz, i.e., the first harmonic of the switching frequency that lies inside of the regulated frequency range, it is observed the following.

1) Higher noise results for operating points in the buck mode, e.g., $V_{out} = 200\,\mathrm{V}$ or 400 V, than for operating points in the boost mode, e.g., $V_{out} = 600\,\mathrm{V}$, 800 V, or 1000 V, since a higher DC-link current, i.e., a constant DC-link current of 25 A in the buck mode instead of a six-pulse-shaped DC-link current with a peak value of 20.5 A in the boost mode, must be used.
2) The worst case at 400 V is expected by comparing the rms values of the HF switched current $i_{a'}$, i.e., 10.5 A at 200 V, 10.8 A at 400 V, and 6.8 A at 800 V.
3) Similar EMI noise spectra are measured for the three operating points in boost mode since the CSR-stage operates identically with 2/3-PWM and, thus, with the same DC-link current. These results indicate that the DC/DC-stage does not strongly affect the ac-side EMI performance.

Finally, considering the worst-case operating point at $V_{out} = 400\,\mathrm{V}$ and $P_{out} = 10\,\mathrm{kW}$, Fig. 14(c) shows a screenshot of the EMI test receiver with a quasi-peak (QP) measurement result of $64.4\,\mathrm{dB\mu V}$ at 200 kHz, which indicates compliance with CISPR 11 Class A.

VI. Conclusion

Targeting advanced ac/dc front-end converters for EV charger applications, this article thoroughly studies and analyzes a 3-Φ bB current DC-link PFC rectifier that consists of a 3-Φ buck-type CSR-stage cascaded by a 3-L boost-type DC/DC-stage via a shared DC-link inductor. An ultrawide-output-voltage range, i.e., from 200 to 1000 V, can be covered by three loss-optimal operating modes: in the buck mode (for low output voltages), the CSR-stage operates with RCM 3/3-PWM and the DC/DC-stage is clamped to avoid switching losses; in the boost mode (for high output voltages), the CSR-stage operates with 2/3-PWM, i.e., only two out of three phases switch within one switching period such that the CSR-stage bridge legs switch less frequently and advantageously only in those respective sectors of the mains' periods where the switching occurs at relatively low voltages and currents; at the same time, still sinusoidal grid currents are achieved by using the DC/DC-stage to shape the DC-link current to follow the typical six-pulse shape given by the maximum absolute values of the 3-Φ mains' currents. Furthermore, a simple and intuitive synergetic control strategy is proposed to operate the CSR-stage and the DC/DC-stage collaboratively in the loss-optimum operating modes, and to achieve an automatic, seamless transition between these loss-optimal operating modes when the output voltage changes. In particular, this also ensures loss-optimum operation in the transition mode (for output voltages between buck mode and boost mode), where the minimum possible DC-link current is always ensured and the system, hence, seamlessly and democratically transitions between 3/3-PWM and 2/3-PWM several times per mains period.

A compact 10-kW hardware demonstrator with a power density of $6.4\,\mathrm{kW/dm^3}$ ($107.5\,\mathrm{W/in^3}$) is presented and used to verify, for the first time, the key functionality of the proposed synergetic control method. Then, comprehensive efficiency measurements over the full output-voltage and power ranges confirm a flat efficiency characteristic (higher than 98% for most operating points with output voltages above 400 V and more than 25% of rated load), and a peak efficiency of 98.8% at $V_{out} = 520\,\mathrm{V}$ and $P_{out} = 5\,\mathrm{kW}$ (partial load). These measurements agree closely with the calculation results presented earlier. Again, for the first time, the efficiency improvement of 2/3-PWM over 3/3-PWM on the system level, i.e., including a DC/DC-stage, has been experimentally confirmed to be up to 1%. Finally, the conducted EMI precompliance tests reveal that, for a given operating point where both PWM schemes are applicable, 2/3-PWM results in lower noise emissions than 3/3-PWM. Using the loss-optimum operating modes, measurements taken over the full output-voltage range and rated power indicate compliance with CISPR 11 Class A.

All in all, current DC-link bB PFC rectifiers, such as the system presented herein, are promising realization options for future EV chargers that require a wide-output-voltage range, high efficiency, and compact size.

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Daifei Zhang (Member, IEEE) received the B.Sc. degree in electrical engineering and automation from the Huazhong University of Science and Technology, Wuhan, China, in 2017, and the M.Sc. and Ph.D. degrees in electrical engineering and information technology from Power Electronic Systems Laboratory, ETH Zurich, Zurich, Switzerland, in 2019 and 2023, respectively.

In 2017, he was with the Institute for Power Generation and Storage Systems, RWTH Aachen, Germany, as a one-year exchange student. Since July 2023, he has been with ETH Zurich as a Postdoctoral Researcher. His research interests include advanced bidirectional three-phase current/voltage DC-link PFC rectifier systems, high-power and/or nonisolated EV chargers, motor drives, and cryogenic power electronic systems.

Jonas Huber (Senior Member, IEEE) received the M.Sc. and Ph.D. degrees from the Swiss Federal Institute of Technology (ETH) Zürich, Zürich, Switzerland, in 2012 and 2016, respectively.

Since 2012, he has been with Power Electronic Systems Laboratory, ETH Zürich; and since 2016, as a Postdoctoral Researcher. Since 2017, he has gained industry experience as a Power Electronics R&D Engineer with ABB Switzerland, working on high-power DC–DC converter systems for traction applications, and as a Business Development Manager with a Swiss utility company. Then, in 2020, he returned to Power Electronic Systems Laboratory as a Senior Researcher. His research interests include solid-state transformers, motor drives, and all types of WBG-semiconductor-based ultracompact, ultraefficient or highly dynamic converter systems.

Johann W. Kolar (Fellow, IEEE) received the M.Sc. and Ph.D. degrees (*summa cum laude* - promotio sub auspiciis praesidentis rei publicae) from the University of Technology Vienna, Vienna, Austria, in 1997 and 1999, respectively.

Since 1984, he has been working as an independent Researcher and international Consultant in close collaboration with the Vienna University of Technology, in the fields of power electronics, industrial electronics, and high-performance drive systems. He was appointed as an Associate Professor and the Head of Power Electronic Systems Laboratory, Swiss Federal Institute of Technology (ETH) Zurich, in 2001, and was promoted to the rank of Full Professor in 2004. He has proposed numerous novel converter concepts, including the Vienna Rectifier, the Sparse Matrix Converter, and the Swiss Rectifier, has spearheaded the development of x-million r/min motors, and has pioneered fully automated multiobjective power electronics design procedures. He has supervised more than 80 Ph.D. students to completion, has authored or coauthored more than 1000 journal and conference papers and four book chapters, and has filed more than 200 patents in the course of international industry research collaborations. His current research interests include ultracompact/efficient WBG converter systems, ANN-based design procedures, solid-state transformers, ultra-high-speed drives, bearingless motors, and life cycle analysis of power electronics converter systems.

He has presented more than 40 educational seminars at leading international conferences and has served as IEEE PELS Distinguished Lecturer from 2012 to 2016. He was the recipient of more than 40 IEEE Transactions and Conference Prize Paper Awards, the 2014 IEEE Power Electronics Society R. David Middlebrook Achievement Award, the 2016 IEEE PEMC Council Award, the 2016 IEEE William E. Newell Power Electronics Award, the 2021 EPE Outstanding Achievement Award, and two ETH Zurich Golden Owl Awards for excellence in teaching. He was elected to the U.S. National Academy of Engineering as an international member in 2021.