# Letters

## A Novel Common-Ground Multisource Inverter

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***Abstract*—This letter proposes a novel switched-capacitor (SC) multisource boosting multilevel inverter featuring common ground connection for photovoltaic (PV)-dominated high-frequency ac applications. The proposed topology requires only eight switches, two diodes, and two SCs for generating a nine-level output voltage. The proposed topology has the ability to accommodate two PV sources while ensuring near zero ground leakage current. With the series/parallel technique, the SCs are self-voltage balanced, achieving sensor-less operation. The devised structure has the lowest conduction losses due to reduced number of conducting devices at each level. Furthermore, switching losses are reduced since fewer devices transit at any level as compared to the state-of-the-art topologies. A comprehensive comparative assessment of the proposed topology is carried out and included to highlight its beneficial features against the counterparts. The experimental evaluation of the proposed inverter topology is carried out and the results are presented to validate its feasibility and operability.**

***Index Terms*—Common-ground, high-frequency AC (HFAC), leakage current, multisource, multilevel inverter (MLI), switched-capacitor (SC).**

### I. Introduction

MULTILEVEL inverters (MLIs) are popular in variety of applications requiring high power quality. In addition to motor drives, solar plants, reactive power compensation, to name a few, their presence is witnessed in the emerging high-frequency AC (HFAC) application fields like aircraft, space, telecommunication, lighting, electric vehicle wireless charging, and microgrid. The advent of MLIs into several application field is due to the virtue of their structures resulting in higher power density, smaller component size, better heat distribution, and higher efficiency [1]. Recently, extensive research is carried out in the area of switched-capacitor (SC)-based MLIs due to their improved power density, reliability, and voltage boosting ability.

The direct application of SCMLIs in the field of photovoltaic (PV) dominated microgrid raises the issue of ground leakage current ($i_{\text{Leak}}$) due to the absence of galvanic isolation [2]. Therefore, the need for common-ground-type (CGT) inverters emerged, wherein, the solid connection between the grid neutral and the negative terminal of the PV ensures zero $i_{\text{Leak}}$. In literature, several single-source (SS) CGT inverter architectures are available with a common objective of synthesizing the structure to achieve higher levels with lesser components [3]. Some of the latest work in this regard suffer due to higher component count, higher device stresses and higher number of conducting devices [4], [5], [6], [7], [8].

Owing to the power processing ability from multiple sources, there is a significant increase in the application of multisource (MS) SCMLIs, particularly in the field of PV microgrids [9], [10]. The possibility to configure PV arrays in series/parallel combination resulting in the realization of the desired asymmetric source arrangement makes it viable for MS-SCMLI applications. A new dual input based SCMLI in [11] required 13 switches to generate 19 levels has a source voltage diversity factor (SVDF) of six. A higher SVDF indicates the need for high dispersed value of voltage sources. Further, the authors in [10] proposed a generalized topology based on MS-SCMLI. It requires 13 switches to generate 17 levels and has an SVDF of four. A further reduced SVDF-based topology requiring 11 switches for 13 levels was presented in [12]. Several efforts have been made to devise an MS-SCMLIs with reduced device stress, lesser current conducting devices, and complexity [9], [13]. In summary, despite the proposal of several MS-SCMLIs, to date, MS-SCMLI addressing the key issue of ground leakage current is unexplored.

This article proposes a CGT-based MS-SCMLI topology, hereafter referred to as common-ground multisource inverter (CGMSI). The proposed topology requires only eight switches, two diodes, and two SCs to generate nine level (9 L) output voltage. Selective harmonic elimination (SHE) technique is used for controlling the proposed inverter. The operating modes are described in detail and an extensive comparative assessment is carried out to benchmark the salient features of the proposed CGMSI against the competent topologies. Finally, the experimental results are included to validate the feasibility of the proposed inverter.

### II. Proposed CGMSI Topology

#### A. Circuit Structure and Description

Fig. 1 shows the proposed CGMSI topology. As evident, the solid connection among the negative terminals of the sources

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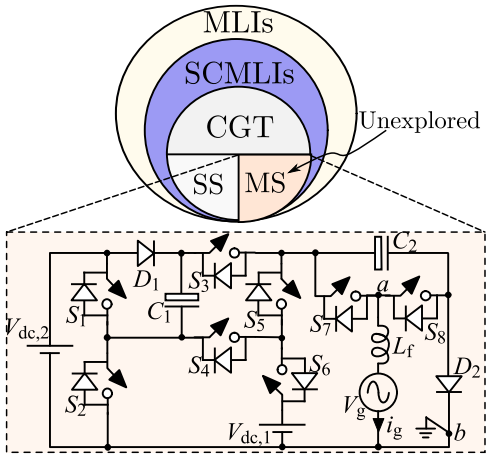


Fig. 1. Area of contribution and the proposed topology.

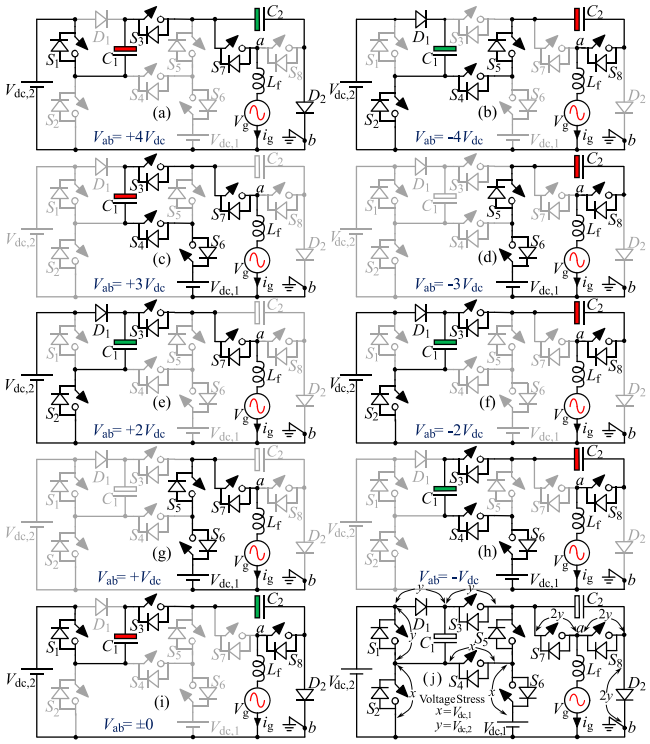


Fig. 2. (a)–(i) Modes of operation. (j) Voltage stress across the devices.

and the grid neutral ensures zero $i_{\text{Leak}}$ due to PVs parasitic capacitance. The proposed topology comprises eight switches ($S_1$–$S_8$), two diodes ($D_1$ & $D_2$), and two capacitors ($C_1$ & $C_2$) for synthesizing a 9 L waveform. For a symmetrical output voltage waveform, the source voltages must have a binary relation, i.e., $V_{dc,2} = 2V_{dc,1}$. Further, the capacitors $C_1$ and $C_2$ are charged to $V_{dc,2}$ and $2V_{dc,2}$, respectively, for ensuring an output voltage with uniform steps. The active devices during each of the switching states are highlighted in Fig. 2.

### B. Description of Operating Modes

Fig. 2(a)–(i) depicts the switching circuit structure for each of the voltage levels in detail. It is important to mention that

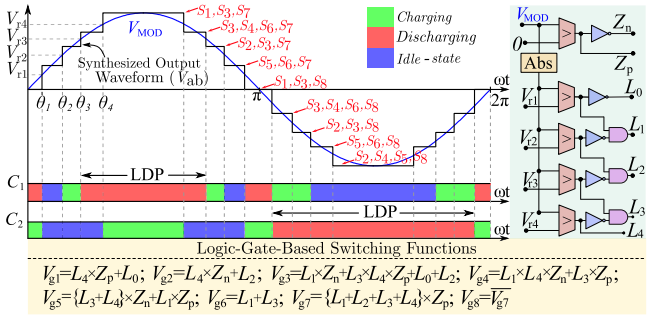


Fig. 3. Modulation strategy and the customized switching functions.

switches $S_7$–$S_8$ are triggered only once in each half cycle, which leads to lower switching power losses. Additionally, switches $S_1$, $S_3$, and $S_5$ experience minimal switching transitions. Besides, Fig. 2(j) highlights the maximum blocking voltages of the devices. Moreover, the impact of each of these switching states on the capacitor voltages is also highlighted.

### C. Modulation Scheme

For the generation of a 9 L waveform, four dc signals $V_{r1} - V_{r4}$ with different amplitudes are arranged and compared with a reference sinusoidal signal ($V_{\text{MOD}}$) as shown in Fig. 3. The magnitude of dc offsets are obtained using the relation $V_{rz} = \hat{V}_{\text{MOD}}\text{Sin}(\theta_z)$ for $z = 1, 2, 3, 4$ and $\theta_z$ are the switching angles based on SHE technique [14]. Furthermore, the dc signals are compared with the reference waveform through comparators, and the comparator outputs are processed using appropriate logic gates [Fig. 3] yielding the level information ($Z_p$, $Z_n$, and $L_0$–$L_4$). Utilizing the level to be generated information and the corresponding switching states, logic relationships are derived for each of the gating signals ($S_{g1}$–$S_{g8}$). Here, the symbol "×" represents the logical "AND" operation, and "+" represents the logical "OR" operation [Fig. 3].

### D. Common Mode Voltage and Leakage Current Behavior

As the potential target application for the proposed topology is an HFAC microgrid dominated by the PV sources, it is essential to analyze its performance pertaining to the total CMV ($V_{\text{TCM}j}$) and $i_{\text{Leak}j}$. Fig. 4(a) shows the simplified representation of the proposed topology for aiding the CMV analysis. The equivalent circuit depicting both the CMV and DMV of the proposed topology is shown in Fig. 4(b). From Fig. 4(b), the CMV ($V_{\text{CM}j}$), DMV ($V_{\text{DM}j}$), $V_{\text{TCM}j}$, and $i_{\text{Leak}j}$ are expressed as

$$V_{\text{CM}j} = \frac{v_{\text{an}j} + v_{\text{bn}j}}{2}; \quad V_{\text{DM}j} = v_{\text{an}j} - v_{\text{bn}j}; \quad [j = 1, 2] \tag{1}$$

$$V_{\text{TCM}j} = V_{\text{CM}j} - \frac{V_{\text{DM}j}}{2} = 0; \quad i_{\text{Leak}j} = C_{\text{PV}j}\frac{dV_{\text{TCM}j}}{dt} = 0. \tag{2}$$

From (1)–(2), unlike the traditional CGT inverters [2], the proposed CGMSI has the unique capability of eliminating the leakage current with the presence of multiple sources.

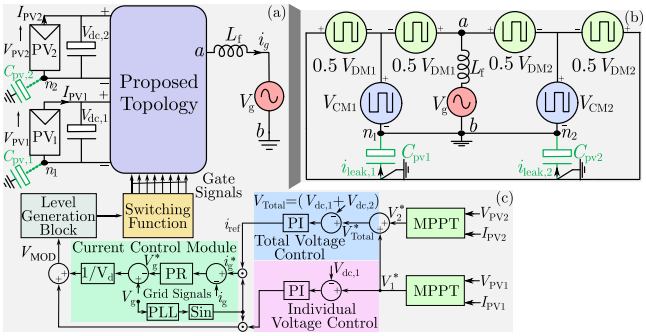


Fig. 4. (a) Proposed topology based setup for grid integration of PVs. (b) Equivalent circuit for aiding the common mode voltage (CMV) and differential mode voltage (DMV) analysis. (c) Control strategy.

TABLE I
COMPARISON OF THE PROPOSED CGMSI WITH 9L-SS-CGT-SCMLIS

| | $N_{SW}$ | $N_D$ | $N_{SC}$ | $N_{(SW+D)}/N_L$ | $N_{CS,max}$ | $TBV_{pu}$ |
|---|---|---|---|---|---|---|
| [4] | 9 | 4 | 4 | 1.44 | 4 | 5.25 |
| [5] | 9 | 1 | 3 | 1.11 | 6 | 6 |
| [6] | 11 | 2 | 3 | 1.44 | 6 | 8 |
| [7] | 9 | 3 | 3 | 1.33 | 5 | 7 |
| [8] | 14 | 1 | 4 | 1.67 | 7 | 6 |
| CGMSI | 8 | 2 | 2 | 1.1 | 4 | 4.75 |

### E. Determination of Capacitance

Maintaining of the capacitor voltages is of paramount concern as it dictates the voltage across the devices and the output voltage waveform quality. Hence, the calculation of the appropriate capacitance value is critical, which depends upon its peak current, ripple voltage, and fundamental frequency ($\omega_0$) [10]. The longest discharge period over the cycle for each of the capacitors, i.e., [$\theta_3$-($\pi - \theta_3$)] and [$\theta_1$-($\pi - \theta_1$)] for $C_1$ and $C_2$, respectively, (Fig. 3). The charge $Q_{C1}$ and $Q_{C2}$ released by $C_1$ and $C_2$, respectively, during the discharge period is given by

$$\Delta Q_{C1} = \frac{4V_{dc,1}}{\omega_0 R_L}(\pi - 2\theta_3); \quad \Delta Q_{C2} = \frac{4V_{dc,1}}{\omega_0 R_L}(\pi - 2\theta_1) \quad (3)$$

where $R_L$ is the load resistance. The capacitor ripple voltage $\Delta V_{C1}$ and $\Delta V_{C2}$ are given by

$$\Delta V_{C1} = 2kV_{dc,1}; \quad \Delta V_{C2} = 4kV_{dc,1} \quad (4)$$

where $k$ is the ripple factor [ranges from 0 to 1]. By selecting a suitable value of $k$, the capacitance of $C_1$ and $C_2$ are obtained using the relation

$$C_1 \geq \frac{2(\pi - 2\theta_3)}{\omega_0 k R_L}; \quad C_2 \geq \frac{(\pi - 2\theta_1)}{\omega_0 k R_L}. \quad (5)$$

## III. COMPARATIVE ASSESSMENT OF THE PROPOSED CGMSI TOPOLOGY

In this section, the comparative analysis is performed using the following figures of merit: the number of levels ($N_L$), number of gate-drives ($N_{GD}$), number of switches ($N_{SW}$), number of diodes ($N_D$), number of SCs ($N_{SC}$), maximum number of conducting switches ($N_{CS,max}$), total blocking voltage ($TBV_{pu}$), SVDF, and $i_{Leak}$.

TABLE II
COMPARISON OF THE PROPOSED CGMSI WITH MS-SCMLIS

| | $N_L$ | $N_{SW}$ | $N_{GD}$ | $N_D$ | $N_{SC}$ | $N_{CS,max}$ | $TBV_{pu}$ | SVDF | $i_{Leak}$ |
|---|---|---|---|---|---|---|---|---|---|
| [11] | 19 | 13 | 12 | 0 | 2 | 8 | 4.9 | 6 | High |
| [10] | 17 | 13 | 12 | 1 | 1 | 6 | 6.7 | 4 | High |
| [12] | 13 | 11 | 10 | 1 | 1 | 7 | 6.3 | 3 | High |
| [9] | 13 | 13 | 11 | 1 | 1 | 6 | 8.5 | 3 | High |
| [13] | 11 | 10 | 9 | 2 | 2 | 4 | 6.2 | 3 | High |
| [15] | 9 | 9 | 9 | 3 | 2 | 4 | 6 | 4 | High |
| [16] | 7 | 7 | 7 | 2 | 1 | 4 | 5.33 | 3 | High |
| CGMSI | 9 | 8 | 8 | 2 | 2 | 4 | 4.75 | 3 | Zero |

First, Table I summarizes the comparison with SS-CGT-SCMLI topologies with boosting ability. It is worth noting that, the proposed topology exhibits the highest device utilization ratio, as indicated by the factor $N_{SW+D}/N_L$ of value 1.1. This indicates that the proposed topology requires the least number of power semiconductor devices to generate a given number of voltage levels. Further, among the 9-L inverter category, the proposed topology exhibits the least $N_{CS,max}$ indicating a lower conduction loss. Furthermore, the least $TBV_{pu}$ of the proposed CGMSI reiterates its improved performance with the need for lower voltage rating devices, hence, it will reduce the overall cost.

Further, the comparative summary of the proposed CGMSI with dual source based SCMLIs is shown in Table II. The topologies in [9], [10], [11], [12], [13], generate an output voltage with higher number levels, while their other figures of merit are less promising. Topology in [15] generated 9 L at the price of a higher $TBV_{pu}$, and SVDF. The prominent feature and advantages of the proposed CGMSI topology highlighted in Table I prevails in Table II as well. In nutshell, the proposed CGMSI, therefore, combines several advantages such as reduced device count, reduced $TBV_{pu}$, reduced conducting devices, reduced SVDF, and the ability to curtail the ground leakage current with the presence of multiple sources while also maintaining similar functionality compare to other CGT inverters.

## IV. RESULTS AND DISCUSSION

The 9-L operation of the proposed CGMSI topology is validated through simulations and experimental tests. Microlab box DS1102 is used as the controller. The dc source voltages $V_{dc,1}$ and $V_{dc,2}$ are set to 75 and 150 V, respectively. Capacitor $C_1$ and $C_2$ is chosen 470 $\mu$F and 330 $\mu$F, respectively, for $k = 0.07$. The fundamental frequency is chosen as 400 Hz. The power MOSFET IRFP460 N driven by gate driver TLP250 and power diode MUR1560 are utilized. Fig. 5 shows the experimental results for standalone operation. Fig. 5(a) and (b) shows the key waveforms during steady-state for a pure resistive (45 $\Omega$) loading. The 9-L voltage and peak output voltage value confirms the self-balancing and boosting ability. Fig. 5(c) and (d) shows the switch voltage stresses. It is worth noting that out of eight, two switches operate at 400 Hz, four switches operate at 1200 Hz, and only two switches operate at 2 kHz resulting in reduced switching power losses. At any instant, a maximum of only 50% of the devices are conducting the load current, reducing the conduction losses. In addition, only fewer devices operating

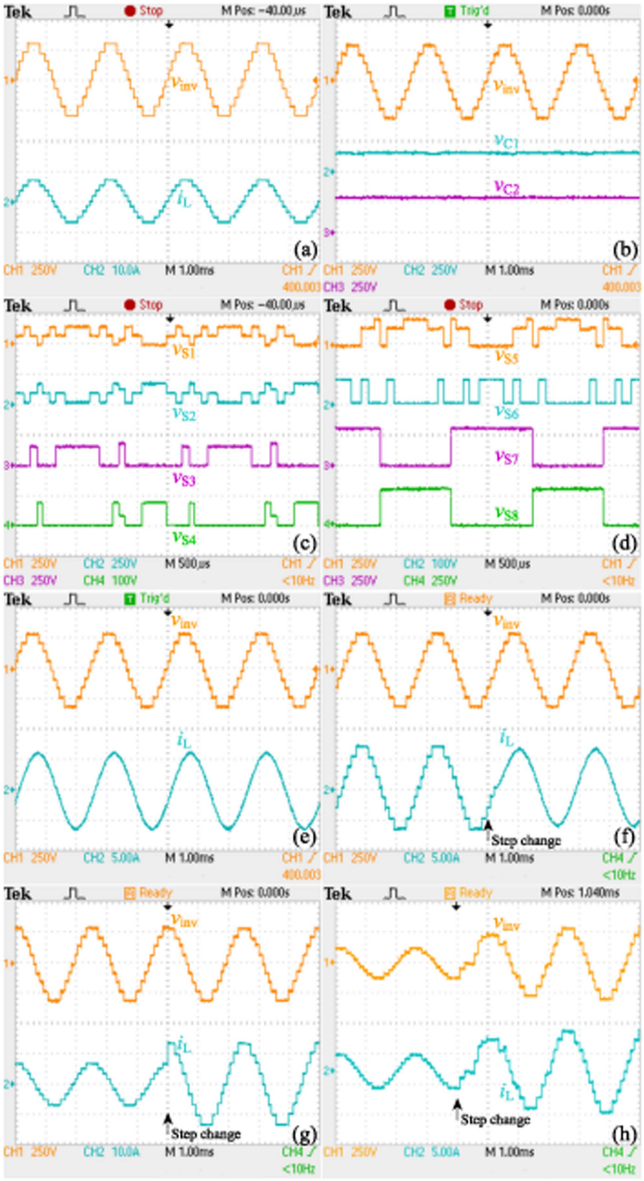


Fig. 5. Experimental results for standalone operation. (a) Inverter output voltage and load current. (b) Inverter output and SCs voltages. (c) and (d) Voltage across switches. (e) Inverter output voltage and load current. Inverter output voltage and load current for (f) PF change (g) step change in load (h) step change in input voltages.

at higher device frequency results in an improved efficiency. Fig. 5(e) shows the key waveforms for the resistive-inductive (35 Ω & 10 mH) loading with 0.8 PF. Fig. 5(f) shows the inverter transient behavior for a step change in load form resistive to resistive-inductive. Fig. 5(g) and (h) shows the inverter response for a step change resistive loading and the input voltage, respectively. From the above dynamic results pertaining to the inverter subjected to the various disturbances, it is evident that the proposed CGMSI performs satisfactorily.

Further, simulation-based performance evaluation of the proposed topology in grid-connected operation is carried out. For this, the grid voltage, frequency, and interfacing inductor ($L_f$) are set to 190 V, 400 Hz, and 5mH, respectively. A simple proportional-resonant controller based scheme is applied [17].

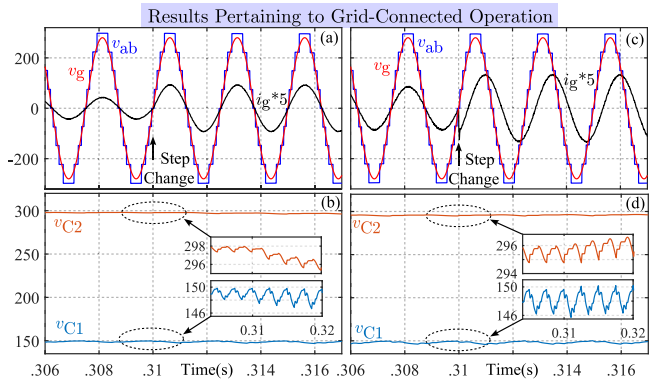


Fig. 6. Simulation results depicting step-change of grid-connected operation in (a) and (b) reference current and (c) and (d) PF.

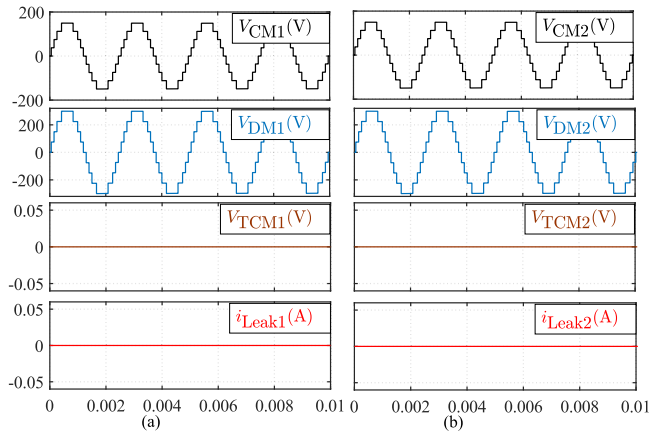


Fig. 7. Common mode behavior for (a) Source 1 and (b) Source 2.

Fig. 6(a) and (b) shows the inverter response for a step change in reference current ($i_g{}^*$) from 12 to 20 A. Further, the inverter is operated to inject reactive power into the grid and the corresponding results are shown in Fig. 6(c) and (d). Finally, the key waveforms pertaining to the common mode behavior of the proposed topology confirming its ability to adequately suppress the ground leakage current are shown in Fig. 7. From the foregoing results, it is observed that the inverter is able to inject a high quality grid current while maintaining the SC voltages at their respective values under steady-state and dynamic conditions. To evaluate the power losses, PLECS-based thermal analysis is carried out for a rated power of 1 kW. The simulated efficiency at rated power is found to be 94.95% with the conduction, switching, and capacitor ripple losses amounting to 12.67 W, 0.73 W, and 1.5 W, respectively.

## V. Conclusion

A novel CGT-based MS-SCMLI topology with reduced component count is presented with self-voltage balancing, boosting ability, and zero $i_{\text{Leak}}$ for a PV-dominated high-frequency ac application. The operating principle, SHE-based modulation scheme, and leakage current behavior were discussed. The functionality of the proposed topology has been thoroughly examined and validated through both simulation and experimental testing. Remarkably, a strong consistency is observed between the theoretical analysis, simulation outcomes,

and experimental results. The detailed comparative analysis attested the benefits of the proposed CGMSI topology in terms of reduced voltage stress across the devices, reduced number of conducting devices, and semiconductor requirements.

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