A 0.25-μm HV-CMOS Synchronous Inversion and Charge Extraction Interface Circuit With a Single Inductor for Piezoelectric Energy Harvesting

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***Abstract*—This article presents an on-chip synchronous inversion and change extraction (SICE) interface circuit, which combines the advantages of both the synchronous switch harvesting on inductor (SSHI) and synchronous electric charge extraction (SECE) interface circuits while utilizing a shared inductor. The SICE employs a bias-flip operation, similar to the SSHI, by inverting the piezoelectric voltage at each extremum multiple times to achieve higher power gain. Subsequently, SICE transfers all energy in piezoelectric harvester to the output capacitor, similar to the harvesting operation used in an SECE, thereby making the transferred energy independent of the loading impedance. A prototype ac–dc converter with the proposed SICE interface circuit was fabricated in a TSMC 0.25-μm process. Experimental results demonstrate an output power ($P_{\rm OUT}$) of 130 μW when the piezoelectric voltage ($V_{\rm PZ}$) is 10V. The SICE interface circuit has been theoretically and experimentally shown to harvest more than 624% compared to the conventional full-bridge rectifier, validating its superior performance.**

***Index Terms*—Piezoelectric energy harvesting, synchronous electric charge extraction (SECE), synchronous switch harvesting on inductor (SSHI).**

I. Introduction

PREVIOUS studies regarding piezoelectric harvesters fabricated with microelectromechanical system (MEMS) technology of around 1 cm^2 can generate tens to hundreds of microwatts [1]. MEMS devices and piezoelectric ceramics are two different piezoelectric harvesters with different characteristics and capabilities. MEMS devices are small and compact but less flexible than Piezoelectric Ceramics, which offer adjustable mass and resonance frequency. However, MEMS devices have lower power consumption due to their miniaturized nature. The selection also depends on requirements in a specific application, including the resonance frequency, parasitic capacitance, and output power.

In a simplified yet equivalent circuit model, the Piezoelectric Harvester current can be modeled as an ac sinusoidal current source ($I_{\rm PZ}$) that alternates its current polarity every half piezoelectric harvester vibration period connected in parallel with a capacitor ($C_{\rm PZ}$) [2]. An interface circuit is required to convert the ac sinusoidal current source into a stable dc voltage to extract energy from the piezoelectric harvester.

The most commonly used interface circuit in conjunction with the piezoelectric harvester is a full-bridge rectifier (FBR), which consists of four diodes. The FBR's output directly connects to the load or energy storage components [3]. However, due to $C_{\rm PZ}$, the voltage and current phases of the piezoelectric harvester are 90° apart, resulting in a low power gain of the FBR. Therefore, the output power ($P_{\rm OUT}$) depends heavily on the loading impedance (R_L). As a result, achieving impedance matching between R_L and the output impedance (R_O) of the piezoelectric harvester is essential for maximizing $P_{\rm OUT}$. Consequently, several interface circuits utilizing nonlinear switching techniques have been proposed [4], [5], [6], [7], [8], [9], [10], [11], [13], [14], [15], [16], [17], [21], [23], [24], [25], [26], [27], [28], aiming to achieve impedance matching.

In order to further increase $P_{\rm OUT}$, an inductor is added to transfer the energy by *LC* resonance. Fig. 1(a) depicts the circuit diagram of a synchronous switch harvesting on an inductor interface circuit (SSHI) [4]. When switch S_0 is turned ON, an *LC* resonant circuit is formed between $C_{\rm PZ}$ and the inductor L_0. This circuit conducts for half of an $L_0C_{\rm PZ}$ resonance period, causing the voltage across $C_{\rm PZ}$, referred to as $V_{\rm PZ}$, to invert its polarity. This operation, known as bias-flip, enhances the amplitude of $V_{\rm PZ}$ and increases $P_{\rm OUT}$. However, the maximum $P_{\rm OUT}$ in pure SSHI still depends on the impedance matching between the piezoelectric harvester and the interface circuit, similar to the FBR. Therefore, in order to maximize $P_{\rm OUT}$, it is typical to maintain the impedance matching condition through maximum power point tracking [5]. The simplest MPPT circuit employs a step-down buck dc–dc converter operating in discontinuous conduction mode to regulate the FBR output [6]. Combining SSHI with a buck dc–dc converter has been reported

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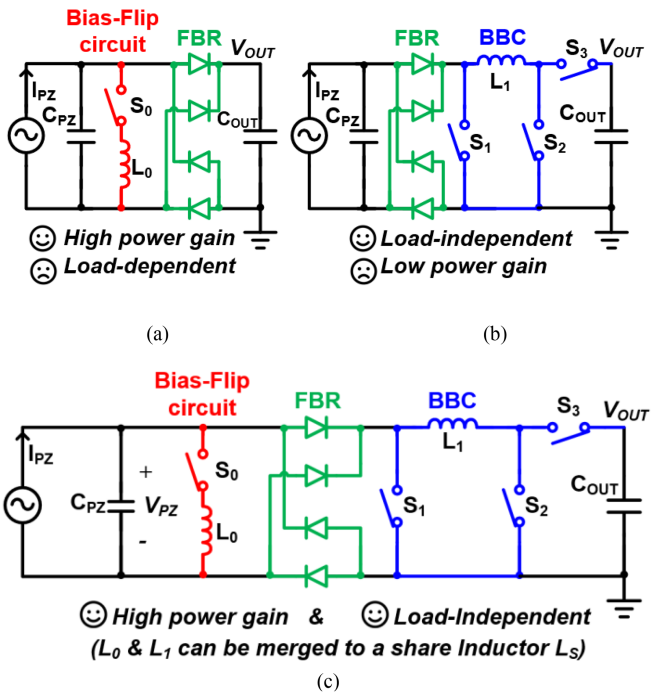

Fig. 1. Circuit diagram of (a) switch harvesting on inductor, (b) synchronous electric charge extraction, and (c) SICE interface circuits.

to improve P_{OUT} by 400% [7]. A variant of SSHI, described in [8], replaces the diodes in the rectifier with MOS transistors to further enhance power extraction by 681% compared to an FBR. Another proposed SSHI, documented in [28] and [30], integrates MPPT and achieves energy-extraction improvements of 417% and 738%, respectively. However, it usually requires complex and power-hungry circuits to sense the $\mathrm{P_{OUT}}$ accurately. Furthermore, the inherent delay in detecting V_{OC} variations reduces tracking efficiency and the overall circuit performance.

On the other hand, a synchronous electric charge extraction interface circuit (SECE) [9] combines a buck-boost dc–dc converter (BBC) with an FBR, as shown in Fig. 1(b). SECE eliminates the need for impedance matching [9], [10] by isolating the Piezoelectric Harvester from R_L using an inductor (L_1). Energy is initially stored in $\mathrm{L_1}$ and then transferred to the output capacitor (C_{OUT}). The SECE was reported to increase power gain by 197% [10] and 222% [23], with a maximum theoretical improvement of 400%. Though SECE has a load-independent characteristic, the power gain of SECE is generally lower than that of SSHI due to VPZ starting from zero voltage in each charge accumulation cycle.

Another proposed interface circuit, a synchronized switch harvesting on capacitor (SSHC), has been proposed in [27] and [29]. The SSHC needs capacitors with several tens of nF, similar to the C_{PZ} of the piezoelectric harvester, which occupy a significant area within the system. Some hybrid techniques have also been proposed, using a pre-charge and accumulation [26], synchronized switch harvesting on capacitor-inductor (SSHCI) [25], and a PCB-level implementation of synchronous inversion and change extraction interface circuit (SICE) [21]. SSHCI combines SSHI and SSHC, but it still requires an MPPT scheme to provide load independence for the circuit. SICE aims to integrate SSHI and SECE, creating a solution that combines the advantage of both techniques while eliminating their drawbacks.

Lallart et al. [21] analyzed the mechanical aspects of SICE, providing a comprehensive understanding of SICE. In contrast hand, our study specifically concentrates on the electrical aspects of SICE. We aim to provide insights into IC-Implementation SICE's performance and design considerations.

As depicted in Fig. 1(c), the proposed SICE combines SSHI and SECE. It consists of a bias-flip circuit, an FBR, and a BBC. Thus, SICE retains two main benefits: high power gain similar to SSHI and load-independent as SECE. This article represents an extended version of previous work,[1] which verified the concept of SICE through the simulation only. Furthermore, since L_0 and L_1 do not operate concurrently, we merged these two inductors into one shared inductor (L_S), further reducing the PCB area and cost of the SICE interface circuit. Besides, the switches used in FBR are merged with the switches (S_1-S_3) used in BBC to lower the conduction loss.

The rest of this article is organized as follows. Section II discusses the operating principle and system architecture. Circuit implementation is described in Section III. Section IV presents the simulation and measurement results. Finally, Section V concludes the article.

II. Proposed Synchronous Inversion and Charge Extraction (SICE) Interface Circuit

A. Concept of Operation

The proposed SICE utilizes the bias-flip operation, which is the same as the one performed in SSHI. Compared to SSHI, there will be n_{BF} consecutive bias-flip operations within one period in SICE. After completing n_{BF} bias-flip operations, a harvesting operation transfers energy to C_{OUT}, the same as in SECE.

Fig. 2 illustrates the SICE waveform for bias-flip number (n_{BF}) is 1. T_{PZ} represents one vibration period of the piezoelectric harvester. $\hat{V}_{\mathrm{PZ}}$ denotes the amplitude of V_{PZ}. I_{LS} represents the current of L_S. The bias-flip factor, denoted as γ, represents the ratio of the $\hat{V}_{\mathrm{PZ}}$ voltage after performing one bias-flip operation to the initial $\hat{V}_{\mathrm{PZ}}$ voltage. In this case, since n_{BF} is 1, a harvesting operation occurs with one bias-flip operation. The bias-flip operation inverts V_{PZ}, while the harvesting operation causes $\hat{V}_{\mathrm{PZ}}$ to approach 0 by transferring all energy in C_{PZ} to C_{OUT}. I_{LS} can be in either positive or negative value depending on the polarity of the V_{PZ} during the previous charge accumulation.

Fig. 3 depicts the circuit configurations for different phases in SICE are depicted in Fig. 3. Fig. 3(a) illustrates the circuit configuration of the open-circuit phase (Φ_{OC}). In Φ_{OC}, all switches are turned off, and the piezoelectric harvester accumulates electric charge in C_{PZ}. V_{PZ} reaches its peak value after half of T_{PZ} due to charge accumulation. Fig. 3(b) shows the circuit configuration

[1] K.-R. Cheng, H.-S. Chen, M. Lallart and W.-J. Wu, "A 0.25 μm HV-CMOS Synchronous Inversion and Charge Extraction (SICE) Interface Circuit for Piezoelectric Energy Harvesting," 2018 IEEE International Symposium on Circuits and Systems (ISCAS), Florence, Italy, 2018, pp. 1-4, doi: 10.1109/ISCAS.2018.8351700.

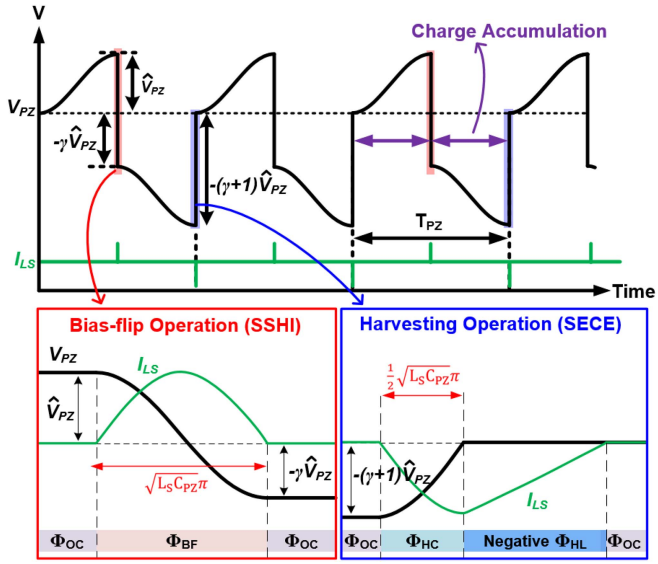

Fig. 2. Waveform of SICE for $n_{BF}=1$.

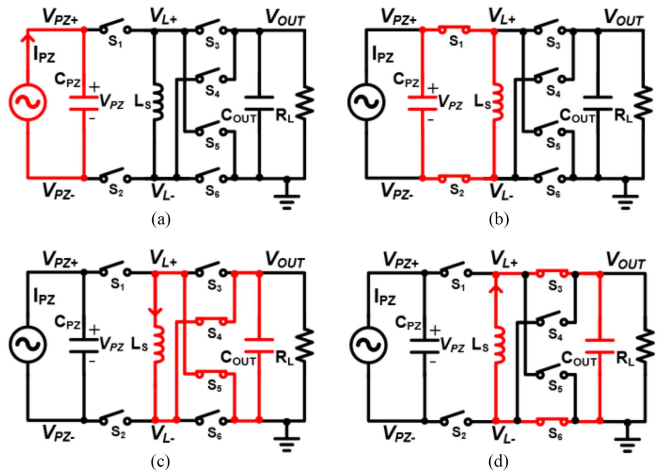

Fig. 3. Circuit configurations of (a) Φ_{OC}, (b) Φ_{BF} and Φ_{HC}, (c) positive Φ_{HL}, and (d) negative Φ_{HL}.

during the bias-flip phase (Φ_{BF}). In Φ_{BF}, S_1 and S_2 are turned ON for half of the $L_S C_{PZ}$ resonance period to invert the polarity of V_{PZ}. $\hat{V}_{PZ}$ flips from $\hat{V}_{PZ}$ to $-\gamma\hat{V}_{PZ}$ after Φ_{BF}, and SICE reenters Φ_{OC} again.

A harvesting operation, which harvests energy from C_{PZ} and L_S, consists of two consecutive phases, Φ_{HC} and Φ_{HL}. Φ_{HC} has the same circuit configuration but differs in duration compared to Φ_{BF}. In Φ_{HC}, S_1 and S_2 turn ON only for a quarter of an $L_S C_{PZ}$ resonance period to make V_{PZ} close to 0, fully transferring the energy from C_{PZ} to L_S. After Φ_{HC} concludes, SICE enters Φ_{HL}, which is responsible for transferring the energy stored in L_S to C_{OUT}. The polarity of V_{PZ} during Φ_{HC} corresponds to different I_{LS} directions in Φ_{HL}, thus requiring two different switch configurations for charging C_{OUT}, as depicted in Fig. 3(c) and (d). An SICE period completes upon finishing of Φ_{HL}.

The duration of the bias-flip operation may vary depending on ambient excitations, actual inductor, and C_{PZ} value. The termination of the Φ_{BF} and Φ_{HC}, which are generated by an internal pulse generator, can be manually calibrated in the measurement.

B. System Architecture

Fig. 4 shows the overall architecture of the SICE interface circuit, which consists of the following circuit blocks.

1) The power stage, which includes a piezoelectric harvester, L_S, C_{OUT}, R_L, two pairs of transmission gates M_{1n}/M_{1p}, M_{2n}/M_{2p}, and an active negative voltage converter (ANVC) [11].
2) A passive negative voltage converter (PNVC), connected in series with a peak detector.
3) A reverse current detector (RCD) with two high voltage isolation circuits.
4) A pulse generator and the control logic along with drivers and level shifters.

During Φ_{BF}, M_{1n}/M_{1p} and M_{2n}/M_{2p} are turned on for half of an $L_S C_{PZ}$ resonance period to flip V_{PZ}. In Φ_{HC}, M_{1n}/M_{1p} and M_{2n}/M_{2p} are turned ON for a quarter of an $L_S C_{PZ}$ resonance period to transfer energy from C_{PZ} to L_S. In Φ_{HL}, the ANVC transistors M_3-M_6 serve as an FBR, establishing a loop between L_S and C_{OUT} to complete the harvesting operation. Based on the direction of I_{LS}, either the transistors pair M_3/M_6 or M_4/M_5 is turned ON. The harvesting operation concludes when the current of M_3/M_6 or M_4/M_5 decreases to zero, transferring all charges to C_{OUT}.

The PNVC rectifies the voltage of V_{PZ} and provides the rectified piezoelectric voltage, V_{RECT}, to the peak detector, which consists of a passive high-pass filter and a dynamic comparator. The high-pass filter output V_{HPF} approaches zero as V_{RECT} reaches its peak value as there is a 90° phase difference between them. When V_{HPF} crosses the zero-voltage threshold, the dynamic comparator output (d_{pk}) signal goes high, indicating the initiation of either a bias-flip or a harvesting operation. Simultaneously, the Pulse Generator generates a pulse corresponding to the duration of Φ_{BF} and Φ_{HC}.

The RCD is essential to prevent reverse current flow from C_{OUT} to L_S during Φ_{HL} [10]. Most control circuits, including the peak detector, pulse generator, control logic, and RCD, comprise 5 V breakdown voltage transistors. The input of the RCD cannot directly connect to the power stage node of the inductor terminals, V_{L+} and V_{L-} since they may reach 12 V, exceeding the breakdown voltage in RCD during bias-flip or harvesting operations. Therefore, a high-voltage isolation between the power stage and RCD effectively isolates the 5 V breakdown voltage transistors from the high-voltage nodes.

Fig. 5 presents the state diagram of SICE operation. I_{PZ} is a sinusoidal current. Thus, it can be divided into positive and negative accumulations depending on the direction of I_{PZ}. In the positive accumulation, V_{PZ} increases due to charge accumulation in C_{PZ}. Conversely, in the negative accumulation, V_{PZ} decreases as the I_{PZ} direction reverses.

Initially, SICE operates in either a positive or negative accumulation Φ_{OC}. If SICE starts with Φ_{OC} in the positive

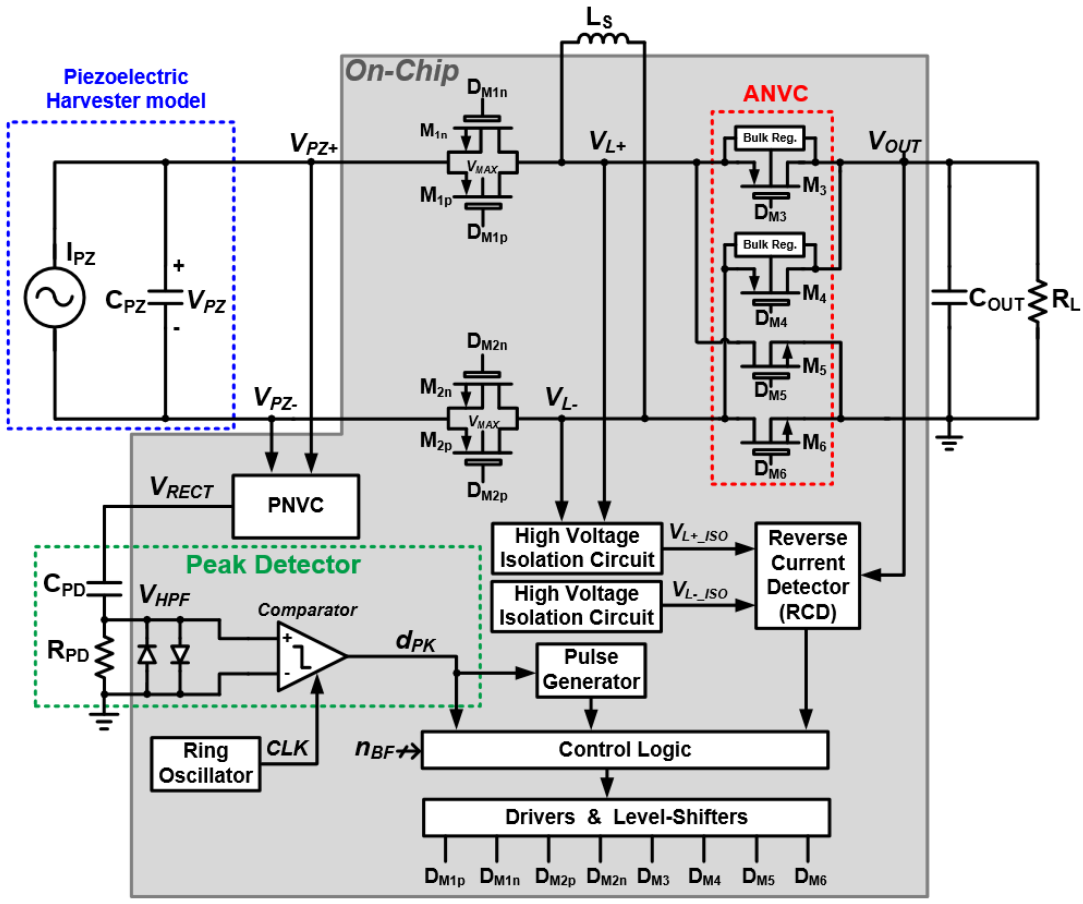

Fig. 4. Overall architecture of the SICE interface circuit.

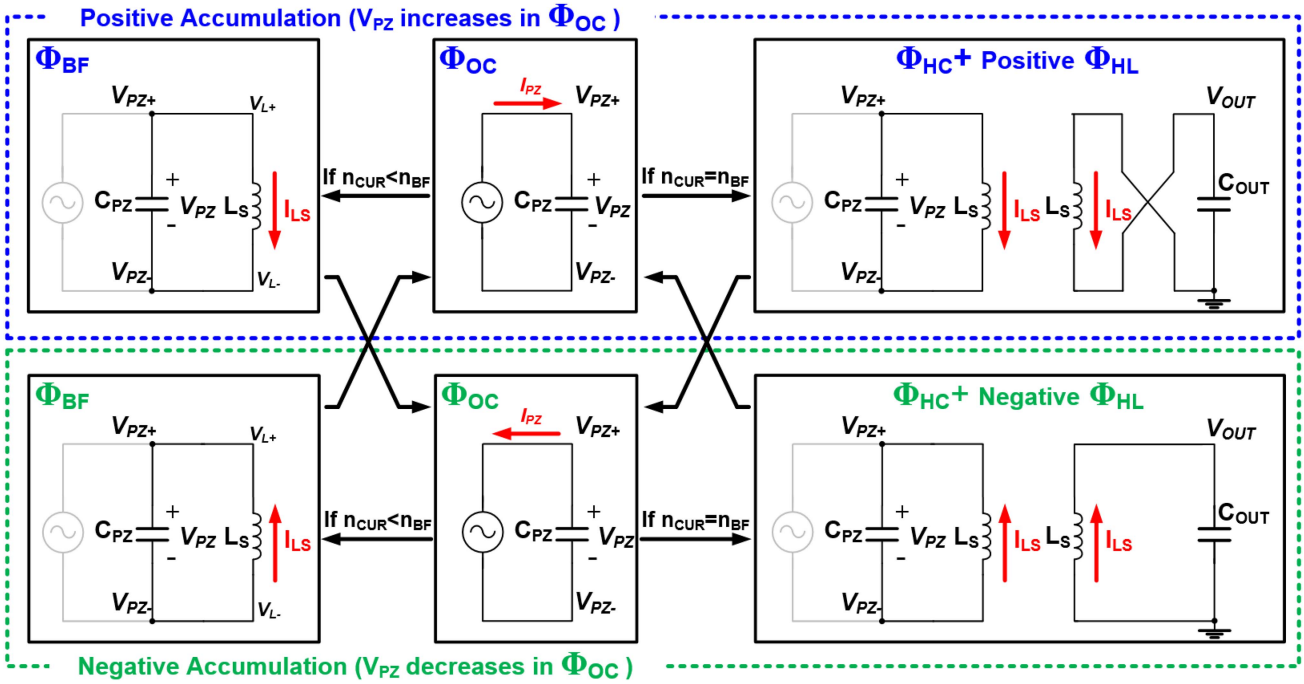

Fig. 5. State diagram of SICE.

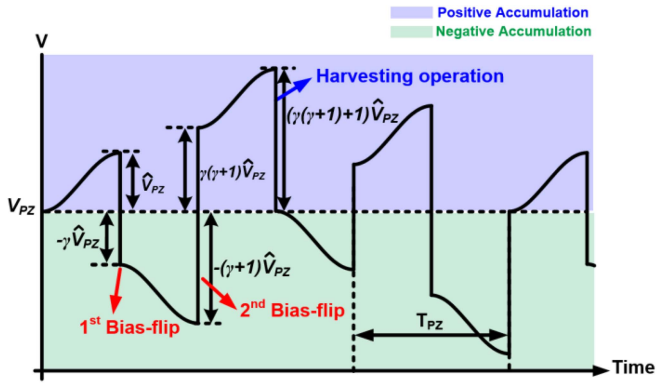

Fig. 6. Waveform of SICE for $n_{\mathrm{BF}}=2$.

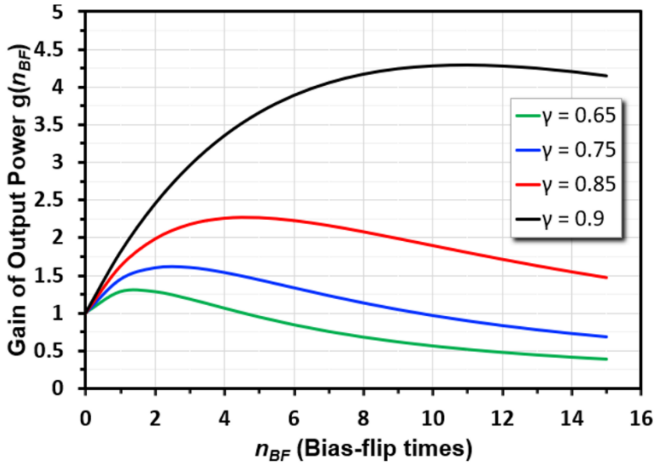

Fig. 7. Gain of $\mathrm{P_{OUT}}$ versus $\mathrm{n_{BF}}$ with different γ.

accumulation (the top-middle state in Fig. 5), the Piezoelectric Harvester accumulates charge during C_{PZ} in Φ_{OC}. As V_{PZ} reaches a positive extremum, the circuit enters Φ_{BF} if the current bias-flip number (n_{CUR}) is lower than the given bias-flip number (n_{BF}). After Φ_{BF}, SICE reenters Φ_{OC} in the negative accumulation (the bottom-middle state in Fig. 5). The Piezoelectric Harvester commences reverse charge accumulation in C_{PZ} until it reaches a negative extremum. The sequential alternation of the Φ_{OC} and Φ_{BF} process repeats until the n_{CUR} reaches the value of n_{BF}. When n_{CUR} equals n_{BF}, SICE enters Φ_{HC} and Φ_{HL} in succession, extracting energy from C_{PZ} to $\mathrm{C_{OUT}}$ through ANVC. Once Φ_{HL} completes, SICE returns to Φ_{OC}.

Fig. 6 illustrates the waveform of SICE for $n_{\mathrm{BF}}=2$. After V_{PZ} reaches its peak value in Φ_{OC}, the first bias-flip operation is performed, resulting in the inversion of V_{PZ} from $\hat{\mathrm{V}}_{\mathrm{PZ}}$ to $-\gamma\hat{\mathrm{V}}_{\mathrm{PZ}}$. Subsequently, all switches in the power stage are turned off, allowing the piezoelectric harvester to charge C_{PZ} in Φ_{OC} until V_{PZ} reaches its peak value, which is $-(\gamma+1)\hat{\mathrm{V}}_{\mathrm{PZ}}$. Since $n_{\mathrm{BF}}=2$, SICE executes a second bias-flip operation, inverting V_{PZ} from $-(\gamma+1)\hat{\mathrm{V}}_{\mathrm{PZ}}$ to $\gamma(\gamma+1)\hat{\mathrm{V}}_{\mathrm{PZ}}$. Once V_{PZ} reaches its peak value again, the value of V_{PZ} becomes $(\gamma^2+\gamma+1)\hat{\mathrm{V}}_{\mathrm{PZ}}$, and SICE initiates a harvesting operation since n_{CUR} equals n_{BF}. All energy stored in C_{PZ} is transferred to C_{OUT} through two bias-flip operations and one harvesting operation.

C. Analysis and Optimization for P_{OUT}

Assuming the parasitic resistances of the Piezoelectric Harvester and $\mathrm{L_S}$ are relatively small compared to R_L, all energy stored in C_{PZ} can be transferred to C_{OUT} through the bias-flip and harvesting operation. The energy (E_{CPZ}) stored in C_{PZ} for $n_{\mathrm{BF}}=0$ can be calculated as

$$E_{C_{\mathrm{PZ}}}=\frac{1}{2}C_{\mathrm{PZ}}\hat{V}_{\mathrm{PZ}}^2 \tag{1}$$

where $\hat{\mathrm{V}}_{\mathrm{PZ}}$ is the voltage charged by I_{PZ} within half of T_{PZ}. Therefore, P_{OUT} of SICE for $n_{\mathrm{BF}}=0$ (P_0) is equal to E_{CPZ} divided by half of T_{PZ}

$$p_o=\frac{\frac{1}{2}C_{\mathrm{PZ}}\hat{V}_{\mathrm{PZ}}^2}{T_{\mathrm{PZ}}/2}=\frac{C_{\mathrm{PZ}}\hat{V}_{\mathrm{PZ}}^2}{T_{\mathrm{PZ}}}. \tag{2}$$

Since the circuit will perform harvesting in every half-cycle and no bias-flip operation, the SICE in $n_{\mathrm{BF}}=0$ is equivalent to the SECE interface circuit. During the Φ_{BF}, V_{PZ} flips from $\hat{\mathrm{V}}_{\mathrm{PZ}}$ to $-\gamma\hat{\mathrm{V}}_{\mathrm{PZ}}$. γ can be expressed using the following equation [7]

$$\gamma=\gamma\left(R_{\mathrm{DCR}},L_S,C_{\mathrm{PZ}}\right)=e^{-\pi/2Q} \tag{3}$$

where f_r is the resonance frequency, R_{DCR} denotes the equivalent series resistance along the L_{S}, C_{PZ} path, and Q is the quality factor of the resonance circuit [12]. It takes T_{PZ} to finish one bias-flip operation and one harvesting operation. Therefore, P_{OUT} of SICE with $n_{\mathrm{BF}}=1$ (P_1) can be written as

$$\begin{aligned}p_1&=\frac{\frac{1}{2}C_{\mathrm{PZ}}\left(\hat{V}_{\mathrm{PZ}}+\gamma\hat{V}_{\mathrm{PZ}}\right)^2}{T_{\mathrm{PZ}}}\\&=\frac{\frac{1}{2}C_{\mathrm{PZ}}\left(\hat{V}_{\mathrm{PZ}}\left(\gamma+1\right)\right)^2}{T_{\mathrm{PZ}}}.\end{aligned} \tag{4}$$

Similarly, the relation between n_{BF} and P_{OUT} of SICE ($P_{n\mathrm{BF}}$) can be derived

$$p_{n_{\mathrm{BF}}}=\frac{C_{\mathrm{PZ}}\left(\hat{V}_{\mathrm{PZ}}\left(\gamma^{n_{\mathrm{BF}}}+\gamma^{n_{\mathrm{BF}}-1}\ldots+1\right)\right)^2}{\left(n_{\mathrm{BF}}+1\right)T_{\mathrm{PZ}}}. \tag{5}$$

Then, the gain of P_{OUT} can be obtained by dividing the $P_{n\mathrm{BF}}$ by P_0, where P_0 is the P_{OUT} for $n_{\mathrm{BF}}=0$. The gain of P_{OUT} after n_{BF} times bias-flip ($g(n_{\mathrm{BF}})$) is derived as

$$g\left(n_{\mathrm{BF}}\right)=\frac{1}{n_{\mathrm{BF}}+1}\left(\frac{1-\gamma^{n_{\mathrm{BF}}+1}}{1-\gamma}\right)^2. \tag{6}$$

The relationship between $g(n_{\mathrm{BF}})$ and n_{BF}, with different γ, are illustrated in Fig. 7. $g(n_{\mathrm{BF}})$ gradually decays with higher n_{BF} since it takes more time for one harvesting with higher n_{BF}. To determine the optimal n_{BF} for the highest P_{OUT}, the function $g(n_{\mathrm{BF}})$ is differentiated to solve for the n_{BF} that results in the highest P_{OUT}

$$\gamma^{n_{\mathrm{BF}}+1}\left[1-2\ln\left(\gamma\right)\left(n_{\mathrm{BF}}+1\right)\right]=1. \tag{7}$$

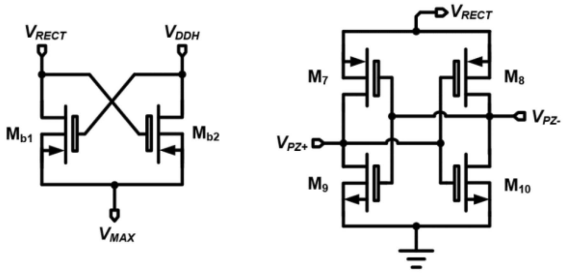

Fig. 8. Schematic of (a) the bulk regulator and (b) the PNVC.

The optimized n_{BF} can be derived from (7). Since the number of voltage bias-flip must be an integer, the actual number n_{BF} is the integer closest to the value of n_{BF} calculated by (7). In practice, the voltage rating of the switch in the power stage should be considered when multiple bias-flip operations are performed.

With $\gamma = 0.75$, the optimal n_{BF} is 3 by (7), and the P_{OUT} is 1.87 times that of SECE power. Since the P_{OUT} of SECE is four times the maximum power of the FBR [9], the P_{OUT} of SICE is 7.48 times the power of the FBR in theory. In order to attain a P_{OUT} close to the theoretical value in SICE, it is necessary to determine the optimal number of bias-flip operations (n_{BF}) and appropriate durations for both Φ_{BF} and Φ_{HC}.

III. Circuit Implementation

This section provides detailed explanations of the implementation of the subcircuits, including the power stage, negative voltage converter, peak detector, RCD, pulse generator, and high voltage isolation circuit.

A. Power Stage

All switches in the power stage are implemented using 12 V breakdown voltage MOSFETs. Additionally, MOS transistors [13] are utilized for ANVC instead of diodes to achieve more efficient rectification. Instead of NMOS only, transmission gates are adopted since the source-gate voltage (V_{SG}) of the PMOS is close to 0 when V_{PZ} approaches 0.

To prevent the body diode of PMOS in Power Stage from conducting, the proposed SICE employs the bulk regulation technique [11] to dynamically bias the body voltage of PMOS with the highest voltage (V_{MAX}), either V_{RECT} or the internal supply voltage VDD. Fig. 8(a) presents the schematic of the bulk regulator, where only one PMOS with a lower gate voltage is turned ON. As a result, the higher voltage between V_{RECT} and VDD is connected to V_{MAX}.

B. Passive Negative Voltage Converter (PNVC)

The PNVC is responsible for converting the negative voltage of V_{PZ} ($V_{\mathrm{PZ+}}$-$V_{\mathrm{PZ-}}$) into a nonnegative signal (V_{RECT}), which is equal to $\left| V_{\mathrm{PZ+}} - V_{\mathrm{PZ-}} \right|$. Fig. 8(b) illustrates the schematic of PNVC. When $V_{\mathrm{PZ+}}$ is higher than $V_{\mathrm{PZ-}}$, M_{10} turns ON, connecting $V_{\mathrm{PZ+}}$ and $V_{\mathrm{PZ-}}$ to V_{RECT} and ground, respectively. Consequently, V_{RECT} always maintains a nonnegative value equal to the absolute value of V_{PZ}.

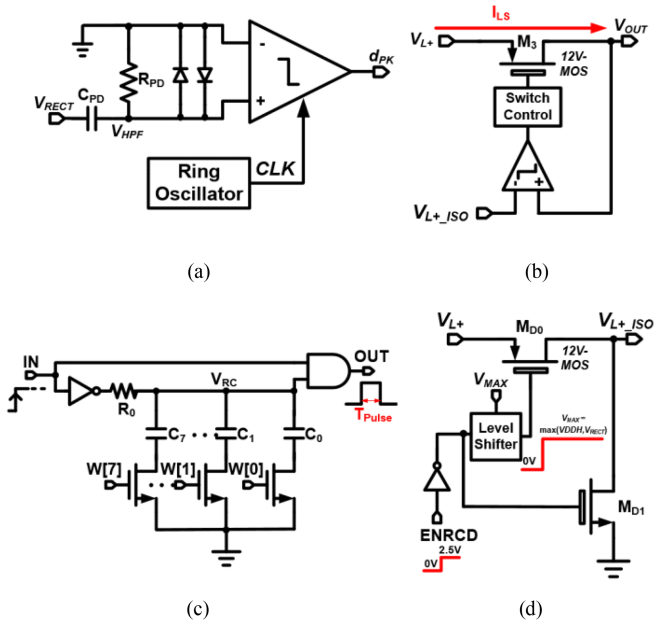

Fig. 9. Schematic of the (a) peak detector, (b) reverse current detector, (c) pulse generator, and (d) high voltage isolation circuit.

C. Peak Detector

As illustrated in Fig. 9(a), peak detector consists of a dynamic comparator [15] and a passive high-pass filter which is composed of C_{PD} (5 pF) and R_{PD} (20 MΩ), resulting in a cut-off frequency of 1.66 kHz. At the resonant frequency of 120 Hz for the piezoelectric harvester, the high pass filter (HPF) demonstrates a phase shift of approximately +90°. As V_{PZ} reaches its peak value, high-pass filter output (V_{HPF}) crosses the zero-voltage level, subsequently causing the d_{PK} signal to go high.

Additionally, the HPF provides a gain of 0.07 to prevent the high voltage of V_{HPF} from causing damage to the dynamic comparator. Diodes are employed to clamp V_{HPF} to ±0.7V, preventing the voltage from exceeding the breakdown voltage of the low-voltage transistor in the dynamic comparator.

Fig. 10 shows the schematic for the dynamic comparator of the peak detector. It consumes zero quiescent currents, making it suitable for low-power applications. The clock signal (CLK) is generated from the internal ring oscillator with an oscillating frequency of 80 KHz. The positive and negative input terminal is labeled V_P and V_N, respectively. V_X and V_Y are pulled low when CLK is low. Dynamic comparator starts working when CLK changes from low to high. If V_P is higher than V_N, V_X rises faster than V_Y to pull V_Y toward the ground. As a result, d_{pk} goes high. As CLK changes from high to low, d_{pk} returns to the low level until the next time CLK rises.

Accurately detecting the peaks in SICE plays a pivotal role as it directly impacts both the maximum V_{PZ} and P_{OUT}. The

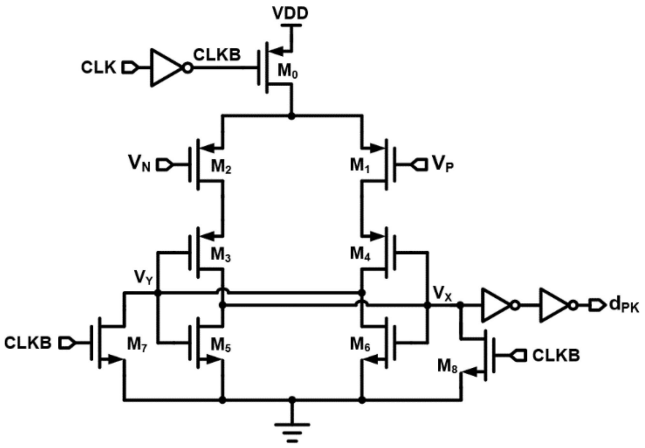

Fig. 10. Schematic of the dynamic comparator.

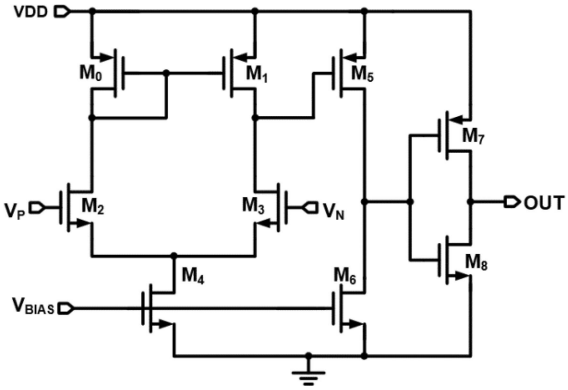

Fig. 11. Schematic of the comparator of the RCD.

accuracy of the peak detector is influenced by three primary error sources, which are discussed as follows.

1) *HPF Phase Shift Error:* In practical scenarios, the HPF can only approximate a phase shift close to, but not precisely equal to, 90° since the gain (A_{HP}) of HPF cannot be excessively small. Consequently, this inherent phase non-ideality and the associated time advancement introduce an error. With an input signal of 120 Hz and an HPF cut-off frequency of 1.66 kHz, the phase shift is 85.8°, corresponding to a time advancement error of 95.4 μs.

An intentional inclusion of comparator offset is incorporated to compensate for this delay in the simulation process to ensure precise peak detection. However, variations in the values of R_{PD} and C_{PD} can still affect the detected peak point.

2) *Comparator Offset:* The accuracy of peak detection is influenced by the presence of a comparator offset. Specifically, a dynamic comparator with a V_{OS} offset of 1 mV results in a shift of ($1/A_{\mathrm{HP}}$) mV in the detected peak point of $\mathrm{V_{PZ}}$. For example, when employing a 3 mV offset and a gain of 0.075, a displacement of 40 mV occurs. However, from an energy standpoint, even with this offset, the energy discrepancy remains below 1% when the peak voltage of V_{PZ} is 10 V. Therefore, a 3 mV offset is deemed acceptable for our peak detector in the simulation process.

3) *Comparator Clock Delay:* The dynamic comparator's output can only change during the rising edge of CLK, thus introducing an additional delay into the peak detector. In the worst-case scenario, the dynamic comparator has to wait for an entire period (12.5 μs) of CLK to output a high-level d_{PK}. However, this delay introduces an error of less than 0.1% of V_{PZ} peak detection in our design.

To alleviate the influence of these error terms, slight adjustments can be made to the R_{PD} and C_{PD}. This fine-tuning enables further improvement in the precision of the measurement process.

D. Reverse Current Detector

The RCD allows the transistor to function as a diode by comparing the drain and source voltage. Fig. 9(b) illustrates the implementation of RCD [16]. Taking transistor M_3 in the power stage as an example, when current flows from the L_S to C_{OUT}, V_{L+} becomes greater than V_{OUT} due to the ON-resistance of M_3. Conversely, the reverse current occurs as V_{OUT} is higher than V_{L+}. RCD turns OFF M_3 by comparing V_{OUT} and V_{L+} to prevent C_{OUT} from discharging back to the piezoelectric harvester. A two-stage OP-amp without compensation, as shown in Fig. 11, is employed as the comparator in RCD.

E. Pulse Generator

The schematic of the pulse generator is presented in Fig. 9(c). The pulse generator converts a level signal into a pulse signal, which determines controlling the duration of Φ_{BF} and Φ_{HC} [17]. When the input signal (IN) goes high, the output signal (OUT) goes high, and V_{RC} is discharged from high to low. After the discharging time of V_{RC} (T_{Pulse}), OUT goes low. T_{Pulse} is determined by an adjustable RC delay string constructed by R_0 and $C_0 \sim C_7$. The control signal W[7:0] can adjust the pulse duration to compensate for the variation in the L_S and the C_{PZ} value.

F. High Voltage Isolation Circuit

Fig. 9(d) illustrates the schematic of the high-voltage isolation circuit. V_{L+} and $V_{L+\mathrm{ISO}}$ are the voltage node in the power stage and control circuits, respectively. The high-voltage isolation circuit isolates the low-voltage components, which refers to devices operated at voltages lower than 5 V, in the control circuits from the high-voltage nodes in the power stage. High-voltage isolation circuit is situated between V_{L+}/V_{L-} and RCD. When M_3 or M_4 of the power stage turns ON, V_{L+} and V_{L-} are less than 5 V. M_{D0} in high voltage isolation circuit conducts, allowing the voltage signal to RCD. When RCD is not working, M_{D0} is turned OFF to prevent the high voltage node V_{L+}/V_{L-} from being connected directly to the RCD. Since V_{L+} varies with time, the level shifter [18], [19], [20] translates the power rail of ENRCD from the VDD domain to the V_{MAX} domain to fully turn OFF M_{D0}.

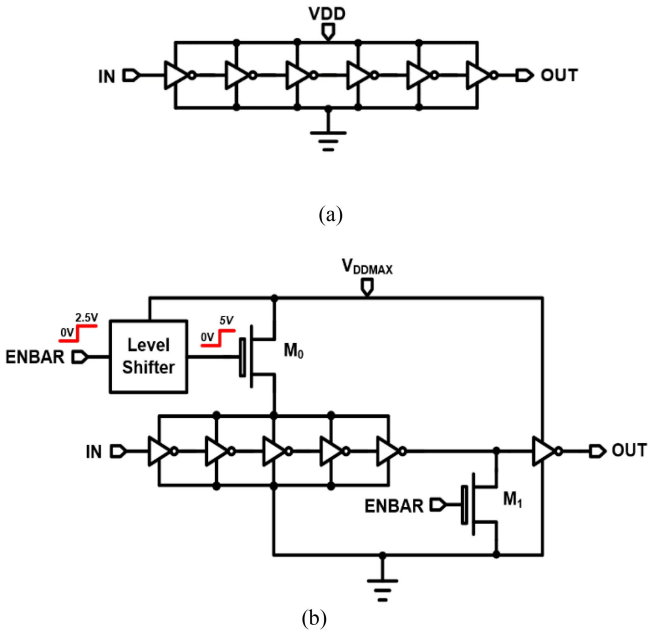

Fig. 12. Schematic of (a) NMOS driver and (b) PMOS driver.

G. Drivers and Level Shifters

Gate driving circuitries are utilized to facilitate faster switching of the large power switch devices. A cascade of CMOS inverters with multiple width-to-length ratios is utilized for the N-type power MOS driver, as shown in Fig. 12(a). However, this circuit cannot drive the high-voltage PMOS since its gate voltage must be the highest across the switch. Therefore, V_{DDMAX}, the bulk regulation output, powers the P-type power MOS driver circuit, as shown in Fig. 12(b).

During the start-up phase of the proposed SICE, the ENBAR input is set to a high-level, effectively isolating the first five inverter strings of the driver. Consequently, the last inverter outputs high, ensuring the PMOS is off. After start-up, the ENBAR goes to a low level, allowing the driver to operate normally.

IV. Simulation and Measurement Results

The ac–dc converter with SICE was fabricated in a 0.25-μm HV-CMOS process. Fig. 13 shows the chip micrograph, with a die area of 2.76 mm^2, including PADs, and 1.92 mm^2 without PADs. Table I gives an overview of the specifications of the custom MEMS piezoelectric harvester and the value of passive components used in the measurement. The measurement setup is also illustrated in Fig. 14. The Signal Generator produces a sinusoidal signal to the power amplifier, which drives the Shaker. The piezoelectric harvester, mounted on the shaker, vibrates at its resonant frequency of 120 Hz with a C_{PZ} of 15 nF. The ac electrical current generated by the Piezoelectric Harvester, measured at 0.4g, serves as the input power for the SICE and amounts to 58 μA.

Piezoelectric harvester's acceleration is monitored by an accelerometer to prevent damage due to over-excitation. Changes in motion or induced forces compress the piezoelectric material, generating an electrical charge that is proportional to the force (acceleration). This charge signal is then converted into a voltage signal using a charge amplifier and displayed on an oscilloscope. Power board, equipped with LDOs, supplies multiple power rails to the SICE Board.

Fig. 15 presents the measured waveform of the SICE interface circuit, including V_{PZ} ($V_{\mathrm{PZ+}}$-$V_{\mathrm{PZ-}}$), V_{OUT} with different n_{BF}

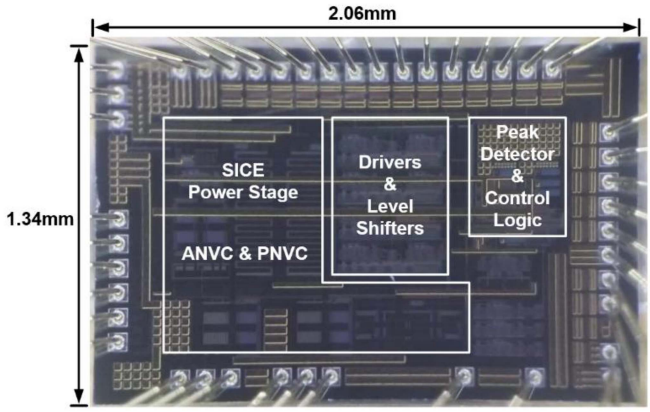

Fig. 13. Chip micrograph of the SICE interface circuit.

TABLE I
Specifications and Component Used in the Measurement

Max. V_{PZ}	12 V
V_{OUT}	<5 V
C_{PZ}	15 nF
C_{PD}	5 pF
C_{OUT}	1 µF
L_S	2.2 mH
R_{DCR}	22 Ω
R_{PD}	20 MΩ
R_L	82/100/150/220/330/390/470KΩ
f_r	120 Hz

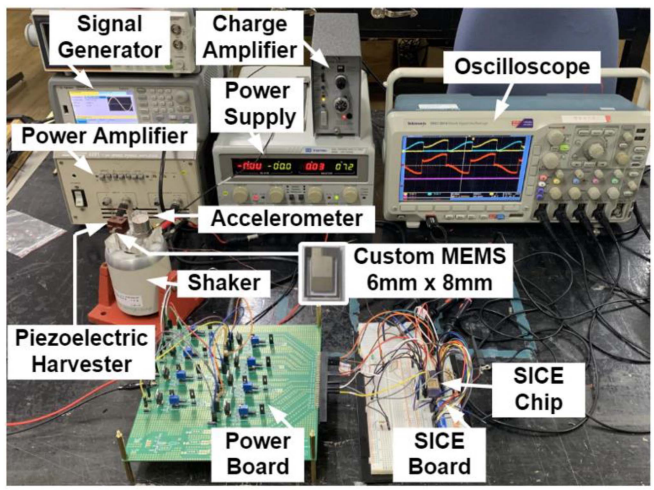

Fig. 14. Measurement setup for the SICE interface circuit.

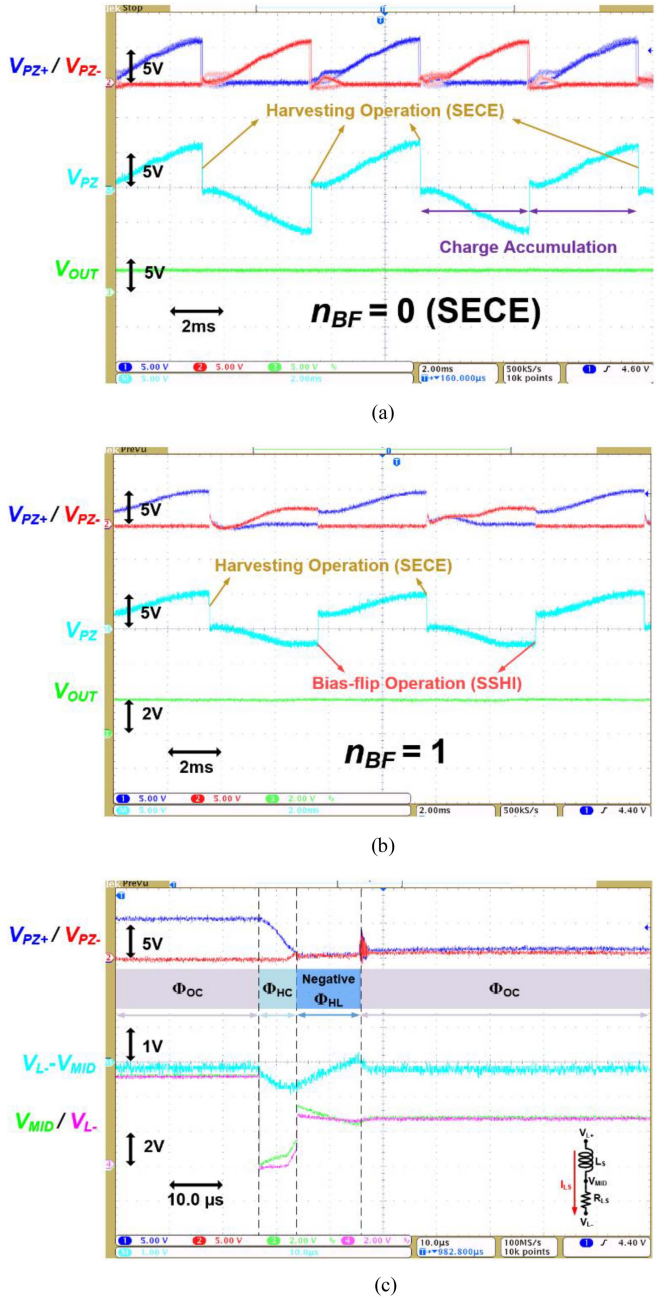

Fig. 15. Measured waveform of the SICE interface circuit for (a) $n_{\mathrm{BF}}=0$, (b) $n_{\mathrm{BF}}=1$, and (c) the voltage across L_S at harvesting operation.

values, and the voltage across L_S during the harvesting operation. Fig. 15(a) shows the waveform of SICE for $n_{\mathrm{BF}} = 0$, which is equivalent to the SECE interface circuit, where only the harvesting operation is performed. V_{PZ} returns to zero after the harvesting operation. Fig. 15(b) demonstrates the operation as $n_{\mathrm{BF}} = 1$, where V_{PZ} inverts the polarity during the bias-flip operation. Each bias-flip operation is accompanied by a harvesting operation. V_{PZ} returns to 0 after the harvesting operation. Fig. 15(c). shows the zoom-in waveform in the harvesting operation. An OFF-chip resistor R_{LS} is connected in series with L_S to observe the current ($\mathrm{I_{LS}}$) waveform of L_S. The node between L_S and the resistor is named V_{MID}. I_{LS} can be measured by evaluating V_L-V_{MID} divided by R_{LS}. After the completion of Φ_{HC}, I_{LS} reaches its peak value since all energy is stored in L_{S}. Upon the completion of Φ_{HL}, I_{LS} returns to zero as the energy has been transferred to C_{OUT}.

Fig. 16 illustrates the measured steady-state waveform for different n_{BF}. The switches in the power stage have a breakdown voltage of 12 V. $\hat{\mathrm{V}}_{\mathrm{PZ}}$ is limited to a maximum of 10V with $n_{\mathrm{BF}} = 0$, as shown in Fig. 16(a). To prevent damage on n power stage switches caused by excessive V_{PZ} voltage, $\hat{\mathrm{V}}_{\mathrm{PZ}}$ is set to 2.8 V for $n_{\mathrm{BF}} = 1,2,3$, also allowing a comparison of P_{OUT} under different n_{BF} values as shown in Fig. 16(b), (c), and (d), respectively.

The input power of 180 μW is obtained by multiplying the RMS values of V_{PZ} and I_{PZ}, as shown in Fig. 16(a). Meanwhile, V_{OUT} is 3.3 V with a 100 kΩ R_L. The calculated harvested P_{OUT} of SICE is 108.9 μW, achieved when $\hat{\mathrm{V}}_{\mathrm{PZ}}$ is 10V and n_{BF} is 0. This result corresponds to an efficiency of 60.5%.

To demonstrate the P_{OUT} across various n_{BF} values, a range of n_{BF} from 0 to 4 is selected. This choice is based on the observation in Fig. 7, where the gain for $\gamma = 0.75$ starts to drop after $n_{\mathrm{BF}} = 3$. Accordingly, the value of $\hat{\mathrm{V}}_{\mathrm{PZ}}$ is selected as 2.8 V to ensure the V_{PZ} is within the withstand voltage limits of the power switches. Fig. 16(b) shows the measurement result when $\hat{\mathrm{V}}_{\mathrm{PZ}} = 2.8$ V and $n_{\mathrm{BF}} = 1$, 2, and 3.

The measured P_{OUT} values for $n_{\mathrm{BF}} = 1$ to $n_{\mathrm{BF}} = 3$ are 14.2, 19, and 22.2 μW. In our design, $\hat{\mathrm{V}}_{\mathrm{PZ}} = 2.8$ V and $n_{\mathrm{BF}} = 3$, the input power after three bias-flip operations corresponds to a power of 32.4 μW. V_{OUT} is 3.22 V with 470 KΩ R_L, which is equal to a measured P_{OUT} of 22.2 μW. Therefore, the measured efficiency of our proposed circuit is calculated as 68.5% (22.2 μW divided by 32.4 μW) without the inclusion of the control circuit. When considering the control circuit, the efficiency is measured as 65.4%. Fig. 19 shows the total simulated power consumption of the sub-blocks amounting to 1 μW, which closely aligns with the measurement result.

To provide a more comprehensive comparison, Fig. 17 shows the theoretical, simulated, and measured P_{OUT} versus $\hat{\mathrm{V}}_{\mathrm{PZ}}$ under different n_{BF} values. P_{OUT} increases with higher $\hat{\mathrm{V}}_{\mathrm{PZ}}$, except when $n_{\mathrm{BF}} = 4$, where the dissipated energy significantly surpasses the harvested P_{OUT}. Fig. 17 also provides the zoom-in view of the measured P_{OUT} under different n_{BF} values in theory, simulation, and measurement when $\hat{\mathrm{V}}_{\mathrm{PZ}} = 2.8$ V. The measured P_{OUT} of 22.2 μW is achieved when $n_{\mathrm{BF}} = 3$, which is 1.57 times higher than theoretical SECE. This result aligns with the theoretical analysis in Fig. 7, where γ is approximately equal to 0.75. Additionally, P_{OUT} is boosted to 288% compared to the FBR for $n_{\mathrm{BF}} = 0$ and $\hat{\mathrm{V}}_{\mathrm{PZ}} = 10$ V. For $n_{\mathrm{BF}} = 3$ at $\hat{\mathrm{V}}_{\mathrm{PZ}} = 2.8$ V, P_{OUT} is boosted to 624%, respectively.

In SICE, varying V_{OUT} can be achieved by adjusting the value of R_L. To verify the loading-independent characteristic of SICE, Fig. 18 presents the relationship between P_{OUT} and V_{OUT} when $\hat{\mathrm{V}}_{\mathrm{PZ}}$ is 2.8 and 10 V. The obtained results indicate that the P_{OUT} of SICE remains relatively constant regardless of the changes in V_{OUT}, in contrast to other interface circuits. Noted that the SECE and SSHI values depicted in this figure are based on theoretical calculations.

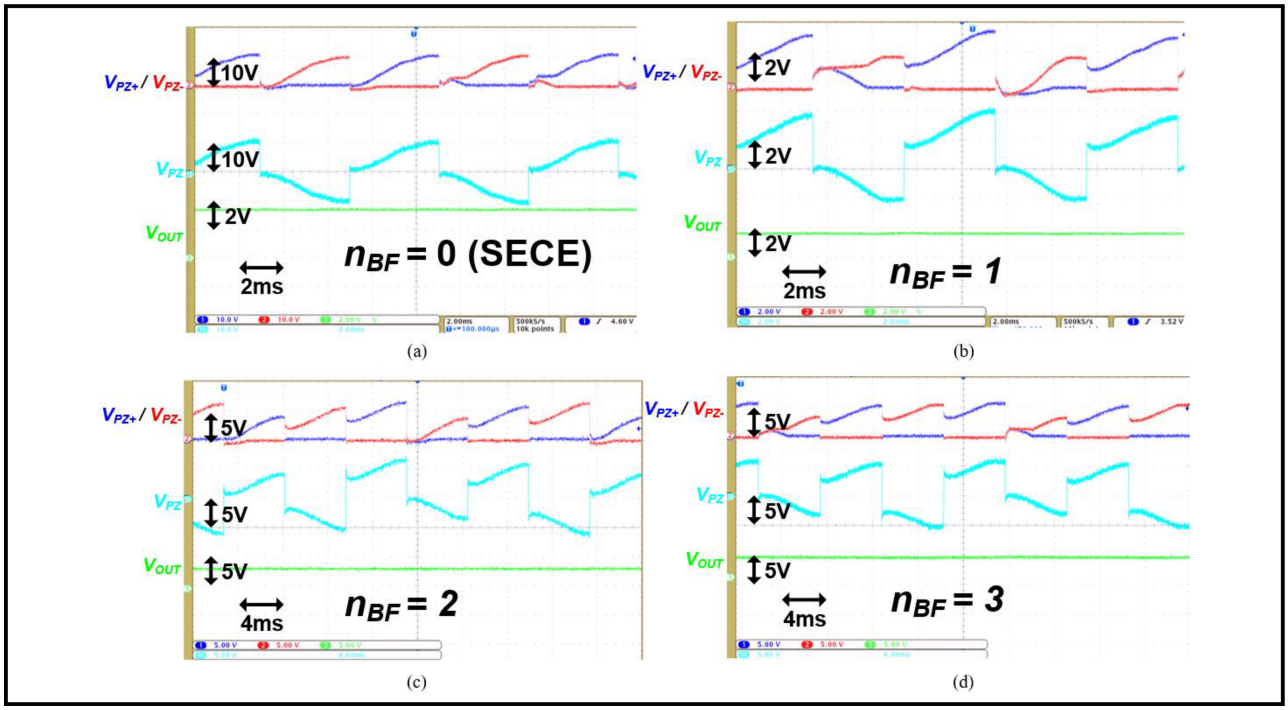

Fig. 16. Steady-state waveform (a) for $n_{\mathrm{BF}} = 0$, $\hat{\mathrm{V}}_{\mathrm{PZ}} = 10\mathrm{V}$ with $R_L = 100\,\mathrm{k\Omega}$, (b) for $n_{\mathrm{BF}} = 1$, $\hat{\mathrm{V}}_{\mathrm{PZ}} = 2.8$ V with $R_L = 180$ KΩ, (c) for $n_{\mathrm{BF}} = 2$, $\hat{\mathrm{V}}_{\mathrm{PZ}} = 2.8$ V with $R_L = 680$ KΩ, (d) for $n_{\mathrm{BF}} = 3$, $\hat{\mathrm{V}}_{\mathrm{PZ}} = 2.8$ V with $R_L = 470$ KΩ.

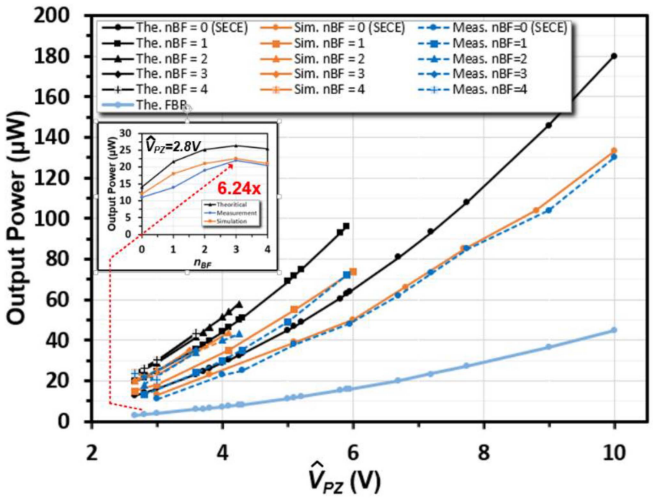

Fig. 17. Simulated and measured $\mathrm{P_{OUT}}$ versus $\hat{\mathrm{V}}_{\mathrm{PZ}}$ under different n_{BF}.

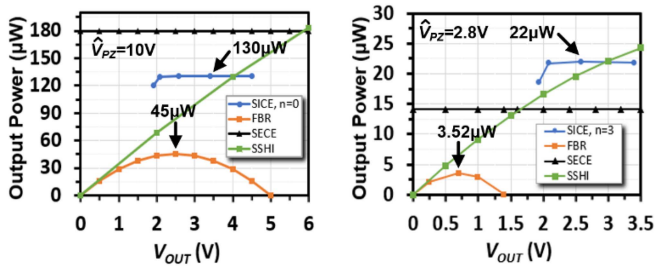

Fig. 18. Measured $\mathrm{P_{OUT}}$ versus $\mathrm{V_{OUT}}$ under different conditions: (a) $n_{\mathrm{BF}} = 0$ and $\hat{\mathrm{V}}_{\mathrm{PZ}} = 10$ V and (b) $n_{\mathrm{BF}} = 3$ and $\hat{\mathrm{V}}_{\mathrm{PZ}} = 2.8$ V.

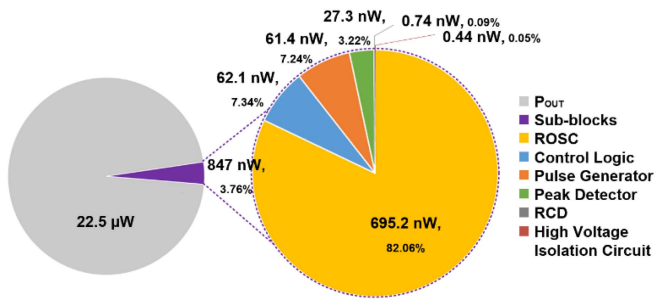

Fig. 19. Simulated power breakdown for $n_{\mathrm{BF}} = 3$ and $\hat{\mathrm{V}}_{\mathrm{PZ}} = 2.8$ V.

Fig. 19 provides the power breakdown of the simulated power consumption for the SICE circuit, using a peak piezoelectric voltage $\hat{\mathrm{V}}_{\mathrm{PZ}}$ of 2.8 V. The simulation yields a P_{OUT} of 22.5 μW, with a total power consumption of the subblocks amounting to 847 nW, which closely aligns with the measurement result. The contributions of each subblocks are also presented. In the pie chart, the ring oscillator is the most significant contributor, accounting for 82.06% of all subblocks' power consumption of the overall power loss because it is continuously turned on compared to other circuit blocks.

Table II compares the performance of our proposed SICE with other IC-based piezoelectric energy harvesting interface circuits within the past four years. When $n_{\mathrm{BF}} = 0$, equivalent to

TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH PRIOR ART

	Javvaji et al. [23] JSSC 2019	Chamanian et al. [24] TPEL 2019	Ciftci et al. [25] TCAS-I 2021	Sankar et al. [26] JSSC 2022	Angelov and Nielsen-Lonn [27] JSSC 2020	Li et al. [28] VLSI 2019	This article	
							n_{BF}=0	n_{BF}=3
Process (CMOS)	0.13-µm	0.18-µm HV	0.18-µm	0.18-µm	0.18-µm	0.13-µm	0.25-µm	
Scheme Type	SSHI	SECE	SSHCI	Pre-charge and Accumulation	SSHC	SSHI	SICE	
Piezoelectric Capacitance	14 nF / 22 nF	4 nF	2 nF	19 nF	6 nF	20 nF / 100 nF	15 nF	
Open-circuit Voltage (V_{OC})	1.5 V	4.75 V	1.02 V	1 V	1.27 V	1.6 V / 2.66 V	10V / 2.8V	
Operation Frequency (*fr*)	441 Hz / 432 Hz	390 Hz	415 Hz	146 Hz	22 Hz	100 Hz - 180 Hz	120 Hz	
Piezoelectric Harvester	MIDE PPA 1022 / MIDE PPA 1021	Custom MEMS a=N/A	Custom MEMS a=1 g	MIDE PPA 1021 a=N/A	Custom MEMS a=N/A	MIDE PPA 1021 / MIDE PPA 1011	Custom MEMS [22] a=0.4g	Custom MEMS [22] a=0.1g
Output Power (P_{OUT})	62.22 µW / 78.75 µW	78 µW	4.7 µW	10.2 µW	1.51 µW	32.3 µW/ 292.2 µW	130 µW ($\hat{V}_{PZ}$=10V)	22 µW ($\hat{V}_{PZ}$=2.8V)
Quiescent Current (IQ)	N/A	N/A	N/A	N/A	N/A	0.9 µA	278.1nA	278.1nA
Power gain*	448% / 428%	222%	544%	368%	701%	417%	288% ($\hat{V}_{PZ}$=10V)	624% ($\hat{V}_{PZ}$=2.8V)

* Power Gain: $= \frac{P_{OUT}}{P_{FBR}} = \frac{P_{OUT}}{C_{PZ}\left(\hat{V}_{PZ}/2\right)^2 f_r}$ . .

SECE, the proposed SICE interface circuit outperforms the work presented in [22] regarding power gain. In the case of the $n_{BF} = 3$, SICE can boost the P_{OUT} to 624% compared to the FBR at $\hat{V}_{PZ} = 2.8$ V. The power gain of our proposed SICE outperforms other hybrid techniques and ranks as the second highest among the state-of-the-art given in Table II. While SSHC described in [27] demonstrates an impressive power gain (701%) at an output voltage of 3 V, it is important to note that the P_{OUT} of SSHC is still dependent on R_L. This comparison demonstrates that SICE significantly increases the P_{OUT} for low $\hat{V}_{PZ}$ by performing multiple bias-flip operations on small vibrations.

V. CONCLUSION

In conclusion, combining SSHI and SECE, the SICE interface circuit offers significant advantages for piezoelectric energy harvesting. It maximizes P_{OUT} without relying on the loading impedance (R_L) and provides up to six times more energy harvesting compared to conventional interface circuits in low-coupling systems. The measurement results demonstrate a 624% increase in P_{OUT} compared to the FBR for $\hat{V}_{PZ} = 2.8$ V. Furthermore, using a single inductor ensures no increase in PCB area and cost, as the operation time of both schemes is nonoverlapping. The integration of ICs leads to lower power consumption due to reduced parasitic capacitance and resistance of the sub-blocks compared to PCB-level SICE. Additionally, with MEMS, it is easier to integrate with other circuits, such as dc/dc converters, enabling the development of a compact, integrated Piezoelectric Energy Harvesting system.

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