# Soft-Switching Bidirectional Step-Up/Down Partial Power Converter With Reduced Components Stress

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***Abstract*—This article introduces a step-up/down series partial power converter (S-PPC) based on isolated current-source dc–dc converter topology. The proposed S-PPC exploits the most important feature of the used current-source topology, such as the capability to operate with both voltage polarities in the series port to decrease its rated power. Other advantages include soft switching in the entire operating range and low current stress of semiconductor components even at very low series voltage. In addition, the proposed S-PPC provides protection and soft-start capabilities due to the integration of a solid-state circuit breaker. The article explains the operation principle of the proposed S-PPC and compares it to the closest known competing S-PPC based on the dual active bridge topology. An experimental prototype rated for 3.5 kW with maximum processed power of 600 W was built to confirm the converter operation principle and its features. Its experimental efficiency reaches 99.3%. The proposed S-PPC also shows a good regulation capability at challenging operating points, like nearly zero series voltage.**

***Index Terms*—Components stress factor, converter topology, dc–dc converter, partial power converter.**

## I. Introduction

RECENT efforts of the power electronics community were targeting emerging applications associated with higher demand for direct current power distribution [1], [2], [3], [4], [5]. The current technology of full power converters is mature, and the performance of full power converters is limited by the technological barriers of semiconductor and magnetic components [6], [7]. To make a new step forward in the low-gain dc–dc converter, the partial power processing concept was adopted to limit the power processed by converter components and, consequently, reduce converter losses and volume. These converters are feasible and practical in applications where the input and output voltages are relatively close; the closer, the better the converter performance.

The partial power processing idea was conceptualized in the 1960s [8], but the new technology of series partial power converters (S-PPCs) saw its first application only thirty years later [9], [10]. These converters comprise a dc–dc conversion cell with one of its ports connected in series between the input and output ports of an S-PPC. Most of the literature on these converters was published in the last decade [11]. S-PPC dominates the literature among different partial power processing architectures [12]. Even though S-PPCs were used in different applications, relevant research favored their use in photovoltaic (PV) applications [13], [14]. However, S-PPCs that step-up PV string voltage to a dc link showed the best performance in photovoltaic applications [15].

Therefore, it is important to distinguish S-PPCs into three classes: step-up, -down, and -up/down [16]. The first two classes are straightforward and could be implemented with more advanced full-bridge topologies [15] as well as a simple flyback topology [17] that, however, has a limited scalability of power level. On the other side, step-up/down S-PPC converters require the series port to operate in two quadrants (positive and negative port voltage) with a unidirectional current. The two-switch forward converter is the simplest dc–dc converter topology used in such converters [18]. A step-up/down S-PPC is introduced in [19] based on a current source full-bridge converter with two-quadrant switches at the low-voltage port. The hard switch operation of the switches and voltage drop of the series switches are the main sources of the total converter loss, which cannot be neglected.

Moreover, the impact of leakage inductance on the voltage spikes is not investigated. The step-up/down S-PPC in [20] is also formed by two quadrant switch that suffers from hard switching problem and extremely high processed power in the low battery voltages that cancels the advantage of the PPC concept. Further development of this concept to bidirectional operation requires the utilization of more advanced dc–dc converter topologies capable of handling any combination of series port voltage polarities and current directions between S-PPC ports. The initial concept of bidirectional step-up/down S-PPC based on the four quadrant switches was presented in [21]. However, it did not discuss modulation strategy and operation principle in detail. It could be assumed that it was operating with hard switching, i.e., high switching losses.

Currently, there are a few examples of the voltage-source dual active bridge (DAB) converter used together with a voltage unfolder to achieve these properties [22]. However, their operation in critical points when S-PPC has to operate with low series voltage and full load current has not been demonstrated in

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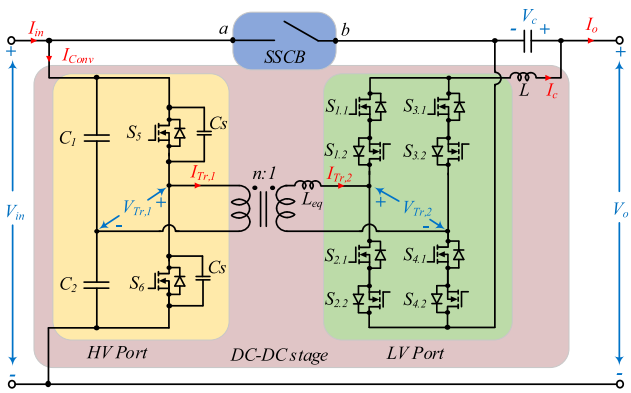


Fig. 1. Proposed bidirectional step-up/down (BDSUD) series partial power converter (S-PPC).

literature due to excessive current stress, which will be quantified in this article.

To overcome the limited voltage regulation and soft-switching properties of the existing solutions, this article proposes to use an advanced isolated current-source full-bridge dc–dc converter topology in the step-up/down S-PPCs. This topology shows superior voltage regulation capabilities and soft switching attainable in the entire converter operation range. The first version of this work was published in [23], where the main concept and some of the functions were demonstrated using simulations. This article presents the next step in developing the proposed S-PPC topology by implementing soft-start, demonstrating the feasibility of operation around zero partiality, developing design guidelines for wide-range soft-switching and confirming it, and comparing the given concept to the closest counterpart from the recent literature. Section II describes the operation principle of the proposed S-PPC and shows the limitations of its nearest competitor from [22]. Section III explains the design guidelines of the novel concept, which is followed by the experimental performance benchmarking, which is discussed in Section IV. Finally, Section V concludes this article.

## II. Proposed S-PPC

This section proposes a novel bidirectional step-up/down (BDSUD) S-PPC based on an isolated current source full-bridge (CSFB) dc–dc converter. The configuration of the S-PPC is input-parallel-output-series (IPOS), which generally leads to less processed power regarding both step-up and step-down modes. In S-PPCs, a wide voltage regulation range capability is required at a low voltage (LV) port. The voltage across this port of the dc–dc stage ranges from zero (in the case of equal input/output voltage) to the maximum voltage regulation range for the desired application. Amongst various current source (CS) topologies, the current-source full-bridge features negligible energy circulation, which is highly favorable for both high/low voltage and power levels and improves the performance of the S-PPC. Fig. 1 introduces the proposed converter, including its main parts.

The first one is the high voltage (HV) port, which is connected in parallel to the input side. Thus, all elements in this port ($C_1$, $C_2$, $S_5$, $S_6$, and the snubber capacitors $C_s$) will be selected in accordance with the input voltage rating with the full voltage stress. Employing a half-bridge voltage doubler (HB/VDR) structure in the HV port is preferable due to less active components in comparison with a full-bridge structure [19]. In the S-PPC configuration, the parallel connected HV port features reduced current flow, which reduces the component current rating requirements.

A full-bridge matrix stage forms the LV port with an inductor at its output. The prominent feature of such a configuration is its capability to provide bipolar series voltage ($Vc$) as well as bidirectional current ($Ic$). This feature is eminent specifically in battery energy storage applications or dc microgrid power flow controllers, where bidirectional operation is required. The switching devices in this port experience rated current and partial voltage stresses.

### A. Modulation Strategy and Operation Modes

Isolated current source converters typically include an auxiliary circuit like a snubber or clamp circuit to suppress the voltage spike across the semiconductors in the CS port generated by the leakage inductance of the transformer. Applying such strategies to eliminate voltage spikes will increase the converter hardware and control complexity as well as its cost. Instead, the clamping of voltage can be attained by an active rectifier at the voltage source (VS) port to redistribute the current in the CS port switches, effectively creating a secondary modulated converter (SMC).

Since the proposed S-PPC assumes energy exchange in both directions, the presence of active semiconductors in both ports is well justified. Both the phase shift modulation (PSM) and the symmetric pulsewidth modulation (PWM) can be implemented for regulation. The disadvantage of PWM-SMC is that it requires RC snubbers for the LV port switches to suppress the voltage spikes. Moreover, its voltage regulation range is limited. The PSM reduces energy circulation between two ports of the dc–dc stage but requires reverse blocking switches at the LV port [24]. The PSM is highly preferred to maintain high efficiency in all operating points, including zero-series port voltage. Again, the use of bidirectional switches is justified in the proposed S-PPC due to the bipolar voltage blocking capability requirement. Fig. 2 depicts the modulation and generalized current/voltage waveforms for the boost and buck modes of the CSFB converter utilized in the proposed S-PPC [24]. It must be stated that the terms buck/boost will be used for the dc–dc stage and the step-up/down for the whole S-PPC. The soft switching of this converter is guaranteed by introducing an additional short resonance period during the shoot-through state to ensure fast recharging of snubber capacitors $C_S$ at the HV port and minimizing the energy circulating between the dc–dc cell ports. It occurs during the time interval ($t_4-t_5$) in the boost mode and ($t_1-t_2$) in the buck mode. Soft switching at the HV and LV ports is load-independent within the required operating range and does not need any further control, which will be investigated in detail in the following section.

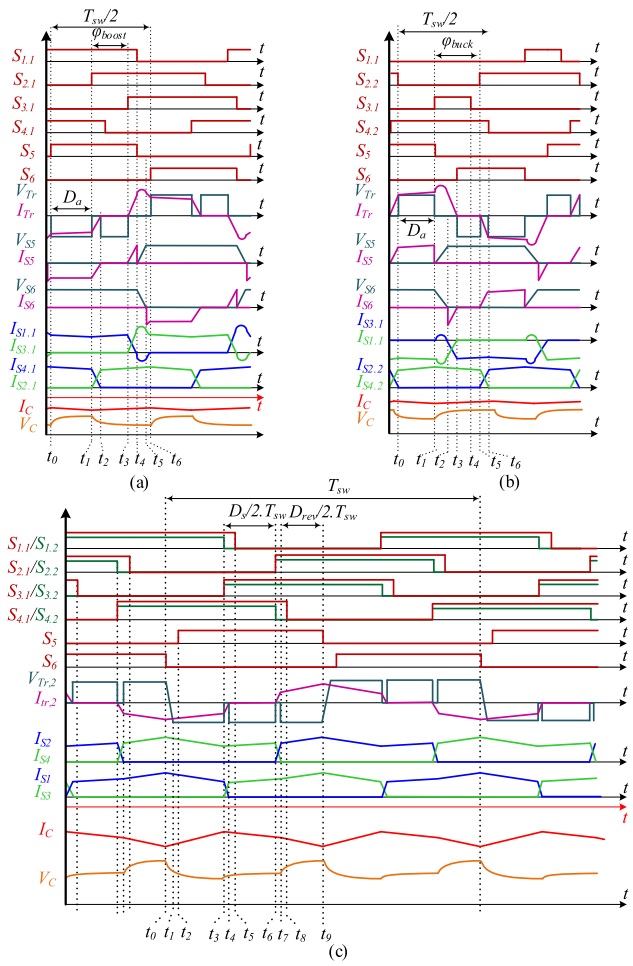


Fig. 2. Operation waveforms of the dc–dc stage in (a) boost mode (power transfer from LV to HV port) and (b) buck mode (power transfer from HV to LV port) (c) reverse power flow modulation.

The four-quadrant operation [see Fig. 3(c)] of the proposed S-PPC could be elaborated as follows.

Quadrant-I ($V_c > 0$ & $I_c > 0$): In this quadrant, the dc–dc stage operates as a buck converter, transferring power from the HV to the LV port, which is in the same direction as the power flow of the system. This mode is depicted in Fig. 3(a). The $S_{1.2}$ and $S_{3.2}$ are turned ON, and $S_{2.1}$ and $S_{4.1}$ are turned OFF or performing synchronous rectification. $S_{1.1}$ and $S_{3.1}$ work with a constant phase shift related to $S_5$ and $S_6$ to allow the resonance period for zero voltage switching (ZVS) of HV port switches and current redistribution for zero current switching (ZCS) of LV port top switches. The Quadrant-III ($V_c < 0$ and $I_c < 0$) is analogous to Quadrant-I if the switching patterns of the top and bottom side switches in the LV port are swapped accordingly.

Quadrant-IV ($V_c > 0$ & $I_c < 0$): In this quadrant, the dc–dc stage works as a boost converter, transferring power from its LV to the HV port in the same direction as the S-PPC power flow. It is demonstrated in Fig. 3(b). Both $S_{1.2}$ and $S_{3.2}$ are turned ON and $S_{2.2}$ and $S_{4.2}$ are turned OFF or performing synchronous rectification. A constant phase shift between the HV port switches and the top switches of the LV port allows the completion of the resonance period, which satisfies the ZVS switching of the HV port switches. Quadrant II ($V_c < 0$ & $I_c > 0$) is identical to Quadrant-IV if the switching patterns of the top and bottom side switches at the LV port are swapped to generate the negative voltage polarity. In all quadrants, the phase shift between the top and bottom switches of the LV port ($\varphi_{\text{buck}}$ and $\varphi_{\text{boost}}$) regulates the LV port voltage and current ($V_c$ and $I_c$).

During the buck mode of the dc–dc stage, the voltage gain is regulated by changing the shoot-through state duration between the top and bottom switches of the LV port. According to [24] the voltage gain can be determined by the following equation:

$$G_{\text{buck}} = \frac{\pi - \left(\varphi^{\text{buck}} + \omega \cdot t_{\text{red}}\right)}{2 \cdot \pi \cdot n} \tag{1}$$

in which $G_{\text{buck}}$ is the voltage gain of the buck mode, $\varphi^{\text{buck}}$ is the phase shift between the top and bottom switches of the LV port, $\omega = 2\pi f_{sw}$, $t_{\text{red}}$ $(t_2 - t_3)$ is the current redistribution time between LV port switches (for example, $S_{2.2}$ and $S_{4.2}$) that will be elaborated in the next sections, and $n$ is the transformer turns ratio. Increasing the phase shift in a way that $\varphi^{\text{buck}} + \omega.t_{\text{red}} = \pi$ will minimize the active state duration and will push the $V_c$ to zero. Therefore, the S-PPC operation near zero series capacitor voltage can be guaranteed.

On the other hand, the PSM modulation Fig. 2(a) is unable to control the boost operation of the dc–dc stage when $|V_c| \leq 10V$. To overcome this issue, a new modulation based on reverse power flow control is presented to smoothly control the S-PPC in the boost mode of the dc–dc stage near zero series capacitor voltage. The modulation strategy is depicted in Fig. 2(c). As can be seen, the reverse power transfer from the HV port to the LV port during the time interval of $(t_8 - t_9)$ charges the LV port inductor and extends the boot factor of the dc–dc stage. The voltage gain in this mode can be written as

$$G_{\text{boost}} = \frac{2 \cdot n}{1 - D_s - 2 \cdot D_{rev}} \tag{2}$$

where $D_s$ is the switching interval of the shoot-through state and $D_{rev}$ corresponds to the duration of reverse power flow mode. It can be seen from (2) that the voltage gain is more sensitive to $D_{rev}$ than $D_s$ for this modulation strategy. A detailed explanation of modulation and operation modes can be found in [25] and [26]. In practice, both $D_s$ and $D_{rev}$ could be used to adjust the voltage in the series port near zero. The utilization of the reverse power flow mode is associated with higher conduction losses [25]. Therefore, it is used only in a narrow input voltage range near zero partiality ($\pm 10$ V in comparison to the full voltage regulation range of $\pm 50$ V). Hence, the effect of reverse power flow on the weighted system efficiency is negligible.

### *B. Comparison of the BDSUD and DAB-Based S-PPC by the Number of Components*

The closest alternative of the proposed converter in the class of BDSUD S-PPCs is the S-PPC based on DAB dc–dc converter and an unfolding circuit in the series port [22]. It is demonstrated in Fig. 4.

Table I compares these two approaches in terms of components count. As mentioned earlier, the number of switches

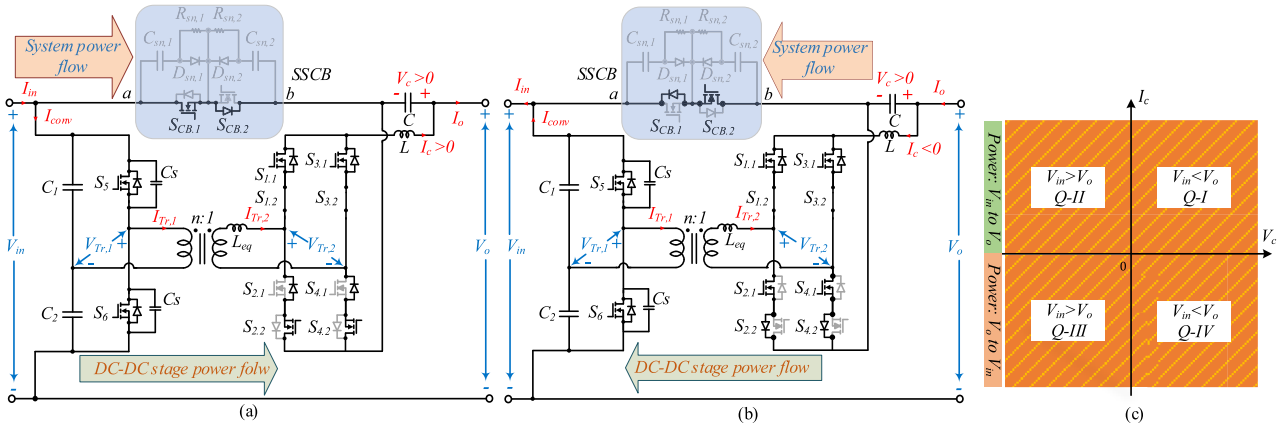


Fig. 3. Operation modes of the proposed S-PPC (a) step-up/forward current (Q-I) and (b) step-up/backward current (Q-IV) (c) operation quadrants.

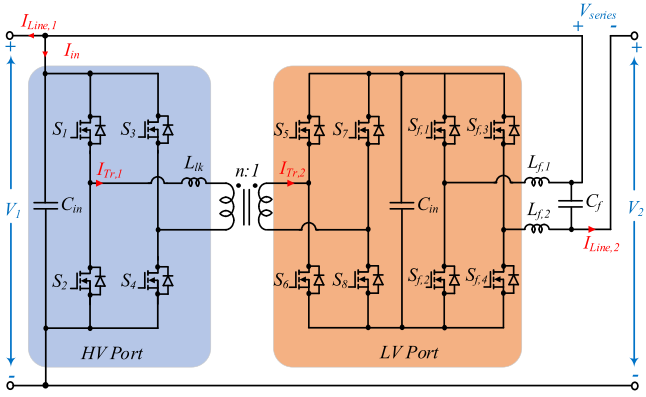


Fig. 4. DAB-based step-up/down bidirectional S-PPC proposed in [22].

TABLE I
COMPARISON OF THE PROPOSED AND DAB-BASED S-PPC FROM [22]

| Component | Proposed BDSUD | DAB based S-PPC [22] |
|---|---|---|
| LV port switches | 8 | 8 |
| HV port switches | 2 | 4 |
| Inductors | 1 | 2 |
| Transformers | 1 | 1 |
| Transformer turns ratio | $n_{min} > \frac{V_{in,min}}{2D_{a,max}.V_{C,max}.}$ | $n_{min} > \frac{V_{in,min}}{V_{C,max}.}$ |
| Capacitors | 5 | 3 |
| Gate driver channels | 10 | 12 |
| Gate Power supplies | 6 | 8 |
| Current sensors | 1 | 1 |
| Voltage sensors | 3 | 3 |

is lower in the proposed converter due to the application of a half-bridge circuit. Moreover, the transformer turns ratio is reduced at least by a factor of 2, considering the same voltage conversion ratio.

The transformer with lower turns ratio is preferable because of the design simplicity and easily achievable low leakage inductance, which is important for the CSFB converters.

Regarding the energy storage elements, the number of inductors in [22] is double that in the proposed BDSUD. On the other hand, the number of capacitors is higher in the proposed converter. However, two of them are small nF-scale ceramic snubber capacitors, much smaller than mF-scale capacitors used in the DAB-based S-PPC.

Another point to consider is that each of the bidirectional switches in the LV port is driven by a single auxiliary dc–dc power supply and one dual-channel gate driver. Accordingly, the driving circuitry is simpler and cheaper as competing solutions require more components. In contrast with [22], the dc-link capacitor at the LV port is eliminated, resulting in higher power density. An additional advantage of eliminating the dc-link capacitor is that in case of any short circuit fault in the LV port, having a dc-link capacitor will lead to a large inrush current through LV port devices, which might require extremely fast protection devices and strategies [27].

### C. Soft-Switching Region of BDSUD and DAB-Based S-PPCs

As mentioned earlier, the proposed converter operates with soft switching within its defined voltage and power range. On the other hand, the DAB converter, which is widely exploited in the literature for step-up/down S-PPCs [22], [27] suffers from excessive power circulation between its high and low voltage ports. This limits the ZVS range of the converter, especially when the voltage across the LV port decreases to almost zero. To overcome this drawback, different modulation strategies could be used in the DAB-based S-PPCs.

The single PSM (SPSM) has the highest circulated power. Hence, dual-PSM (DPSM) could be used to reduce the power circulation and widen the ZVS range of the converter. Although DPSM reduces the high-power circulation in the converter power range compared to the SPSM, it cannot eliminate the power circulation, especially at small phase shifts where the converter works in light load conditions. The soft-switching range of the DAB converter is illustrated in Fig. 5. The voltage gain is normalized by the transformer voltage conversion ratio $n$ for DAB and $2{\cdot}n$ for the isolated CSFB converter, considering the utilization of the half-bridge circuit in the HV port. The red line depicts the ZVS boundary of the DAB converter. Below the line, it loses the soft-switching operation in the LV port.

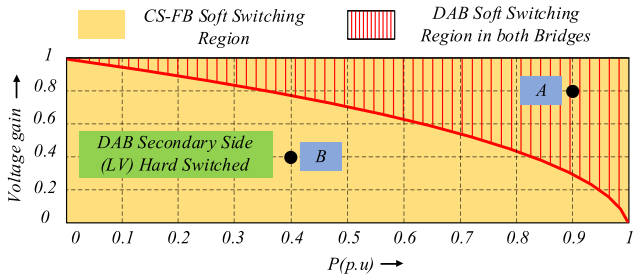


Fig. 5. Soft-switching range of the proposed BDSUD and the DAB-based S-PPC versus voltage gain and normalized output power.

The only parameter that affects this soft-switching border is the leakage inductance of the transformer. Increasing the leakage will widen the soft-switching region of the DAB-based S-PPC. However, the power transfer capacity between the two ports will be decreased by increasing the leakage inductance. A tradeoff between these two issues must be considered when designing an S-PPC based on the DAB converter. On the other hand, the BDSUD is based on a current-source converter. Its soft-switching region covers the whole operation range by considering duty cycle values for the HV and the LV port, the transformer leakage inductance, and the snubber capacitors in the HV port. The soft-switching design criteria will be discussed in Section III.

### D. Component Stress Factor (CSF) Comparison

To compare the proposed S-PPC in terms of voltage and current stresses of components, the component stress factor (CSF) is calculated. It is based on the component load factor (CLF), which is a numerical method considering the root mean square (rms) current and the maximum voltage of the devices. The results are normalized to the nominal power of the converter to have a dimensionless parameter for better comparison. In order to simplify CSF calculations, two main assumptions are considered. All the converter elements are assumed to be lossless, and the inductor current is ripple free. For each type of converter element, CSF will be calculated independently. Therefore, there will be three categories of devices that have different CSF calculations. For the switching devices (active and passive), the semiconductor CSF (SCSF) is the maximum blocking voltage multiplied by the rms current of the device. The capacitor CSF (CCSF) is also derived by the multiplication of maximum voltage to the rms current. Regarding magnetic components of a converter, winding CSF (WCSF) is determined by the maximum average voltage across a component winding multiplied by its rms current. The mentioned parameters are estimated by the following equations:

$$\mathrm{SCSF}_i = \frac{\sum_j W_j}{W_j} \cdot \frac{V_{\max}^2 \cdot I_{\mathrm{rms}}^2}{P_{\mathrm{rated}}^2} \tag{3}$$

$$\mathrm{CCSF}_i = \frac{\sum_j W_j}{W_j} \cdot \frac{V_{\max}^2 \cdot I_{\mathrm{rms}}^2}{P_{\mathrm{rated}}^2} \tag{4}$$

$$\mathrm{WCSF}_i = \frac{\sum_j W_j}{W_j} \cdot \frac{V_{\max\_avg}^2 \cdot I_{\mathrm{rms}}^2}{P_{\mathrm{rated}}^2} \tag{5}$$

$$V_{\max\_avg} = \sum_i D_i \cdot |V_i| \tag{6}$$

where $P_{\mathrm{rated}}$ is the nominal power of the converter. The term $\sum_j W_j/W_j$ is the weight factor related to the resource distribution in the different components, which is assumed one for simpler calculation. The $V_{\max\_avg}$ is the maximum average voltage on the windings of magnetic devices. For both the proposed converter and the reference converter [22] the same input/output voltage and nominal power are defined to obtain a tangible comparison. The input voltage is 350 V, and the output voltage varies from 350.5 V, i.e., the relative amount of processed power regarding the total power ($K_{pr}$) of 0.1%, to 400 V ($K_{pr} = 12.5\%$). The nominal power is 3.5 kW, resulting from the nominal output voltage of 350 V and rated output current of 10 A. The impact of the solid-state circuit breaker (SSCB) on the CSF is neglected in both converters as it conducts 10 A dc with the same voltage drop across the SSCB. The results from (3) to (5) are portrayed in Fig. 6 in normalized units.

It can be observed that at the low voltage in the series port, the DAB-based S-PPC has considerably higher CSFs due to significant circulating power. To operate near zero voltage at the series port with single PSM, the DAB-based S-PPC needs to be overdesigned to withstand high current stress. At the higher voltage levels, the rms current of the transformer and the reactive power decreases, and the SCSF of DAB becomes lower than the proposed converter (at $K_{pr} = 5.4\% \ldots 10.7\%$). But this range is limited, and the SCSF increases at partiality coefficients above 12.5%. The CCSF and WCSF of the DAB-based S-PPC present similar behavior as the SCSF, but these parameters are always higher than the values of the CSFB.

On the other hand, the CSF values of the CSFB-based S-PPC are strongly correlated only with the amount of active power processed by the dc–dc cell. It can be seen from Fig. 6 that the CSF of all of the components is minimum at near zero partiality coefficient, and the CSFs increase slightly up to their maximum value at $K_{pr} = 12.5\%$. A similar comparison was also performed in [28] to investigate the feasibility of the DAB and CSFB converters configured as S-PPC. It also concludes that due to the high CSF values compared to the CSFB, the DAB topology does not always provide high performance in BDSUD S-PPCs.

### E. SSCB Structure and Function

Considering the recent S-PPCs in the literature, in almost all of the studied converters, the start-up transients and the strategy for the precharging series capacitor are neglected [14]. One of the key roles of the SSCB is to help the converter to start safely and prevent any inrush current of the initially charged series capacitor. The structure of SSCB is demonstrated in Fig. 3, while its design constraints are elaborated in [29]. It includes two back-to-back connected MOSFETs and a snubber circuit to protect switches from overvoltage. In terms of voltage and current, the SSCB elements are selected for the full voltage and current of the S-PPC. In all four quadrant operation modes of the converter, the SSCB is initially turned off. After the converter starts up, the

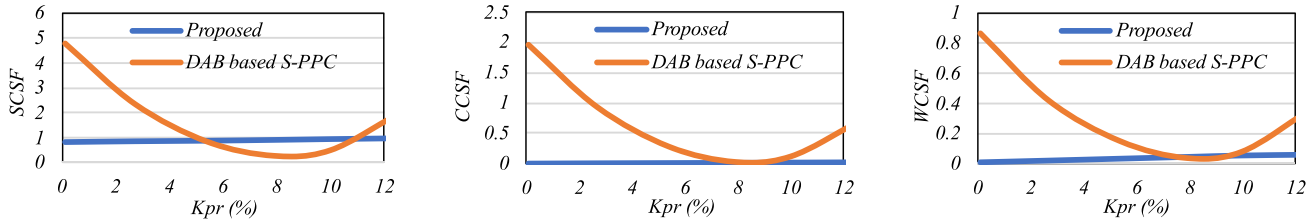


Fig. 6. CSF for both the proposed and DAB based [22] S-PPCs as a function of partiality coefficient ($K_{pr}$) (a) SCSF, (b) CCSF, (c) WCSF.

series capacitor is charged up to the voltage difference between the two dc sources ($V_{in}$-$V_o$). It must be noted that the charging operation is performed by one of the dc–dc stage buck operation modes according to the required voltage polarity of the series capacitor ($V_c > 0$ or $V_c < 0$). As soon as the capacitor voltage reaches the voltage difference ($V_c = V_{in} - V_o$), the SSCB turns ON and links the series path between input and output. By doing so, a high *dv/dt* is eliminated at the start-up, and the series capacitor charging will cause no inrush current. From this moment on, based on the sign of the reference current and the amplitude of the input/output voltage, one of the operation quadrants will be chosen, and the converter will start to work normally. Hence, the safe operation of the LV port could be ensured.

## III. Design Guidelines

The most crucial factor in any S-PPC is the amount of active power processed by the dc–dc stage of the converter, which impacts the system efficiency. Hence, the first part of this section discusses the partiality of the proposed converter. It is followed by an analysis of how soft-switching requirements should be considered in the converter design. The guidelines for selecting passive and magnetic components are given in the last two sections.

### A. Rated Power Selection

The amount of power processed by the S-PPCs is directly related to the voltage difference between both sides of the converter. In IPOS configuration, the voltage and current equations of the system can be written as follows:

$$V_o = V_{in} + V_c \tag{7}$$

$$I_{in} = I_o + I_{conv}. \tag{8}$$

It can be seen from Fig. 1 that $I_o = I_c$. The bipolar output voltage feature of the CSFB at its LV port allows us to quickly implement the step-up/down S-PPC based on (7). Therefore, the partiality coefficient, which is the ratio of processed power to the total power, can be defined as

$$K_{pr} = \frac{P_{Cout}}{P_{\text{out}}} = \frac{V_c \cdot I_c}{V_o \cdot I_c} = \frac{V_o - V_{in}}{V_o} = 1 - \frac{V_{in}}{V_o} \tag{9}$$

where $K_{pr}$ is the S-PPC partiality coefficient. Considering constant input voltage ($V_{in}$) and variable output voltage ($V_o$), the variation of $K_{pr}$ is illustrated in Fig. 7. Based on the application

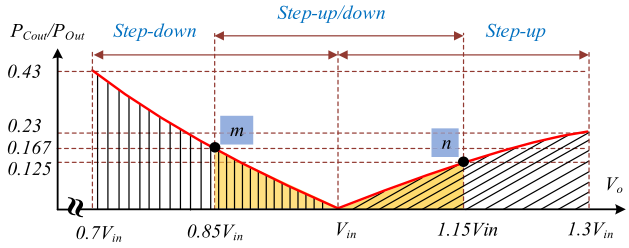


Fig. 7. Partiality of the S-PPC with constant $V_{in}$ and variable $V_o$.

TABLE II
Case Study System Parameters

| Parameter | Symbol | Value |
|---|---|---|
| Input voltage | $V_{in}$ | 350 V |
| Output voltage | $V_o$ | 350 V (± 50V) |
| Rated power | $P_{reated}$ | 3.5 kW |
| Dc-dc stage rated power | $P_{Conv\text{-}rated}$ | 600 W |
| Switching frequency | $f_{SW}$ | 50 kHz |

requirements, both input and output voltages can change in a defined range. This voltage variation defines the voltage regulation range ($\Delta V_c$).

The voltage regulation range is the only parameter that determines the amount of the processed power by the dc–dc stage and must be carefully chosen for every application. The advantage of the presented CSFB is that the $\Delta V_c$ can vary from a minimum negative voltage ($V_{c,\min}$) to zero and finally to the maximum positive voltage ($V_{c,\max}$). The limits are constrained by the transformer turn ratio ($n$) and the parallel port voltage.

The superiority of step-up/down S-PPCs over step-up or step-down SPPCs is distinctly evident in Fig. 7 regarding the maximum power processed by the dc–dc stage. These figures are drawn for the maximum 30 percent voltage regulation range for the input or output port ($\Delta V_c = V_{c,\max} - V_{c,\min}$). With a maximum $\Delta V_c$ of 50 V, the partiality is limited to 17%, based on the case study parameters in Table II. Points $m$ and $n$ in Fig. 7 depict the operating boundaries for the designed S-PPC. Considering $\eta_c$ as the dc–dc stage efficiency, the system efficiency can also be calculated according to the following equation:

$$\eta_{sys} = 1 - K_{pr} \cdot (1 - \eta_c). \tag{10}$$

In this equation, $\eta_{sys}$ stands for S-PPC efficiency. From (10), it can be perceived that the S-PPC efficiency is affiliated with both the partiality coefficient and the dc–dc stage efficiency. This is the phase in which improving the dc–dc stage efficiency could slightly improve the overall S-PPC efficiency. The partiality coefficient depends on the voltage regulation range, which is not entirely under control in every application.

For example, in PV systems defining the number of series connected PV modules determines the nominal output voltage of the PV string. The PV string output voltage, in most cases, varies within thirty percent variation from its nominal voltage [14]. On the other hand, in battery applications, the battery cell voltages at the state of charge (SoC) of 20% and 80% specify the voltage regulation range, which is typically wider than in PV systems [30]. The other parameter that is affected by the power electronics design is the dc–dc stage efficiency. Therefore, various sources of power loss ought to be carefully analyzed and designed to maximize the $\eta_{sys}$.

### B. Soft-Switching Criteria

For the CSFB, the maximum output current at the LV port determines the soft-switching operation of LV port switches. The maximum output current is defined to fulfill the application of the S-PPC, which for instance, in battery energy storage applications, is the maximum permissible charge/discharge current. Considering $I_{c,\max} = I_{o,\max}$, the duty cycle ($D_{lv}$) of the LV port switches ($S_{1.1} \ldots S_{4.2}$) can be calculated as follows:

$$D_{lv} \geq 0.5 + \frac{2 \cdot n \cdot I_{c,\max} \cdot L_{eq} \cdot f_{sw}}{V_{in}}. \tag{11}$$

The duration of overlapping of the switches must be chosen to permit full ZCS for the switches to prevent any voltage spike across them caused by the current mismatch. It is understandable that above the maximum output current, the ZCS criterion of the converter will be violated. Therefore, in applications where the maximum output current is not a constant value, the adaptive regulation of the overlap time is recommended. With the parameters of the designed converter, $D_{lv} = 0.51$ is enough to ensure full soft-switching operation under the maximum output current of 10 A. The current redistribution time for LV port switches could be written as

$$t_{\text{red}} = \frac{2 \cdot n \cdot I_c \cdot L_{eq}}{V_{in}}. \tag{12}$$

From Fig. 2(a) and considering (12), the minimum phase shift in the boost mode must be high enough to allow for complete current redistribution between the switches

$$\varphi_{\text{min}}^{\text{boost}} = \omega \cdot t_{\text{red}} \tag{13}$$

where $\omega = 2\pi f_{sw}$. The resonance time can be estimated by the following equation:

$$t_{res} = \frac{\frac{\pi}{2} - arctg\left(\frac{2 \cdot n \cdot I_c \cdot Z_r}{V_{in}}\right)}{\pi \cdot f_r}, \tag{14}$$

in which $Z_r = \sqrt{L_{eq}/C_{eq}}$, and $f_r = 1/\left(2 \cdot \pi \cdot \sqrt{L_{eq}/C_{eq}}\right)$ $C_{eq} = C_S \cdot n^2/2$. The longest resonance time occurs at no load conditions, which is the critical point for the selection of $C_S$. The unique feature of CSFB with asymmetric SMC modulation allows the $C_{eq}$ to recharge by the resonant current (whose peak is equal to or higher than $I_{c,\max}$) regardless of the output current and operation point of the dc–dc stage. Consequently, the capacitor charge is load-independent and satisfies the complete soft switching in the operation range of the converter regardless of $I_c$ value. As can be seen from Fig. 2(b), the resonance state during the buck mode of the dc–dc stage starts when one of the LV port switches turns ON and one of the HV port switches turns OFF. The duration of this time interval in the buck mode is load-independent and depends on only $L_{eq}$ and $C_s$ values. On the other hand, when the dc–dc stage operates in the boost mode, the resonance period starts right after finishing the current redistribution time ($t_{\text{red}}$). Consequently, the variation of the load current will change the $t_{\text{red}}$ and resonance period start point as well as its duration. This dependency of resonance period in the boost mode appears as arctg term in (14).

There must also be a constant time interval between both port switches to allow for ZVS of the HV port switches. From Fig. 2, one can observe that this time interval is the accumulation of resonance time and current redistribution time in the buck mode. Hence, with the longest resonance time occurring in $I_c = 0$, the maximum duty cycle of HV port switches $D_{hv}$ can be derived as

$$D_{hv} \leq 0.5\left(1 - \frac{f_{sw}}{f_r}\right). \tag{15}$$

Real prototype parameters require 2.8% dead time at the control of the HV port switches to allow resonance and current redistribution periods. Thus, $D_{hv} = 0.47$ is applied to the $S_5$ and $S_6$. The minimum phase shift in the buck mode is also the sum of both $t_{\text{red}}$ and $t_{res}$

$$\varphi_{\text{min}}^{\text{buck}} = \omega \cdot (t_{\text{red}} + t_{res}). \tag{16}$$

The minimum phase shift in buck mode is the basis for choosing the $C_{eq}$ and $L_{eq}$ due to more duty cycle loss in this mode. Fulfilling (11), (13), (15), and (16) guarantee the full soft switching of the CSFB within its operating range.

### C. Design of Passive Components

The capacitors ($C_1 = C_2 = C_{\text{in}}$) and inductor ($L$) are selected regarding allowed voltage and current ripples at the HV and LV ports, respectively. The current ripple of the inductor can be determined as

$$\Delta i_L = \frac{V_c \cdot (1 - D_a)}{4 \cdot L \cdot f_{sw}} \tag{17}$$

where the $D_a$ is the active power transfer duration, which is shown in Fig. 2 for both the buck and boost operation of the dc–dc stage.

Regarding the HV port capacitors, the voltage ripple across them can be estimated by

$$\Delta V_{\text{HV}} = \frac{P \cdot (1 - D_a)}{2 \cdot C_{in} \cdot V_{in} \cdot f_{sw}} \tag{18}$$

where the $\Delta V_{\text{HV}}$ is the voltage ripple across the HV port of the converter.

### D. Transformer Design

The isolation transformer is undoubtedly one of the most critical components of the dc–dc stage in every S-PPC, as it denotes the voltage regulation range between input and output. In the selected CSFB dc–dc converter, a careful design of the transformer is one of the crucial design steps. Minimizing the leakage inductance reduces the resonance time ($t_{res}$) and the duty cycle loss, leading to reduced component stresses. In addition, the power circulation during the resonance period within LV port switches can be minimized. It is of significant importance due to the flow of high current through four series switches in every resonance period that could add to the conduction loss. The lowest HV port voltage specifies the minimum dedicated turns ratio, so

$$n_{\min} \geq \frac{V_{in,\min}}{2 \cdot D_{a,\max} \cdot V_{c,\max}} \tag{19}$$

$$V_{c,\max} = V_{in,\min} - V_{o,\max}. \tag{20}$$

In (19), the maximum absolute value is to be calculated since (20) would yield a negative value. The $D_{a,\,\max}$ is limited by the $t_{res}$, $t_{\mathrm{red},}$ and the voltage drop in components of the converter. It is different for the buck and boost operation modes, but the worst case, the boost mode, must be considered as the design basis. In the final design $D_{a,\,\max} = 0.9$ is considered to include all the mentioned duty cycle losses. The maximum flux density for the square-wave transformer is the result of the expression as follows:

$$B_{\max} = \frac{V_{in,\max}}{4 \cdot n_1 \cdot f_{sw} \cdot A_e} \tag{21}$$

where $n_1$ is the number of HV side turns and $A_e$ is the effective cross section of the transformer core. Due to the application of a half-bridge circuit at the HV port, the transformer turns ratio is half for the same voltage values compared to the full-bride structure. From the transformer point of view, the result is a smaller and cheaper transformer with low leakage inductance.

## IV. Experimental Results and Discussion

To confirm the theoretical analysis and prove the mentioned claims, a prototype with a rated power of 3.5 kW is assembled (see Fig. 8). Two iTECH IT6000C bidirectional dc power supplies are connected to the S-PPC ports. They can apply a defined function of voltage/current to both ports. The control system is based on an STM32G474 Cortex M4 microcontroller. The whole system is connected to the Yokogawa WT1800 high-performance power analyzer was used to measure the efficiency of the converter. Table III lists the real parameter values and component types in the tested converter.

To verify the soft-switching operation, two points are selected in Fig. 5. Point (A) represents 0.9 p.u. of output power and 0.8 normalized voltage gain. As can be seen from Fig. 9, the HV port switches turn ON in ZVS condition, which is clear in Fig. 9(a). In the turn-OFF process [see Fig. 9(b)], the switching loss is reduced by limiting *dv/dt* using snubber capacitors.

Moreover, Fig. 9(c) depicts the switching waveforms of the LV port switches in which $S_{3.1}$ turns OFF by natural commutation

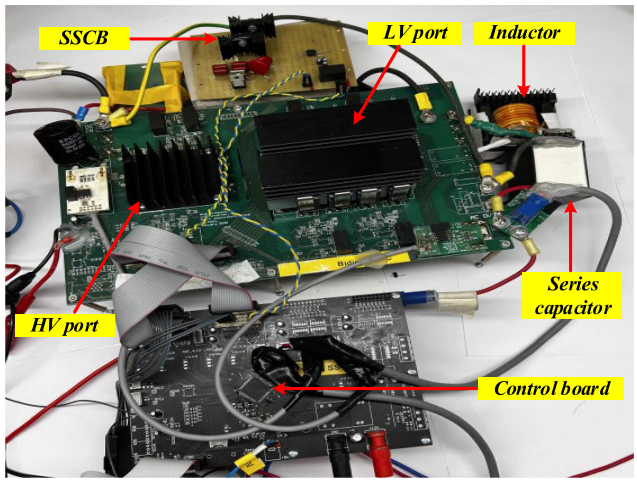


Fig. 8. Proposed BDSUD experimental prototype.

TABLE III
Components and Parameters of the Experimental Prototype

| Component/Parameter | Symbol | Value/Type |
|---|---|---|
| LV port switches | $S_{1.1}$-$S_{4.2}$ | C3M0120090D |
| HV port switches | $S_5$, $S_6$ | C3M0120090J |
| LV port inductor | $L$ | 100μH |
| Inductor core | - | ETD54/28/19/3C97 |
| Transformer leakage inductance | $L_{eq}$ | 850nH |
| Transformer turns ratio | $n$ | 2.3:1 |
| Transformer core | - | ETD54/28/19/3C97 |
| HV port capacitors | $C_1$=$C_2$ | 60μF |
| Series capacitor | $C$ | 100μF |
| HV port snubber capacitors | $C_s$ | 1.1nF |
| Isolated gate drivers | - | UCC21520-Q1 |

of the body diode during the synchronous rectification period. The $S_{4.2}$ also turns OFF totally in ZCS condition. The current redistribution between LV port switches happens successfully during their turn-ON/OFF period. The same measurements in point (B) from Fig. 5 are given in Fig. 10 to prove the soft-switching operation at low power and low series port voltages.

The turn-ON process of switches $S_{3.1}$ and $S_{4.2}$ are shown in Fig. 11. To clearly distinguish each figure, the turn-ON points in Figs. 9(c) and 10(c) are marked with the numbers from 1 to 4 depicting the turn-ON of $S_{3.1}$ and $S_{4.2}$ in high and low powers respectively. During the turn-ON time of the LV port switches, both for top and bottom switches, they become in series with the leakage inductance of the transformer. Due to this reason, the *di/dt* is limited by the leakage inductance. The current of the switch $S_{3.1}$ starts from zero and enters resonance mode. During this time interval, the peak resonance current is limited to less than 2 A, which is evident from Fig. 11(a) and (c). The current rise during the turn-ON process is even lower than this number (around 1A). The current of the switch $S_{4.2}$ starts to increase from zero to the maximum value because of the current redistribution from the switch $S_{2.2}$. As can be seen from Fig. 11(b) and (d), the current slope is low, and the peak current during the turn-ON process reaches 1 A. Therefore, the turn-ON condition of the LV side switches is a

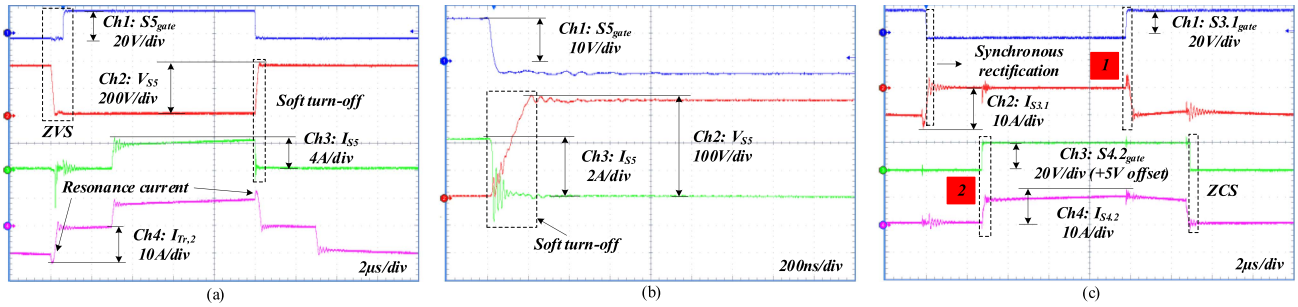


Fig. 9. Experimental waveforms at point (A) of Fig. 5($P$(p.u.) $= 0.9 = 3150$ W and $G = 0.8$). (a) Current and voltages of the switch $S_5$ and transformer current. (b) Soft turn-OFF of the switch $S_5$. (c) ZCS of the LV port switches.

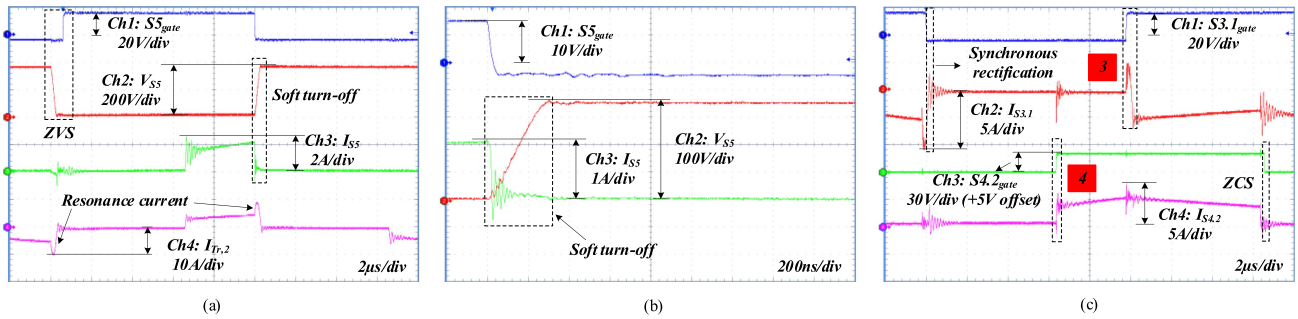


Fig. 10. Experimental waveforms at point (B) of Fig. 5 ($P$(p.u.) $= 0.4 = 1400$ W and $G = 0.4$). (a) Current and voltages of the switch $S_5$ and transformer current. (b) Soft turn-OFF of the switch $S_5$. (c) ZCS of the LV port switches.

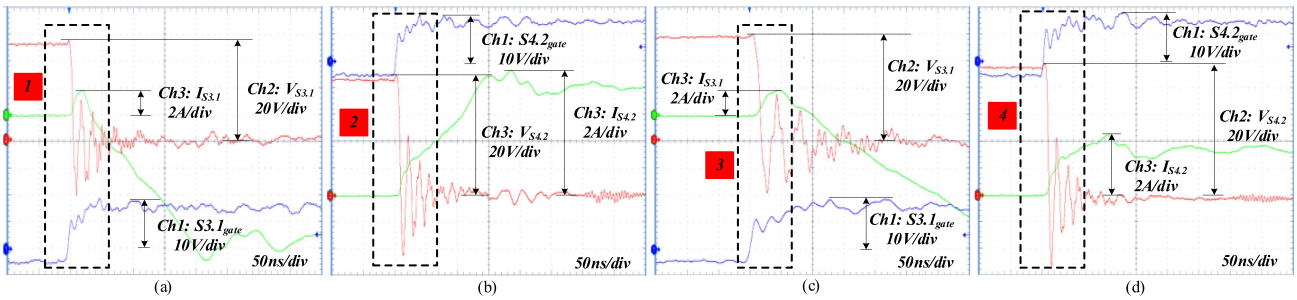


Fig. 11. Soft turn-ON of LV side switches. (a) $S_{3.1}$ turn-ON [point 1 in Fig. 9(c)]. (b) $S_{4.2}$ turn-ON [point 2 in Fig. 9(c). (c) $S_{3.1}$ turn-ON (point 3 in Fig. 10(c)), (d) $S_{4.2}$ turn-ON [point 4 in Fig. 10(c)].

soft turn-ON that is fulfilled by the leakage inductance of the transformer.

Fig. 12(a) demonstrates the soft start when the series capacitor starts to charge ($t_1$) and reaches the voltage difference between the input and the output ($t_2$). Afterward, the SSCB connects ($t_3$) to create a series path for unprocessed power transfer. It is visible that there is no inrush current after the SSCB connection, and the controller can smoothly increase the output current from almost zero to 4 A. In Fig. 12(b), the current reference ramp is applied as reference output current to the controller to observe the capability of the S-PPC to follow the ramp current. The result shows that the PI regulator successfully follows the reference current without any perturbation. It is worth noting that the series capacitor voltage increases slightly by the current ramp due to the parasitic resistances of the component. In Fig. 12(c), the output voltage ramps up from 360 V to 390 V, and the PI controller regulates the output current at the constant reference current of 10 A.

The S-PPC functionality near zero voltage of the series capacitor is also examined to confirm the claims of the previous sections. The result in Fig. 13 verifies the capability of the proposed BDSUD S-PPC to operate at this critical point. Fig. 13(a) illustrates the converter operation in the Q-I where the dc–dc stage works as a buck converter. The modulation strategy here is the PSM implemented throughout the entire voltage regulation range. It can be seen from Fig. 13(a) that the S-PPC can deliver 5 A current without any power circulation between the HV and LV ports. These results prove that S-PPC can regulate the energy transfer to the LV port down to zero.

The results for Q-IV near zero operation are shown in Fig. 13(b). Both $D_{rev}$ and $D_s$ are regulated in a way that $D_s$ is regarded as a constant value ($D_s = 0.25$) and varies to regulate

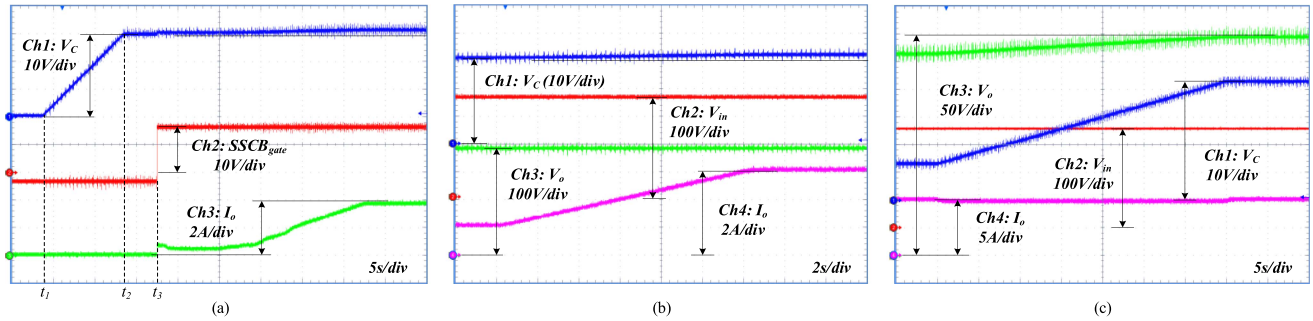


Fig. 12. Dynamic operation of the proposed converter. (a) Soft start procedure to $I_{o\_ref} = 4$ A. (b) S-PPC response to a ramp reference current ($I_{o\_ref}$ = 2–6 A). (c) S-PPC response to a voltage ramp at the output port ($V_o$ = 360–390 V).

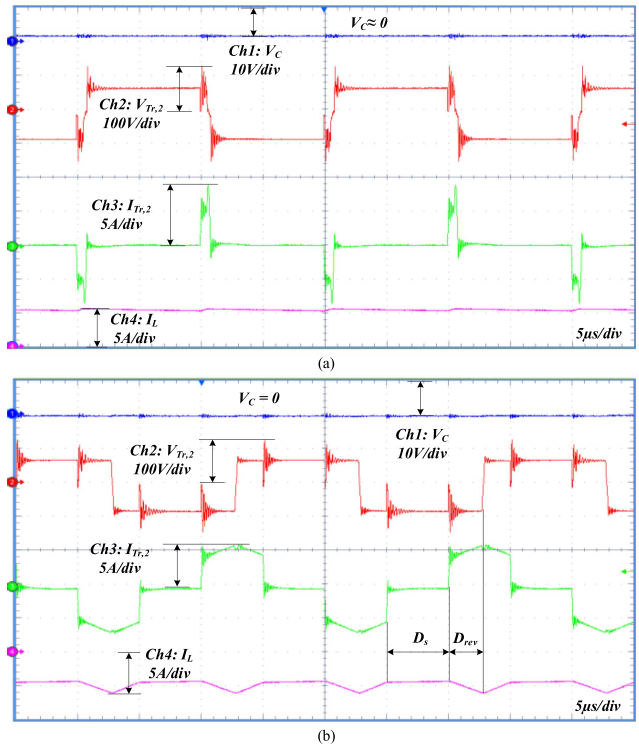


Fig. 13. Operation near the zero voltage of the series capacitor (a) PSM in Q-I with $V_{in} = 350$ V, $V_o = 350$ V (b) Reverse power flow control modulation in Q-IV with $V_{in} = 350$ V, $V_o = 350$ V.

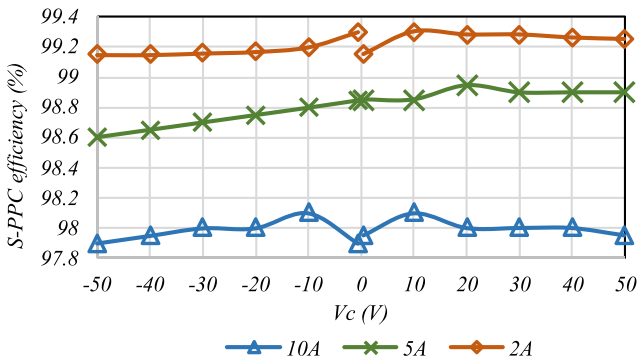


Fig. 14. Efficiency of the proposed S-PPC versus $V_c$ for different currents.

the current at the output port. Both of them are designated in Fig. 13(b). Using the reverse power flow mode of duration $D_{rev}$ provides an opportunity to control the LV side inductor current when the input voltage is too low for its regulation using $D_s$. During $D_{rev}$, the energy from the HV port charges the LV port inductor, which can be seen from this figure. When compared to the DAB structure in [22], almost zero energy circulation in Q-I operation mode [see Fig. 13(a)] and controllable limited energy circulation in Q-IV operation mode [see Fig. 13(b)] confirm much better controllability of the BDSUD. As expected, the proposed concept provides low total CSF, over the DAB-based S-PPC. It must be noted that the functionality of DAB-based step-up/down S-PPCs is not investigated in detail in the literature.

Finally, the efficiency measurement is done throughout the different $V_C$ voltages for three current levels (2 A, 5 A, and 10 A in Fig. 14). The peak efficiency of 99.3% is achieved at the output current of 2 A and $V_C = 10$ V, which agrees with (8), as discussed in Section III.

It is worth noting that the given prototype was designed to prove the proposed concept and does not contain any costly components, like transistors with very low $R_{DSon}$. It was built for robust operation while testing soft-start and soft-switching functionality, resulting in relatively high conduction losses, leaving room for improvement. However, the proposed prototype can still achieve efficiency values of over 99%. Based on the experimental results, the proposed concept could be compared to the other S-PPCs in Table IV. It is worth noting that the comparison demonstrates strong dependence between the range of partiality $K_{pr}$ and maximum efficiency. The wider the range, the lower peak efficiency could be due to design tradeoffs. Also, the efficiency of the reference S-PPC was not provided in [21] to compare with the proposed concept.

Although the closest topology to the BDUSD is the one presented in [22], a comparison table including some of the other similar S-PPCs is demonstrated in Table IV. None of these topologies provide full-range soft switching, and only [22] works with ZVS conditions at high load levels, as discussed in previous sections. The components count is generally higher in bidirectional step-up/down SPPCs than in unidirectional analogs. The same could be concluded about the step-up and step-down S-PPCs, which results in higher maximum power processed by the components. Additional switches are employed

TABLE IV
COMPARISON OF THE PROPOSED S-PPC TO THE EXISTING SOLUTIONS

| Ref. | Configuration | Voltage conversion mode | No. of components (S+D+C+M)* | $V_{in}$ | $V_o$ | $K_{pr,max}$ | Nominal power (W) | Efficiency range | Soft switching | Soft start |
|---|---|---|---|---|---|---|---|---|---|---|
| **[14]** | IPOS | Step-up/down | 6+2+2+2 | 187-253 | 220 | 15 | 750 | 98.6-99.6 | no | no |
| **[16]** | IPOS | Step-up | 4+2+1+2 | 154-220 | 220 | 30 | 750 | 99 | no | no |
| **[18]** | IPOS | Step-up/down | 4+4+2+2 | 187-253 | 220 | 15 | 950 | 98.7-99.48 | no | no |
| **[19]** | - | Step-up/down | 8+4+2+2 | 400 | 347-435 | 8 | 7300 | 98.5-99.6 | no | no |
| **[21]** | IPOS | Step-up/down | 12+0+3+3 | 350 | 300-400 | 7 | 1500 | - | partial | no |
| **[27]** | - | Step-up | 8+0+2+2 | 2-23 | 50-58 | 22 | 3456 | 80-98.2 | no | no |
| **This work** | IPOS | Step-up/down | 12+0+5+2 | 300-400 | 350 | 17 | 3500 | 97.9-99.3 | yes | yes |

* S – switches, D – diodes, C – capacitors, M – magnetic components.

to form four-quadrant switches or unfolding circuits to enable bipolar operation of the dc–dc stage in the LV port. The presence of diodes in [14], [16], [18], and [19] creates additional conduction loss due to the forward voltage drop of the diodes.

Regarding soft start and near-zero-voltage operation of the series LV port, the existing literature does not demonstrate how the asserted current controllability and high efficiency have been achieved other than by short-circuiting the LV port switches. As the smooth operation of S-PPC at this critical point is important, the methodology to operate at this point must be demonstrated. In [19], the mode change from step-down to step-up is depicted, but the transformer current/voltage becomes zero during this mode change. Apparently, the dc–dc stage stops delivering power in this interval, but the control strategy is not provided. Being based on a current-source dc–dc topology, the converter from [19] is a unidirectional alternative to the proposed converter. It is worth mentioning that the proposed converter provides good current control capabilities by utilizing nearly 90% of the $\pm 0.5$ phase-shift duty cycle theoretical range, while the converter in [19] employs shoot-through duty cycle control, which has little dependence on the power level. As a result, the converter from [19] performs current control at the constant dc voltage gain in a very narrow duty cycle range, raising concerns about its robustness in battery energy storage applications.

## V. CONCLUSION

The S-PPC concept can be considered a highly promising solution for various dc–dc applications. However, its practical feasibility is highly influenced by the voltage regulation range requirement and corresponding partiality coefficient. To deal with the application requirements, the S-PPCs based on basic topologies often have to be designed for relatively large power levels, reducing their practical feasibility due to cost and complexity reasons. The proposed BDSUD solution addresses this issue thanks to its step-up/down capability, effectively reducing the partiality coefficient twofold. Moreover, the solution allows bidirectional power flow, making it suitable for various storage and dc microgrid applications. The operation was verified with an experimental prototype with dc–dc stage power of 600 W and total power of 3.5 kW in start-up, steady-state and transient operation modes. When compared to the other known BDSUD S-PPC based on DAB, the proposed solution based on CSFB topology features the following advantages.

1) Thanks to the HB/VDR structure, the turns ratio of the transformer is reduced by at least a factor of 2, simplifying its design.
2) Having the same number of semiconductor devices, the number of gate driver channels and isolated gate supplies is reduced by 2.
3) The topology can be designed for full-range soft switching with simple single phase shift control.
4) The regulation close to zero series port voltage can be provided without excessive energy circulation.
5) The overall component stress factor is lower for most of the operating points

At the same time, the design and operation of the converter are highly influenced by the leakage inductance of the transformer, which has to be always minimized at the design stage. The parasitic oscillations at the LV stage appear regardless of the modulation strategy, resulting in higher voltage stress and requiring approximately 50% higher voltage rating of the devices than that in the DAB counterpart. Nevertheless, the cumulative advantages of the proposed BDSUD make it among the most versatile and promising S-PPC concepts for practical applications.

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