Letters

Origin of Soft-Switching Output Capacitance Loss in Cascode GaN HEMTs at High Frequencies

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***Abstract*—Output capacitance (C_{OSS}) loss (E_{DISS}) is produced when the C_{OSS} of a power device is charged and discharged, which ideally should be a lossless process. This loss was recently revealed to be a crucial concern for GaN high electron mobility transistors (HEMTs) in high-frequency soft-switching applications. Among various GaN devices, the composite-type, cascode GaN HEMT was reported to show the largest E_{DISS} with a voltage dependence distinct from discrete GaN HEMTs. However, the physical origins of the E_{DISS} in cascode GaN HEMTs remain unclear. This article fills this gap by identifying three loss components and, for the first time, experimentally quantifying them in the multi-MHz resonant switching. These loss components include: a) the avalanche loss of Si MOSFET; b) the intrinsic E_{DISS} of GaN HEMT; and c) the Si avalanche-induced GaN turn-ON loss. The last component was found to dominate E_{DISS} at high voltage. By eliminating the Si avalanche and the associated loss components (a) and (c), the E_{DISS} of cascode GaN HEMTs can be reduced by up to 75% at the price of an increase in output charge and switching transition time. These results provide new physical insights and practical guidelines to trim the soft-switching loss of cascode GaN HEMTs in high-frequency applications.**

***Index Terms*—Cascode, GaN HEMT, output capacitance losses, resonant converter, soft-switching.**

I. Introduction

BENEFITING from high channel mobility and breakdown field, GaN high electron mobility transistor (HEMT) has significantly advanced the switching frequency, power density, and form factor of power electronic systems [1]. However, many dynamic characteristics of GaN HEMTs are known to differ from their static counterparts, e.g., dynamic on-resistance and breakdown voltage [2]. Recently, the output capacitance (C_{OSS}) of GaN HEMTs was found to present dynamic hysteresis in a cycle of charging and discharging, producing a device loss in this ideally lossless process [3], [4]. This C_{OSS} loss (E_{DISS}) could dominate the GaN device loss in high-frequency (>MHz), soft-switching applications, e.g., resonant converters [4], [5].

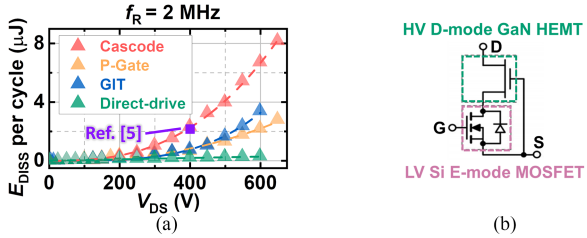

Fig. 1. (a) Measured E_{DISS} of different types of GaN HEMTs. (b) Schematic of a cascode GaN HEMT.

Up to now, several methods have been developed for C_{OSS} loss measurements [3], [6], [7], [8], unveiling the E_{DISS} in various GaN HEMTs including p-gate HEMT, gate injection transistor, cascode HEMT, and direct-drive HEMT. The results from several methods have revealed unanimously that the cascode GaN HEMT shows a larger E_{DISS} than other GaN devices, and its E_{DISS} ramps up more rapidly with the peak drain-to-source voltage (V_{DS}) [3], [5], [8]. As an example, Fig. 1(a) shows the E_{DISS} of 650 V cascode GaN HEMTs reported in [5] and [8] in comparison with other similarly-related GaN devices.

Despite many studies on the physical mechanisms of E_{DISS} in discrete GaN HEMTs [7], [9], the origin of the larger E_{DISS} in cascode GaN HEMTs has not been fully understood, due to the complicated interaction between the Si MOSFET and GaN HEMT and various loss origins inside the cascode device [10], [11]. Some early works looked into the soft-switching loss of cascode GaN HEMTs [10], [12], [13], but the switching frequency is relatively low and the E_{DISS} of GaN HEMT was not considered.

This article, for the first time, uncovers the physical origins of E_{DISS} in cascode GaN HEMTs under MHz resonant switching and quantitatively separates the power losses from different mechanisms at various V_{DS}. This loss decoupling is enabled by carefully decapsulating the off-shelf cascode devices, adding additional test points, and intentionally suppressing the specific loss component. Finally, an effective method to mitigate E_{DISS} and an E_{DISS}-V_{DS} model are provided for cascode GaN HEMTs.

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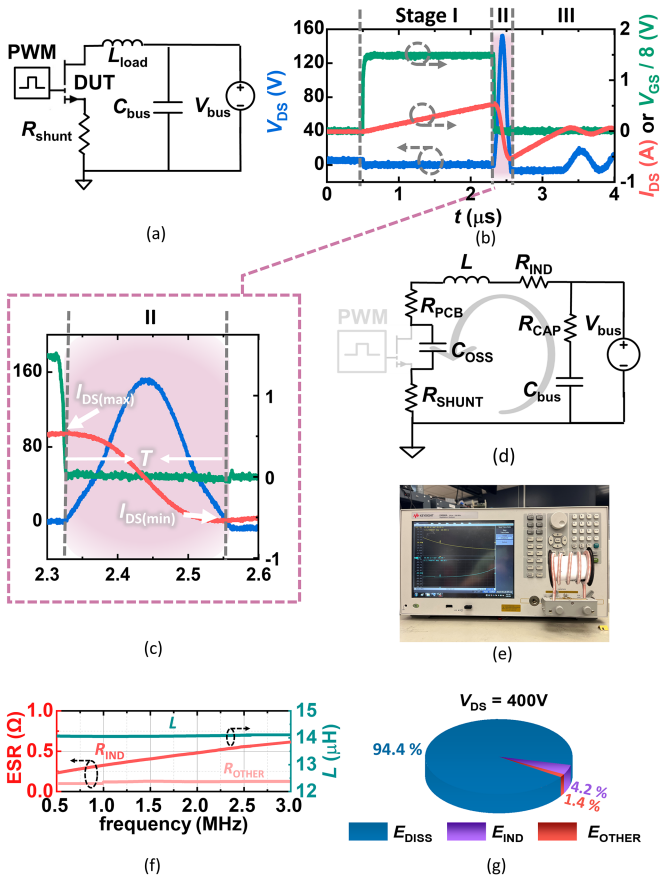

Fig. 2. (a) Schematic of a UIS circuit. (b) A typical UIS waveform. (c) Zoom-in waveform of stage II. (d) Illustration of parasitic ESR of each component along the power loop. (e) ESR and L measurement on a Keysight E4990A impedance analyzer. (f) Measured ESR and L. (g) Loss breakdown in the UIS test at $V_{\mathrm{DS(peak)}}$ of 400 V.

II. DUT, Test Methodology, and Test Results

The device under test (DUT) is a commercial 650V/36A cascode GaN HEMT [14], which consists of a low-voltage E-mode Si MOSFET and a high-voltage D-mode GaN HEMT to realize the E-mode high-voltage operation [see Fig. 1(b)]. The E_{DISS} measurement is based on an unclamped inductive switching (UIS) test [see Fig. 2(a)], which has been thoroughly described in [15]. During the UIS test [11], the DUT is placed in series with an air-core load inductor (L_{load}) and a low-voltage power supply (V_{bus}). Fig. 2(b) displays a typical waveform from the UIS test, which is used to extract E_{DISS} [8]. The UIS test involves three stages: in stage I, the DUT is turned ON, and V_{bus} charges L_{load}; in stage II, the DUT is turned OFF and L_{load} resonates with the DUT's C_{OSS} for approximately a half cycle, which imitates the DUT's operation in resonant converters; in stage III, the DUT turns ON reversely, and L_{load} is discharged. The E_{DISS} extraction mainly relies on the UIS waveforms in stage II.

Fig. 2(c) provides a zoomed-in view of the stage II waveform to illustrate the principle of E_{DISS} extraction. The total loss (E_{TOTAL}) in this half resonance cycle can be calculated from the peak and valley values of the DUT's drain-to-source current (I_{DS}), denoted as $I_{\mathrm{DS(min)}}$ and $I_{\mathrm{DS(max)}}$, respectively,

$$E_{\mathrm{TOTAL}} = 0.5\, L \left(I_{\mathrm{DS(max)}}^2 - I_{\mathrm{DS(min)}}^2 \right) \tag{1}$$

where L is air-core L_{load}'s inductance, measured at different frequencies in the range of 1 to 15 MHz on a Keysight E4990A impedance analyzer.

To obtain the DUT's E_{DISS}, the winding loss of L_{load} (E_{IND}) and the conduction loss of other parasitic components (E_{OTHER}) are then subtracted from E_{TOTAL}

$$E_{\mathrm{IND}} = \left(I_{\mathrm{DS(max)}}/2 \right)^2 R_{\mathrm{IND}}\, T \tag{2}$$

$$E_{\mathrm{OTHER}} = E_{\mathrm{SHUNT}} + E_{\mathrm{PCB}} + E_{\mathrm{CAP}} = \left(I_{\mathrm{DS(max)}}/2 \right)^2 \left(R_{\mathrm{SHUNT}} + R_{\mathrm{PCB}} + R_{\mathrm{CAP}} \right) T \tag{3}$$

where $I_{\mathrm{DS(max)}}/2$ is the RMS value of I_{DS} over the half-resonance cycle; T is the time of the half-resonance cycle. Here E_{OTHER} includes the losses on the PCB board and the shunt resistor. R_{IND}, R_{SHUNT}, R_{PCB}, and R_{CAP} are the equivalent serial resistance (ESR) of the L_{load}, shunt, PCB, and C_{bus} [see Fig. 2(d)]. R_{OTHER} is the sum of R_{SHUNT}, R_{PCB}, and R_{CAP}. Fig. 2(e) shows a photo of the ESR and L measurement on the impedance analyzer. The measured L, R_{IND}, and R_{OTHER} are shown in Fig. 2(f). In principle, the DUT's turn-OFF loss is not included in E_{DISS}. To eliminate its possible interference due to circuit parasitics, we use a very low V_{bus} of 5 V to minimize the DUT's turn-OFF loss. The E_{DISS} is given by

$$E_{\mathrm{DISS}} = E_{\mathrm{TOTAL}} - E_{\mathrm{IND}} - E_{\mathrm{OTHER}}. \tag{4}$$

For the DUT in the stage II resonance, its frequency (f_R) is tuned by L; $I_{\mathrm{DS(max)}}$ and the peak resonant V_{DS} ($V_{\mathrm{DS(peak)}}$) are modulated by the DUT ON-time in stage I. In this article, a constant L of 14 μH is used to generate an f_{R} of about 2 MHz. Fig. 2(g) shows the experimental loss breakdown for E_{TOTAL} with a $V_{\mathrm{DS(peak)}}$) of 400 V. The DUT's E_{DISS} accounts for 94.4% of E_{TOTAL}, suggesting the impact of E_{IND} and E_{OTHER} is marginal.

Fig. 3(a)–(c) shows the complete test setup, measurements, and the prototyped test system, respectively. Air-core Litz-wire-based inductors are used for small and computable losses at high frequencies. An off-shelf screw-in co-axial shunt with 2 GHz bandwidth and a minimal insertion inductance is utilized for the accurate measurement of DUT's I_{DS} [16]. The repetitive E_{DISS} measurements reveal an error bar of $\pm 3\%$.

To accurately monitor the behavior of the Si MOSFET and GaN HEMT in the cascode, the DUT is decapsulated and an extra test point is attached to the floating point, i.e., the Si MOSFET's drain (GaN HEMT's source), to monitor the V_{DS} of Si MOSFET ($V_{\mathrm{DS(Si)}}$) [see Fig. 3(d)]. The fabrication of this decapsulated DUT started by immersing the packaged device into a mixture of hot fuming nitric acid and sulfuric acid (HNO_3:H_2SO_4 = 1:2). Then, hydrochloric was applied to dissolve the original interconnection between the Si MOSFET and GaN HEMT. A thin piece of copper band was finally inserted between these two devices by reflow soldering. After the test point was placed, the device was re-encapsulated with silicone gel to ensure adequate electrical isolation. This decapsulated device with an extra test point is

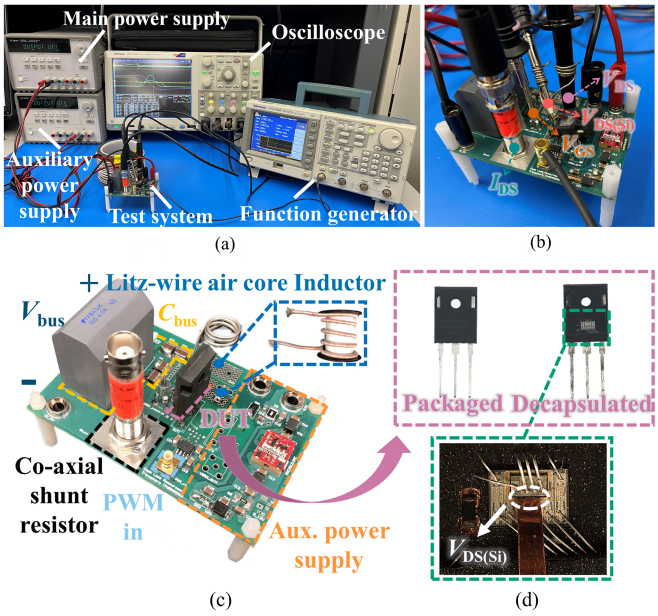

Fig. 3. (a) Photo of the complete test setup. (b) Photo showing all the voltage and current measurements. (c) Photo of the UIS test setup. (d) Picture of the decapsulated device showing the added extra point.

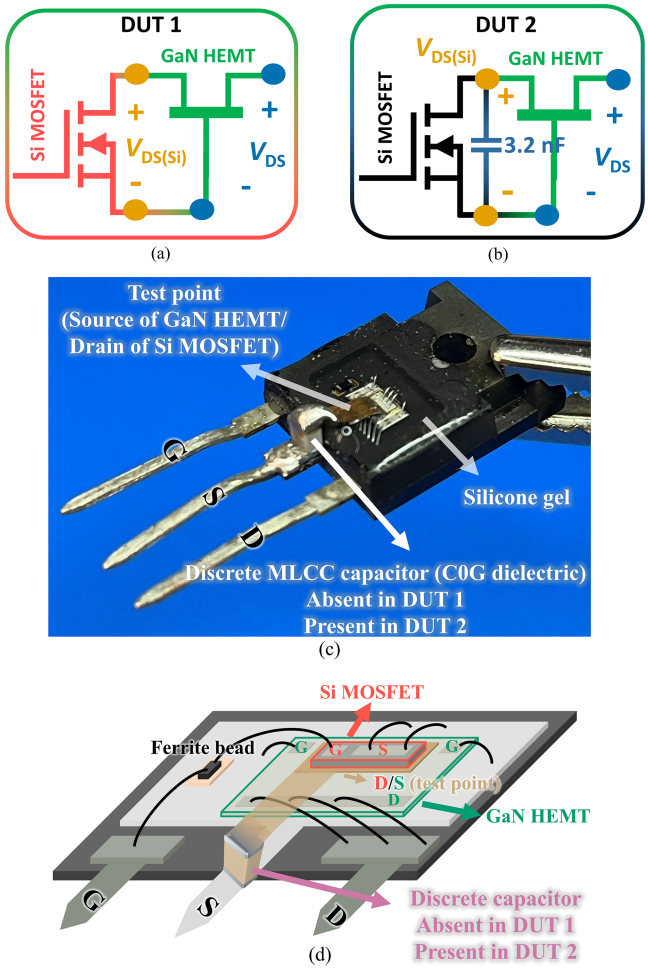

Fig. 4. Equivalent circuit models of (a) DUT 1 and (b) DUT 2. (c) Photo and (d) illustration of the corresponding components of the fabricated DUT 1/ DUT 2.

marked as DUT 1 [see Fig. 4(a)]. Its *I–V* and *C–V* characteristics are confirmed to be nearly identical to the packaged device. In addition, we assemble the other type of DUT, the DUT 2, which comprises an extra capacitor (3.2 nF) connected in parallel with the Si MOSFET [see Fig. 4(b)]. The photo of DUT 1/DUT 2 and their three-dimensional (3-D) schematics are shown in Fig. 4(c) and (d), respectively. The extra capacitor in DUT 2 is a discrete MLCC capacitor with C0G dielectric material, soldered between the Si MOSFET's drain (the added test point) and source (source lead of the cascode). The parasitic inductance and resistance of the test point along with the cap are nearly negligible with the magnitude being 2.4 nH and 16 mΩ, respectively, as measured by a Keysight E4990A impedance analyzer. This extra cap increases the effective C_{OSS} of Si MOSFET, lowers its shared voltage in switching, and prevents the Si avalanche [10].

Fig. 5(a)–(e) shows the major electrical characteristics of DUT 1 and DUT 2, revealing an increase of C_{OSS} mainly at V_{DS} below 22 V (i.e., before GaN HEMT is turned OFF), leading to a larger output capacitance charge (Q_{OSS}) (~60% increase at 400 V) and output capacitance stored energy (E_{OSS}) (13% increase at 400 V). The threshold voltage (V_{TH}) and on-resistance (R_{ON}) show a minimal shift.

Despite the limited changes in static characteristics, the measured E_{DISS} of DUT 2 is significantly lower than DUT 1, particularly at high $V_{DS(peak)}$. As shown in Fig. 5(f), the E_{DISS} of DUT 2 is only 25% of that of DUT 1 at $V_{DS(peak)}$ of 650 V. A natural thought is to attribute this E_{DISS} difference to the elimination of the Si avalanche energy [E_{AVA}(Si)] in DUT 2. To examine this hypothesis, we employ the $V_{DS(Si)}$ waveform obtained at the test point and the analytical model reported in [11] to extract the total avalanche charge in Si MOSFET (Q_{AVA}) and further calculate E_{AVA}(Si) (= Q_{AVA}·BV_{Si}, BV_{Si} is the Si MOSFET's avalanche breakdown voltage). As shown in Fig. 5(f), the E_{DISS} difference between the two DUTs is larger than E_{AVA}(Si), and the difference increases with $V_{DS(peak)}$. This suggests an additional loss in DUT 1, which will be analyzed in Section III.

III. Physical Origins and Loss Breakdown

As shown in Fig. 6, stage II of the UIS waveforms for DUT 1 and DUT 2 are scrutinized under various phases, with the equivalent circuit model and internal dynamics within the cascode illustrated in Fig. 7 for these phases.

For *DUT 1*, stage II can be divided into six phases following the sequence shown in Fig. 7(a)–(f). The equivalent C_{OSS} and internal dynamics can be categorized into four scenarios.

a) *Si-OFF GaN-ON* (phases 1 and 6): The Si MOSFET is turned OFF. V_{DS} of the Si MOSFET builds up but below the GaN HEMT's $|V_{TH}|$ (V_{TH_GaN}) (~17 V). As shown in Fig. 7(a) (DUT turn-OFF) and (f) (DUT reverse turn-ON), the equivalent C_{OSS} of the cascode HEMT for phases 1 and 6 (C_{OSS_1}) are given by

$$C_{OSS\_1} = C_{GS\_GaN} + C_{GD\_Si} + C_{DS\_Si} + C_{GD\_GaN}. \quad (5)$$

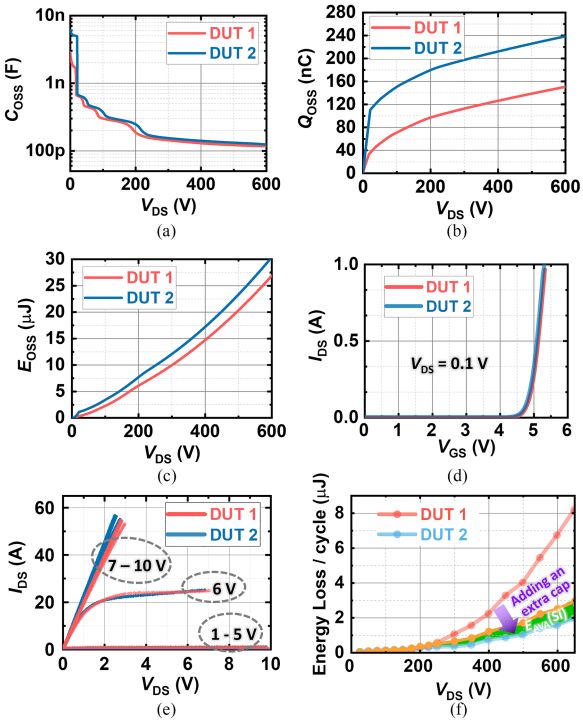

Fig. 5. (a) C_{OSS}-V_{DS}, (b) Q_{OSS}-V_{DS}, (c) E_{OSS}-V_{DS}, (d) transfer, and (e) output characteristics of DUT 1 and DUT 2. (f) Measured E_{DISS} of DUT 1 and DUT 2 in the UIS test, showing a difference larger than E_{AVA}(Si).

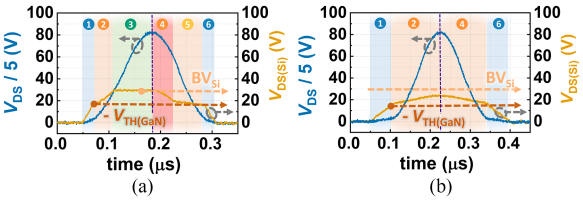

Fig. 6. Typical UIS waveforms of (a) DUT 1 and (b) DUT 2, and the illustration of different phases. The V_{TH} of GaN HEMT is also marked.

b) *Si-OFF GaN-OFF* (phases 2 and 4): Both Si MOSFET and GaN HEMT are OFF, with the C_{OSS} of both devices being charged or discharged simultaneously. An *L*–*C* resonance occurs between L_{load} and the cascode HEMT's C_{OSS}. As shown in Fig. 7(b) (part of the charging period) and (d) (part of the discharging period), the cascode HEMT's C_{OSS} in this scenario (C_{OSS_2}) can be written as

$$C_{OSS\_2} = \frac{C_{DS\_GaN}\ (C_{GS\_GaN} + C_{DS\_Si} + C_{GD\_Si})}{C_{DS\_GaN} + C_{GS\_GaN} + C_{DS\_Si} + C_{GD\_Si}} + C_{GD\_GaN}. \quad (6)$$

c) *Si-AVA GaN-OFF* (phase 3): When the DUT's V_{DS} exceeds ~150 V, the Si MOSFET avalanches and $V_{DS(Si)}$ clamps at BV_{Si} = 30 V [see Fig. 6(a)]. The resonance is no longer lossless but accompanied by the resistive energy loss in the Si avalanche. While Q_{AVA} is dissipated in Si MOSFET via an avalanche, the same amount of charge is charged to C_{DS_GaN}. This phase lasts until the DUT's V_{DS} reaches $V_{DS(peak)}$, at which moment I_{DS} reduces to zero.

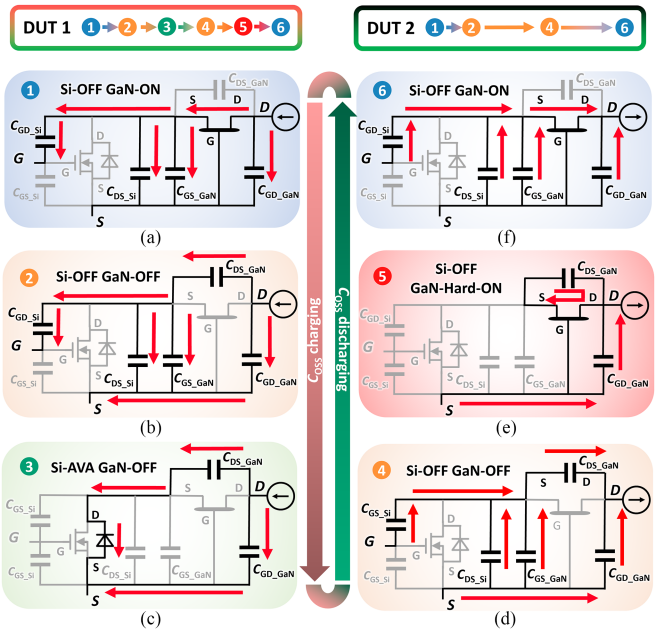

Fig. 7 Equivalent circuits of six distinct phases of DUT 1 and DUT 2 in stage II. (a)–(c) C_{OSS} charging, and (d)–(f) are C_{OSS} discharging.

As shown in Fig. 7(c), the DUT's C_{OSS} (C_{OSS_3}) equals to the GaN HEMT's C_{OSS}

$$C_{OSS\_3} = C_{OSS\_GaN} = C_{DS\_GaN} + C_{GD\_GaN} \quad (7)$$

$$E_{AVA}\ (\text{Si}) = \text{BV}_{\text{Si}}\ Q_{AVA} \quad (8)$$

Note that Q_{AVA} can be calculated using the model in [11].

d) *Si-OFF GaN-Hard-ON* (phase 5): After phase 4, when $V_{DS(Si)}$ drops to the GaN HEMT's $|V_{TH}|$. The GaN HEMT starts to turn ON and the energy stored in C_{DS_GaN}, E(GaN_HO), is dissipated through the GaN HEMT channel, similar to a hard turn-ON process. Note that, in phase 5, the Si avalanche is absent as the polarity of I_{DS} has been inverted. As shown in Fig. 7(e), the DUT's C_{OSS} (C_{OSS_4}) and E(GaN_HO) are

$$C_{OSS\_4} = C_{DS\_GaN} + C_{GD\_GaN} \quad (9)$$

$$E\ (\text{GaN\_HO}) = \int 0.5\ C_{DS\_GaN}\ (V_{DS})\ V_{DS}\ dV_{DS} \quad (10)$$

where (10) is integrated from zero V_{DS} up to the V_{DS} value at the start point of GaN hard turn-ON (V_{GaN_HO}). To calculate E(GaN_HO), C_{DS_GaN} is measured on a Keysight B1505A power device analyzer, showing little dependence on V_{DS} [see Fig. 8(a)]. V_{GaN_HO} is directly extracted from the experimental UIS waveform, as illustrated in Fig. 8(b). Since C_{DS_GaN} shows little dependence on V_{DS}, (10) can be simplified as

$$E\ (\text{GaN\_HO}) = 0.5\ C_{DS\_GaN}\ V_{GaN\_HO}^2. \quad (11)$$

For DUT 2, due to the absence of Si avalanche, the charging and discharging process is symmetrical; phase 3 and phase 5 are eliminated [see Fig. 6(b)]. Hence, energy losses from Si avalanche and GaN hard turn-ON are saved. In the resonance of DUT 2, the only loss is the intrinsic E_{DISS} of the GaN HEMT

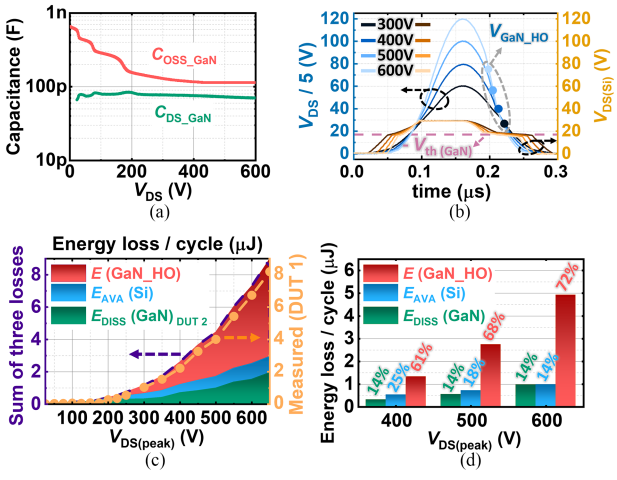

Fig. 8 (a) Measured C–V characteristics of the GaN HEMT. (b) Extraction of $V_{\mathrm{GaN\_HO}}$ from the UIS waveforms of DUT 1 with $V_{\mathrm{DS(peak)}}$ of 300–600 V. (c) Three types of losses in E_{DISS} of cascode GaN HEMT and measured E_{DISS} of DUT 1 as a function of $V_{\mathrm{DS(peak)}}$. (d) Comparison of E_{DISS} loss breakdown at $V_{\mathrm{DS(peak)}}$ of 400 to 600 V.

within the cascode (E_{DISS}(GaN)). Note that the E_{DISS} of Si MOSFET is negligible. As the E_{DISS} of GaN HEMTs primarily depends on f_{R} and $V_{\mathrm{DS(peak)}}$ [3], [5], considering the GaN HEMTs in DUT 1 and DUT 2 see identical $V_{\mathrm{DS(peak)}}$ and similar f_{R}, the measured E_{DISS} of DUT 2 can be used to approximate the E_{DISS}(GaN) in DUT 1.

Now three loss components in DUT 1 have all been extracted experimentally. E_{AVA}(Si) and E(GaN_HO) are calculated by (8) and (11) using experimental waveforms, and E_{DISS}(GaN) is approximated by the measured E_{DISS} of DUT 2. As shown in Fig. 8(c), the sum of these three losses shows a general consistency with the measured E_{DISS} of DUT 1 at various $V_{\mathrm{DS(peak)}}$, suggesting they have accounted for major losses of the cascode E_{DISS}. At high $V_{\mathrm{DS(peak)}}$, the sum is slightly larger than the measured E_{DISS} of DUT 1 (difference within 12%). This is because the GaN's C_{OSS} in DUT 1 does not experience a full cycle of charging and discharging due to GaN's early turn-ON in phase 5. Hence, the E_{DISS} of DUT 2 slightly overestimates the E_{DISS}(GaN) in DUT 1.

Fig. 8(d) shows the loss breakdown of E_{DISS} of the DUT at V_{DS} of 400 to 600 V, revealing that E(GaN_HO) becomes increasingly dominant at the higher $V_{\mathrm{DS(peak)}}$, e.g., accounting for 72% of E_{DISS} at the $V_{\mathrm{DS(peak)}}$ of 600 V. Also, compared to the other two losses, E(GaN_HO) grows much faster with $V_{\mathrm{DS(peak)}}$, which explains the stronger $V_{\mathrm{DS(peak)}}$ dependence of the cascode E_{DISS} that has been widely reported. Finally, to assist device users in applications, the E_{DISS} (in μJ) of DUT 1 and DUT 2 are fitted by a power law to capture their $V_{\mathrm{DS(peak)}}$ (in V) dependence

$$E_{\mathrm{DISS}}\,(\mathrm{DUT\ 1}) = 2.15 \cdot 10^{-13}\, V_{\mathrm{DS(peak)}}^{2.70} \tag{12}$$

$$E_{\mathrm{DISS}}\,(\mathrm{DUT\ 2}) = 3.26 \cdot 10^{-12}\, V_{\mathrm{DS(peak)}}^{2.04}. \tag{13}$$

IV. Design of Avalanche-Free Cascode GaN HEMT

The loss breakdown provides useful guidelines for deploying cascode GaN HEMTs in high-frequency, soft-switching applications. It is revealed that by adding a capacitor in parallel with Si MOSFET (i.e., DUT 2), the E_{DISS} of cascode GaN HEMTs can be significantly reduced, e.g., by up to 75% at $V_{\mathrm{DS(peak)}}$ of 400 V [see Fig. 5(f)]. The prices are an increase in Q_{OSS} and a consequentially increased switch time to charge/discharge the cascode's C_{OSS}. For example, as shown in Fig. 6(a) and (b), the resonance period increases from 0.55 to 0.7 μs. This increased (dis-)charging time could possibly limit the switching frequency. This tradeoff between switching loss and switching time needs to be considered when upscaling the switching frequency of cascode HEMTs. As long as the prolonged transition time does not limit the frequency, it will be beneficial to increase the Si MOSFET's C_{OSS} for reducing the cascode's loss in high-frequency, soft-switching applications.

The discussion above suggests the effective C_{OSS} of the Si MOSFET ($C_{\mathrm{OSS\_Si}}$) to be an important design consideration for cascode GaN HEMT in soft-switching applications. The $C_{\mathrm{OSS\_Si}}$ can be tuned by either paralleling a capacitor (C_{ext}) with the off-the-shelf Si MOSFET (like this article) or designing a customized Si MOSFET. From the analysis above, the increased $C_{\mathrm{OSS\_Si}}$ will suppress the Si avalanche at the price of a longer transition time of the cascode. Hence, for a given GaN HEMT, the recommended $C_{\mathrm{OSS\_Si}}$ is to just eliminate the avalanche at the cascode's peak V_{DS} ($V_{\mathrm{DS\_PK}}$).

According to the circuit analysis in phases 2 and 3, the voltage drop across the Si MOSFET should be lower than BV_{Si}

$$\frac{C_{\mathrm{DS\_GaN}}\left(V_{\mathrm{DS\_PK}} - |V_{\mathrm{TH\_GaN}}|\right)}{C_{\mathrm{DS\_GaN}} + C_{\mathrm{GS\_GaN}} + C_{\mathrm{OSS\_Si}}} + |V_{\mathrm{TH\_GaN}}| \le \mathrm{BV_{Si}}. \tag{14}$$

This gives the minimum $C_{\mathrm{OSS\_Si}}$ for avalanche-free cascode

$$C_{\mathrm{OSS\_Si}} \ge \left(\frac{V_{\mathrm{DS\_PK}} - |V_{\mathrm{TH\_GaN}}|}{\mathrm{BV_{Si}} - |V_{\mathrm{TH\_GaN}}|} - 1\right) C_{\mathrm{DS\_GaN}} - C_{\mathrm{GS\_GaN}}. \tag{15}$$

As an example, for the cascode studied in this article, if $V_{\mathrm{DS\_PK}}$ equals 400 V (bus voltage), $C_{\mathrm{OSS\_Si}}$ should be at least 2 nF to enable an avalanche-free cascode.

As shown in Fig. 5(a)–(c), the major adverse effect of a larger $C_{\mathrm{OSS\_Si}}$ is the increased Q_{OSS} of the cascode. In soft-switching, this increased Q_{OSS} may not induce additional loss but will prolong the total switching time. Although the increased time is dependent on many circuit parameters, the increased Q_{OSS} is more device intrinsic and can be estimated quantitatively.

Take the addition of C_{ext} as an example. It will increase the cascode's C_{OSS} across the entire V_{DS} range. Whereas, as shown in Fig. 5(a), such an increase is more pronounced in the low voltage range when the GaN HEMT is still ON. This is because, after the GaN HEMT is OFF, the cascode's C_{OSS} could be impacted more by the GaN HEMT than the Si MOSFET. Hence, the increased Q_{OSS} due to C_{ext} can be approximated by

$$\Delta Q_{\mathrm{OSS}} \approx C_{\mathrm{ext}}\ |V_{\mathrm{TH\_GaN}}|\,. \tag{16}$$

For the DUT in this article, the ΔQ_{OSS} calculated from (16) is 71 nC, while the ΔQ_{OSS} from the complete C–V integral

(see Fig. 5(a)) is 80 nC, revealing that the low-voltage range contributes to over 89% of the total ΔQ_{OSS}.

Equation (16) also suggests that the ΔQ_{OSS} can be reduced by selecting a GaN HEMT with a less negative $V_{\mathrm{TH\_GaN}}$. In general, for soft-switching applications, the selection of a larger $C_{\mathrm{OSS\_Si}}$, a high $\mathrm{BV_{Si}}$, a smaller $C_{\mathrm{DS\_GaN}}$, and a less negative $V_{\mathrm{TH\_GaN}}$ could all reduce the switching loss while minimizing the increased Q_{OSS} and charging/discharging time ("dead time").

Finally, it should be noted that the above design guidelines for cascode GaN HEMTs may not apply to hard-switching applications, as the hard-switching loss is directly related to Q_{OSS} and switching transition time. The reduction of loss due to the elimination of the Si avalanche may not make up for the added loss due to the longer switching time. A more detailed analysis is needed in future work.

V. Conclusion

In summary, this article, for the first time, experimentally unveils and quantifies the physical origins of the E_{DISS} in cascode GaN HEMTs. Three loss components, the Si avalanche loss, GaN HEMT's E_{DISS}, and the Si avalanche-induced GaN turn-ON loss, are extracted at various $V_{\mathrm{DS(peak)}}$. These results address the long gap regarding the large E_{DISS} in cascode GaN HEMTs and provide key guidelines for their high-frequency, soft-switching applications. In such applications, the E_{DISS} of cascode GaN HEMTs can be significantly reduced by enlarging the C_{OSS} of Si MOSFET and eliminating the Si MOSFET avalanche.

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