High Cycle Fatigue Testing of Silicon IGBT Devices Under Application-Close Conditions

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***Abstract*—To speed up the testing time in a power cycling test, normally high-acceleration factors induced by high temperature swings are applied. With a classical Coffin–Manson lifetime approach, the induced fatigue can be modeled. This work uses test conditions at the transition between the elastic and plastic deformation zones. Testing the high cycle fatigue zone requires evolved equipment, so active power cycling with switching losses is implemented. It was found that for high junction temperatures ($T_{\mathrm{vj,max}} = 150\,^{\circ}$C), a transition between the plastic and the elastic zones could not be detected down to $\Delta T = 18$ K. However, for reduced junction temperatures ($T_{\mathrm{vj,max}} = 115\,^{\circ}$C), the start of the elastic zone was found at around $\Delta T < 29$ K. The main failure mechanism was found to be chip solder fatigue in the center of the solder layer. The experimental data are transferred into a 3-D simulation environment to further investigate the failure mode. With the findings, a lifetime model is described and applied, which predicts, depending on conditions, lifetime benefits up to 268% compared with a standard lifetime approach.**

***Index Terms*—High cycle fatigue (HCF), insulated gate bipolar transistor (IGBT), lifetime estimation, power cycling, reliability.**

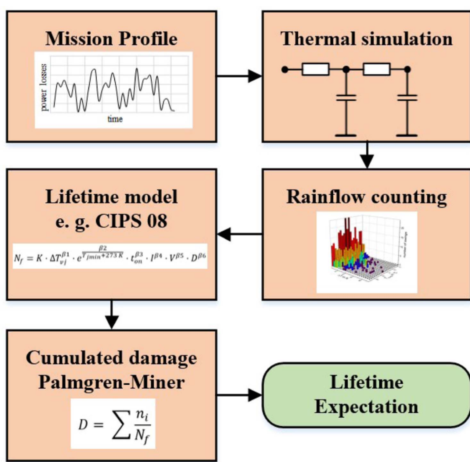

Fig. 1. Possible algorithm used for analyzing the estimated lifetime of a power device according to [4].

I. Introduction

In PAST years, the requirements of power semiconductor devices are increasingly rising: high power density, higher operating temperatures, and also increasing reliability. Power cycling reliability is an important point for the overall system reliability. Caused by the coefficient of thermal expansion (CTE) mismatch and different temperatures for the layers in the power device, fatigue stress cannot be avoided. Hence, sufficient reliability is required to guarantee faultless 20 or more years of service. Not only a reinforced package design but also a suitable power rating is important. To calculate the expected reliability of a power device in the application, the load profile and the cooling performance is used to estimate the number of thermal swings. A possible workflow is shown in Fig. 1.

The known mission profile can be transferred into a simulation environment. The tool allows us to analyze the number and amplitudes of the thermal swings which occur. The rainflow method has been established to calculate the number of fatigue cycles. After analyzing the amount of different thermal swings, the lifetime is calculated with a lifetime model and the Palmgren–Miner [1], [2] rule is usually applied to estimate the accumulated fatigue of the power electronic device. Different optimizations can be further implemented to achieve higher accuracy, e.g., additional finite element method (FEM) analysis or the implementation of 3-D-thermal networks [3].

A crucial point in this analysis is the applied lifetime model. This article studies the applicability of a standard lifetime model, such as the CIPS 08 model [5], to application-close conditions. Limitations of lifetime models are discussed on the basis of experimental results and optimizations, which are implemented in Section IV.

II. Elastic–Plastic Transition Zone

The lifetime of power electronic packages can be described by different lifetime models. They can be categorized into stress-based, crack growth-based, strain-based, and empirical models.

Stress-based models are based on the mechanical stress σ. The models are suitable for isothermal conditions and geometries where no stress peaks occur and the stress is constant [6]. The temperature gradients in power electronic packages and the variable load, especially when reaching end-of-life, make them less suitable in a power cycling environment.

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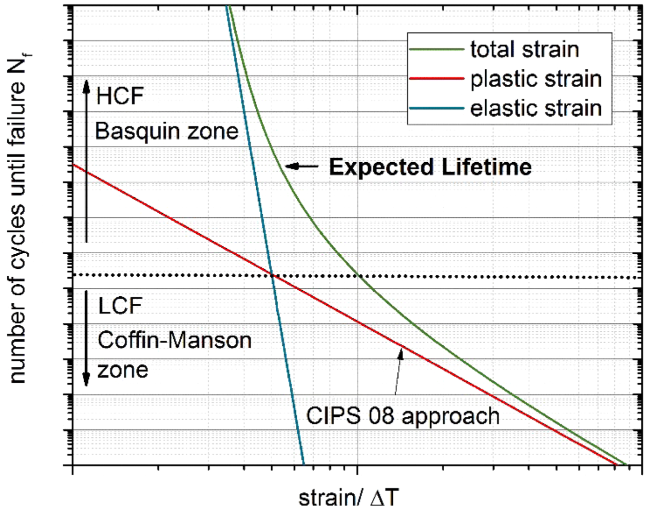

Fig. 2. Strain-life model separated in two segments: LCF with high-acceleration factors described by a Coffin–Manson term and HCF zone described by a Basquin term adapted from [10].

A second large group of models is based on crack initiation and crack growth. The most common one is the Paris–Erdogan law [7], which was found suitable to describe solder layer cracks, see Darveaux [8]. The model is quite suitable to describe crack growth also during power cycling [9]. In the failure analysis, in Section V of this work, it can be observed that for the performed tests, no clear single crack forms, which makes the model unsuitable for this work.

The strain-based models are more flexible than the models discussed before. They are based on the mechanical strain $\varepsilon_{\text{total}}$ induced by thermal expansion. They are also valid when temperature gradients are present, which makes them suited for power cycling. However, strain life models are more complex. The total strain $\varepsilon_{\text{total}}$ can be calculated by the sum of elastic and plastic strains

$$\varepsilon_{\text{total}} = \varepsilon_{\text{el}} + \varepsilon_{\text{pl}}. \tag{1}$$

The elastic strain ε_{el} is dominant for low elongations while the plastic strain ε_{pl} is dominant for high strain values. These two regions are described by different approaches, as shown in Fig. 2. Power cycling conditions with high ΔT and high plastic strain ε_{pl} can be found on the right-hand side in the low cycle fatigue zone (LCF). High cycle fatigue zone (HCF) on the left-hand side is dominated by elastic strain ε_{el}. A large temperature swing ΔT during power cycling is inducing a high amount of the plastic strain, which leads to a lower number of power cycles until failure. In contrast, under application conditions, most of the temperature ripples are low, respectively, and the strain is mainly induced as the elastic portion. A drawback of the model is the determination of the strain, which must be done by simulation. This requires a digital model and accurate material models, which are often hard to obtain.

A fourth large group of lifetime models are the empirically based ones, which require a high number of experimental power cycling results in the LCF zone. The advantage of empirical lifetime models is the use of parameters, which can be directly gained by the power cycling experiment and no additional simulation is required to determine mechanical stress or strain values. Several different models exist starting with the Lesit model [11] for modules, the model from Scheuermann et al. [12], or the model from Zeng et al. [13] for discrete devices. The most common model with the highest set of parameters is the CIPS 08 model [5]. Equation (1) gives the lifetime model as follows:

$$N_f = K \cdot \Delta T_{\text{vj}}^{\beta 1} \cdot \exp\left(\frac{\beta 2}{273 + T_{\text{vj,min}}}\right) \cdot t_{\text{on}}^{\beta 3} \cdot I^{\beta 4} \cdot V^{\beta 5} \cdot D^{\beta 6}. \tag{2}$$

Temperature swing ΔT_{vj}, minimum junction temperature $T_{\text{vj,min}}$, ON-time t_{on}, and load current I are the test parameters. The voltage class V divided by 100 and the bond wire diameter D are both geometrical parameters. The remaining parameters are fitting parameters, such as the base lifetime K [14], and the exponents $\beta 1$–$\beta 6$ also taken from [5]. For evaluating the lifetime in a lab environment, high-acceleration factors are used. Hence, the ΔT_{vj} dependency is modeled with a strain-based Coffin–Manson approach [15], [16], which is also shown in Fig. 2.

According to the theory, as described for the strain-based models, there is a transition from LCF to HCF, in which the number of possible cycles rises rapidly. This increasing trend for power electronic devices was first identified in [17] and described in more detail in [18] and [19]. Also different semiconductor device manufacturers indicate increasing lifetime for small temperature swings [20], [21]. Large power cycling surveys show that most tests apply temperature swings between 50 and 150 K. For swings below <50 K, the results are rare and below 30 K and no results were available before 2019 [22], [23].

This white spot of lifetime results is caused by the long runtime of a standard test. A test with 2-s cycle time and an expected number of cycles until end of life of 500M cycles would result in a testing time of 32 years. It is obvious that standard equipment and test strategies reach their limitations. Due to the expected high number of power cycling swings, the ON-time is highly reduced in the millisecond range to speed up the cycle count. A drawback when testing with short pulses < 100 ms is usually that the load current can be much higher than the rated current. This problem leads to accelerated aging of the bond interconnection and lifetime results are to be taken with care. Therefore, a special advanced power cycling method is applied to investigate the lifetime of power devices tested in this white spot area. This is the first possible strategy to allow the same measurement methods like in standard dc power cycling while enabling short ON-times without overstressing the bond interconnections by higher current than rated current.

III. Advanced Power Cycling Methods

Advanced power cycling methods have to be used to get comparable lifetime data in the elastic–plastic transition range. With this kind of test, conduction and switching losses can be adjusted to gain high temperature swings without using a

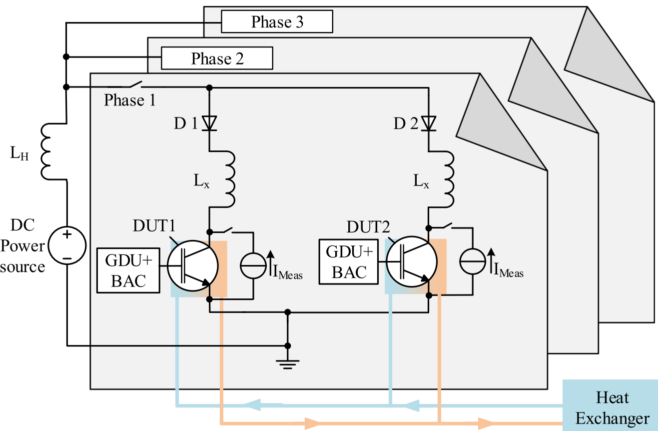

Fig. 3. Example schematic circuit of a possible advanced power cycling tester with an adjustable portion of switching and conduction losses.

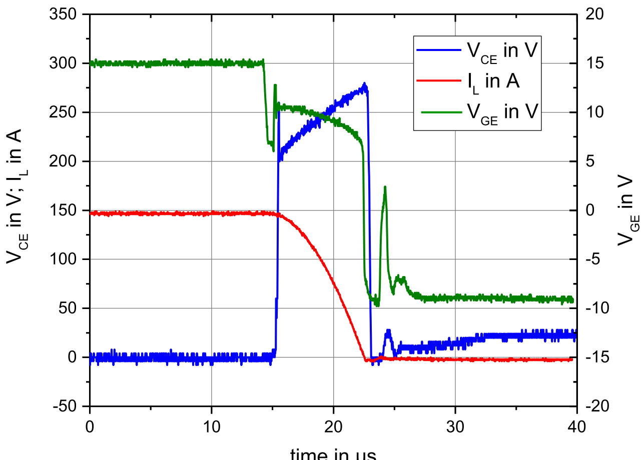

Fig. 4. Single clamped turn-OFF for the IGBT under test for a load current of 150 A and a clamping voltage of 250 V from [26].

nonapplicational current value. Fig. 3 shows a schematic circuit for an advanced power cycling test with switching losses.

In order to achieve switching losses, a parasitic inductance L_x is placed in series to the device under test. The load current is switched with a frequency in the high kHz range between the legs. During turn-OFF, the additional inductance causes a voltage peak and, thus, significant switching losses [24]. As the inductive voltage peak should not exceed the breakdown voltage of the device under test, a clamping circuit boosted active clamping (BAC) has to provide an upper voltage limit. Fig. 4 shows the clamped turn-OFF leading to switching losses. Depending on load current and switching frequency, the portions between switching and conduction losses can be adjusted [25].

The load current as well as the switching frequency of the devices under test (DUT 1, DUT 2) can adjust the ratio of switching losses. When dimensioning the parasitic inductance L_x, it is necessary to ensure that the imprinted losses during the turn-OFF process do not cause significant heating in the device. In the tests, a smaller stray inductance with temperature ripples < 0.5 K has been prevailed. With the lower inductance, the impact on lifetime calculation can be neglected and the losses can be easily adjusted with the switching frequency. Two devices with switching and conduction losses can be tested per phase. Thus, for three phases, up to six devices are tested, which is the minimum requirement according to AQG 324 [27]. The test strategy has been considered as comparable to the standard testing procedure in several previous investigations [24], [28], [29], when the failure mode is solder fatigue and bond wire lift-off. Also, the temperature determination with the established $V_{\text{CE}}(T)$ method is applied, using the p-n-junction as temperature sensor [30]. Due to the short cycle time in the millisecond regime (see Table II), a deviation between an area weighted average and the determined temperature by the $V_{\text{CE}}(T)$ method can be possible; however, it allows the extension of results gained with the established method.

IV. Experimental Testing

A total of five power cycling tests were performed in the elastic–plastic deformation regime. As device under test, an Econo pack (FS150R12KT4) with standard packaging technology was used. The package is rated for 1.2 kV and 150 A, which is selected as the test current. The insulated gate bipolar transistors (IGBTs) are packaged with Al-bond wires, tin-based solder, Al_2O_3 ceramic, and Cu baseplate. The module is encapsulated using soft gel. It contains a full three-phase inverter but only a single switch is tested in power cycling at a time.

The investigation starts with relatively high temperature swings $\sim$55 K and is lowering the swing for each test down to $\Delta T =$ 18–19 K. All tests are performed with an ON-time of 10 ms and a t_{off} of 20 ms. The detailed test parameters are listed in Table I.

In power cycling, the measured maximum junction temperature is always lower due to the measurement delay ΔT_{md}. After turning OFF the load current and measuring the junction temperature with a lower measurement current used for the $V_{\text{CE}}(T)$ method, the carriers in the p-n-junction need a certain time for recombination [31], such as in standard power cycling. For the test series, a delay time of 200 μs could be achieved. Different techniques, such the square-root-(t) method [32] or FEM simulation, can be applied to correct the experimental data. Other authors found that the square-root-(t) method is not suitable for IGBT devices [33]; therefore, the correction is made with FEM simulation (for more details, see Section VI). It was found that under the used conditions, the error is linear in dependency of the temperature swing ΔT and is corrected with (3) [26]

$$\Delta\, T_{\text{md}} = 0.114 \cdot \Delta T. \tag{3}$$

The failure mode for the devices is mixed. The failure mode in the standard dc-test is bond wire lift-off, similar to test 1 with $\Delta T = 55$ K, and a V_{CE} increase at load current of $+5\%$ is detected. However, the failure mode changes for decreasing temperature swings into solder fatigue, respectively, with an increase of $+20\%$ thermal resistance $\underline{R}$th. For swings smaller $<$30 K, the increase in Rth is the only failure mechanism.

TABLE I
TEST PLAN FOR THE FIVE POWER CYCLING TESTS WITH $T_{\rm ON} = 10$ MS AND $T_{\rm OFF} = 20$ MS WITH MEASUREMENT DELAY CORRECTED TEMPERATURE DATA AND A STANDARD REFERENCE TEST IN THE LCF RANGE (DC-TEST WITH $T_{\rm ON} = T_{\rm OFF} = 1$ S)

Name	**Temp. swing**	**Maximum junction temp.**	**Ratio of switching losses**	**Switching frequency**	**Load current**	**Losses per area**
	ΔT in K	T_{vjmax} in °C	in %	f in kHz	I_L in A	P_v/A in W/mm²
DC-Test	80	150	0	0	150	2.88
Test 1	50–55	175*	78	13.7	150	11.7
Test 2	32–33	150	66	9.6	150	6.18
Test 3	26–28	150	58	7.1	150	4.88
Test 4 a	18–19	150	26	4.2	150	3.31
Test 4 b	30	150	64	9.1	150	6.14
Test 5	28–29	115	56	7.6	150	4.34

* The cooling performance of the heat exchanger was not sufficient to realize a junction temperature of 150 °C.

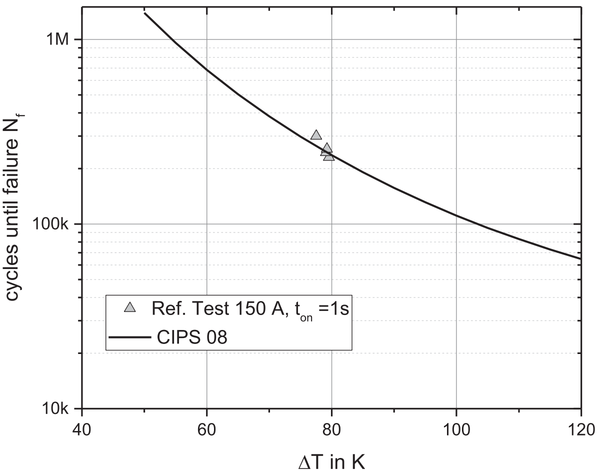

Fig. 5. Lifetime results for the reference test with Si-IGBTs $t_{\rm on} = 1$ s and $T_{\rm vj,max} = 150$ °C for standard dc power cycling without switching losses.

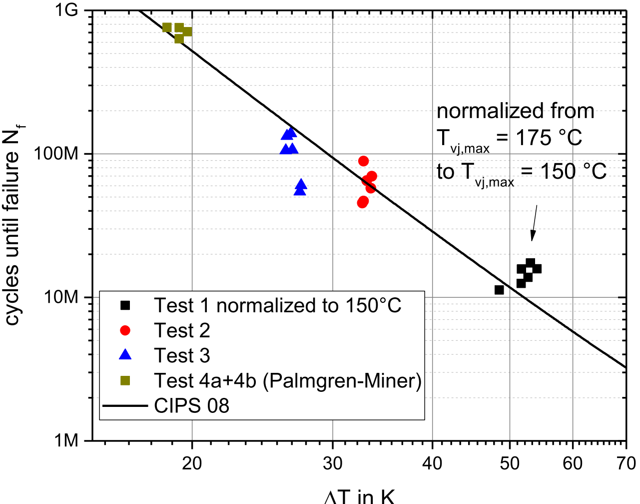

Fig. 6. Results of tests 1–4 with high max. Junction temperature $T_{\rm vj,max} = 150$ °C with CIPS 08 expectation as the reference line. The results in test 4 are determined with Palmgren–Miner (4).

First, the results for a standard LCF power cycling test (dc-test) with only conduction losses are shown in Fig. 5. The results are in good agreement with the CIPS 08 expectation.

In Fig. 6, the lifetime data for tests 1–4 are displayed in a double logarithmic diagram. The Coffin–Manson-based CIPS 08 approach is a linear function in this plot printed in black as reference line. All test data are close to this lifetime model, which confirms the validity of the experimental testing approach in the ms-regime. No exponential increase in lifetime for low temperature swings down to $\Delta T \approx 18$ K can be observed. Since the maximum junction temperature was kept constant at $T_{\rm vj,max} = 150$ °C and the failure mode is shifted to the chip solder layer, it is expected that the high average temperature of the system weakens the mechanical stability of the solder material and, therefore, allows major parts of the plastic strain to develop.

To speed up testing for very low temperature swings, test 4 is separated into two parts. At first the modules were predamaged with the target temperature swing of 18–19 K in test 4a. After a certain number of power cycles in test (198 million), the conditions were changed to a $\Delta T \approx 30$ K (test 4b) to speed up end-of-life testing. End-of-life was achieved after additional 72 million cycles. For calculation, the Palmgren–Miner rule in (4) is used for the final cycles until failure.

$$D = \sum \frac{n_i}{N_f}. \tag{4}$$

In (4), the number of cycles at a certain load step is $n_{\rm i}$, $N_{\rm f}$ is the total number of cycles, and D is the damage value. If $D > 1$, a failure can be stated. In [34], it was found that it can be applied for power cycling tests, but with some limitations. First, the failure mode has to be the same, which is expected in this work since for low ΔT, solder fatigue is the dominating failure. Second, the devices under test should not be suspected to extreme loads before testing small loads. This was implemented by testing the low ΔT regime first, followed by higher temperature swings. Investigating this effect, test 5 was set up with a reduced $T_{\rm vj,max}$ to 115 °C. The results of this test are shown in Fig. 7.

It can be observed that for reduced maximum junction temperature, the number of cycles until failure is significantly above the expectation. This indicates the elastic–plastic transition zone where the lifetime starts to increase steeply. The red lifetime curve, so-called CIPS modified model from [18], which takes

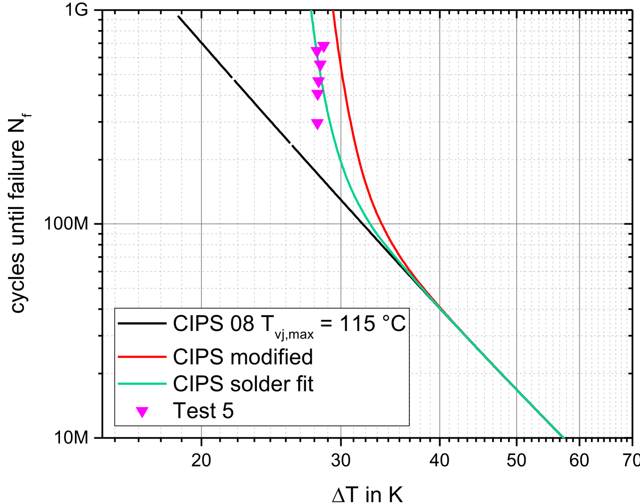

Fig. 7. Results of test 5 with decreased $T_{\mathrm{vj,max}}$ to 115 °C; plotted with different lifetime models CIPS 08, CIPS 08 modified, and a fitted version (solder fit) to the test data of test 5.

this effect into account by a variable $\beta 1$ parameter in (1), does not show a good agreement with the experimental data. The $\beta 1$ parameter in (1) is calculated according to

$$\beta 1' = \mathrm{e}^{-\frac{\Delta T_{\mathrm{vj}} - 27.1\ \mathrm{K}}{2.08\ K}} + \beta 1. \quad (5)$$

A major root cause for the deviation is the different failure mode. In the CIPS modified approach, it is bond wire lift-off, and the experiment in this work, as discussed previously, it is solder fatigue. Hence, new coefficients are fitted to the test data written in bold, leading to a solder fit for the results of this work in the following:

$$\beta 1' = \mathrm{e}^{-\frac{\Delta T_{\mathrm{vj}} - 26.2\ \mathrm{K}}{1.74\ K}} + \beta 1. \quad (6)$$

The confidence interval for the fit at $\Delta T = 28$ K for the parameter $\beta 1'$ is ± 0.219.

V. Failure Analysis

The failure analysis after test is important to understand the shift from bond wire degradation for higher temperature swings to solder fatigue for lower temperature swings. In a first step, the silicone gel was removed. With an optical microscope, the metallization surface was investigated.

Fig. 8 shows a chip tested in test 2. Strong aluminum modification in the center of the die and minor modification at the edge of the chip can be observed. All tested devices throughout the other tests show a similar pattern on the topside surface. In the simulation Section VI, the highest temperature, respectively, thermal strain rates occur in the center. Therefore, a more pronounced damage accumulation in the center region is expected, leading to a higher aluminum modification of the topside metallization compared with the edge region.

Scanning acoustic microscopy (SAM) images were made to investigate the state of health of the solder layer. The results are shown in Fig. 9. The tested chip solder layer in Fig. 9 shows strong degradation around the center gate. Especially for the tests with very long runtime, respectively, low $\Delta T < 35$ K, this phenomenon is very pronounced.

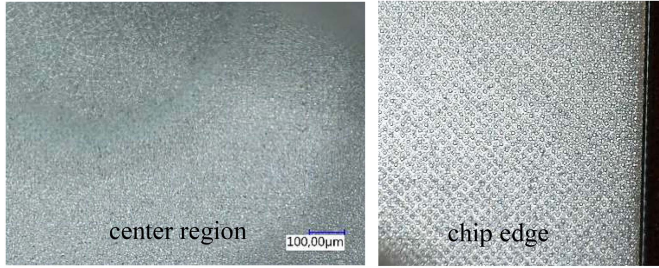

Fig. 8. Strong aluminum modification in the center region of the chip while in the edge of the die the cell structure is still visible.

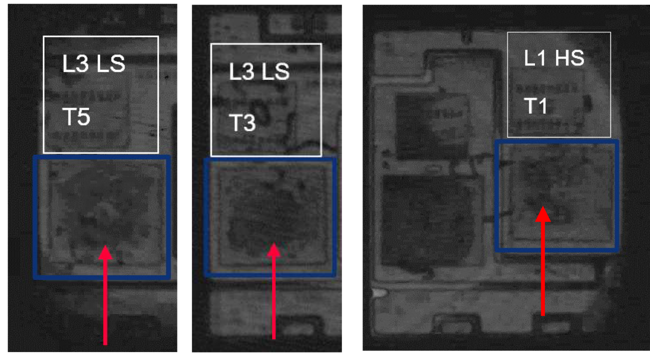

Fig. 9. Exemplary SAM images after end of life for tests 1, 3, and 5 with high damage in the center area of the device especially for lower ΔT.

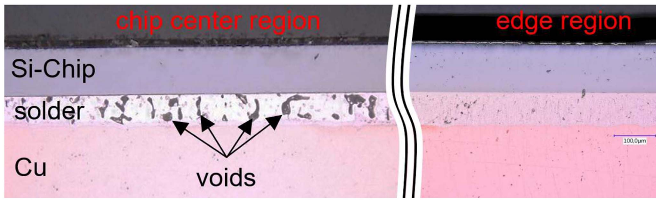

Fig. 10. End-of-life chip solder layer close to the center of the chip with a high number of larger voids developed in the solder.

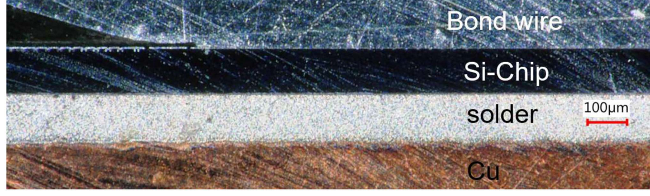

Fig. 11. Untested reference chip (center) with intact solder layer similar to Fig. 10 in the edge region.

For further analysis of the solder layer, a cross section of the failed devices is performed. Figs. 10 and 11 show the solder layer of the same chip. While the part close to the center (see Fig. 10) shows a large number of voids, which developed during the test, the solder at the edge of the chip is still intact and does not show any crack formation. This is in contrast to the failure

TABLE II
LAYER DESCRIPTION AND PACKAGED MATERIALS FOR MECHANICAL MODELING

Layer	Material	Thickness
bond wire	aluminum	Ø 400 µm
metallization	aluminum	4 µm
chip	silicon	120 µm
chip solder	Sn96Ag3.5Cu0.5	50 µm
DCB top	copper	300 µm
ceramic	Al_2O_3	381 µm
DCB bottom	copper	300 µm
system solder	Sn96Ag3.5Cu0.5	75 µm
baseplate	copper	3 mm
TIM	Dow corning 340	75 µm
heat sink	copper	8 mm

TABLE III
PROPERTIES SUCH AS THERMAL CONDUCTIVITY (TH. COND.), SPECIFIC HEAT, CTE, AND YOUNG'S MODULUS ARE NONLINEAR

	Al	Al_2O_3	Cu	SAC_{305}	Si	TIM
density [kg/m³]	2710	3800	8960	7490	2330	2100
Th. cond. [W/mK]	239	23	394	58	101	0.67
Spec. heat [J/K]	948	302	405	232	790	100
CTE [ppm/K]	24	4	18	21	4	---*
Poisson coef.	0.35	0.22	0.35	0.31	0.28	---*
Youngs mo. [GPa]	62	345	110	25	169	---*

* Not used in mechanical domain.
An excerpt at T = 150 °C.

pattern often observed in standard power cycling tests, where the damage is starting at the edge of the solder layer, forming a crack, which propagates toward the center. In [20] and [35], tests with short ON-times were also conducted causing the same failure mechanism as observed in this experiment.

VI. 3-D SIMULATION

A 3-D simulation was performed for deeper analysis. On the one hand, the temperature error was corrected by the simulation data. On the other hand, the strain in the device is investigated to further analyze the failure mode. The material composition and the thickness of the layers are given in Table II.

Table III lists the material with its properties at the target temperature of 150 °C. Most material models are deposited as nonlinear models in the simulator. The most important material model is the one for the chip solder layer, since the experiment revealed that die attach layer as main failure location for low temperature swings. This is additionally displayed in Fig. 12. In [36], it is observed that for fast ON-times, the elastic–plastic deformation is dominant and the creep fatigue is less pronounced. Hence, a nonlinear stress–strain model is used in this work to simulate the fatigue also to save computation time.

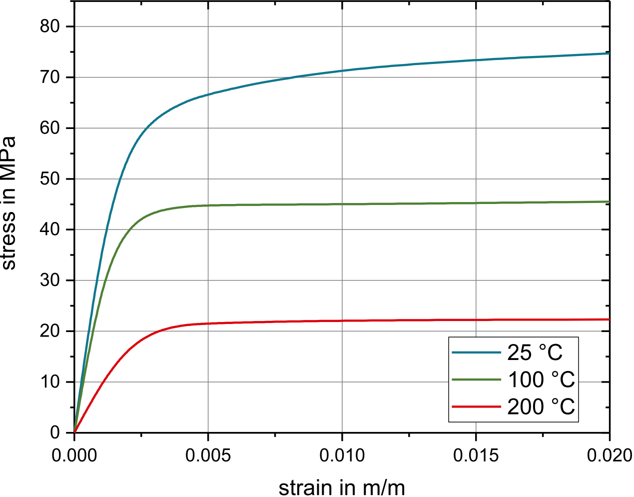

Fig. 12. Nonlinear temperature-dependent stress–strain curve for SAC305 solder from [37].

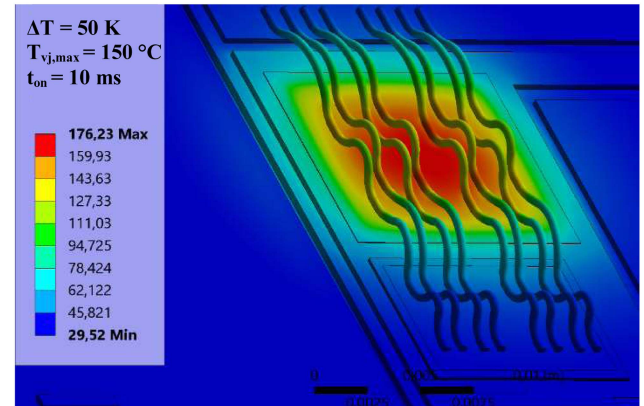

Fig. 13. Temperature distribution of the active IGBT chip for $\Delta T = 50$ K.

In a first step, a transient thermal simulation was performed to correct the experimental measurement data. Fig. 13 shows an exemplary temperature distribution on the active IGBT chip with $\Delta T = 50$ K (see test 1). Due to the high power loss density of 11.7 W/mm^2, a very large temperature gradient can be observed between the center and the edge of the chip. Due to the small ON-time, the heat flux is concentrated around the active die and does not warm up the neighboring package significantly. In addition, the bond wires have the highest temperature at the bond stitches, while the wire loop remains relatively cold.

Fig. 14 shows the junction temperature depending on the power loss density, in an evaluation path on the topside of the semiconductor starting at device center. The path is crossing two bond stitches, which can be seen as plateaus. All conditions have an equal virtual junction temperature of $T_{\mathrm{vj,max}} = 150$ °C, which is evaluated as area weighted average. It can be stated that the greater the temperature swing ΔT, the greater the gradient along the chip. The thermal results are then transferred into the mechanical domain and simulated for stress–strain analysis.

Fig. 15 shows the strain in the chip solder layer for two different conditions. The reddish lines result from simulated

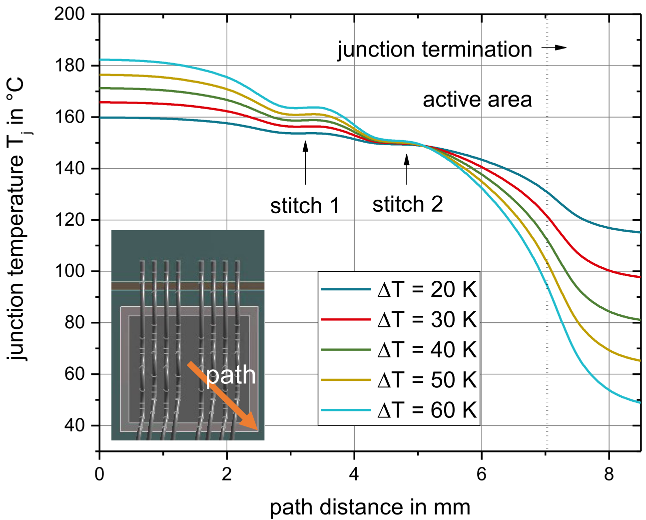

Fig. 14. Temperature distribution on the topside of the IGBT along the evaluation path (see the orange arrow in the inset) crossing two bond stitches for different ΔT but constant $T_{\mathrm{vj,max}} = 150$ °C.

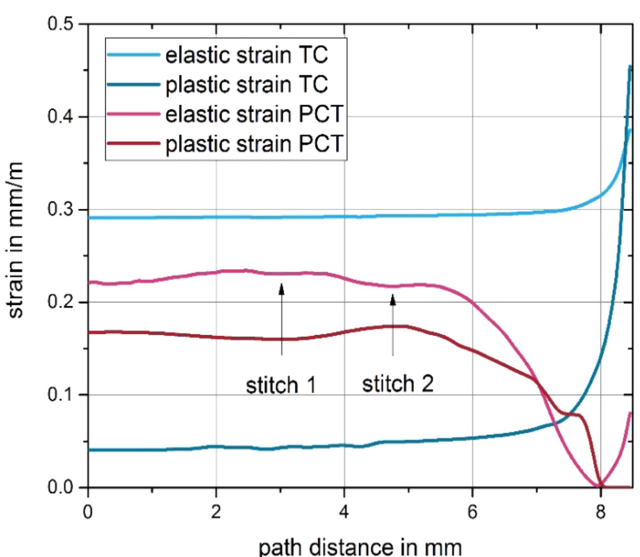

Fig. 15. Strain evaluation for $\Delta T = 30$ K in the middle height of the solder layer for an equal temperature cycle for the total system and similar power cycling conditions with high temperature gradients in the package. The same evaluation path as in Fig. 14 is used.

power cycling conditions, such as test 2 ($\Delta T = 30$ K). In contrast are the bluish lines, where a constant temperature swing for the total system is simulated, as it would occur with pure temperature cycling. It can be observed that for a high temperature gradient, such as in power cycling, the strain reaches its maximum in the center, while for a balanced temperature, the strain is concentrated at the edge of the solder. The simulation results confirm the failure analysis, which exposed the center region as main failure location. This is caused first by the highest junction temperature at this position, which weakens the mechanical stability of the solder material. In addition, the highest cyclic ΔT is present at this location leading to the highest strain rates (see Fig. 15). Thus, the simulation confirms the experimental results, which

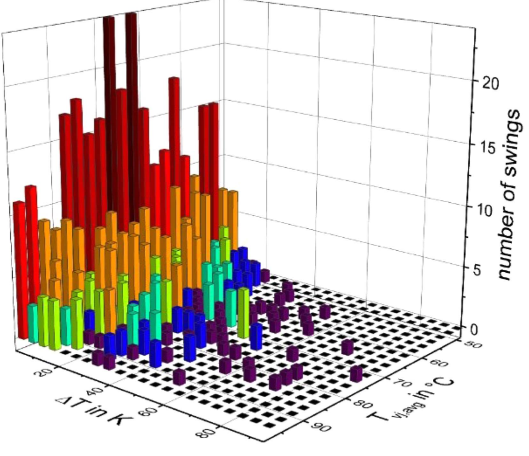

Fig. 16. Temperature profile for the automotive inverter.

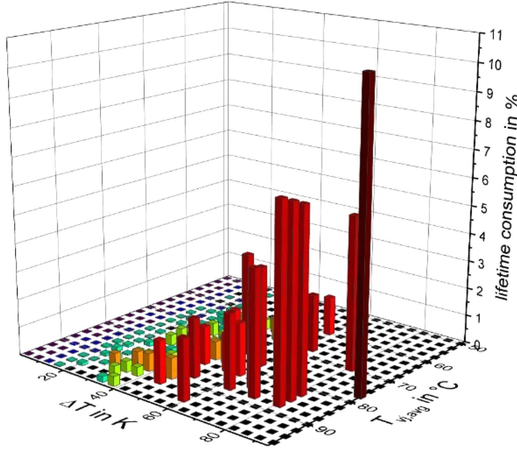

Fig. 17. Lifetime consumption for the automotive inverter calculated with the CIPS 08 lifetime model and the Palmgren–Miner approach.

expose the chip solder center region as main failure location. Nevertheless, it should be noted that the simulation is a small extraction of only a few power cycles, not considering long-term aging effects of the solder layer. This would, especially for high operation temperatures, weaken the mechanical stability of the solder layer significantly over time [38], [39].

VII. Example Lifetime Benefit

The findings of the experimental section of a significant increase in lifetime for low temperature swings are implemented in an application-close lifetime study. Two different fields of application were investigated, and the influence of the elastic–plastic area is discussed. It should be kept in mind that only the active power cycles are considered. The device used for calculation is the same as in the experimental section for which the lifetime data were gained. In Figs. 16 and 19, a randomized temperature profile for an automotive inverter and a wind turbine inverter was simulated using LabView. Both show comparable fluctuation in the average temperature $T_{\mathrm{vj,avg}}$. The automotive inverter has more spikes due to load variation such as acceleration (e.g.,

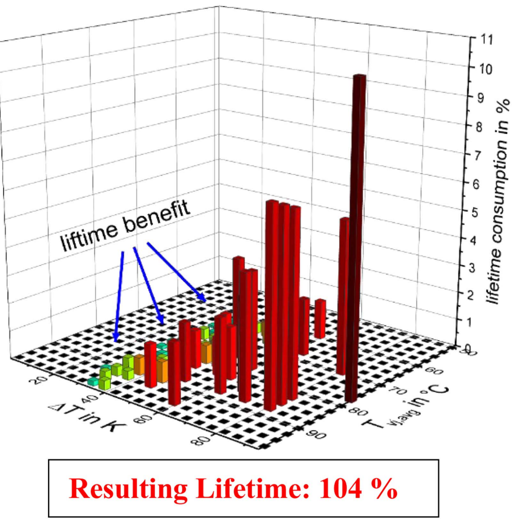

Fig. 18. Lifetime consumption according to the CIPS08 modified lifetime model and the Palmgren–Miner approach.

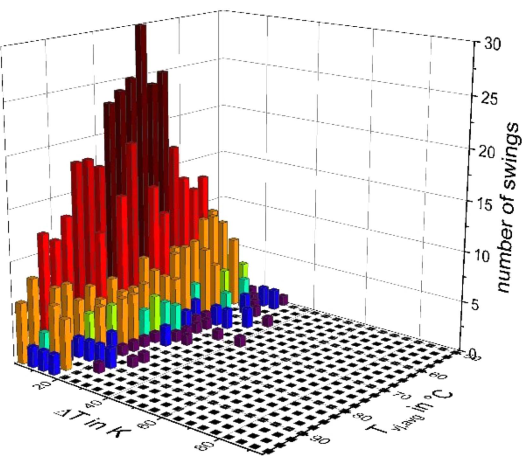

Fig. 19. Temperature profile for a wind turbine inverter.

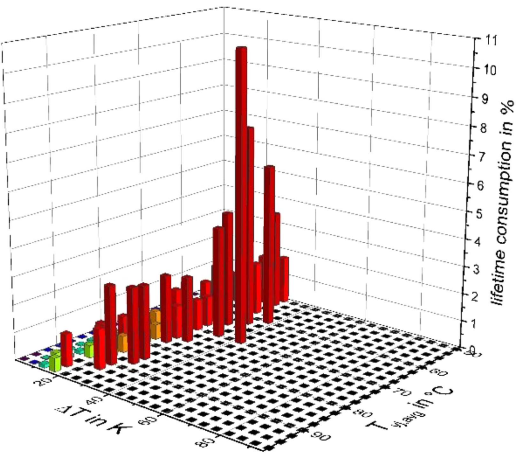

Fig. 20. Lifetime consumption for the wind turbine inverter calculated with the CIPS 08 lifetime model and the Palmgren–Miner approach.

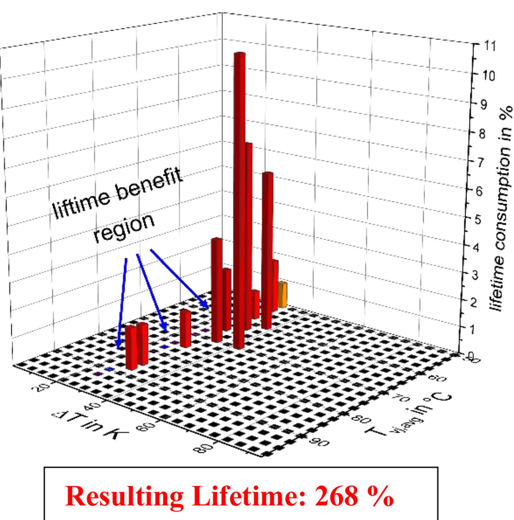

Fig. 21. Lifetime consumption according to the proposed CIPS08 modified lifetime model and the Palmgren–Miner approach.

kick-down) and breaking events where the load is orientated on the new European driving cycle, e.g., in [40]. In contrast the wind turbine inverter is oriented to the mission profile in [3]. The inverter has significantly less power peaks. This is caused by the constant output grid frequency and the inertia of the turbine, leading to a damping effect for load spikes. Hence, more power cycles are crowded in the low ΔT regime.

As shown in the workflow of Fig. 1, a rainflow analysis is performed with two different lifetime models, which are accumulated with the Palmgren–Minor approach using (4). Figs. 17 and 20 show the result for the standard CIPS lifetime model. The conditions used for calculation are similar to the test conditions in Section IV with a load current of I_{load} = 150 A, t_{on} = 10 ms, D = 400 μm, and V = 12 (1.2 kV). The $\beta 1$–$\beta 6$ coefficients are taken from [5] and the base lifetime K = $9.3{\cdot}10^{14}$ is taken from [14]. As expected, the most cirtical fatigue is caused by the high ΔT but also in the low ΔT regime lifetime consumption is visible. Figs. 18 and 21 show the results calculated under the same conditions, such as Figs. 17 and 20, but under consideration of an elastic deformation zone for which the proposed model in (6) is used. Both applications show a benefit in lifetime when the elastic deformation is taken into account for calculation. However, the influence differs significantly. While in the automotive application major load peaks are present, which consume a lot of lifetime, the benefit using the new approach is only around +4%. In contrast, in the wind turbine application, no major temperature swing peaks occur and most of them can be considered in the transition to the elastic branch respectively to HCF, leading to a resulting lifetime of +268%.

VIII. Conclusion

In this work, the elastic–plastic deformation zone for power electronic packages is investigated and further analyzed. To the best of authors' knowledge, current power cycling results do not cover a temperature ripple ΔT < 30 K. In the experimental section, results down to ΔT = 18 K are gained by experiment. The following statements regarding the

reliability performance in the elastic–plastic transition zone can be made.

1) Solder fatigue is the dominating failure mode in power cycling tests with low temperature swings. The most damage occurs in the device center area, driven by the high temperature gradient on the chip, which allows locally higher elastic and plastic strain rates.
2) Power cycling with high power densities and short ON-times will cause high thermomechanical strain and heat in the center region, which triggers strong degradation in the chip solder layer leading to microvoids in the center area. In this case, the microvoids are expected to be caused by unavoidable defects in the solder, which cause fatigue concentration points that accelerate plastic strain accumulation.
3) The topside metallization surface is subjected to strong modification of the aluminum, especially in the hotter center region.
4) No exponential increase in lifetime can be found for temperature swings $\Delta T > 18$ K and a high maximum junction temperature of $T_{\mathrm{vj,max}} \approx 150$ °C. Due to the loading and temperature conditions, it seems that the chip solder layer is exposed to a combination of LCF (e.g., center region) and HCF (e.g., edge region).
5) For lower maximum junction temperatures, such as $T_{\mathrm{vj,max}} \approx 115$ °C, an exponential increase in lifetime can be observed in the experiment and fitted with a modified $\beta 1$ exponent of the ΔT.

The findings from experiment and simulation were used for the calculation of an expected lifetime of an inverter. It could be demonstrated that for applications with load peaks, e.g., e-mobility, the lifetime benefit is minor. A huge lifetime boost can be gained when no or only a few peaks occur. Therefore all deformation results in the transition from the elastic domain to the HCF domain. The calculated expected life of the wind turbine is increased by a factor of 2.7. Even though first results in the HCF zone tested in power cycling were obtained, more research in this region will be valuable. More testing has to be done to identify the lifetime behavior between $T_{\mathrm{vj,max}} = 150$ °C and $T_{\mathrm{vj,max}} = 115$ °C. Also the impact of a varying solder thickness due to production variations is suggested as a subject of future research.

References

[1] A. Palmgren, "Die lebensdauer von kugellagern," *Zeitschrift Vereins Deutscher Ingenieure*, vol. 68, pp. 339–341, 1924.

[2] M. Miner, "Cumulative damage in fatigue," *J. Appl. Mech.*, vol. 12, pp. A159–A164, 1945.

[3] A. S. Bahman, F. Iannuzzo, and F. Blaabjerg, "Mission-profile-based stress analysis of bond-wires in SiC power modules," in *Microelectronics Reliability*. Amsterdam, The Netherlands: Elsevier, 2016.

[4] M. Fogsgaard, A. S. Bahman, F. Iannuzzo, and F. Blaabjerg, "Mission profile simplification method for reliability analysis of PV converters," in *Microelectronics Reliability*. Amsterdam, The Netherlands: Elsevier, 2022.

[5] R. Bayerer, T. Licht, T. Herrmann, J. Lutz, and M. Feller, "Model for power cycling lifetime of IGBT modules - various factors influencing lifetime," in *Proc. Procurement Supply 5th Int. Conf. Integr. Power Electron. Syst.*, 2008, pp. 37–42.

[6] T. Poller, "Thermal and thermal-mechanical simulation for the prediction of fatigue processes in packages for power semiconductor devices," in Ph.D. dissertation, TU Chemnitz, Chemnitz, Germany, 2014.

[7] P. Paris and F. Ergogan, "A critical analysis of crack propagation laws," *ASME. J. Basic Eng.*, vol. 85, vol. 4, pp. 528–533, Dec. 1963, doi: 10.1115/1.3656900.

[8] R. Darveaux, "Effect of simulation methodology on solder joint crack growth correlation," in *Proc. Electron. Compon. Technol. Conf.*, 2000, pp. 158–169.

[9] H. S. Chung, H. Wang, F. Blaabjerg, and M. Pecht, "Reliability of power electronic converter systems," *IEEE Power Electron. Mag.*, vol. 3, no. 4, pp. 103–160, Dec. 2016, doi: 10.1109/MPEL.2016.2616118.

[10] T. Frondelius et al., "A continuum based macroscopic unified low- and high cycle fatigue model," in *Proc. ICMFF12-12th Int. Conf. Multiaxial Fatigue Fracture*, 2019.

[11] M. Held, P. Jacob, G. Nicoletti, P. Scacco, and M. H. Poech, "Fast power cycling test of IGBT modules in traction application," in *Proc. 2nd Int. Conf. Power Electron. Drive Syst.*, 1997, pp. 425–430.

[12] U. Scheuermann and R. Schmidt, "Impact of load pulse duration on power cycling lifetime of Al wire bonds," *Microelectronics Rel.*, vol. 53, pp. 1687–1691, 2013.

[13] G. Zeng, L. Borucki, O. Wenzel, O. Schilling, and J. Lutz, "First results of development of a lifetime model for transfer molded discrete power devices," in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Energy Manage.*, 2018, pp. 1–8.

[14] J. Lutz, H. Schlangenotto, U. Scheuermann, and R. D. Doncker, *Semiconductor Power Devices: Physics, Characteristics, Reliability*. Berlin, Germany: Springer, 2018.

[15] S. S. Manson, "Behavior of materials under conditions of thermal stress," Nat. Advisory Committee Aeronaut., Tech. Note TN-2933, 1954.

[16] L. F. Coffin, Jr., "A study of the effects of cyclic thermal stresses on a ductile metal," *Trans. Amer. Soc. Mech. Engineers*, vol. 76, pp. 931–950, 1953.

[17] S. Hartmann and E. Özkol, "Bond wire life time model based on temperature dependent yield strength," in *Proc. Power Convers. Intell. Motion Eur., Power Electron.-Compon.-Technol.-Appl.-Syst.*, 2012, pp. 494–501.

[18] J. Lutz, C. Schwabe, G. Zeng, and L. Hein, "Validity of power cycling lifetime models for modules and extension to low temperature swings," in *Proc. 22nd Eur. Conf. Power Electron. Appl.*, 2020, pp. P.1–P.9.

[19] N. Dornic et al., "Stress-based model for lifetime estimation of bond wire contacts using power cycling tests and finite-element modeling," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 3, pp. 1659–1667, Sep. 2019, doi: 10.1109/JESTPE.2019.2918941.

[20] A. Wintrich and U. Scheuermann, "Power cycle model for IGBT product lines," Semikron Danfoss, Nuremberg, Germany, Application Note AN21-001, 2021.

[21] T. Methfessel, F. Sauerland, K. Mainka, and O. Schilling, "Enhanced lifetime and power-cycling modelling for PrimePACK$^{\mathrm{TM}}$ .XT power modules," in *Proc. Power Convers. Intell. Motion*, 2020, pp. 1–8.

[22] C. Durand, M. Klingler, C. Daniel, and H. Naceuer, "Power cycling reliability of power module: A survey," *IEEE Trans. Device Mater. Rel.*, vol. 16, no. 1, pp. 80–97, Mar. 2016, doi: 10.1109/TDMR.2016.2516044, 2016.

[23] A. Hutzler, "Untersuchungen zur lastwechselfestigkeit von halbleiteranbindungen unter hochtemperaturbelastung," Ph.D. dissertation, F.-A.-Universität Erlangen-Nürnberg, Nürnberg, Germany, 2019.

[24] P. Seidel, C. Herold, J. Lutz, C. Schwabe, and R. Warsitz, "Power cycling test with power generated by an adjustable part of switching losses," in *Proc. 19th Eur. Conf. Power Electron. Appl.*, 2017, pp. P.1–P.10.

[25] J. Abuogo, C. Schwabe, J. Lutz, and T. Basler, "Switch mode power cycling test of silicon carbide MOSFETs using repetitive avalanche for heat generation," in *Proc. Power Convers. Intell. Motion*, 2023, pp. 1–7.

[26] C. Schwabe et al., "Power cycling lifetime investigation under low temperature swings and 50 Hz load with experiment and simulation," in *Proc. Power Convers. Intell. Motion*, 2021, pp. 1377–1384.

[27] ECPE, "Qualification of power modules for use in power electronics converter units in motor vehicles," in *Proc. ECPE Eur. Center Power Electron.*, 2019.

[28] C. Schwabe, N. Thönelt, and T. Basler, "Reliability investigation of SiC MOSFETs under switching operation in various packages," in *Proc. Chartered Inst. Procurement Supply 12th Int. Conf. Integr. Power Electron. Syst.*, 2022, pp. 1–6.

[29] A. Krupin, J. Fuhrmann, and H.-G. Eckel, "Power cycle test with switching losses and integrated hot-spot measurement," in *Proc. Power Convers. Intell. Motion*, 2020, pp. 996–1002.

[30] R. Schmidt and U. Scheuermann, "Using the chip as a temperature sensor—The influence of steep lateral temperature gradients on the Vce(T)-measurement," in *Proc. 13th Eur. Conf. Power Electron. Appl.*, 2009, pp. 1–9.
[31] C. Herold, J. Franke, R. Bhojani, A. Schleicher, and J. Lutz, "Requirements in power cycling for precise lifetime estimation," in *Microelectronics Reliability*. Amsterdam, The Netherlands: Elsevier, 2015.
[32] D. L. Blackburn, "An electrical technique for the measurement of the peak junction temperature of power transistors," in *Proc. IEEE Int. Rel. Phys. Symp.*, 1975, pp. 142–150.
[33] E. Deng and J. Lutz, "Measurement error caused by the square root t method applied to IGBT devices during power cycling test," in *Proc. 32nd Int. Symp. Power Semicond. Devices ICs*, 2020, pp. 545–548.
[34] G. Zeng, C. Herold, T. Methfessel, M. Schäfer, O. Schilling, and J. Lutz, "Experimental investigation of linear cumulative damage theory with power cycling test," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4722–4728, May 2019, doi: 10.1109/TPEL.2018.2859479.
[35] M. Junghänel and U. Scheuermann, "Impact of load pulse duration on power cycling lifetime of chip interconnection solder joints," *Microelectronics Rel.*, vol. 76, pp. 480–484, 2017.
[36] R. Bürgel, H. Maier, and T. Niendorf, *Handbuch Hochtemperatur-Werkstofftechnik*. Heidelberg, Germany: Springer, 2011.
[37] M. S. Alam, M. Basit, P. Lall, and J. C. Suhling, "Mechanical characterization of SAC305 lead free solder at high temperatures," in *Proc. IEEE 15th ITHERM Conf.*, 2016, pp. 755–760.
[38] M. Sabri, D. Shnawah, I. Badruddin, S. Said, F. Che, and T. Ariga, "Microstructural stability of Sn–1Ag–0.5Cu–xAl ($x = 1$, 1.5, and 2 wt.%) solder alloys and the effects of high-temperature aging on their mechanical properties," *Mater. Characterization*, vol. 78, pp. 129–143, 2013.
[39] M. Mustafa, J. Roberts, J. Suhling, and P. Lall, "The effects of aging on the fatigue life of lead free solders," in *Proc. Electron. Compon. Technol. Conf.*, 2014, pp. 666–683.
[40] G. Kadijk, N. Ligternik, P. van Mensch, and R. Smokers, "NOx emissions of Euro 5 diesel vans – test results in the lab and on the road," TNO, The Hague, The Netherlands, TNO Rep. TNO 2016 R10356, doi: 10.13140/RG.2.2.30386.61126, 2016.

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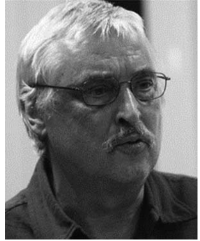

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