Computer-Aided Comprehensive Operation Analysis of DC–DC Converters Considering Uncertain States of Diodes

Jixiang Song, Guipeng Chen, and Liping Mo

***Abstract*—Unlike controllable switches, the ON/OFF states of diodes are uncertain, which often results in various unknown operation modes for converters under different working conditions. Thus, the comprehensive operation analysis of converters is usually hard to achieve with the conventional manual analysis method. Aiming to overcome this shortcoming, a computer-aided automatic analysis method of dc–dc converters is proposed in this article. First, the converter is mathematically modeled on the basis of electrical network theory, so that its analysis can be further processed in the computer program. Then, all possible working states of diodes in different switching modes are automatically evaluated according to fundamental circuit law. Finally, by arbitrarily combining the feasible submodes, comprehensive operation modes of converters satisfying the power electronics principle are automatically derived. More than that, their corresponding steady-state performance analysis results including operation mode boundaries, voltage gains, and components' voltage/current would be obtained simultaneously. Therefore, the proposed computer-aided automatic analysis method is not only capable of conveniently obtaining a comprehensive understanding of different converters after considering uncertain states of diodes, but also is beneficial for the converter design in engineering applications.**

***Index Terms*—Automatic analysis, computer-aided, DC–DC converters, diode state.**

I. Introduction

BY EMPLOYING switches, diodes, inductors, capacitors, etc., dc–dc converters can realize voltage regulation and power control for many applications [1], [2], [3], [4], [5], [6], [7], [8]. The performance characteristics of dc–dc converters are various, which are determined by the ON/OFF states of switches/diodes and the corresponding commutation circuits of passive components. Hence, in order to better select and apply an optimal converter to a specified application, a comprehensive operation analysis of the converter is essential.

Up to now, the operation analysis of dc–dc converters are mainly implemented by analytic method, which depends on manual effort to enumerate commutation modes and formulate equations [9], [10], [11], [12], [13], [14]. The commutation modes can be easily obtained if the ON/OFF states of switches/diodes are already known. Then, equations in each commutation mode are manually formulated based on Kirchhoff voltage law (KVL), Kirchhoff current law (KCL), voltage-second balance (VSB) principle, ampere-second balance (ASB) principle, etc. Finally, the combined equations in all commutation modes are solved to complete the operation analysis for converters. Although the manual analysis method is feasible, it is tedious and time-consuming when there are a number of converters to be analyzed. Moreover, the ON/OFF states of switches are explicitly known from the modulation strategy, but diodes are uncontrollable, in that their working states are uncertain and are determined by the instantaneous voltage/current of the working circuit. Hence, even with a given modulation strategy, a converter may have multiple operation modes under different working conditions resulting from the different diode states, e.g., continuous conduction mode (CCM) and discontinuous conduction mode (DCM). However, in practice, only a part of operation modes is usually revealed and analyzed for the converter, as it is difficult to manually enumerate all states of diodes and solve the equations with the conventional analysis method. Therefore, incomplete operation analysis is often obtained for converters, especially for the complicated converters [15], [16], [17]. For example, only the CCM operation mode is introduced for the enhanced gain buck-boost converter (EGBBC) in [15], while its four DCM operation modes in correspondence with different ON/OFF states of diodes are not explained.

As a supplement of analytic analysis, simulation software such as PSIM [18], SIMULINK [19], PSPICE [20] has been widely employed to acknowledge converters more intuitively. They can quickly acquire the voltage/current waveforms of each component in the converter by calculating through iterative algorithms including Runge-Kutta method and Euler method. Hence, the computer-aided simulation method can effectively avoid the cumbersome manual effort required in the conventional manual analysis method. However, the simulation method can

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only analyze the converter operation at one operating point with specified components' parameters at a time. Although the parameters can be arbitrarily modified to simulate and acquire the performance characteristics for converters at various operating points, it is blind and it cannot guarantee that all operation modes are included. Therefore, the simulation method is favorable for the effective validity of analytic analysis, but it is not effective to discover all operation modes and obtain comprehensive analysis for converters.

On the other hand, computer-aided analytic operation analysis has been successfully applied in nonswitched circuit networks based on the electrical network theory (ENT) which fundamental is mathematically modeling the non-switched circuit by graph theory. Recently, graph theory also gains increasing applications in power electronics research [21]. In [22], the connecting information of converters was transformed into the adjacent matrix to quickly and precisely accomplish the identification of equivalent converters with the aid of computer program. In [23], graph theory is used to find out the sneak circuit paths of the converter, with the aim of avoiding undesired function to occur at some certain conditions. In [24], by transforming the working criteria of converters into the corresponding graph constraints, the topology derivation can be automatically and conveniently completed. In [25], a systematic topology simplification method is proposed on the basis of graph theory. Nevertheless, graph theory has not been employed to implement operation modes automatic analysis for converters yet, which should be attainable through extending ENT on the basis of the intrinsic switching characteristics of converters.

From above, a computer-aided comprehensive operation analysis method combining the classical ENT with fundamental circuit law (FCL) and power electronics principle (PEP) is proposed for dc–dc converters in this article.

1) First, ENT is employed to mathematically model the converter, so that its operation analysis can be automatically processed in the computer program.
2) Then, FCL is utilized to automatically evaluate the effectiveness of all possible working states of diodes in different switching modes.
3) Finally, PEP is adopted to automatically search all possible operation modes of converters.

With the proposed method, all the workable operation modes of the converter fully considering uncertain states of diodes can be conveniently obtained, and their corresponding steady-state performance analysis results are derived at the same time. Therefore, it is not only comprehensive but also efficient in comparison with the traditional manual analytic analysis method, which is very beneficial for the topology comparison and converter design in practical applications.

The rest of this article is organized as follows. The comprehensive operation analysis of dc–dc converters considering uncertain states of diodes is introduced in Section II. Then, the proposed computer-aided automatic analysis method is elaborated in Section III. Next, the comprehensive operation analysis results are demonstrated in Section IV. Afterward, experimental results are provided to verify the theoretical analysis in Section V. Section VI concludes the article.

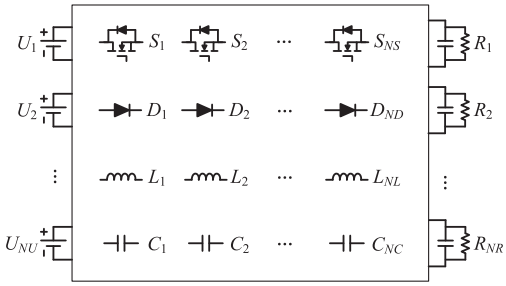

Fig. 1. Generic DC–DC converter configuration.

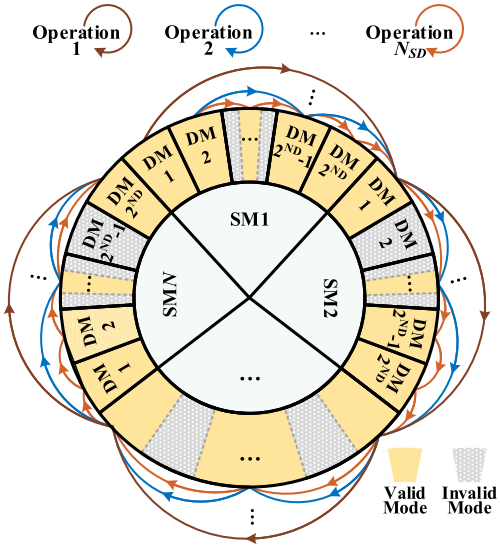

Fig. 2. Comprehensive operations of DC–DC converter considering definite switching modes and uncertain diodes states.

II. Comprehensive Operation Analysis of DC–DC Converters Considering Uncertain States of Diodes

For a generic dc–dc converter as shown in Fig. 1, it contains N_S switches, N_D diodes, N_L inductors, N_C capacitors, N_U voltage-type inputs, and N_R voltage-type output loads. Under a given modulation strategy, the N_S switches will turn ON or OFF explicitly, and they are assumed to generate N successive switching modes SM1, SM2, …, SMN in a period. Nevertheless, in each switching mode SMi ($i = 1, 2, \ldots, N$), the ON/OFF states of N_D diodes are unknown, which are determined by the voltage and current they withstand in the main circuit. What's worse, some diodes may turn from ON state to OFF state in a switching mode when the converter operates in DCM instead of CCM. Therefore, in order to achieve a comprehensive operation analysis of dc–dc converters, all possible workable states of diodes must be considered.

In theory, depending on the ON/OFF state of diodes, 2^{ND} possible submodes (DM1, DM2, …, DM2^{ND}) in total may appear in each switching mode, as illustrated in Fig. 2. While in practice, some of them are invalid due to violating the well-known FCL as depicted in Fig. 3(a). The first law is that voltage sources must not be short-circuited or in parallel connection, and the second one is that current sources must not be open-circuited

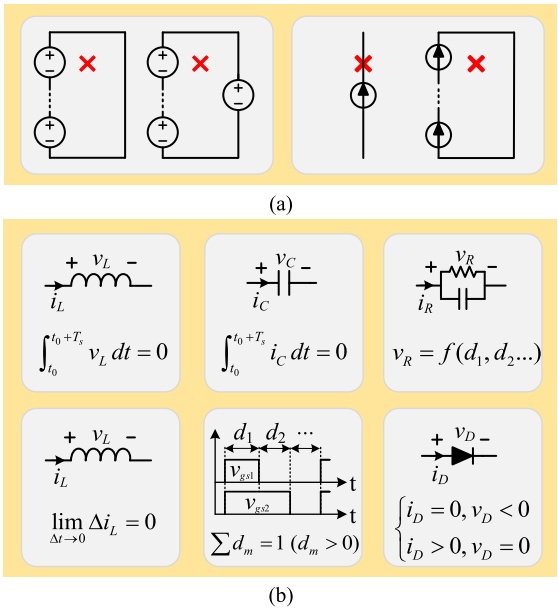

Fig. 3. FCL for valid submodes and PEP for workable operation modes. (a) FCL. (b) PEP.

or in series connection. Therefore, it is necessary to evaluate the effectiveness of the 2^{ND} submodes in each switching mode SMi. After evaluation, it is assumed that the number of the valid submodes in different switching modes SM1, SM2, …, SMN are VM_1, VM_2, …, VM_N.

For the VM_i valid submodes in the switching mode SMi ($i = 1, 2, \ldots, N$), they may appear alone or may be combined to form different converter operation modes, as depicted in Fig. 2. If there is j ($j = 1, 2, \ldots, VM_i$), submodes appearing in the switching mode SMi, A^j_{VMi} possible combinations can be achieved. Then, a total of $\sum_{j=1}^{VMi} A^j_{VMi}$ submode combinations can be obtained in the switching mode SMi. Finally, by multiplying the number of submodes combinations in all switching modes SM1–SMN as calculated in (1), N_{SD} possible operation modes of the dc–dc converter can be enumerated. Likewise, not all the possible operation modes are valid for the converter, and a further validity examination is required according to PEP in Fig. 3(b). The switching period is denoted as T_s and its initial time is t_0. The duty cycle of the mth submodes in a switching period is denoted as d_m. v_* and i_* are, respectively, the voltage/current of the component of * ($^* = D, L, C, R$). It includes the following six principles.

1) Inductors should obey the VSB principle.
2) Capacitors should obey the ASB principle.
3) Output voltage is controllable.
4) The inductor current must not change abruptly.
5) The sum of the duty cycle of each submode in a switching period is equal to one.
6) Voltage and current of the semiconductor devices should meet their intrinsic relationship.

$$N_{SD} = \prod_{i=1}^{N} \left(\sum_{j=1}^{VMi} A^j_{VMi} \right). \tag{1}$$

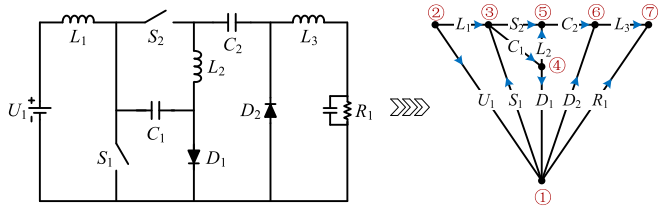

Fig. 4. Correspondence between example EGBBC and its graph.

From above, in order to achieve a comprehensive operation analysis of dc–dc converters considering the uncertain states of N_D diodes, the effectiveness of the 2^{ND} submodes in each switching mode SMi ($i = 1, 2, \ldots, N$) should be one-by-one evaluated first, and then N_{SD} possible operation modes composed of one or several valid submodes from each switching mode SMi will be one-by-one examined to select out workable operation modes. It is obvious that 2^{ND} and N_{SD} in (1) increase dramatically as the number of diodes N_D and the number of switching modes N increases. For example, the EGBBC in [15] has three switching modes SM1–SM3 with the given modulation strategy, and the number of the valid submodes in different switching modes SM1, SM2, and SM3 are, respectively, $VM_1 = 2$, $VM_2 = 4$, and $VM_3 = 3$. Then, according to (1), $N_{SD} = 3840$ is calculated, which is too large to be examined and analyzed purely through manual effort. Consequently, a comprehensive steady-state performance analysis is difficult to be obtained for the converter with the conventional manual analytic analysis method, especially for the complex ones with multiple switching modes and diodes.

III. Proposed Computer-Aided Automatic Analysis Method

In order to overcome the aforementioned limitation of manual effort on the comprehensive operation analysis of converters, a computer-aided automatic analysis method is proposed in this article. With the proposed method, all the workable operation modes and their corresponding steady-state performance analysis results can be conveniently obtained for the converter with negligible voltage ripple on capacitors after considering all possible states of diodes, with the aid of computer program. First, in order to automate the analysis, the converter is mathematically modeled based on ENT so that its general KVL&KCL equations can be automatically obtained in the computer program. Second, based on the ON/OFF states of switches/diodes, the specific KVL&KCL equations of all possible submodes of the converter are enumerated, with which the valid submodes would be automatically selected according to FCL. Finally, the valid submodes are combined to generate various operation modes, among which the effective ones would be selected on the basis of PEP. Besides, the corresponding steady-state performance analysis results of all these effective operation modes also will be obtained simultaneously. In this section, the EGBBC in [15] which is redepicted in Fig. 4, is chosen as an example to illustrate the proposed method intuitively. The example converter contains an input U_1, an outputs R_1, two switches S_1–S_2, two diode

TABLE I
PSEUDOCODE OF MATHEMATICAL MODEL OF CONVERTER

Function: Converter Mathematical Modeling
Input: Adjacent Matrix *Adj*
Output: KVL & KCL Equations
1 $\{T, \widehat{T}\} = f_{\mathrm{DFS}}(Adj)$
2 $B_f = f_{\mathrm{Loop}}(Adj, T, \widehat{T})$
3 $Q_f = f_{\mathrm{Cutset}}(T, B_f)$
4 KVL = $B_f \cdot V^{\mathrm{T}}$
5 KCL = $Q_f \cdot i^{\mathrm{T}}$

D_1–D_2, three inductors L_1–L_3, and two energy buff capacitors C_1–C_2. It is assumed that the capacitor voltage remains constant in a switching period as their voltage ripple is relatively small.

A. Mathematical Model of the Converter Based on ENT

In essence, the power electronics converter is comprised of nodes, components, and their connecting relationships, which can be mathematically modeled as an adjacent matrix *Adj* through its corresponding graph according to the graph theory. Then, based on ENT, a pair of tree T and cotree $\widehat{T}$ can be searched for the converter by depth-first-search (DFS) algorithm to help list the fundamental loop matrix B_f and the fundamental cutset matrix Q_f. Finally, KVL&KCL equations of the converter are formulated with matrix B_f and Q_f. The pseudo-code of the mathematical model of converter in Matlab is shown in Table I.

Adjacent Matrix Adj: According to [22] and [25], the adjacent matrix is used to store the connecting relationships among nodes and components of the converter in mathematical form, so that the converter analysis can be automatically conducted in the computer. According to the equivalent graph in Fig. 4, the example EGBBC has seven nodes {①–⑦} and eleven edges $\{U_1, S_1, D_1, D_2, R_1, L_1, C_1, S_2, L_2, C_2, L_3\}$. Therefore, its Adj is a 7×7 matrix with all diagonal elements as zero. For other elements a_{pq} and a_{qp} ($p, q = 1, 2, \ldots, 7$ and $p \neq q$), their absolute values are equal to the component connected between node p and q, and they are opposite. If the current reference direction of this component is from p to q, $a_{pq} = -a_{qp}$ is positive. Otherwise, $a_{pq} = -a_{qp}$ is negative.

Tree T *& Cotree* $\widehat{T}$ *:* The tree T is a connected subgraph that connects all nodes through tree branches without any loop, while the cotree $\widehat{T}$ is made up of the remaining link branches. The DFS algorithm can be employed to search the tree T from the adjacent matrix *Adj*. For the example EGBBC, it starts from node ①, accesses nodes ②-③-④-⑤-⑥, and finally accesses node ⑦ at the end, as depicted in Fig. 5. Hence, $T = [U_1, L_1, C_1, L_2, C_2, L_3]$ is searched, and complementary to the tree, cotree $\widehat{T} = [S_1, D_1, D_2, R_1, S_2]$ is conveniently obtained.

Fundamental Loop Matrix $\mathrm{B_f}$*:* Adding each link branch in cotree $\widehat{T}$ to the tree T separately through function $f_{\mathrm{Loop}}()$ with the aid of DFS algorithm, fundamental loops can be found. The example EGBBC has five fundamental loops Lp_1: ①-③-②-①, Lp_2: ④-①-②-③-④, Lp_3:③-⑤-④-③, Lp_4: ①-⑥-⑤-④-③-②-①, and Lp_5: ①-⑦-⑥-⑤-④-③-②-①, as shown in Fig. 6. Therefore, the corresponding fundamental loop matrix

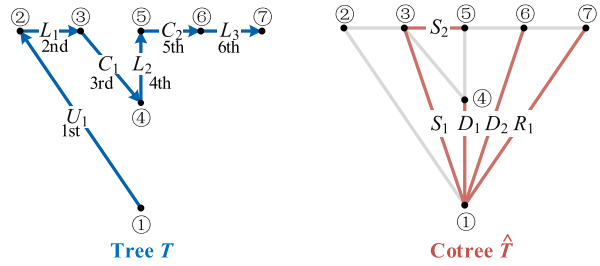

Fig. 5. Pair of tree and cotree of EGBBC.

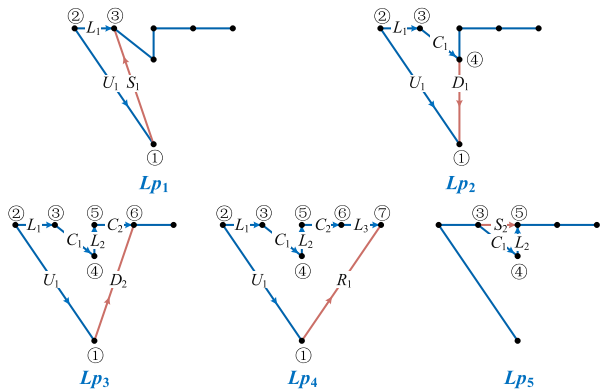

Fig. 6. Five fundamental loops of EGBBC.

B_f is obtained in the Matlab program, which consists of two submatrices E_l and B_t, as shown in (2). E_l is an identity matrix corresponding to link branch S_1, D_1, D_2, R_1, S_2 and B_t contains the tree branches in each fundamental loop Lp_1–Lp_5 having link branch S_1, D_1, D_2, R_1, S_2. In B_t, value 1 represents that the current direction of the tree branch is the same as that of link branch, while value −1 represents that they are opposite. Taking the fundamental loop Lp_1 as an example, it contains one link branch S_1 and two tree branches U_1 and L_1. The current reference direction of U_1 is the same as that of S_1 and the current reference direction of L_1 is the opposite of S_1. Therefore, in the first row of B_f, elements that correspond to S_1 and U_1 are 1 while the element that corresponds to L_1 is −1. The fundamental loop matrix B_f will be employed to automatically derive KVL equations for the converter.

$$B_f = \begin{array}{c} \\ Lp_1 \\ Lp_2 \\ Lp_3 \\ Lp_4 \\ Lp_5 \end{array} \begin{array}{c} \overbrace{\begin{array}{ccccc} S_1 & D_1 & D_2 & R_1 & S_2 \end{array}}^{\text{Link branches}} \\ \left[\begin{array}{ccccc} 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{array}\right. \\ E_l \end{array} \begin{array}{c} \overbrace{\begin{array}{cccccc} U_1 & L_1 & C_1 & L_2 & C_2 & L_3 \end{array}}^{\text{Tree branches}} \\ \left.\begin{array}{cccccc} 1 & -1 & 0 & 0 & 0 & 0 \\ -1 & 1 & 1 & 0 & 0 & 0 \\ 1 & -1 & -1 & -1 & -1 & 0 \\ 1 & -1 & -1 & -1 & -1 & -1 \\ 0 & 0 & -1 & -1 & 0 & 0 \end{array}\right] \\ B_t \end{array} . \quad (2)$$

Fundamental Cutset Matrix Q_f*:* Furthermore, in order to automatically obtain KCL equations for the converter, the fundamental cutset matrix Q_f is needed to store the information of fundamental cutsets, which is made up of one tree branch and several link branches. On the basis of matrix B_f, the matrix Q_f in (3) is easily obtained through function $f_{\mathrm{Cutset}}()$ by employing

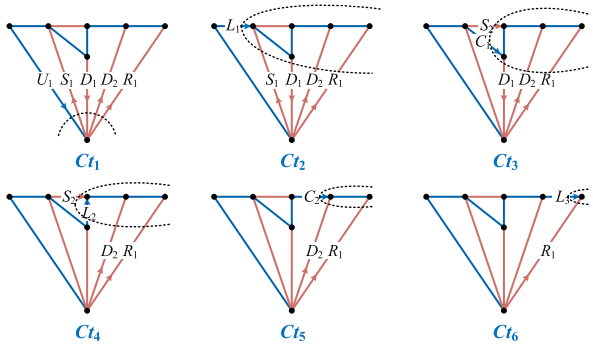

Fig. 7. Six fundamental cutsets of EGBBC.

the submatrix B_t in B_f to generate the submatrix Q_l for Q_f, according to the relationship $Q_l = -B^T{}_t$ in ENT. Similar to E_l in (2), the submatrix E_t is an identity matrix. According to the obtained result of Q_f, there are six cutsets Ct_1–Ct_6 in the example EGBBC, as depicted in Fig. 7

$$Q_f = \begin{array}{c} \\ Ct_1 \\ Ct_2 \\ Ct_3 \\ Ct_4 \\ Ct_5 \\ Ct_6 \end{array} \begin{array}{c} \overbrace{\begin{array}{cccccc} U_1 & L_1 & C_1 & L_2 & C_2 & L_3 \end{array}}^{\text{Tree branches}} \\ \left[\begin{array}{cccccc} 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{array}\right. \\ E_t \end{array} \begin{array}{c} \overbrace{\begin{array}{ccccc} S_1 & D_1 & D_2 & R_1 & S_2 \end{array}}^{\text{Link branches}} \\ \left.\begin{array}{ccccc} -1 & 1 & -1 & -1 & 0 \\ 1 & -1 & 1 & 1 & 0 \\ 0 & -1 & 1 & 1 & 1 \\ 0 & 0 & 1 & 1 & 1 \\ 0 & 0 & 1 & 1 & 0 \\ 0 & 0 & 0 & 1 & 0 \end{array}\right] \\ Q_l \end{array}. \quad (3)$$

KVL & KCL Equations: Finally, multiplying matrix B_f by the voltage vector $V^{\mathrm{T}} = [V_{S1}, V_{D1}, V_{D2}, V_{R1}, V_{S2}, V_{U1}, V_{L1}, V_{C1}, V_{L2}, V_{C2}, V_{L3}]^{\mathrm{T}}$, and multiplying matrix Q_f by the current vector $i^{\mathrm{T}} = [i_{U1}, i_{L1}, i_{C1}, i_{L2}, i_{C2}, i_{L3}, i_{S1}, i_{D1}, i_{D2}, i_{R1}, i_{S2}]^{\mathrm{T}}$, the general KVL&KCL equations of the example EGBBC are conveniently formulated in (4) and (5), respectively

$$\mathrm{KVL}\begin{cases} V_{S1} + V_{U1} - V_{L1} = 0 \\ V_{D1} - V_{U1} + V_{L1} + V_{C1} = 0 \\ V_{D2} + V_{U1} - V_{L1} - V_{C1} - V_{L2} - V_{C2} = 0 \\ V_{R1} + V_{U1} - V_{L1} - V_{C1} - V_{L2} - V_{C2} - V_{L3} = 0 \\ V_{S2} - V_{C1} - V_{L2} = 0 \end{cases} \quad (4)$$

$$\mathrm{KCL}\begin{cases} i_{U1} - i_{S1} + i_{D1} - i_{D2} - i_{R1} = 0 \\ i_{L1} + i_{S1} - i_{D1} + i_{D2} + i_{R1} = 0 \\ i_{C1} - i_{D1} + i_{D2} + i_{R1} + i_{S2} = 0 \\ i_{L2} + i_{D2} + i_{R1} + i_{S2} = 0 \\ i_{C2} + i_{D2} + i_{R1} = 0 \\ i_{L3} + i_{R1} = 0 \end{cases}. \quad (5)$$

B. Automatic Selection of Valid Submodes Based on Fundamental Circuit Law

With the obtained general KVL&KCL equations in (4) and (5), specific KVL&KCL equations of each submode with different ON/OFF states of switches/diodes can be easily obtained

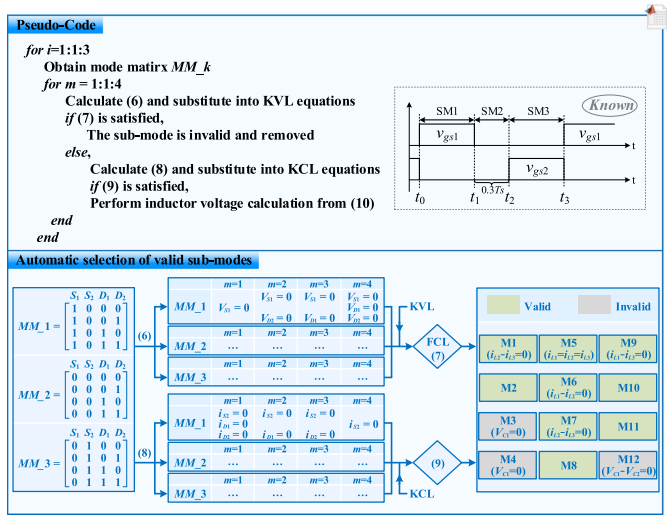

Fig. 8. Automatic selection of valid submodes of EGBBC.

by substituting the corresponding zero turn-on voltage and zero turn-off current. They will be employed to automatically examine the validity of all submodes according to FCL to select valid ones and solve the voltage/current relationships among different components in each valid submode.

According to Section II, in each switching mode SMi (i = 1, 2, …, N), the ON/OFF state of switches S_1–S_{NS} are explicit under a given modulation strategy while it is unclear for diodes D_1–D_{ND}. Therefore, a mode matrix *MM_i* with 2^{ND} rows and $N_S + N_D$ columns is employed to traverse the diodes states of all submodes in the switching mode SMi. The element is equal to 1 or 0 depending on the on or off state of the corresponding switch/diode. With the drive signals in Fig. 8, the example converter has three switching modes SM1, SM2, and SM3 in $[t_0, t_1]$ with S_1 on, in $[t_1, t_2]$ with S_1, S_2 both off, and in $[t_2, t_3]$ with S_2 on. Then, three mode matrices *MM*_1, *MM*_2, and *MM*_3 are automatically generated, all of which include four rows as the diodes D_1 and D_2 may be on or off, as shown in Fig. 8. Hence, the example EGBBC has 12 submodes M1–M12 in total, whose equivalent circuits are respectively demonstrated in Fig. 9.

Afterward, voltages of the on-state switches/diodes in the mth (m = 1, 2, 3, 4) submode of the switching mode SMk (k = 1, 2, 3) which are equal to zero, would be calculated in (6). diag[*MM_k*(m, :)] is a diagonal matrix whose diagonal elements are equal to the elements in mth row of *MM_k*. For example, as shown in Fig. 8, $V_{S1} = 0$ for submode M1, $V_{S1} = V_{D2} = 0$ for submode M2, $V_{S1} = V_{D1} = 0$ for submode M3, $V_{S1} = V_{D1} = V_{D2} = 0$ for submode M4, and so on are automatically obtained and they are substituted into the general KVL equations in (4) which would be simplified to achieve the specific KVL equations for the mth submode of switching mode SMk.

After simplification, if only the voltages of voltage-type inputs, capacitors, and voltage-type output loads appear in some KVL equations as illustrated in (7), this submode is invalid because it violates the FCL that voltage sources (including input, output, and capacitor) are short-circuited or connected

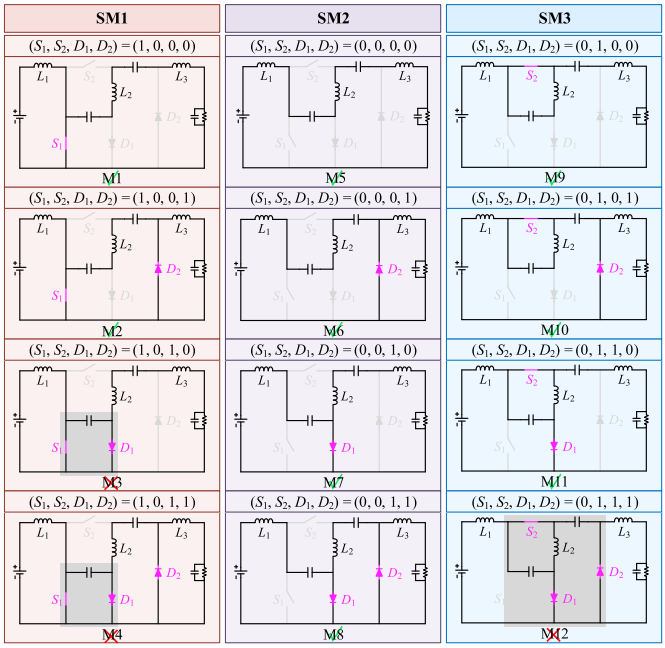

Fig. 9. Equivalent circuits of twelve submodes of EGBBC.

in parallel. For the example converter, $V_{C1} = 0$ in M3 and M4, $V_{C1}-V_{C2} = 0$ in M12 are achieved, which indicates that the capacitors C_1 and C_2 are short circuited as shown in Fig. 9. Therefore, M3, M4, and M12 are judged to be invalid due to the violation of the FCL. Otherwise, voltages of inductors, turn-off switches and diodes would be calculated as a function of the input voltage V_{U1}, output voltage $V_{R1,}$ and capacitor voltages V_{C1}, V_{C2} for the valid submodes

$$\text{diag}\left[MM\_k(m,:)\right] \cdot \left[V_{S1}^m, V_{S2}^m, V_{D1}^m, V_{D2}^m\right]^T = 0 \tag{6}$$

$$\sum_{a\in 1} V_{Ua} + \sum_{b\in 1,2} V_{Cb} + \sum_{c\in 1} V_{Rc} = 0. \tag{7}$$

In addition, for switches/diodes that are turned off, their turn-off current (equal to zero) is calculated in (8), where "¬" is not function operation. For example, as shown in Fig. 8, $i_{S2} = i_{D1} = i_{D2} = 0$ for submode M1, $i_{S2} = i_{D1} = 0$ for submode M2, $i_{S2} = i_{D2} = 0$ for submode M3, $i_{S2} = 0$ for submode M4, etc., are automatically obtained and they are substituted into the general KCL equations in (5) to achieve the specific KCL equations. Likewise, there may be some KCL equations only containing inductor currents as shown in (9), which may cause the converter to work in DCM. For the example converter, it is found that i_{L2}-$i_{L3} = 0$ in M1 and M7, $i_{L1} = i_{L2} = i_{L3}$ in M5, i_{L1}-$i_{L2} = 0$ in M6 and i_{L1}-$i_{L3} = 0$ in M9. As a result, the sum of their derivative is also equal to zero, so that the voltage relationships among these inductors are derived in (10), e.g., $\frac{V_{L2}}{L2} - \frac{V_{L3}}{L3} = 0$ for M1 and M7, $\frac{V_{L1}}{L1} = \frac{V_{L2}}{L2} = \frac{V_{L3}}{L3}$ for M5, $\frac{V_{L1}}{L1} - \frac{V_{L2}}{L2} = 0$ for M6 and $\frac{V_{L1}}{L1} - \frac{V_{L3}}{L3} = 0$ for M9. It is useful for solving the steady-state performance of the converter in DCM operation modes. Otherwise, the current of all components in each valid submode is also automatically achieved in terms of inductor currents i_{L1}–i_{L3}.

$$\text{diag}[\neg MM\_k(m,:)] \cdot [i_{S1}^m, i_{S2}^m, i_{D1}^m, i_{D2}^m]^T = 0 \tag{8}$$

$$\sum_{d\in 1,2,3} i_{Ld}^m(t) = 0 \tag{9}$$

$$\sum_{d\in 1,2,3} \frac{V_{Ld}^m}{L_d} = \sum_{d\in 1,2,3} \frac{di_{Ld}^m(t)}{dt} = 0. \tag{10}$$

C. Automatic Exploration of Workable Operations Based on Power Electronics Principle

After selecting the valid submodes in each switching mode SMk (k = 1, 2, 3), all their possible arrangements to generate various operation modes as analyzed in Section II would be further automatically judged to explore the workable ones on the basis of PEP.

Firstly, the PEP listed in Fig. 3(b) is needed to be expressed in mathematical expressions. Assume that each operation mode consists of N_m ($N_m \geq 2$) submodes in a switching period and the duty cycle of each submode is denoted as d_1, d_2, …, d_{Nm}. As shown in (11), it is required that the average voltage of each inductor L_d (d = 1, 2, 3) in a switching period must be equal to zero. Likewise, it is also required that the average current of each capacitor C_b (b = 1, 2) in a switching period must be equal to zero, as displayed in (12). Besides, from (13), the voltage of load R_1 should be a function of duty cycles. Moreover, in order to avoid abrupt variation in inductor current, the end value of the previous submode should be equal to the initial value of the next submode, as shown in (14). And the sum of the duty cycle of each submode in a switching period is needed to equal to 1, as illustrated in (15). It is noted that V_*^m and I_*^m in (11)–(13) represents the average voltage and current of the component $*$ in the mth submode, which can be calculated as a function of input/output voltages and inductor currents

$$\left[V_{Ld}^1, V_{Ld}^2, \ldots, V_{Ld}^{Nm}\right] \cdot [d_1, d_2, \ldots, d_{Nm}]^T = 0 \tag{11}$$

$$\left[I_{Cb}^1, I_{Cb}^1, \ldots, I_{Cb}^{Nm}\right] \cdot [d_1, d_2, \ldots, d_{Nm}]^T = 0 \tag{12}$$

$$\left[I_{R1}^1, I_{R1}^2, \ldots, I_{R1}^{Nm}\right] \cdot [d_1, d_2, \ldots, d_{Nm}]^T = \frac{V_{R1}}{R_1} \tag{13}$$

$$i_{Ld}^m(d_m \times T) = i_{Ld}^{m+1}(d_m \times T) \tag{14}$$

$$\sum_{m=1}^{Nm} d_m = 1(d_m > 0). \tag{15}$$

Then, by solving PEP (11)–(15) together in the computer program, the inductor currents, capacitor voltages, and output voltage can be conveniently solved, as a function of input voltages, output resistances, and duty cycles. Afterward, voltages and currents of all other components in each submode would be obtained. Among the solved results, it is needed to further judge whether the voltage and current of diodes D_e (e = 1, 2) meet the constraints (16) to guarantee its normal operation

$$\begin{cases} \text{if } i_{De}^m = 0,\ V_{De}^m < 0 \\ \text{if } i_{De}^m > 0,\ V_{De}^m = 0 \end{cases}. \tag{16}$$

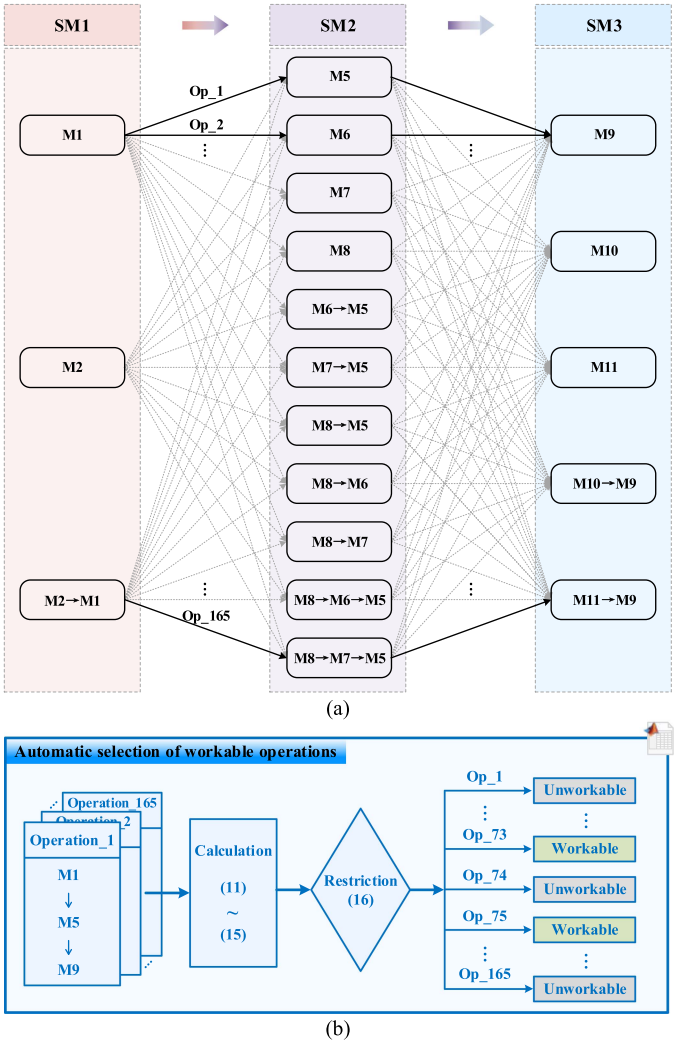

Fig. 10. Automatic selection of workable operations of EGBBC. (a) All possible operations. (b) Implementation schematic.

For the example EGBBC, it is found that in all 3840 possible operation modes calculated by (1), the diode states cannot change from on to off for the example converter in a switching mode according to the analysis results. Therefore, excluding the corresponding operation modes, a total of 165 possible operation modes are derived as follows. Since the valid submodes can appear alone or be combined in each switching mode, there are three permutations in SM1, eleven in SM2 and five in SM3, as shown in Fig. 10(a). Hence, 165 possible operation modes (Op_1–Op_165) in total can be obtained by multiplying three, eleven and five for the example converter. After 165 iterations in the computer program as depicted in Fig. 10(b), 9 workable operation modes Op_73(M2→M8→M11), Op_75(M2→M8→M11→M9), Op_98(M2→M8→M7→M11), Op_100(M2→M8→M7→M11→M9), Op_101(M2→M8→M6→M5→M9), Op_106(M2→M8→M7→M5→M9), Op_123(M2→M1→M7→M11), Op_125(M2→M1→M7→M11→M9), and Op_136(M2→M1→M7→M5→M9) as shown in Fig. 11 are automatically obtained for the example converter.

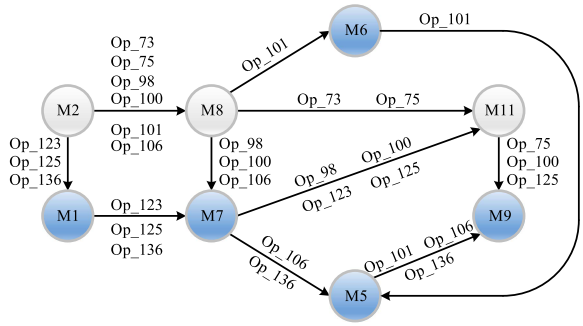

Fig. 11. Different submodes in each workable operation mode of EGBBC.

D. Comparison

From above, the proposed computer-aided automatic analysis method is capable of conveniently discovering all the workable operation modes for converters by considering all possible ON/OFF states of diodes, hence it is more comprehensive than the traditional manual analytic analysis method and the simulation method. For the traditional manual analytic analysis method, it is cumbersome to traverse all diodes' states and combine them to acquire all possible operation modes totally dependent on manual effort. On the other hand, for the simulation method, it can only analyze the converter operation at one operating point at a time and it is difficult to cover all operation modes. Therefore, the conventional manual analysis as well as simulation methods are usually incomprehensive. Besides, in terms of computational time, it is time-consuming to formulate and solve the circuit equations in the conventional manual analysis method, while it is much optimized in the proposed analysis method, e.g., only a few seconds are taken to complete the comprehensive operation modes and steady-state performance analysis for the typical buck or boost converter. Although the calculation time will increase when the converter configuration is getting complex, it is still much less than the manual analysis. Theoretically, the simulation method can quickly achieve the steady-state performance for the converter at one specified operating point, but it will also take a lot of time to randomly modify parameters to acknowledge the steady-state performance of all workable operations. Finally, in terms of accuracy, it is not easy to guarantee the correctness of the steady-state analysis results through manual effort, while it can be ensured in the computer program with the simulation method and the proposed method only if the summarization of FCL and PEP are correct. Therefore, the proposed automatic analysis method is more attractive than the conventional manual analytic analysis and simulation method. As a summary, the overall comparison results among the three analysis methods are listed in Table II.

IV. Comprehensive Operation Analysis Results

In this section, the comprehensive operation considering uncertain states of diodes and their corresponding steady-state performance analysis results of the example EGBBC are illustrated in detail.

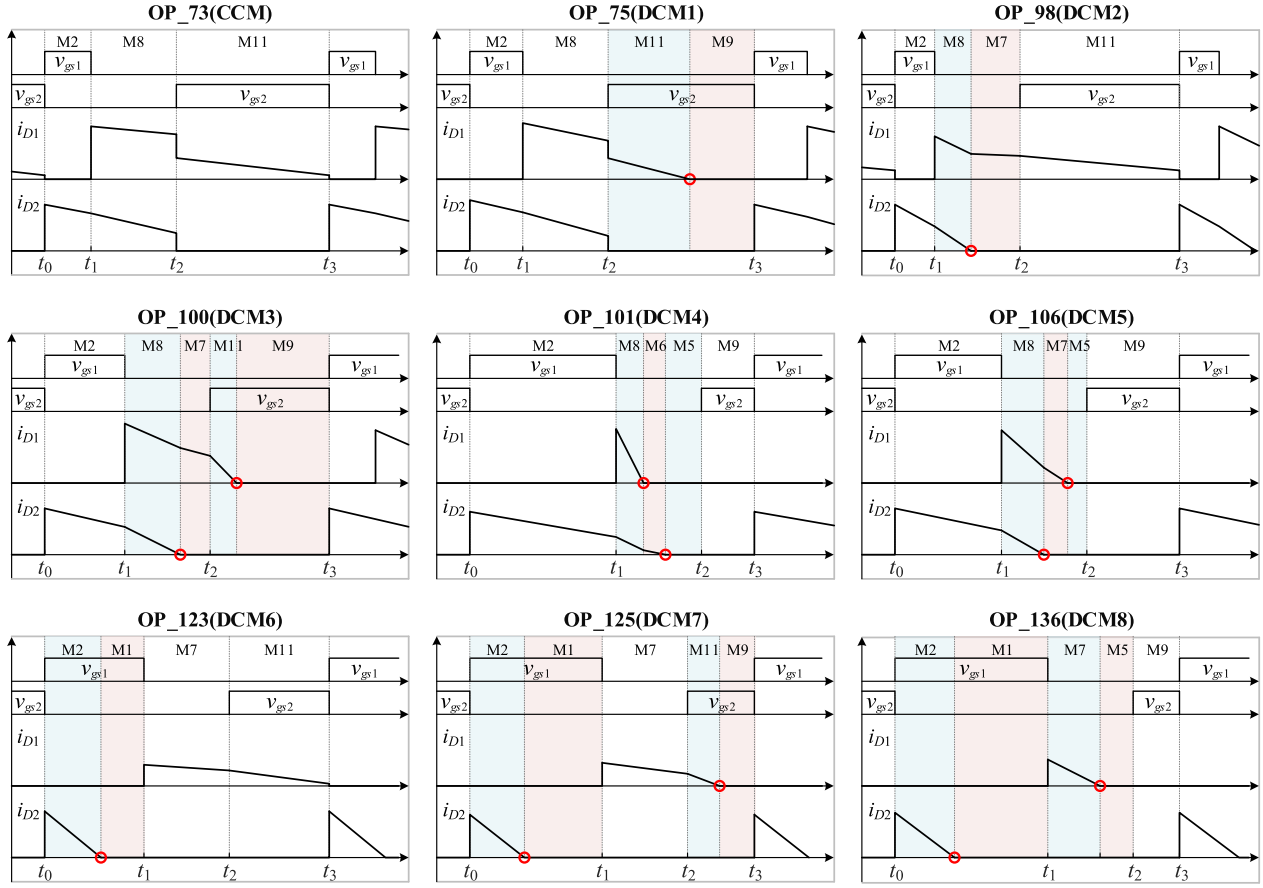

Fig. 12. Steady-state waveforms of v_{gs1}–v_{gs2} and i_{D1}–i_{D2} in nine workable operations of example EGBBC.

TABLE II
COMPARISON OF CONVERTER ANALYSIS METHOD

Method	Comprehensiveness	Speed	Accuracy
Manual Analysis	Incomprehensive	Slow	Uncertain
Simulation Analysis	Incomprehensive	Slow	Accurate
Proposed Automatic Analysis	Comprehensive	Medium	Accurate

A. Comprehensive Operation Modes Analysis Results

For the nine workable operation modes abovementioned, their corresponding drive signals of switches v_{gs1}–v_{gs2} and diode currents i_{D1}–i_{D2} are depicted in Fig. 12 to illustrate the difference between various operation modes caused by the uncertain diode states. For example, in Op_73, the switching mode SM1 during $[t_0, t_1]$, SM2 during $[t_1, t_2]$, and SM3 during $[t_2, t_3]$ has only one submode M2, M8, and M11, since the diodes D_1 and D_2 are always on or off in each switching mode, so the Op_73 operates in CCM. On the other hand, in Op_75, i_{D1} drops to zero between t_2 and t_3 which is discontinuous, and hence there are two submodes M11 and M9 in the switching mode SM3, so the Op_75 operates in DCM. Likewise, both Op_98 and Op_123 operate in DCM with four submodes in a switching period in total. In addition, i_{D2} decays to zero between t_1 and t_2 as well as i_{D1} drops to zero between t_2 and t_3 in Op_100, and hence there are two submodes M8 and M7 in the switching mode SM2 and M11, M9 in the switching mode SM3, so the Op_100 operates in DCM. Similarly, Op_101, Op_106, Op_125, and Op_136 operate in DCM with five submodes in total appear. To sum up, the example converter has nine workable operation modes including one CCM and eight DCM. In the following, Op_73, Op_75, Op_98, Op_100, Op_101, Op_106, Op_123, Op_125, and Op_136 are, respectively, denoted as CCM, DCM1–DCM8.

B. Steady-State Performance Analysis Results of All Workable Operation Modes

While nine workable operation modes are automatically discovered for the converter with the aid of computer program, their corresponding steady-state performance analysis results under arbitrary given system parameters can also be obtained automatically. In order to fully present the steady-state performance analysis results, two working conditions (I and II) that cover all nine workable operation modes are used as examples, and the system parameters of the example EGBBC are set in Table III.

1) Boundaries of Different Workable Operation Modes: The nine workable operation modes CCM, DCM1–DCM8 will appear under working conditions I or II with different input

TABLE III
PARAMETER SPECIFICATIONS

Working Condition I		Working Condition II	
Parameter	Value	Parameter	Value
Switching period T_S	1/75000 s	Switching period T_S	1/75000 s
Output voltage V_{R1}	50 V	Output voltage V_{R1}	50 V
Capacitance C_1	47 μF	Capacitance C_1	47 μF
Capacitance C_2	47 μF	Capacitance C_2	47 μF
Inductance L_1	60 μH	Inductance L_1	360 μH
Inductance L_2	240 μH	Inductance L_2	50 μH
Inductance L_3	150 μH	Inductance L_3	150 μH
Input voltage $V_{U1,\min}$	27 V	Input voltage $V_{U1,\min}$	12 V
Input voltage $V_{U1,\max}$	28 V	Input voltage $V_{U1,\max}$	13 V
Load resistance $R_{1,\min}$	20 Ω	Load resistance $R_{1,\min}$	180 Ω
Load resistance $R_{1,\max}$	40 Ω	Load resistance $R_{1,\max}$	200 Ω

voltage V_{U1} and output load R_1 condition and their boundaries are conveniently derived with the proposed automatic analysis method. From the automatic analysis results, diode currents $i_{D1}(t_3)$ and $i_{D2}(t_2)$ in CCM are solved in (17) and (18), which are determined by input voltage V_{U1} and output load R_1. Then, the boundary of operation CCM as a function of V_{U1} and R_1 can be easily derived through setting $i_{D1}(t_3) = 0$ and $i_{D2}(t_2) = 0$. Likewise, the boundary of eight operations DCM1–DCM8 can be further obtained by setting their diode currents i_{D1} and i_{D2} to be zero at the end of the corresponding submode. As the solution expressions of i_{D1} and i_{D2} in DCMs are complex, they are not shown here. For the working condition I, the example EGBBC can work in CCM, DCM1, DCM3, DCM4, or DCM5, and their boundaries are demonstrated in Fig. 13(a). Similarly, the example EGBBC can work in DCM2, DCM6, DCM7, and DCM8 under working condition II, and their boundaries are also depicted in Fig. 13(b)

$$\begin{aligned} i_{D1}(t_3) = {} & 40L_1L_3V_{R1}\sigma_1(V_{U1}+V_{R1})^2 \\ & + T_S V_{U1}^2 R_1 \left[L_3\left(3V_{U1}-7V_{R1}-\sigma_2\right)+3L_1V_{R1}\right] \\ & + L_1T_SV_{U1}V_{R1}R_1\sigma_1\left(13V_{R1}+\sigma_2\right) \end{aligned} \tag{17}$$

$$\begin{aligned} i_{D2}(t_2) = {} & 120L_1L_2V_{R1}\sigma_3\left[17V_{U1}^2+27V_{R1}^2\right. \\ & \left.+44V_{U1}V_{R1}-\sigma_2\left(V_{U1}+V_{R1}\right)\right] \\ & + T_SV_{U1}R_1\sigma_3V_{U1}^2\left(1765L_1+1918L_2\right) \\ & + T_SV_{U1}R_1\sigma_3V_{R1}^2\left(2375L_1+1820L_2\right) \\ & + T_SV_{U1}R_1\sigma_3V_{U1}V_{R1}\left(4140L_1+2478L_2\right) \\ & + T_SV_{U1}R_1\sigma_3V_{U1}\sigma_2\left(23L_1+14L_2\right) \\ & + T_SV_{U1}R_1\sigma_3V_{R1}\sigma_2\left(23L_1+140L_2\right) \end{aligned} \tag{18}$$

$$\text{where}\begin{cases} \sigma_1 = 1/\sqrt{40L_1L_3V_{U1}R_1(V_{U1}+V_{R1})} \\ \sigma_2 = \sqrt{289V_{U1}^2+169V_{R1}^2+358V_{U1}V_{R1}} \\ \sigma_3 = 1/\sqrt{1680L_1L_2V_{U1}R_1(V_{U1}+V_{R1})} \end{cases}.$$

According to Fig. 13, it indicates that there may be more than one operation mode for a particular working point by setting different duty cycles of switching modeSM1 or SM3, which

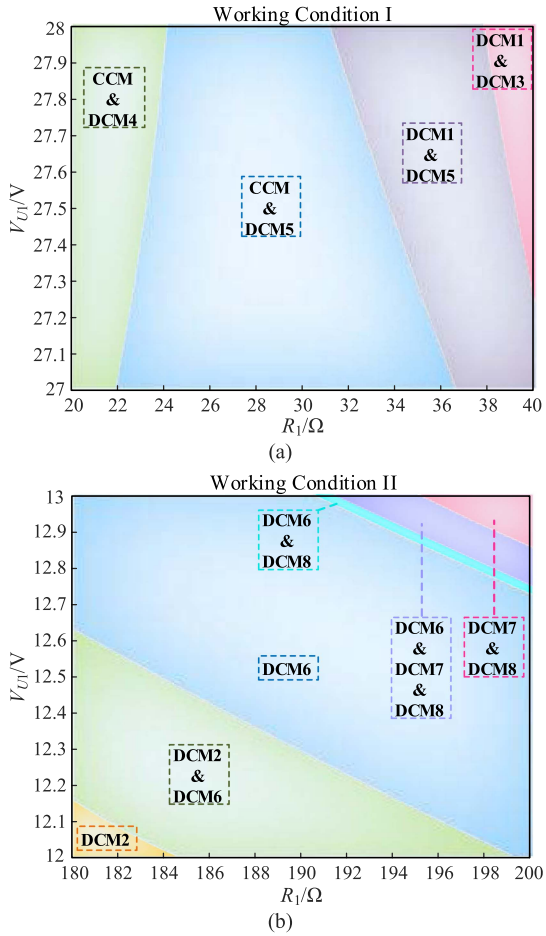

Fig. 13. Boundaries of nine workable operation modes as a function of input voltage V_{U1} and output load R_1 in the example EGBBC under different working conditions. (a) Working condition I. (b) Working condition II.

will exhibit different performance. For example, the EGBBC may operate in DCM6 with the duty cycle of switching mode SM1 $d_{\mathrm{SM1}} = 0.3492$ and that of SM3 $d_{\mathrm{SM3}} = 0.3508$ or DCM7 with $d_{\mathrm{SM1}} = 0.5205$ and $d_{\mathrm{SM3}} = 0.1795$ or DCM8 with $d_{\mathrm{SM1}} = 0.6556$ and $d_{\mathrm{SM3}} = 0.0444$ at the same working point @V_{U1} = 13 V, R_1 = 195 Ω under working conditions II. As shown in Fig. 14, the root-mean-square value of currents of switches S_1–S_2, the average current of diodes D_1–D_2, and the maximum voltage of them in DCM6, DCM7, and DCM8 for the same working point are respectively demonstrated. From Fig. 14, the example converter has smaller voltage stress in DCM6 compared with DCM7 and DCM8. In addition, the performance of the current stress is relatively small in DCM8. And when compromise performance is preferred, DCM7 is a good choice. Therefore, the converter can be designed to operate in the appropriate operation mode according to the application requirements by adjusting the duty cycle of the switching modes.

2) Relationship Between Voltage Gains and Duty Cycles: In addition to the boundaries, the voltage gains as a function of duty cycles in all workable operation modes also can be automatically derived. Since the expressions are also complicated in DCMs, they are not shown here.

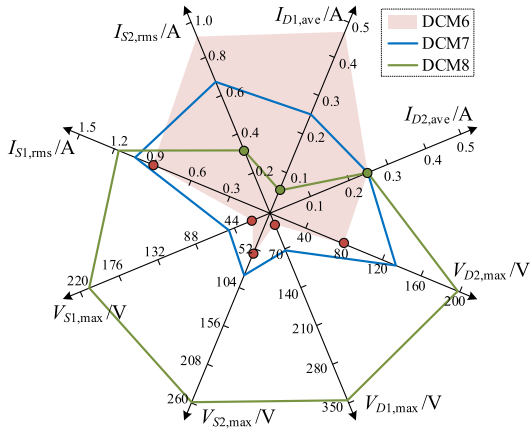

Fig. 14. Performance comparison of different operation modes for the same working point.

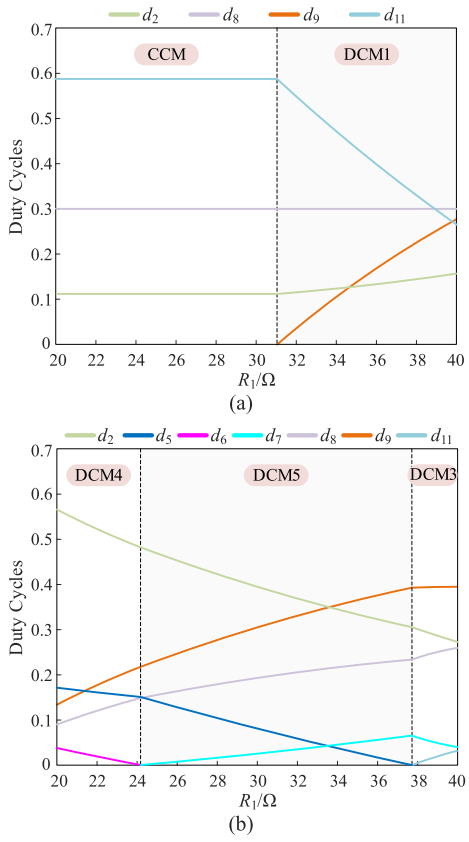

Fig. 15. Duty cycle of each submode in different operation modes as a function of R_1. (a) In CCM and DCM1. (b) In DCM4, DCM5, and DCM3.

For example, according to the solution results, Fig. 15 demonstrates the required duty cycles to achieve rated output voltage V_{R1} with $V_{U1} = 28$ V and different output load R_1 under working condition I. As depicted in Fig. 15(a), there are three submodes M2, M8, and M11 when the EGBBC operates in CCM and their duty cycles d_2, d_8, and d_{11} are constant, which are respectively equal to 0.5876, 0.3, and 0.1124. With the increases of R_1, the EGBBC will operate in DCM1 from CCM and the duty cycle d_9 of new submode M9 will grow from zero. On the other hand, d_2, d_8, and d_{11} will, respectively, increase, remain constant, and decrease as R_1 grows in DCM1. Likewise, as depicted in Fig. 15(b), d_2, d_5, and d_6 will decrease and d_8 and d_9 will increase with the increase of R_1 in DCM4. When d_6 drops to zero, the submode M6 will disappear, then the duty cycle d_7 of the new submode M7 will grow from zero, so the converter is going from DCM4 to DCM5. Similarly, the converter will operate in DCM3 from DCM4 when d_5 drops to zero and M11 emerges. The duty cycle of other submodes will also increase or decrease correspondingly to maintain the rated output voltage as shown in Fig. 15.

TABLE IV
SOLVED COMPONENT CURRENTS IN EACH SUBMODE

	M1	M2	M5	M6	M7	M8	M9	M11
i_{U1}	$-i_{L1}$	$-i_{L1}$	$-i_{L1}$	$-i_{L1}$	$-i_{L1}$	$-i_{L1}$	$-i_{L1}$	$-i_{L1}$
i_{S1}	i_{L2}-i_{L1}	i_{L2}-i_{L1}	0	0	0	0	0	0
i_{S2}	0	0	0	0	0	0	i_{L1}-i_{L2}	i_{L3}-i_{L2}
i_{D1}	0	0	0	0	i_{L1}-i_{L2}	i_{L1}-i_{L2}	0	i_{L1}-i_{L3}
i_{D2}	0	i_{L3}-i_{L2}	0	i_{L3}-i_{L2}	0	i_{L3}-i_{L2}	0	0
i_{C1}	i_{L2}	i_{L2}	i_{L1}	i_{L1}	i_{L1}	i_{L1}	i_{L2}	i_{L1}+i_{L2}-i_{L3}
i_{C2}	i_{L2}	i_{L2}	i_{L2}	i_{L2}	i_{L2}	i_{L2}	i_{L3}	i_{L3}
i_{R1}	$-i_{L3}$	$-i_{L3}$	$-i_{L3}$	$-i_{L3}$	$-i_{L3}$	$-i_{L3}$	$-i_{L3}$	$-i_{L3}$

TABLE V
WORKING PARAMETER OF NINE WORKABLE OPERATION MODES

		V_{U1}(V)	R_1(Ω)	d_{SM1}	d_{SM3}
Working Condition I	CCM	28	30	0.1124	0.5876
	DCM1	28	37	0.1388	0.5612
	DCM3	28	40	0.2718	0.4282
	DCM4	28	20	0.5661	0.1339
	DCM5	27	35	0.3681	0.3319
Working Condition II	DCM2	12	181	0.0917	0.6083
	DCM6	13	190	0.3368	0.3632
	DCM7	13	191	0.4798	0.2202
	DCM8	13	199	0.5919	0.1081

3) Voltage/Current of All Components: First, currents i_{L1}–i_{L3} of inductors L_1–L_3 can be automatically derived according to (11)–(15) in the computer program. Then, for all components in the converter, the solutions of their current are achieved in terms of inductor currents i_{L1}–i_{L3} according to Table IV. Therefore, the current stresses of components can be conveniently obtained, for example EGBBC, which is conductive to the hardware design.

For example, as shown in Fig. 16, the steady-state waveforms of i_{L1}–i_{L3} in CCM and DCM1–DCM8 under working conditions I or II with different input voltage V_{U1}, output load R_1, and duty cycle d_{SM1} and d_{SM3} listed in Table V are conveniently depicted. From Fig. 16, in CCM with submodes M2, M8, and M11, i_{L1} and i_{L3} are divided into two parts with different change slopes and i_{L2} is divided into three parts with different change slopes. In DCM1, the submode M9 is added, during which the change slope of i_{L1} and i_{L3} is different from the previous ones and that of i_{L2} is unchanged. Similarly, with the addition of

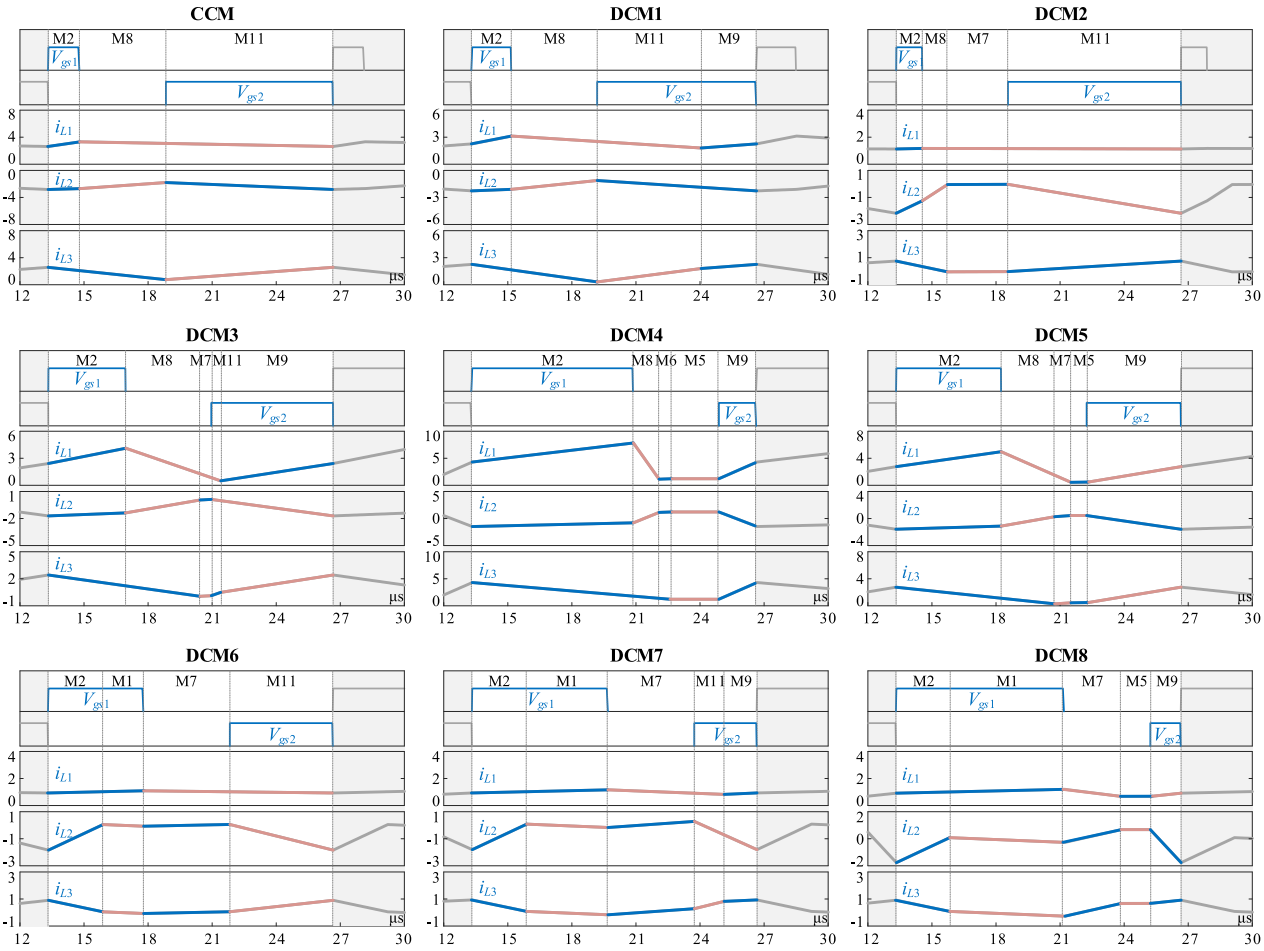

Fig. 16. Calculation results of i_{L1}–i_{L3} in different operation modes.

different submodes in other seven workable operation modes, the change slope of i_{L1}–i_{L3} may be changed accordingly. The calculation results are in well accordance with the equivalent circuit of different submode in Fig. 9.

Second, voltages V_{C1} and V_{C2} of capacitors C_1 and C_2 can be automatically derived according to (11)–(15) in the computer program. As shown in Table VI, under different operation modes, V_{C1} can be calculated as a function of the input voltage V_{U1}, output voltage $V_{R1,}$ and duty cycles of submodes in each operation mode. Furthermore, given that $V_{C1} + V_{C2} = V_{U1} + V_{R1}$, V_{C2} is conveniently obtained by $V_{U1} + V_{R1} - V_{C1}$.

Then, from the automatic analysis results, the voltage of all components in each submode is also automatically acquired as a function of the input voltage V_{U1}, output voltage $V_{R1,}$ and capacitor voltages V_{C1} and V_{C2}, as illustrated in Table VII.

Therefore, the voltage stress of components also can be comprehensively acknowledged, which is conductive to the hardware design. From Table VII, the voltage across different components in submodes M1, M5, M6, M7, and M9 are dependent on the inductance of L_1–L_3 resulting from $i_{L2} - i_{L3} = 0$, $i_{L1} = i_{L2} = i_{L3}$, $i_{L1} - i_{L2} = 0$, $i_{L2} - i_{L3} = 0$ and $i_{L1} - i_{L3} = 0$, respectively. In addition, from the calculation result of inductor voltages, they may change in some submodes, e.g., V_{L2} and V_{L3} are changed in submodes M1 in comparison with M2 while V_{L1} remains unchanged, and hence only the change slope of i_{L2} and i_{L3} are changed in switching mode SM1 while i_{L1} remains unchanged, which is also well matched with Fig. 16.

TABLE VI
SOLVED CAPACITOR VOLTAGE V_{C1} IN EACH OPERATION MODE

	V_{C1}
CCM	$\frac{V_{U1}}{1-d_2}$
DCM1	$\frac{(V_{U1}+V_{R1})(d_2+d_8)}{d_8-d_9-d_{11}}$
DCM2	$\frac{V_{U1}}{1-d_2}$
DCM3	$\frac{V_{U1}L_2d_7+(V_{U1}+V_{R1})(L_2+L_3)(d_2+d_8)}{L_2d_7+(L_2+L_3)(d_8-d_9-d_{11})}$
DCM4	$\frac{V_{R1}(L_1+L_3)(d_2+d_6+d_8)}{-L_3d_9}$
DCM5	$\frac{V_{U1}(L_1+L_3)(d_2+d_7+d_8)}{-L_1d_9+(L_1+L_3)(d_7+d_8)}$
DCM6	$\frac{V_{U1}}{d_7+d_{11}}$
DCM7	$\frac{V_{U1}(L_1+L_3)(1-d_9)}{-L_1d_9+(L_1+L_3)(d_7+d_{11})}$
DCM8	$\frac{V_{U1}(L_1+L_3)(d_1+d_2+d_7)}{L_1(d_7-d_9)+L_3d_7}$

TABLE VII
VOLTAGE OF OTHER COMPONENTS EXPRESSED AS VOLTAGE SOURCE IN EACH SUBMODE

	M1	M2	M5	M6	M7	M8	M9	M11
V_{S1}	0	0	$-\frac{(L_2+L_3)V_{U1}-L_1V_{C1}+L_1V_{C2}+L_1V_{R1}}{L_1+L_2+L_3}$	$-\frac{L_2V_{U1}+L_1V_{C1}+L_1V_{C2}}{L_1+L_2}$	$-V_{C1}$	$-V_{C1}$	$-\frac{L_3V_{U1}+L_1V_{C2}-L_1V_{R1}}{L_1+L_3}$	$-V_{C1}$
V_{S2}	$\frac{L_3V_{C1}-L_2V_{C2}+L_2V_{R1}}{L_2+L_3}$	$-V_{C2}$	$\frac{L_2V_{U1}+(L_1+L_3)V_{C1}-L_2V_{C2}+L_2V_{R1}}{L_1+L_2+L_3}$	$\frac{L_2V_{U1}+L_1V_{C1}-L_2V_{C2}}{L_1+L_2}$	$\frac{(L_2+L_3)V_{C1}-L_2V_{C2}+L_2V_{R1}}{L_2+L_3}$	$V_{C1}-V_{C2}$	0	0
V_{D1}	$-V_{C1}$	$-V_{C1}$	$\frac{(L_2+L_3)V_{U1}-(L_2+L_3)V_{C1}+L_1V_{C2}-L_1V_{R1}}{L_1+L_2+L_3}$	$\frac{L_2V_{U1}-L_2V_{C1}+L_1V_{C2}}{L_1+L_2}$	0	0	$\frac{L_3V_{U1}-(L_1+L_3)V_{C1}+L_1V_{C2}-L_1V_{R1}}{L_1+L_3}$	0
V_{D2}	$\frac{L_3V_{C1}+L_3V_{C2}+L_2V_{R1}}{L_2+L_3}$	0	$-\frac{L_3V_{U1}+L_3V_{C1}+L_3V_{C2}+(L_1+L_2)V_{R1}}{L_1+L_2+L_3}$	0	$\frac{L_3V_{C2}+L_2V_{R1}}{L_2+L_3}$	0	$-\frac{L_3V_{U1}-L_3V_{C2}-L_1V_{R1}}{L_1+L_3}$	$-V_{C1}+V_{C2}$
V_{L1}	V_{U1}	V_{U1}	$\frac{L_1V_{U1}-L_1V_{C1}-L_1V_{C2}+L_1V_{R1}}{L_1+L_2+L_3}$	$\frac{L_1V_{U1}-L_1V_{C1}-L_1V_{C2}}{L_1+L_2}$	$V_{U1}-V_{C1}$	$V_{U1}-V_{C1}$	$\frac{L_1V_{U1}-L_1V_{C2}+L_1V_{R1}}{L_1+L_3}$	$V_{U1}-V_{C1}$
V_{L2}	$-\frac{L_2V_{C1}+L_2V_{C2}-L_2V_{R1}}{L_2+L_3}$	$-V_{C1}-V_{C2}$	$\frac{L_2V_{U1}-L_2V_{C1}-L_2V_{C2}+L_2V_{R1}}{L_1+L_2+L_3}$	$\frac{L_2V_{U1}-L_2V_{C1}-L_2V_{C2}}{L_1+L_2}$	$\frac{L_2V_{C2}+L_2V_{R1}}{L_2+L_3}$	$-V_{C2}$	$-V_{C1}$	$-V_{C1}$
V_{L3}	$-\frac{L_3V_{C1}+L_3V_{C2}-L_3V_{R1}}{L_2+L_3}$	V_{R1}	$\frac{L_3V_{U1}-L_3V_{C1}-L_3V_{C2}+L_3V_{R1}}{L_1+L_2+L_3}$	V_{R1}	$-\frac{L_3V_{C2}+L_3V_{R1}}{L_2+L_3}$	V_{R1}	$\frac{L_3V_{U1}-L_3V_{C2}+L_3V_{R1}}{L_1+L_3}$	$V_{C1}-V_{C2}+V_{R1}$

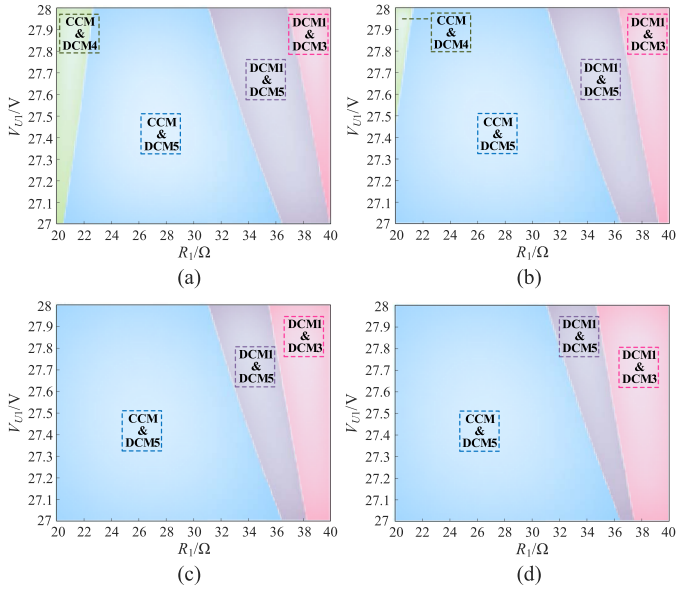

Fig. 17. Boundaries of different workable operation modes as L_2 degrades in the example EGBBC. (a) $|\Delta L_2|/L_2 = 5\%$. (b) $|\Delta L_2|/L_2 = 10\%$. (c) $|\Delta L_2|/L_2 = 15\%$. (d) $|\Delta L_2|/L_2 = 20\%$.

4) Influence of Inductor Degradation: Besides, the influence of component degradation on the converter performance also can be conveniently obtained with the proposed automatic analysis method, which is also beneficial for the component design of the converter in the practical application.

Fig. 17 demonstrates the change of boundaries when the EGBBC operates under working condition I with all system parameters in Table III except for the degradation of L_2. Comparing Fig. 13(a) with Fig. 17(a)–(d), it indicates that as the inductance of L_2 degrades, the areas of CCM will remain unchanged, which can also be explained according to the expressions (17) and (18) of $i_{D1}(t_3)$ and $i_{D2}(t_2)$. Since (17) does not include L_2 and (18) will always be greater than zero within the range of L_2 degrading to 20%, the boundary of CCM will not be affected by L_2 degradation. On the other hand, from the comparison of Fig. 17(a) with Fig. 17(b), the area of DCM4 will taper as L_2 degrades. Until L_2 degrades to 15%, DCM4 has disappeared in Fig. 17(c). In addition, as the degradation of L_2, the area of DCM1 and DCM3 will enlarge and that of DCM1 and DCM5 will shrink as depicted in Fig. 17(a)–(d).

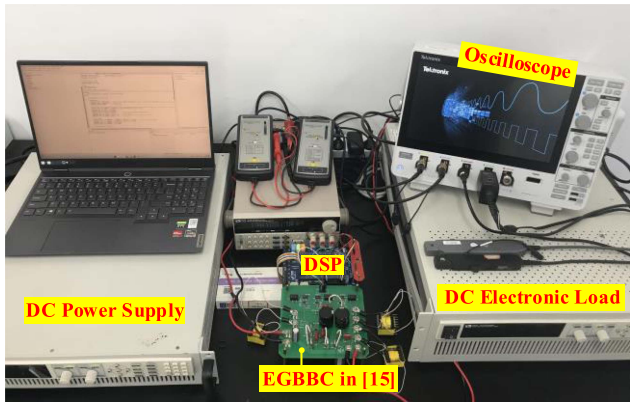

Fig. 18. Photograph of experimental platform.

V. EXPERIMENT VERIFICATION

To verify the theoretical analysis of the proposed computer-aided automatic analysis method, an experimental platform shown in Fig. 18 with the system parameters in Table III is built. The input source of the prototype employs a dc power supply IT6526C from ITECH, and a dc electronic load IT8816 from ITECH is used as the load. Switches S_1–S_2 and diodes D_1–D_2, respectively, use IPA60R080P7XKSA1 and IDH04G65C6 in the prototype circuit. All control signals are generated by TMS320F28335.

According to the theoretical analysis results in Section IV, the EGBBC can operate in CCM and DCM1–DCM8 with different system parameters and eight operation modes except DCM4, in which the voltage stress of switches S_1–S_2 and diodes D_1–D_2 are very high, are selected to be verified. The

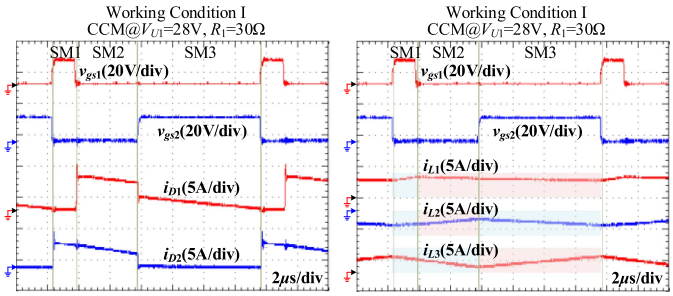

Fig. 19. Steady-state waveforms in CCM. (a) v_{gs1}, v_{gs2}, i_{D1}, i_{D2}. (b) v_{gs1}, v_{gs2}, i_{L1}, i_{L2}, i_{L3}.

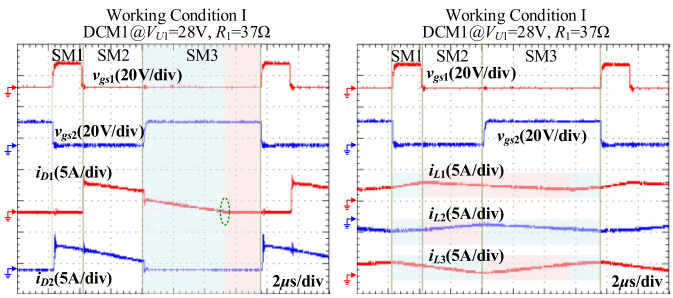

Fig. 20. Steady-state waveforms in DCM1. (a) v_{gs1}, v_{gs2}, i_{D1}, i_{D2}. (b) v_{gs1}, v_{gs2}, i_{L1}, i_{L2}, i_{L3}.

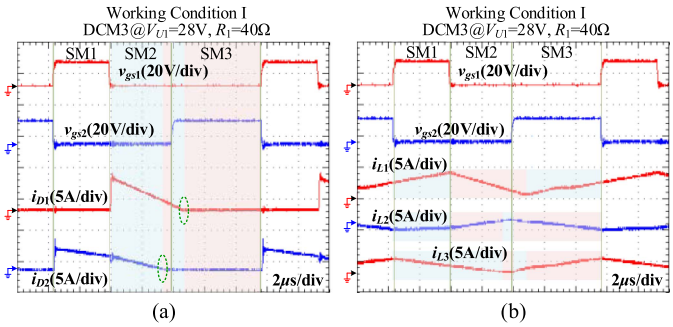

Fig. 21. Steady-state waveforms in DCM3. (a) v_{gs1}, v_{gs2}, i_{D1}, i_{D2}. (b) v_{gs1}, v_{gs2}, i_{L1}, i_{L2}, i_{L3}.

steady-state waveforms of operation modes CCM, DCM1, DCM3, DCM5 under working condition I and DCM2, DCM6, DCM7, DCM8 under working condition II are, respectively, depicted in Figs. 19–26, including the driving signals v_{gs1}–v_{gs2}, the diode currents i_{D1}–i_{D2} and the inductor currents i_{L1}–i_{L3}. They are in good agreement with the theoretical analysis.

From Table V, the EGBBC will operate in CCM @V_{U1} = 28 V and R_1 = 30 Ω with $d_{\rm SM1}$ = 0.1124 and $d_{\rm SM3}$ = 0.5876. From the experimental waveforms Fig. 19(a), the diode current i_{D1} is equal to zero in switching mode SM1, and it is always greater than zero in switching mode SM2 and SM3. The diode current i_{D2} is always greater than zero in switching mode SM1 and SM2, and it is equal to zero in switching mode SM3.

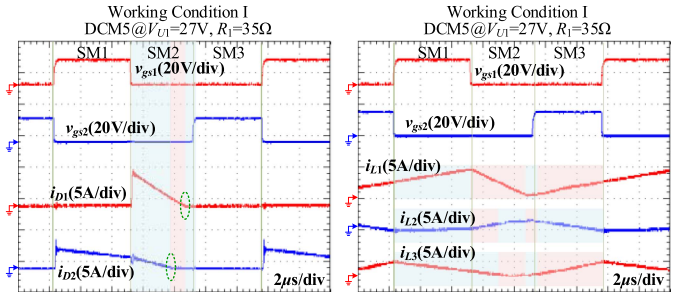

Fig. 22. Steady-state waveforms in DCM5 (a) v_{gs1}, v_{gs2}, i_{D1}, i_{D2}. (b) v_{gs1}, v_{gs2}, i_{L1}, i_{L2}, i_{L3}.

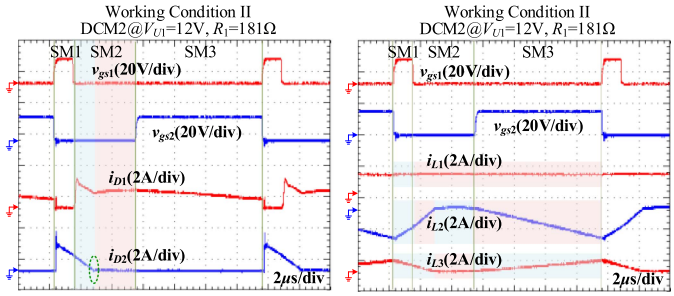

Fig. 23. Steady-state waveforms in DCM2. (a) v_{gs1}, v_{gs2}, i_{D1}, i_{D2}. (b) v_{gs1}, v_{gs2}, i_{L1}, i_{L2}, i_{L3}.

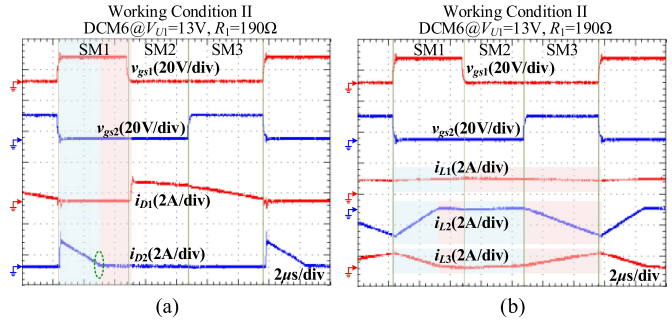

Fig. 24. Steady-state waveforms in DCM6. (a) v_{gs1}, v_{gs2}, i_{D1}, i_{D2}. (b) v_{gs1}, v_{gs2}, i_{L1}, i_{L2}, i_{L3}.

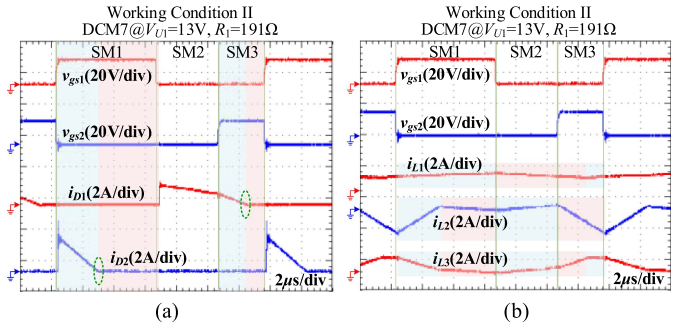

Fig. 25. Steady-state waveforms in DCM7. (a) v_{gs1}, v_{gs2}, i_{D1}, i_{D2}. (b) v_{gs1}, v_{gs2}, i_{L1}, i_{L2}, i_{L3}.

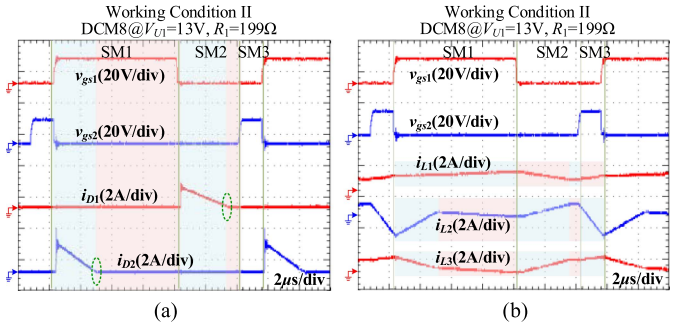

Fig. 26. Steady-state waveforms in DCM8. (a) v_{gs1}, v_{gs2}, i_{D1}, i_{D2}. (b) v_{gs1}, v_{gs2}, i_{L1}, i_{L2}, i_{L3}.

Therefore, since the state of diodes D_1 and D_2 has not changed in each switching mode, the EGBBC is proven to operate in CCM. On the other hand, from Fig. 19(b), the inductor currents i_{L1}–i_{L3}, respectively, are divided into two parts, three parts, and two parts with different change slope, which is also well matched with the theoretical analysis in Fig. 16. In addition to CCM operation mode, DCM operation modes derived from the proposed comprehensive operation analysis method are also verified. As depicted in Fig. 20(a), when the input voltage V_{U1} is held at 28 V and the output load R_1 is increased to 37 Ω with the duty cycles $d_{\rm SM1} = 0.1388$ and $d_{\rm SM3} = 0.5612$, the state of diode D_1 in switching modes SM1–SM2 and D_2 in SM1–SM3 is the same as in CCM. However, the diode current i_{D1} will drop to zero from positive in switching mode SM3 which is discontinuous and a new submode emerges, so the EGBBC is proven to operate in DCM1. Likewise, as shown in Fig. 20(b), during the new submode, the change slope of i_{L1} and i_{L3} is different from the previous ones and that of i_{L2} is unchanged, which is well corresponded with Fig. 16 too. In addition, as shown in Fig. 21(a), when the output load R_1 is further increased to 40 Ω and the input voltage V_{U1} is still maintained at 28 V with the duty cycles $d_{\rm SM1} = 0.2718$ and $d_{\rm SM3} = 0.4282$, the diode current i_{D1} is equal to zero in switching modes SM1 and it is greater than zero in SM2, but it will decrease to zero from positive in SM3. The diode current i_{D2} is greater than zero in switching modes SM1 and it is equal to zero in SM3, but it will decrease to zero from positive in SM2. Therefore, the EGBBC is proven to operate in DCM3 in which both the i_{D1} and i_{D2} are discontinuous. Furthermore, when the input voltage V_{U1} descends to 27 V and output load R_1 descends to 35 Ω with the duty cycles $d_{\rm SM1} = 0.3681$ and $d_{\rm SM3} = 0.3319$, as shown in Fig. 22(a), both the diode currents i_{D1} and i_{D2} will drop to zero from positive, so the EGBBC is proven to operate in DCM5. Likewise, from Figs. 23–26, the feasibility of DCM2, DCM6, DCM7, and DCM8 are also verified, for example EGBBC, respectively, with the diode current i_{D1} being discontinuous in switching mode SM2, i_{D1} being discontinuous in SM1, i_{D1}/i_{D2} being discontinuous in SM3/SM1, and i_{D1}/i_{D2} being discontinuous in SM2/SM1.

From the above, the effectiveness of the proposed computer-aided automatic analysis method is verified. Through this method, the comprehensive operation modes analysis for the converter is able to be accomplished considering all states of diodes, which is not only in favor of converter design but also engineering applications.

VI. Conclusion

In this article, a computer-aided automatic analysis method of dc–dc converters is proposed, which utilizes the typical ENT to mathematically model the converter, and then automatically discovers all the valid submodes and workable operation modes by considering all possible ON/OFF states of diodes according to the FCL and PEP. Besides, the steady-state performance of the converter working in different operation modes is also automatically obtained simultaneously. Therefore, the proposed method is capable of conveniently implementing comprehensive operation analysis for converters. It is expected to be a favorable substitutive for the conventional manual analysis method which is usually incomplete and inefficient in practical applications, especially when a large number of converters are needed to be wholly acknowledged to perform topology comparison and converter design.

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