Comprehensive Analysis and Optimization of Parasitic Capacitance on Conducted EMI and Switching Losses in Hybrid-Packaged SiC Power Modules

Yifan Zhang, Yue Xie, Cai Chen, *Member, IEEE*, Xinyue Guo, Yiyang Yan, Lei Yang, and Yong Kang, *Fellow, IEEE*

***Abstract*—The high switching speeds of Wide BandGap (WBG) devices promise further breakthroughs in the development of power modules. However, parasitic parameters bring more adverse effects at high-speed switching conditions, which makes WBG bring more power loss and ElectroMagnetic Interference (EMI) problems. In this article, a 1200-V/24-A SiC half-bridge power module is presented with ultralow parasitic capacitance and inductance for low common-mode (CM) EMI and low power loss. This module is designed from a stacked substrate hybrid package structure by optimizing the layout pattern. The effects of parasitic capacitance on the switching loss and conducted EMI of SiC devices are comprehensively investigated based on the analysis models. And the parasitic capacitance reduction methods and the tradeoff optimization for geometrical parameters are given accordingly. The power module's layout is designed, optimized, and fabricated based on the analysis results. The proposed SiC half-bridge module reduces CM current by 17 dB and total switching loss by 28.5% compared to discrete devices. Experimental results validate the superior performance of the optimized module.**

***Index Terms*—ElectroMagnetic Interference (EMI), packaging structure, parasitic parameters, power module, switching loss.**

I. Introduction

With the development of Wide BandGap (WBG) devices, such as GaN and SiC devices, the field of power electronics has witnessed a new round of changes [1], [2]. WBG devices possess higher bandgap energy, higher breakdown electric field strength, and higher electron saturation drift velocity compared to traditional silicon devices. These physical characteristics enable switch devices based on WBG semiconductors to exhibit faster switching speed, lower ON-resistance, and higher voltage withstand capability. However, the high-speed switching performance of WBG devices poses numerous challenges in device packaging and power electronics system design. The impact of parasitic parameters on switching performance intensifies, and high-frequency operation leads to increased switch losses [3]. The combination of high switching speed and frequency also exacerbates ElectroMagnetic Compatibility (EMC) issues in the system [4].

Existing studies have done much work to address ElectroMagnetic Interference (EMI) issues by optimizing circuit topology and circuit parameters [5], optimizing modulation [6], and optimizing EMI filter design [7]. But these solutions may increase switching losses, control complexity, and the passive components' size. The WBG power module is the core component of new power electronic converter systems. If the WBG power module can be optimized to suppress EMI noise, the complexity of the external circuits' design can be greatly reduced. However, the lack of comprehensive consideration of many good optimization methods for reducing EMI has hindered its application in WBG power modules. For example, H-bridge diode rectifier modules based on a vertical package structure can significantly reduce common-mode (CM) EMI [8], but heat dissipation issues can hinder their application in SiC MOSFET power modules. In addition, there are some efforts to integrate capacitors in power modules for filtering or decoupling [16] or introducing additional bridge arms for active filtering [17], but this approach requires additional components and terminals inside the power module, increasing the size and complexity of the power module.

The fast-switching performance of SiC devices allows the system to operate at a high switching frequency, and thus achieve the goal of high power density. However, the bad effect of parasitic parameters on switching loss and EMI can be more significant in high frequency. Therefore, it is necessary to reduce EMI and switching losses in the direction of optimizing the packing structure and reducing the parasitic parameters.

Existing research works for performance enhancement of SiC power modules can be mainly classified into three categories: improved wire bonding structures [9], [10], planar interconnection structures [11], [12], and hybrid packaging structures [13],

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Yifan Zhang, Yue Xie, Cai Chen, Xinyue Guo, Yiyang Yan, and Yong Kang are with the School of Electrical and Electronic Engineering, Huazhong University of Science and Technology, Wuhan 430074, China (e-mail: z_yifan@hust.edu.cn; xie_yue@hust.edu.cn; caichen@hust.edu.cn; xinyueguo@hust.edu.cn; yanyiyang@hust.edu.cn; ykang@hust.edu.cn).

Lei Yang is with the Beijing Institute of Precision Mechatronics and Controls, Beijing 100076, China (e-mail: ylforeverbit@126.com).

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[15]. Among these, the improved wire bonding structure offers a simple process but fails to effectively reduce the parasitic inductance of the module. The planar interconnection structure enables 3-D commutation paths to optimize the parasitic inductance, but it entails complex fabrication processes, high costs, and concerns regarding reliability. To simultaneously meet the requirements of reduced parasitic inductance, simplified fabrication, and high reliability, a hybrid packaging structure was proposed in [13]. The hybrid packaging structure combines the advantages of wire bonding and planar interconnection structures, improving the 2-D commutation path of the wire bonding structure into a 3-D one, effectively reducing the parasitic inductance of the commutation path while achieving lower process complexity.

Reducing the parasitic parameters requires modeling and analysis. Optimizing the EMI source and the conduction path is the main method of EMC optimization for power electronic systems. The drain-source voltage of the SiC devices in the power electronic system is considered as the source of EMI. The path between the switching devices and the EMI receiver in the power electronics system is the conduction path of EMI. The analysis and optimization of the EMI source require the establishment of an accurate switching model of the switching device. The parameters of the switching device are needed in this model. And the influence of each parameter on the switching transient waveform can be calculated and analyzed through this model. As for the analysis of the parasitic parameters on EMI conduction path, an accurate EMC model is required. The switching losses of power electronic systems need to be calculated from the switching waveforms [18]. So, an accurate switching model is needed for analyzing and optimization of parasitic parameters.

The parasitic parameters brought by the package structure are mainly divided into parasitic inductance and capacitance. Regarding the influence of parasitic inductance on SiC devices, the drain inductance increases the turn-OFF overvoltage and the common-source inductance increases switching loss as per Chen et al. [3]. Research works [19] specified that the parasitic inductance would significantly increase the overvoltage and the oscillation amplitude of SiC devices. In [20], the influence of power module's parasitic parameters on switching oscillations has been studied in detail. In [21] and [22], the influence of parasitic inductance has been studied through theoretical analysis and circuit simulation, and the same conclusion as earlier is obtained. The work in [23] and [24] presents the design of a SiC power module with a reduced length of the commutation loop through the utilization of a 3-D package layout. This design approach effectively mitigates parasitic inductance, leading to an enhanced switching speed. Regarding the effect of parasitic capacitance, the effect of ground capacitance on CM EMI was analyzed using a frequency domain model in a boost converter [25]. The study in [26] found that the parasitic capacitance in the integrated power module provides a path for the voltage disturbance in the main power circuit to propagate to the driver circuit. The parasitic capacitance in high-voltage SiC modules increases the switching overcurrent as per [27]. There are some researches aimed at reducing the parasitic capacitance in the power module's EMC optimization. The study in [27] provides a module with a decreased area of the copper layer to reduce the output to ground capacitance. The CM current in SiC power module is greatly reduced in this way. Research works in [28] reduced the output to ground capacitance by the technique of flip-flop soldering the chip. Experimental results show that the CM EMI generated by the module is greatly reduced. In [29], a double-layer ceramic substrate structure is proposed, and the output to ground capacitance is reduced by the shielding effect, and CM EMI is suppressed. The chip-on-chip structure proposed in [30], [31], and [32] also uses the shielding effect to reduce the CM EMI. In this structure, SiC chips are placed in stacks and DBC substrates are located on both sides. The output copper layer is shielded by the positive and negative copper layers, thus a very low output to ground capacitance can be achieved.

Among the existing studies on parasitic parameters of power modules, the reduction of parasitic inductance effects by optimizing the structure is relatively well studied. However, there are relatively few studies based on the structural optimization of hybrid-packaged power modules to reduce parasitic capacitance, improve EMC level, and reduce losses. The stacked substrate hybrid package structure proposed in the paper [33] has both low parasitic inductance and low parasitic capacitance, showing a small CM EMI. However, the advantages of low parasitic capacitance in this research only exist when the module's size is small, and the optimization principle and the detailed optimization method are not given. In addition, parasitic inductance and capacitance optimization interfere with each other in traditional module packaging [34].

This article presents a 1200-V/24-A hybrid package SiC power module with comprehensively optimized parasitic parameters. The optimization method proposed in this article can be applied to other three-dimensional package structures. The rest of this article is organized as follows. In Section II, the effects of parasitic parameters on switching losses and EMI are investigated in detail based on the switching model and EMI analysis model of SiC devices. Next, a comprehensive optimization method to reduce parasitic capacitance, parasitic inductance, and geometric parameters is given in Section III. And by optimizing the hybrid package module's layout, a partially shielded (PS) structure of the power module with low EMI and low switching loss is designed and fabricated. Experimental results in Section IV show the advantages of the PS module in low EMI and low switching losses. Finally, Section V concludes this article.

II. Analysis of Parasitic Parameters of SiC Power Module

This section studies the effect of parasitic capacitance in a buck circuit with a half-bridge power supply module. First, the effect of parasitic capacitance on the EMI conduction path is analyzed by an EMI analysis model. Then, the effect of parasitic capacitance on the switching performance is analyzed by the switching model of the SiC device.

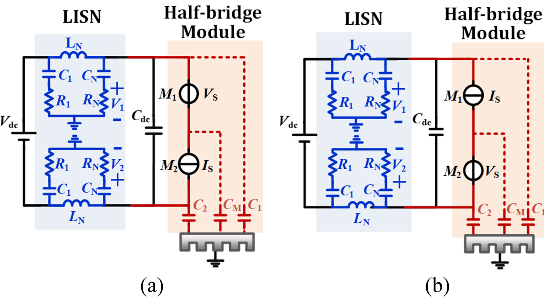
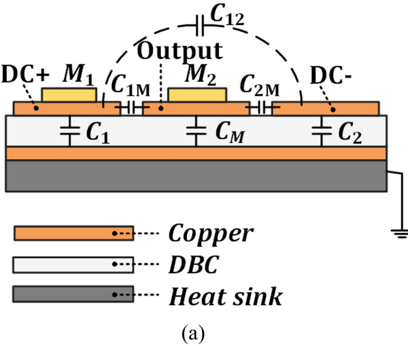


Fig. 1. EMI frequency domain analysis model of buck circuit. (a) HVLC equivalent circuit. (b) HCLV equivalent circuit.



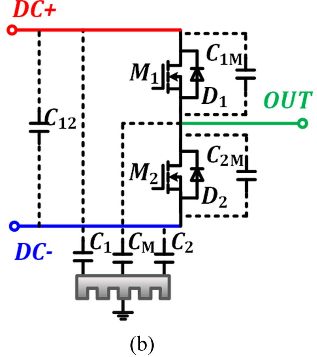


Fig. 2. Internal parasitic capacitance and equivalent circuit of SiC half-bridge module. (a) Schematic diagram of parasitic capacitance inside the power module. (b) SiC half-bridge module circuit model considering parasitic capacitance.

A. Analysis of Parasitic Capacitance on EMI

EMI analysis model is the most widely used method to analyze the principles of EMI. The EMI analysis model typically falls into two categories: time domain and frequency domain analyses. The time domain model is simulated using circuit simulation software, and the obtained time domain results are transformed into EMI spectra by fast Fourier transform (FFT) [35], [36]. The time domain analysis method is computationally accurate but time-consuming and not intuitive. Frequency domain analysis model divides the circuit into EMI sources and conduction paths for separate calculations. The final results of the frequency domain analysis model are calculated by frequency domain calculations [37]. This method is faster and can demonstrate the effect of parameters on EMI.

Although the nonideal nature of the actual noise source limits the accuracy, this can be solved by calculating the transient characteristics of the switching waveform [38].

In this section, the frequency domain analysis method proposed in [39] is referred for modeling, as shown in Fig. 1. In this model, the lower switch M_2 acts as the active tube. M_2, which is ON, can be equated as an equivalent low-resistance voltage source, and M_2, which is OFF, can be equated as a high-resistance current source. Based on this, two equivalent circuits can be built for the High-side Voltage source and Low-side Current source (HVLC) equivalent circuit, and the High-side Current source and Low-side Voltage source (HCLV) circuit. The CM and differential-mode (DM) EMIs calculated from the model are ${V^{HVLC}}_{CM}(s)$, ${V^{HCLV}}_{CM}(s)$, ${V^{HVLC}}_{DM}(s)$, and ${V^{HCLV}}_{DM}(s)$. Equations (1) and (2) are the function of switching mode, and they are convolved with the calculation results of the equivalent circuits in the frequency domain. Equations (3) and (4) show the final computation formula of the equivalent circuit

$$f_{\mathrm{HVLC}}(t) = \begin{cases} 1 & \text{When } M_2 \text{ is OFF} \\ 0 & \text{When } M_2 \text{ is ON} \end{cases} \tag{1}$$

$$f_{\mathrm{HCLV}}(t) = \begin{cases} 1 & \text{When } M_2 \text{ is ON} \\ 0 & \text{When } M_2 \text{ is OFF} \end{cases} \tag{2}$$

$$V_{\mathrm{CM}}(s) = V_{\mathrm{CM}}^{\mathrm{HVLC}}(s) * F(f_{\mathrm{HVLC}}(t)) + V_{\mathrm{CM}}^{\mathrm{HCLV}}(s) * F(f_{\mathrm{HCLV}}(t)) \tag{3}$$

$$V_{\mathrm{DM}}(s) = V_{\mathrm{DM}}^{\mathrm{HVLC}}(s) * F(f_{\mathrm{HVLC}}(t)) + V_{\mathrm{DM}}^{\mathrm{HCLV}}(s) * F(f_{\mathrm{HCLV}}(t)). \tag{4}$$

Formulas (5)–(8) illustrate the mechanism of parasitic parameters on the conducted EMI

$$V_{\mathrm{CM}}^{\mathrm{HVLC}}(s) = F_{\mathrm{CM_v}}^{\mathrm{HVLC}}(s)V_{\mathrm{S}}(s) + F_{\mathrm{CM_i}}^{\mathrm{HVLC}}(s)I_{\mathrm{S}}(s) \tag{5}$$

$$V_{\mathrm{DM}}^{\mathrm{HVLC}}(s) = F_{\mathrm{DM_v}}^{\mathrm{HVLC}}(s)V_{\mathrm{S}}(s) + F_{\mathrm{DM_i}}^{\mathrm{HVLC}}(s)I_{\mathrm{S}}(s) \tag{6}$$

$$V_{\mathrm{CM}}^{\mathrm{HCLV}}(s) = F_{\mathrm{CM_v}}^{\mathrm{HCLV}}(s)V_{\mathrm{S}}(s) + F_{\mathrm{CM_i}}^{\mathrm{HCLV}}(s)I_{\mathrm{S}}(s) \tag{7}$$

$$V_{\mathrm{DM}}^{\mathrm{HCLV}}(s) = F_{\mathrm{DM_v}}^{\mathrm{HCLV}}(s)V_{\mathrm{S}}(s) + F_{\mathrm{DM_i}}^{\mathrm{HCLV}}(s)I_{\mathrm{S}}(s). \tag{8}$$

The noise source and conduction path in the model are separated for analysis, where ${F^{HVLC}}_{CM\cdot v}(s)$, ${F^{HVLC}}_{CM\cdot i}(s)$, ${F^{HVLC}}_{DM\cdot v}(s)$, and ${F^{HVLC}}_{DM\cdot i}(s)$ are the transfer function of the voltage noise source $V_S(s)$ and current noise source $I_S(s)$ to CM voltage ${V^{HVLC}}_{CM}(s)$ and DM voltage ${V^{HVLC}}_{DM}(s)$ in HVLC equivalent circuit, and ${F^{HCLV}}_{CM\cdot v}(s)$, ${F^{HCLV}}_{CM\cdot i}(s)$, ${F^{HCLV}}_{DM\cdot v}(s)$, and ${F^{HCLV}}_{DM\cdot i}(s)$ are the transfer function of the voltage noise source $V_S(s)$ and current noise source $I_S(s)$ to CM voltage ${V^{HCLV}}_{CM}(s)$ and DM voltage ${V^{HCLV}}_{DM}(s)$ in HCLV equivalent circuit. By solving the transfer function, the conduction path and the noise source can be analyzed separately.

The parasitic capacitance of the module is shown in Fig. 2. In this figure, C_{12} is the half-bridge module positive–negative parasitic capacitance, C_{1M} is the half-bridge module positive-output parasitic capacitance, C_{2M} is the half-bridge module negative-output parasitic capacitance, C_1 is the half-bridge module positive-to-ground capacitance, C_2 is the half-bridge module negative-to-ground capacitance, and C_M is the half-bridge module output-to-ground capacitance.

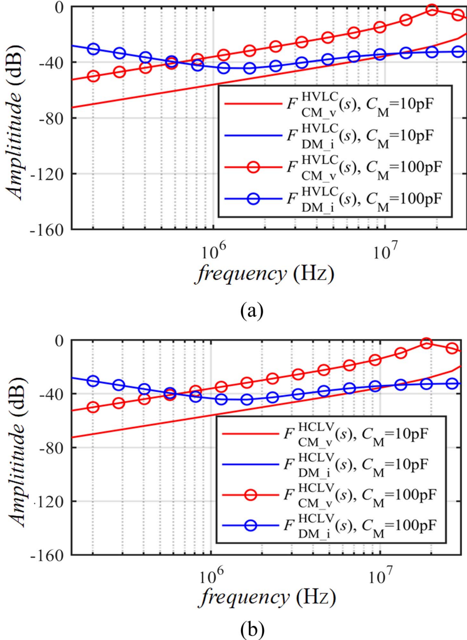


Fig. 3. Influence of output-to-ground capacitance C_{M} on the transfer function of EMI conduction path. (a) HVLC equivalent circuit. (b) HCLV equivalent circuit.

According to the frequency domain analysis model, the influence of C_{M}, C_1, and C_2 inside the module on the EMI conduction path is analyzed. In accordance with the frequency range specified in the international standard CISPR 11 for conducted EMI, the analysis is conducted on the transfer function of EMI within the frequency range of 150 kHz to 30 MHz. Change the output-to-ground capacitance C_{M}, and the resulting transfer function is shown in Fig. 3. When C_{M} increases from 10 to 100 pF, $F^{\mathrm{HVLC}}{}_{\mathrm{DM\cdot i}}(\mathrm{s})$ and $F^{\mathrm{HCLV}}{}_{\mathrm{DM\cdot i}}(s)$ do not change. This result means that the ground capacitance C_{M} will not affect the conduction path of DM EMI. And when C_{M} increases from 10 to 100 pF, $F^{\mathrm{HVLC}}{}_{\mathrm{CM\cdot v}}(s)$ and $F^{\mathrm{HCLV}}{}_{\mathrm{CM\cdot v}}(\mathrm{s})$ both increase by around 20 dB. The results in Fig. 3 show that C_{M} dominates the conduction path of CM EMI. And reducing C_{M} can significantly suppress CM EMI.

Fig. 4 shows the influence of the dc- to ground capacitances C_1 and C_2 on the EMI conduction path's transfer function. It can be seen that C_1 and C_2 only have little effect on $F^{\mathrm{HVLC}}{}_{\mathrm{DM\cdot i}}(s)$ and $F^{\mathrm{HCLV}}{}_{\mathrm{DM\cdot i}}(s)$. The value of C_1 and C_2 almost have no effect on $F^{\mathrm{HVLC}}{}_{\mathrm{CM\cdot v}}(s)$ and $F^{\mathrm{HCLV}}{}_{\mathrm{CM\cdot v}}(s)$ in the frequency range below 10 MHz. In the frequency range between 10 and 30 MHz, C_1 and C_2 have little effect on $F^{\mathrm{HVLC}}{}_{\mathrm{CM\cdot v}}(s)$ and $F^{\mathrm{HCLV}}{}_{\mathrm{CM\cdot v}}(s)$. The result in Figs. 3 and 4 shows the influence of the parasitic capacitance in the SiC power module. According to Fig. 3, C_{M} will have a decisive influence on the CM EMI. The results in Fig. 4 indicate that the influence of C_1 and C_2 on the conducted EMI path is not as significant as C_{M}. Therefore, reducing C_{M} in the design of the SiC module packaging is of great help to reduce CM EMI.

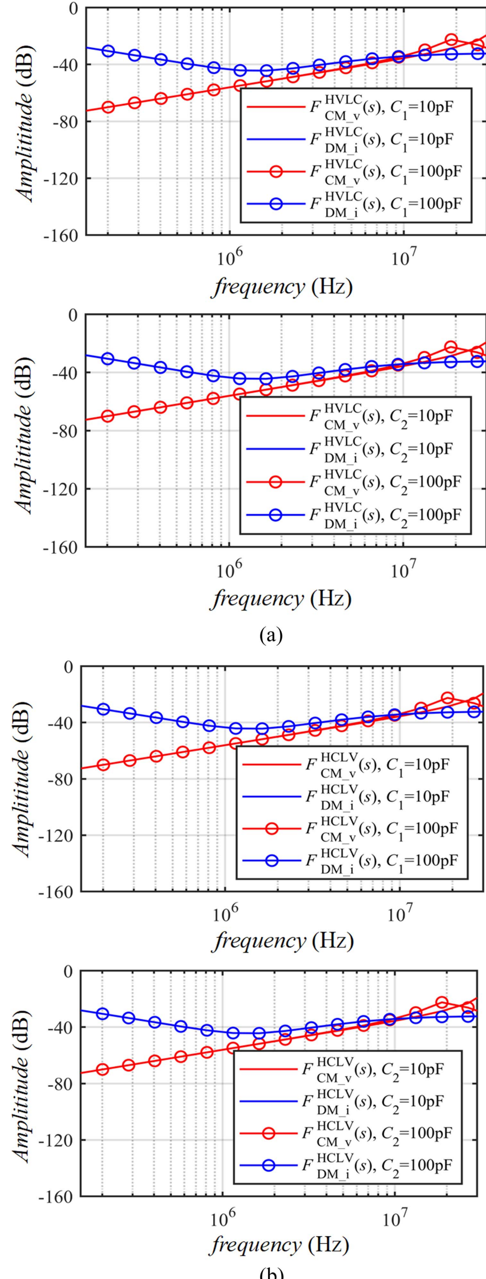


Fig. 4. Influence of DC+ to ground capacitances C_1 and DC– to ground capacitances C_2 on the transfer function of the EMI conduction path. (a) HVLC equivalent circuit. (b) HCLV equivalent circuit.

B. Analysis of Parasitic Capacitance on SiC MOSFET's Switching Performance

EMI sources also have a particularly large impact on system EMI. Changing the transient switching waveform from ideal trapezoidal waves to real switching functions $V_{\mathrm{s}}(s)$ and $I_{\mathrm{s}}(s)$ can improve the accuracy of EMI analysis [40]. In this section, the improved SiC switching model from Xie et al. [41] is used to predict the switching transient waveforms. Based on the double-pulse test (DPT) circuit [42], the switching waveforms of SiC power devices can be tested and analyzed. The switching waveform test circuit is constructed, as shown in Fig. 5.

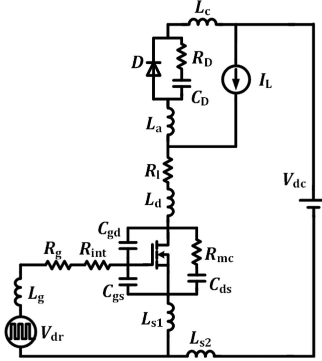


Fig. 5. DPT circuit considering parasitic parameters.

The parasitic inductance of the equivalent circuit comes from the package and external circuits, including the drain inductance $L_{\rm d}$, the common-source inductance $L_{\rm s1}$, the source inductance $L_{\rm s2}$, the driving inductance $L_{\rm g}$ of the SiC MOSFET, the anode inductance $L_{\rm a}$, and the cathode inductance $L_{\rm c}$ of the SiC diode. Parasitic capacitances can be considered in parallel with the junction capacitance.

The stray resistance mainly affects the attenuation of the voltage and current oscillation. In Fig. 5, the stray resistance of the main power commutation circuit is equivalent to $R_{\rm l}$. In the driving part of the circuit, $R_{\rm int}$ is the gate internal resistance of the SiC MOSFET, $R_{\rm g}$ is the external driving resistance, and $V_{\rm dr}$ is the driving voltage. $V_{\rm dc}$ is the applied dc voltage. Since DPT is completed in a very short switching transient state, and there is a dc support capacitor at the dc end, $V_{\rm dc}$ can be considered constant during the switching processes. $I_{\rm L}$ can also be considered constant during switching since the load inductance is large.

Based on the switching model of the SiC device, the influence of the parasitic capacitance on the switching waveform and interference source is analyzed. The comparative analysis is made by changing the size of the parasitic capacitance $C_{\rm 1M}$ while keeping other parameters at their default values. The position of $C_{\rm 1M}$ is shown in Fig. 2(b). The calculated turn-ON and turn-OFF voltage and current waveforms are shown in Fig. 6. The picture intuitively reflects that the parasitic capacitance $C_{\rm 1M}$ has little influence on the switching process. When $C_{\rm 1M}$ increases from 0 to 100 pF, the switching speed of the SiC half-bridge module decreases very little. When $C_{\rm 1M}$ increases, the voltage and current spikes are also not significantly affected. The effect of $C_{\rm 1M}$ on the switching waveform characteristics shows that it has little effect on switching loss and the spectrum of the noise source.

Fig. 7 shows the change curve of switching energy with output capacitance value under different $C_{\rm 1M}$. With the increase of $C_{\rm 1M}$, the turn-ON energy increases with a change rate of 0.14 μJ/pF, and the total energy increases with a change rate of 0.12 μJ/pF. The total switching loss at $C_{\rm 1M}$ of 100 pF is only about 6% higher than that when $C_{\rm 1M}$ is 0. Since the parasitic capacitance brought by the package in SiC power modules is usually well below 100 pF, it can be seen that the

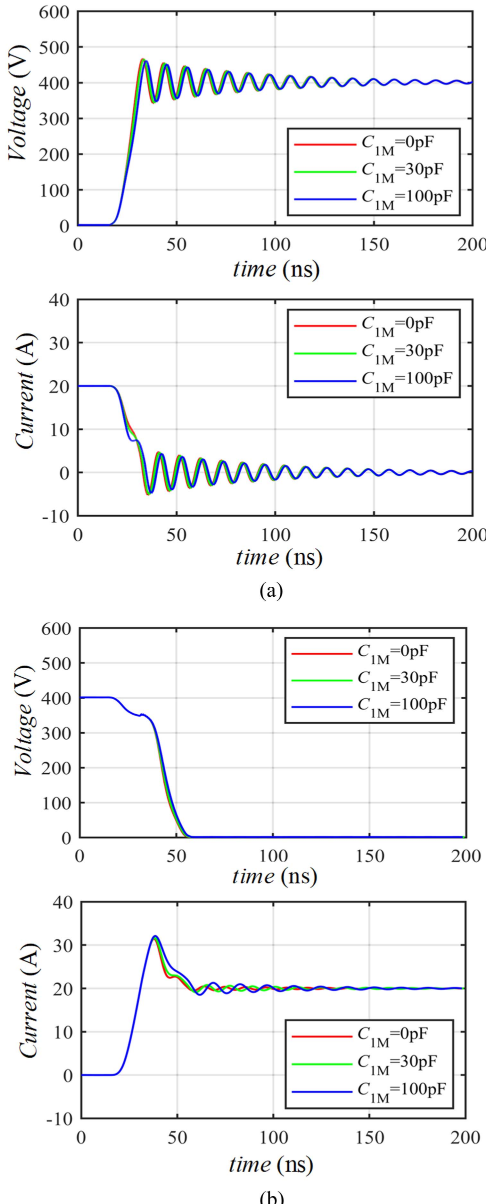


Fig. 6. Influence of the positive-output parasitic capacitance $C_{\rm 1M}$ on switching waveforms $v_{\rm ds}$ and $i_{\rm d}$ of SiC devices. (a) Turn-OFF waveform. (b) Turn-OFF waveform.

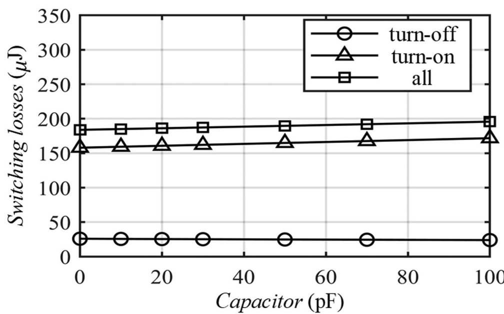


Fig. 7. Influence of the positive-output parasitic capacitance $C_{\rm 1M}$ on switching energy of SiC devices.

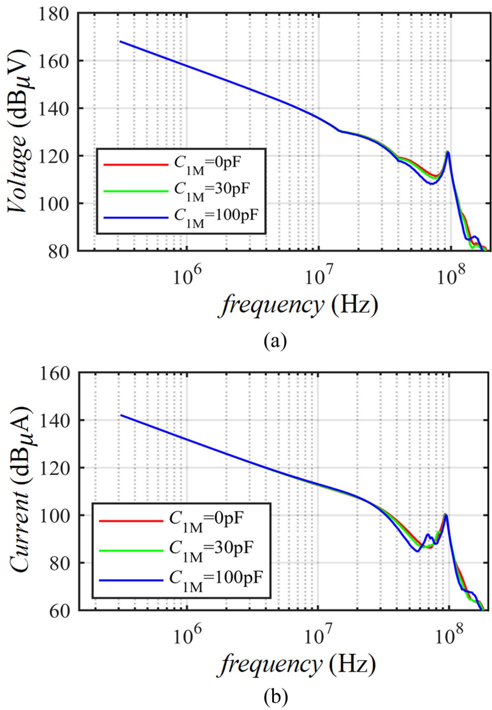


Fig. 8. Influence of the positive-output parasitic capacitance $C_{\rm 1M}$ on EMI noise source spectrum. (a) Spectrum of $v_{\rm ds}$. (b) Spectrum of $i_{\rm d}$.

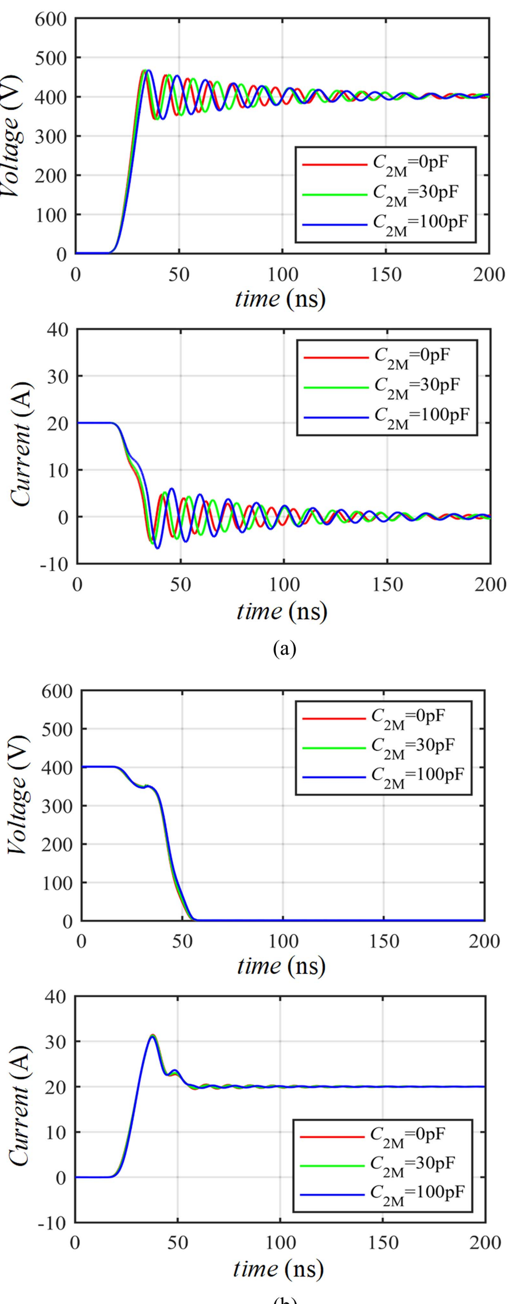


Fig. 9. Influence of the negative-output parasitic capacitance $C_{\rm 2M}$ on switching waveforms $v_{\rm ds}$ and $i_{\rm d}$ of SiC devices. (a) Turn-OFF waveform. (b) Turn-OFF waveform.

increase of the parasitic capacitance $C_{\rm 1M}$ has little impact on the switching loss. The voltage and current spectrum envelopes under different $C_{\rm 1M}$ are shown in Fig. 8. When $C_{\rm 1M}$ is 0, 30, and 100 pF, respectively, the voltage and current spectrums do not have significant changes. Therefore, the effects of $C_{\rm 1M}$ on the EMI noise source are negligible. The parasitic capacitance $C_{\rm 1M}$ in half-bridge power modules is usually lower than 100 pF. Taking the SiC MOSFET CPM2-1200-0080B and SiC Schottky diode CPW4-1200-S010B as examples. The information in the datasheet indicated that the plane dimensions of CPM2-1200-0080B are 3.36×3.1 mm^2, and the plane dimensions of CPW4-1200-S010B are 2.26×2.26 mm^2. The area of the DBC substrate is calculated by ten times the area of the chip, and the parasitic capacitance between the upper and lower copper layers is about 30 pF. If the copper layer is on the same side of the DBC substrate, the parasitic capacitance will be much smaller than this value. Moreover, the value of $C_{\rm 1M}$ is much lower than the junction capacitance of the SiC device in practice. According to the aforementioned analysis result, the influence of $C_{\rm 1M}$ on the switching process can be ignored.

Changing the size of the negative-output parasitic capacitance $C_{\rm 2M}$, and the obtained turn-ON and turn-OFF voltage and current waveforms are shown in Fig. 9. It can be seen from the figure that the influence of $C_{\rm 2M}$ on the turn-ON process can be ignored. However, $C_{\rm 2M}$ will have a certain impact on the turn-OFF process. When $C_{\rm 2M}$ increases, the frequency of voltage and current oscillation will decrease accordingly. Specifically, when $C_{\rm 2M}$ is 0, 30, and 100 pF, the oscillation frequencies are 95, 86, and 72 MHz, respectively. The reason for this effect is that when the lower switch is used as the active one and is turned OFF, the parasitic capacitance and inductance in the circuit form an LC oscillation circuit. Therefore, the increase in $C_{\rm 2M}$ will increase the capacitance in the LC circuit and then decrease the oscillation frequency.

Fig. 10 shows the curve of the turn-ON energy, the turn-OFF energy, and the total energy when $C_{\rm 2M}$ changes from 0 to 100 pF. With the increase of $C_{\rm 2M}$, the change of the turn-ON energy can be ignored, and the turn-OFF energy increases with a rate of change of 0.09 μJ/pF. Besides, the total energy increases with a rate of change of 0.12 μJ/pF when $C_{\rm 2M}$ increases. Using the switching losses at 0-pF $C_{\rm 2M}$ as a benchmark, a 100-pF increase

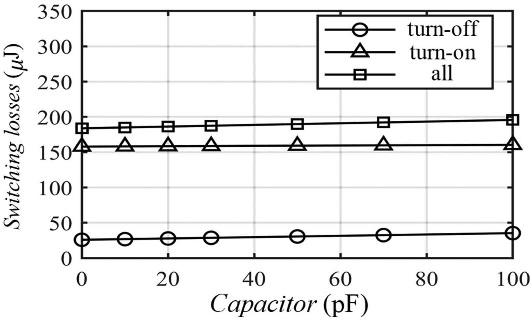


Fig. 10. Influence of the negative-output parasitic capacitance C_{2M} on switching energy of SiC devices.

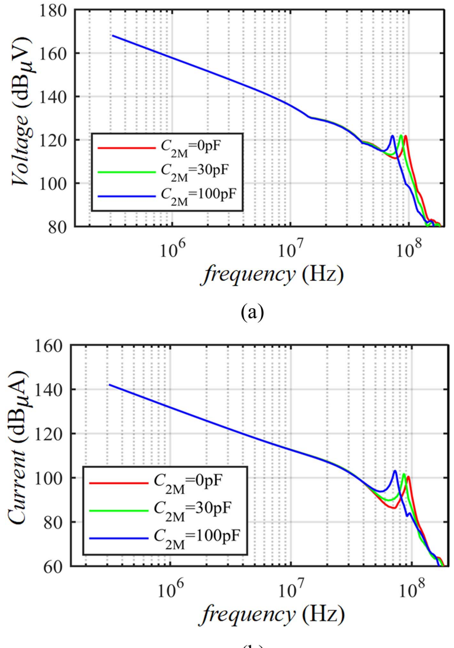


Fig. 11. Influence of the positive-output parasitic capacitance C_{2M} on EMI noise source spectrum. (a) Spectrum of v_{ds}. (b) Spectrum of i_d.

in C_{2M} increases the total switching losses by 6%. Overall, C_{2M} will increase the switching loss of the SiC module, but the increase is not significant.

The voltage and current spectrum envelopes under different C_{2M} are shown in Fig. 11. It can be seen from the figure that C_{2M} will not affect the spectrum of the noise source in the low-frequency band. But in the range of the high-frequency band, C_{2M} will change the peak of the noise source. The spectral peak will move to lower frequencies with the increase of C_{2M}. Due to the smaller junction capacitance of C_{2M}, the change of the spectral peak caused by C_{2M} is small. In general, C_{2M} will not have a significant impact on the spectrum of noise source.

Under reasonable design parameters, the order of magnitude of the parallel parasitic capacitance of the bridge arm is much smaller than the junction capacitance of the SiC device itself. Through the comparative analysis of the influence of C_{1M} and C_{2M}, it can be found that the influence of the parallel parasitic capacitance of the active switch is greater than that of the freewheeling tube parallel parasitic capacitance, which mainly affects the oscillation frequency of voltage and current. Besides, increasing the parasitic capacitance in parallel with the bridge arms will only slightly increase the switching losses of the SiC half-bridge module, but the effect is small. Generally speaking, the influence of such parasitic capacitance on switching loss and interference source spectrum is not significant.

III. Optimal Design of SIC Power Module With Low Capacitance to Ground Based on the PS Structure

According to the previous analysis, the output-to-ground capacitance C_M should be minimized to suppress CM EMI. The parasitic capacitance in the power module is related to the area and layout of the devices and the conductor layer. The module with mutual inductance cancellation (MIC) structure can reduce the area of the substrate [43], [44], thereby reducing the ground capacitance C_M. But the substrate and the copper layer in the MIC structure are still large relative to the area that the chip required. There is still room for further optimization. In this section, the packaging structure of the MIC module is optimized. A new packaging structure with lower capacitance to ground is proposed using layout optimization.

A. Influencing Factors of Parasitic Capacitance Inside the Power Module

The parasitic capacitance inside the power module mainly comes from the copper layer of the DBC substrate. For a single-layer DBC substrate, the parasitic capacitance between the upper and lower copper layers facing each other can be approximated by formula (9). According to formula (9), there are three main factors affecting the capacitance: the relative permittivity of the insulating medium of the DBC substrate ε_r, the thickness of the insulating medium d, and the copper layer's area S. Therefore, improvements can be made in three aspects: selecting low dielectric constant materials, increasing the thickness of the dielectric, and reducing the area of the copper layer to reduce the parasitic capacitance

$$C = \varepsilon_r \varepsilon_0 \frac{S}{d}. \tag{9}$$

However, these methods are not easy to implement. Considering the needs of chip soldering, the connection of the bonding wire, and the layout of the power terminal, the area of the copper layer is difficult to further minimize. Because of the difficulty of minimizing the layout area, the method of reducing the area of the copper layer is difficult to implement. Therefore, a reasonable layout is very important for the optimization of parasitic capacitance. Besides, SiC power modules require low thermal resistance for good heat dissipation [32]. For the method of reducing the dielectric constant ε_r, it is difficult to further reduce ε_r because ε_r of commonly used media is fixed. For the method of increasing the thickness d, it is also difficult to realize due to need to ensure the heat dissipation performance. Therefore, for a power module with a single-layer DBC structure, the optimization of parasitic capacitance is limited. Reducing the copper area is the best way to optimize parasitic capacitance.

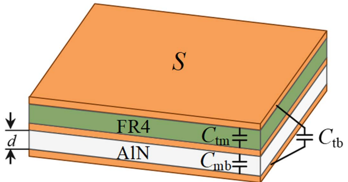


Fig. 12. PCB+DBC packaging structure diagram.

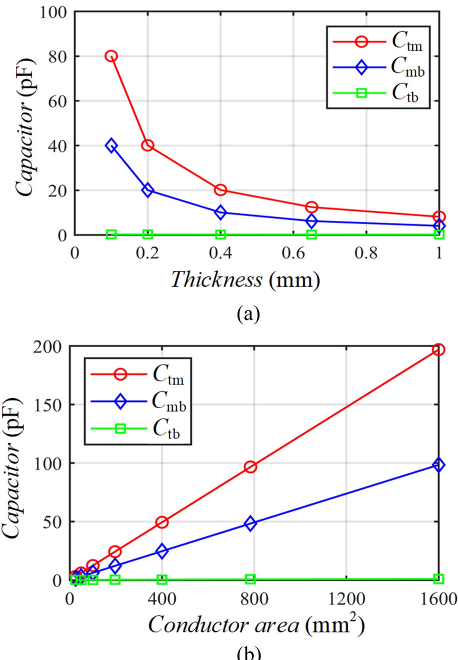


Fig. 13. Variation pattern of the capacitance between copper layers in the PCB+DBC packaging structure. (a) Variation of capacitance with dielectric thickness. (b) Variation of capacitance with conductor area.

For the stacked substrate structure, it is possible to find new method to reduce the ground capacitance. For the PCB+DBC structure shown in Fig. 12, the middle copper layer divides the parasitic capacitance to ground into three parts, including C_{tm}, C_{mb}, and C_{tb}. When the middle copper layer is connected with other voltage potential points and forms a low-impedance loop of CM current, the CM current will flow to that potential point through C_{tm}, and only a very small part of the CM current will pass through C_{tb} to the bottom copper layer. The equivalent capacitance between the upper and lower copper layers is reduced, and the conduction path between the top copper layer and the bottom copper layer is shielded by the middle copper layer. Since the electric field lines passing through the edge of the plate produce extremely small parasitic capacitance, the parasitic capacitance produced in this case is orders of magnitude smaller than in the unshielded case. Based on the permittivity of these materials, the capacitance between each copper layer is calculated by the finite element simulation software.

Fig. 13(a) shows the changing trend of capacitance with the thickness of the insulating layer when the conductor area is constant. Fig. 13(b) shows the changing trend of capacitance with the area when the thickness of the insulating layer is constant. It can be seen from the figure that the capacitance C_{tm} and the capacitance C_{mb} are basically in line with the calculation of formula (9). The magnitude of the capacitance C_{tb} is much smaller than the aforementioned two. Therefore, in the layout of the SiC module packaging structure, the copper layer that generates the voltage jump should be arranged at the top as much as possible.

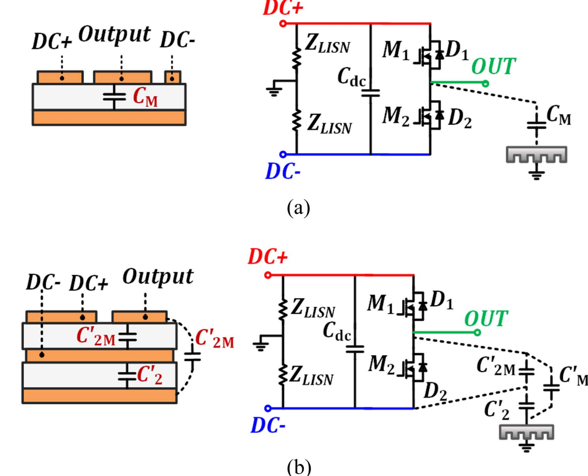


Fig. 14. Output shielding structure to ground capacitance equivalent circuit. (a) Unshielded structure. (b) Shielded structure.

The aforementioned analysis shows that the output-to-ground capacitance C_{M} of the half-bridge module plays a leading role in the conduction path function of CM EMI. In the traditional single-layer DBC, there is no shielding copper layer between the output copper layer and the bottom copper layer, as shown in Fig. 14(a). C_{M} in the unshielded module is much larger than that in the shielding one. If the dc– copper layer is arranged between the output and bottom copper layers, most of the electric field between the upper and bottom conductors can be shielded. In this case, the original C_{M} becomes $C'_{2\mathrm{M}}$ and C'_2, as shown in Fig. 14(b).

According to the aforementioned results, the effects of $C'_{2\mathrm{M}}$ and C'_2 on switching losses and conducted EMI are negligible, and only reducing C'_{M} has a greater effect on reducing CM EMI. Therefore, when C'_{M} is much lower than C_{M}, the CM EMI generated by the half-bridge module can be effectively reduced.

B. Design of SiC Power Module Based on the PS Structure

In the MIC module, in addition to soldering with the SiC chip of the lower bridge arm, the DBC output layer needs to connect with the upper PCB and the external circuits. Therefore, the area of the output copper layer in the MIC module is much larger than the area required for SiC chip welding. There is room for further reduction of the ground capacitance C_{M}. In this section, based on designing and optimizing the internal layout of the hybrid packaging structure, a PS packaging structure with lower capacitance to ground and lower parasitic inductance is proposed. And a SiC half-bridge module is fabricated accordingly. The schematic-side structure and overall view of the module are given in Figs. 15 and 16.

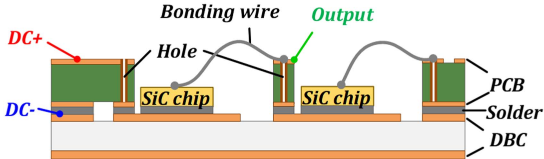


Fig. 15. Side view of a SiC half-bridge module based on a PS structure.

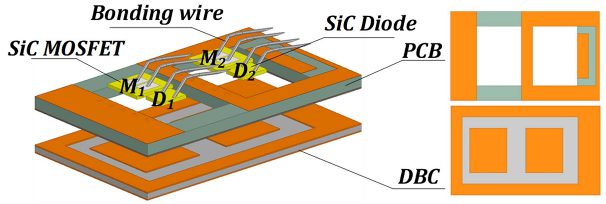


Fig. 16. Overall view of a SiC half-bridge module based on a PS structure.

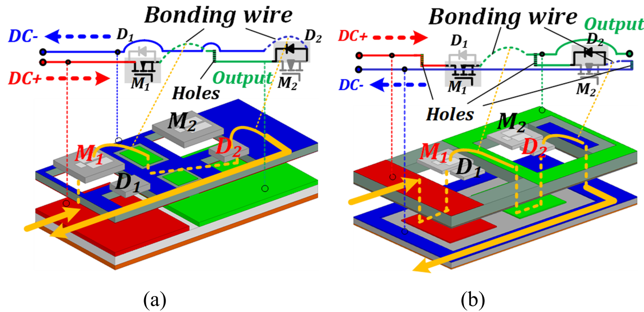


Fig. 17. Packaging structure comparison of MIC module and PS module. (a) Commutation circuit of the MIC module. (b) Commutation circuit of the PS module.

TABLE I
EXTRACTION RESULTS OF PARASITIC INDUCTANCE

Inductance (nH)	L_1	L_2	L_3
L_1	0.819	0.0868	-0.726
L_2	0.0868	2.06	-0.793
L_3	-0.726	-0.793	5.47

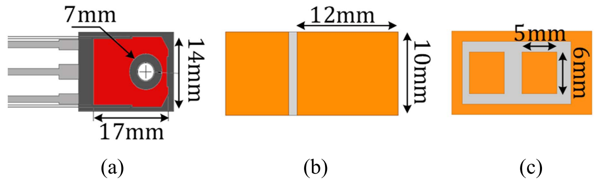


Fig. 18. Size comparison of output copper layers of different packaging structures. (a) TO-247 discrete device. (b) MIC module. (c) PS module.

The PS module packaging structure is in the form of PCB and DBC hybrid packaging. The PCB board is located on the upper layer and the DBC substrate is located on the lower layer. The PCB and DBC are mechanically and electrically connected through the solder layer. The SiC chip is soldered on the DBC substrate through the opening on the PCB to achieve good heat dissipation performance. The dc+ layer of PCB is located on the left side of the top copper layer and is connected to the dc+ copper layer on the DBC substrate through holes, and then connected to the SiC chip on the upper bridge arm.

The upper surface electrode of the upper bridge arm's SiC chip is connected to the output layer on the top of the PCB through bonding wires, and the output layer on the top of the PCB is led out to the external circuit. The pad of the output pole passes through the hole and the DBC to connect to the output layer, and the SiC chip of the lower bridge arm is welded on the copper layer of the output pole of the DBC. The layout optimization reduces the area of the output layer on the DBC substrate. The output layer on the top of the PCB and the layer at the bottom of the DBC are shielded by the dc– layer in the middle, thereby reducing the capacitance to ground. The electrode on the upper surface of the lower arm SiC chip is connected to the dc– pole on the upper of the PCB through bonding wires, and then connected to the dc-pole on the DBC through the holes, and finally led out through the dc– pole at the bottom of the PCB. The bonding wire for driving is perpendicular to the main power loop to form a Kelvin connection to eliminate common source inductance. Fig. 17 shows the comparison of the commutation circuits of the MIC module and the PS module. The copper layers corresponding to the dc+, dc–, and output layers are shown in red, blue, and green, respectively. Taking the action of M_1 as an example, the commutation path is indicated by a yellow arrow. It can be seen from Fig. 17(b) that the dc+ and dc– of the PS modules are located on the same side to form the MIC effect, but for the optimization of capacitance, part of the commutation paths are located on the same plane, the coupling coefficient of the mutual inductance will be lower than that of the MIC module, so the loop parasitic inductance of the PS module is slightly larger than that of the MIC module. ANSYS Q3D simulation software is used to extract the parasitic inductance matrix of the commutation loop in the PS module. The results are shown in Table I. Compared with the MIC module, the self-inductance of the PS modules is increased, and the MIC effect is weakened.

Fig. 18 shows the size of the copper layer of the DBC output electrode under different packaging structures. The area of the copper layer of a single TO-247 device is about 200 mm^2, the area of the copper layer of the output pole after forming the half-bridge circuit is 400 mm^2, and the area of the corresponding copper layer of the MIC module is 120 mm^2. The area of the PS module's corresponding copper layer with the optimized layout was reduced to 30 mm^2. The finite element software ANSYS Maxwell is used for simulating C_{M} of different packages, and the results are listed in Table II. It can be seen that the ground capacitance C_{M} of PS modules is reduced by 68.1% based on the MIC module, which is 89.4% lower than that of discrete devices.

The SiC half-bridge module manufactured based on the PS structure is shown in Fig. 19. The overall size of the power module is about 20.5 $\times$ 15.5 mm^2, which is at least 80% lower than the half-bridge composed of discrete SiC devices. The PCB on the top layer of the module can be extended to integrate the drive circuit and the external main circuit to form

TABLE II
COMPARISON OF GROUND CAPACITANCE OF DIFFERENT PACKAGING STRUCTURES

Packaging structure	Area of copper layer (mm^2)	Medium	C_M (pF)
Discrete device	400	Insulator wafer (0.3mm)	63.9
MIC module	120	AlN (0.45mm)	21.3
PS module	30	AlN (0.45mm)	6.8

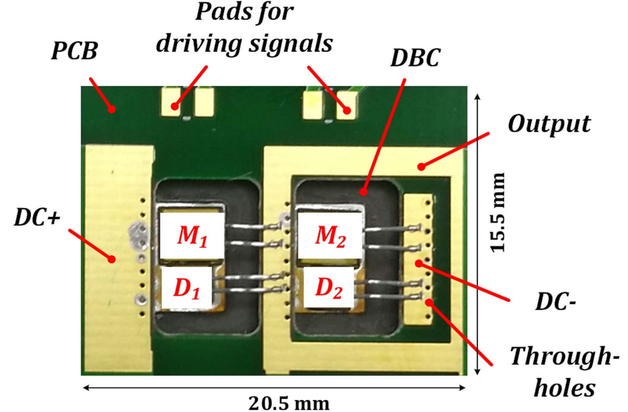


Fig. 19. Physical diagram of a SiC half-bridge module with a PS structure.

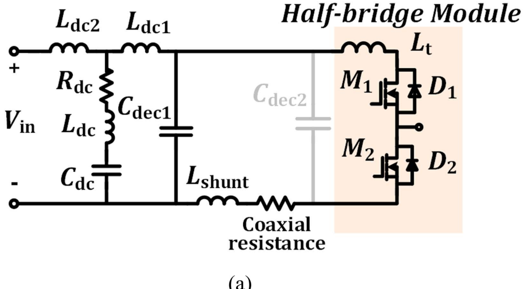
a compact circuit layout, thereby increasing the power density of the converter.

IV. Experimental Result

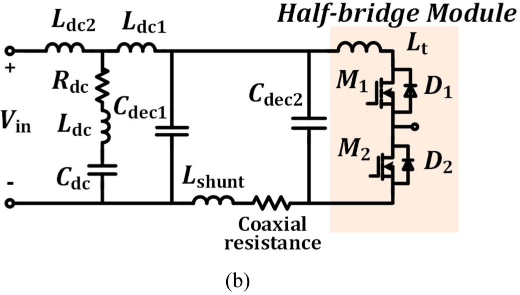
To verify the effect of parasitic capacitance optimization on switching loss and conducted EMI, DPT s and EMC tests will be performed. When selecting the control subjects, in addition to ensuring the consistency of the SiC devices, the parasitic parameters of the control group should also be clarified. Therefore, this article selects the MIC hybrid package module with the same power level and device parameters, and the TO-247-packaged SiC discrete devices (model C2M0080123D for SiC MOSFETs and C4D10120D for SiC diodes) were compared with the PS module proposed in this article.

A. Results of DPT

Since the parasitic inductance of the PS module is very small, the coaxial resistance and the connection circuit will introduce some line inductance when testing. Therefore, the evaluation of the module's parasitic parameters will be affected. To address this issue, we designed two test conditions for the DPT of the switching performance, as shown in Fig. 20. In the test circuit shown in Fig. 20(a), there is only one decoupling capacitor C_{dec1}. In this condition, the drain-source voltage V_{ds} and current I_{d} of the lower arm can be measured at the same time, and the influence of the line inductance L_{shunt} introduced by the



(a)



(b)

Fig. 20. Switching performance test circuit under two conditions. (a) Without the near-end decoupling capacitor. (b) With the near-end decoupling capacitor.

coaxial resistance on the loss can be ignored, so this testing condition can be used to evaluate the switching loss of SiC modules. However, although L_{shunt} has a negligible effect on losses, it increases the switching overvoltage, which affects the evaluation of the loop inductance of the SiC half-bridge module. To solve this problem, an end-near decoupling capacitor C_{dec2} is placed as close as possible to the module, as shown in Fig. 20. This structure cannot be used to measure the switching current, only the switching voltage V_{ds}, so it can only be used to evaluate the switching speed and overvoltage of SiC modules.

Under the test conditions of 400 V/20 A, the discrete device, MIC module, and PS module are subject to the DPT. The testing results without the near-end decoupling capacitors are shown in Fig. 21. Fig. 21(e) is the turn-OFF waveform of the PS module, the current fall time is 15.2 ns. Fig. 21(f) is the turn-ON waveform of the PS module, the current rise time is 6.8 ns, and the overcurrent is 20.5 A. The test results under the same test conditions with the near-end decoupling capacitors are shown in Fig. 22. Fig. 22(e) is the turn-OFF waveform of the PS module, the voltage rise time is 12 ns, the overvoltage is 17 V, and the oscillation frequency is 156.3 MHz. Fig. 22(f) is the turn-ON waveform of the PS module, and the voltage fall time is 19.2 ns. Through the oscillation frequency and the junction capacitance of the SiC device, it can be calculated that the commutation loop inductance of the PS module is 6.9 nH. The commutation loop inductance of the PS module is 71.6% lower than that of the discrete device. But the commutation loop inductance of the PS module is slightly higher than that of the MIC module. It can be seen that the switching performance of the PS module is improved compared to the discrete device, and because the parasitic inductance of the PS module and the MIC module is not much different, the switching performance of the PS module is the same as that of the MIC module.

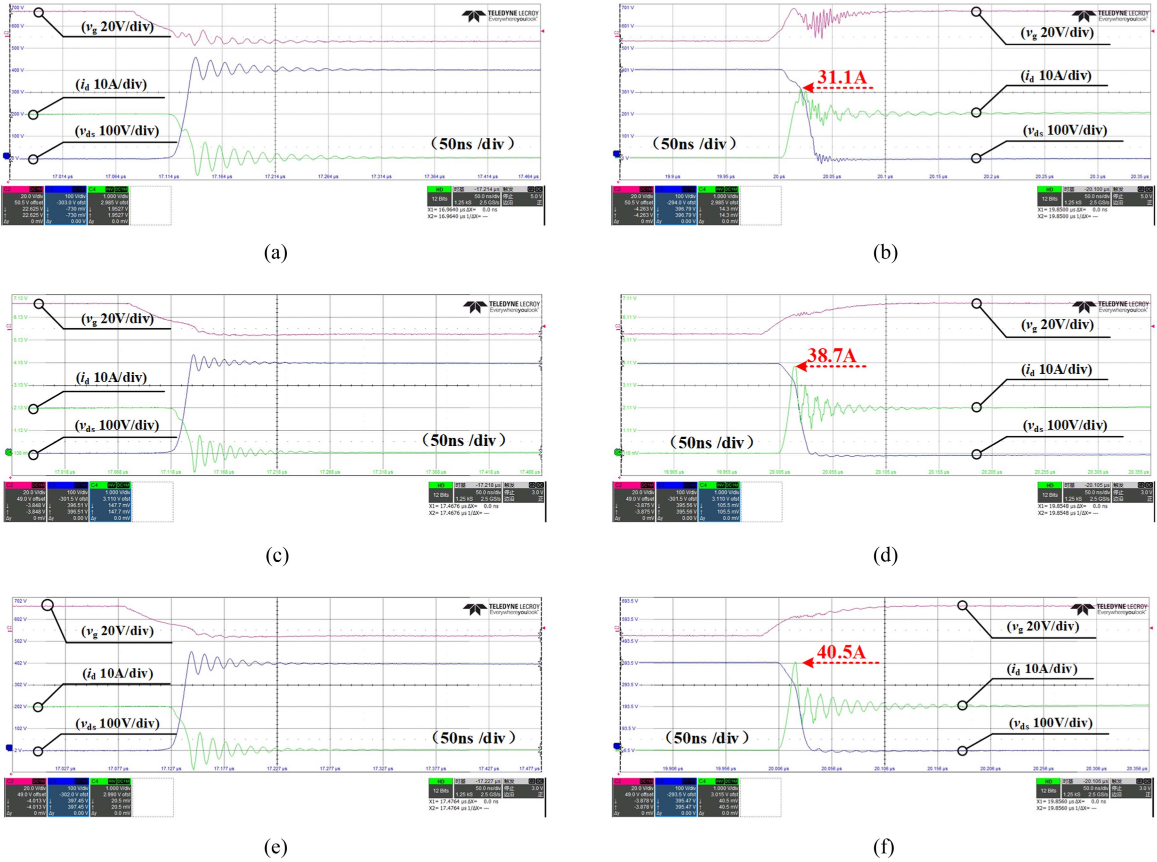


Fig. 21. DPT results without the near-end decoupling capacitor. (a) Turn-OFF waveform based on discrete device. (b) Turn-ON waveform based on discrete device. (c) Turn-OFF waveform based on MIC module. (d) Turn-ON waveform based on MIC module. (e) Turn-OFF waveform based on PS module. (f) Turn-ON waveform based on PS module.

Fig. 23 shows the turn-ON and turn-OFF characteristics of the PS module under different currents, including turn-ON time, turn-OFF time, and turn-OFF overvoltage. These data are the test results under the condition of a near-end decoupling capacitor, which is shown in Fig. 20(b). It can be seen from the comparison results that the switching characteristics of the PS module and the MIC module are almost the same. Compared with discrete devices, the PS module has faster turn-ON and turn-OFF speeds and lower overvoltage. When the current is 30 A, the PS module reduces the turn-OFF time by 12.9%, the turn-ON time by 28.6%, and the turn-OFF overvoltage by 54.8% compared with the discrete device.

Fig. 24 shows the switching energy of the PS module at different currents. The test results are compared with the discrete device and the MIC module. This test is performed without near-end decoupling capacitors, as shown in Fig. 20(a). It can be seen from the figure that the turn-ON and turn-OFF energies of the PS module are almost the same as that of the MIC module, and are significantly lower than that of discrete devices. When the current is 30 A, the turn-OFF energy of the PS module is reduced by 44.6%, the turn-ON energy is reduced by 25.0%, and the total switching energy is reduced by 28.5% compared with the discrete devices.

From the results of the DPT, the SiC half-bridge module based on the PS structure significantly reduces the ground capacitance C_M to 6.8 pF, which is 89.4% lower than that of discrete devices and 68% lower than that of MIC modules. But at the same time, the optimization of the capacitance to ground weakens the MIC effect of the commutation loop, which increases the loop inductance of the PS structure module from 3.8 nH of the MIC structure to 5.5 nH. Based on the experimental results of switching waveforms and losses, it is confirmed that the method of improving the packaging structure to optimize the parasitic capacitance of the SiC half-bridge module will not have a significant impact on the switching performance of the SiC module.

B. Results of Conducted EMI Test

A 300-kHz, 1-kW, CCM-modulated buck converter was constructed for experimental testing. The dc input voltage of the converter is 400 V, and the duty cycle is 0.5.

First, perform FFT transformation on v_{ds} to obtain the voltage interference source spectrum. Then, v_{ds} voltage spectrum of the PS module is compared with that of the discrete devices and the MIC module, as shown in Fig. 25. It can be seen from the figure that v_{ds} voltage spectrum of the PS module is the same as that of the MIC module. This result verifies that the change of the parasitic capacitance in the SiC module will influence the interference source significantly.

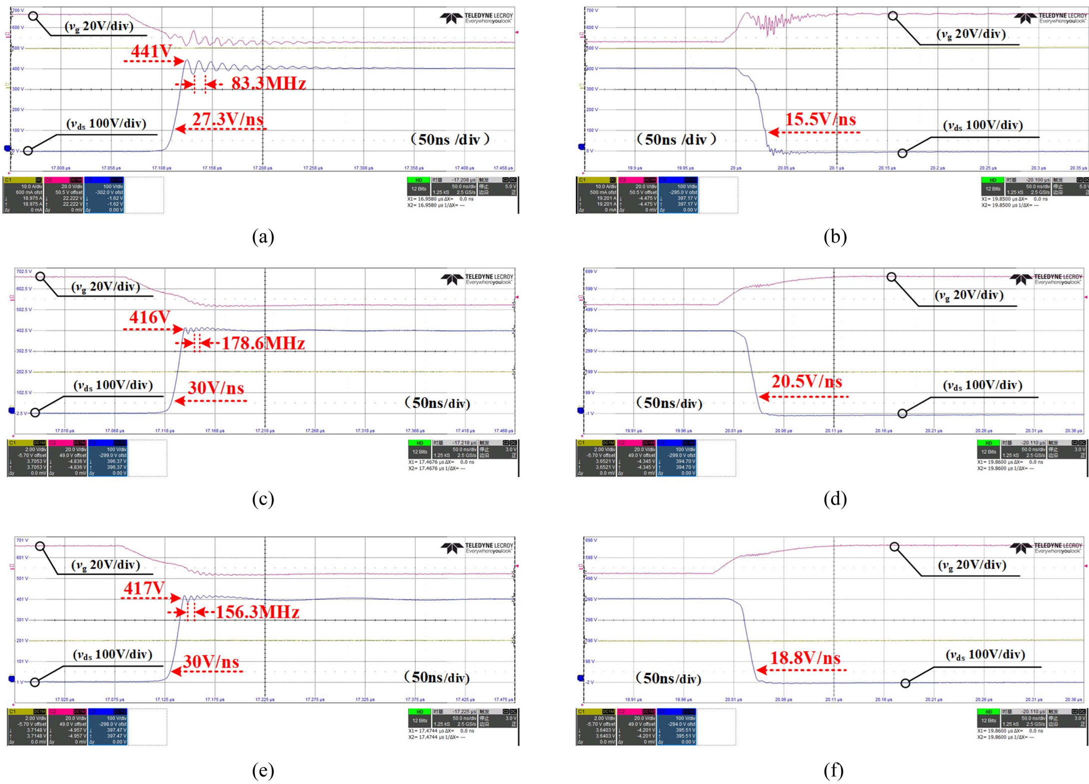


Fig. 22. DPT results with the near-end decoupling capacitors. (a) Turn-OFF waveform based on discrete device. (b) Turn-ON waveform based on discrete device. (c) Turn-OFF waveform based on MIC module. (d) Turn-ON waveform based on MIC module. (e) Turn-OFF waveform based on PS module. (f) Turn-ON waveform based on PS module.

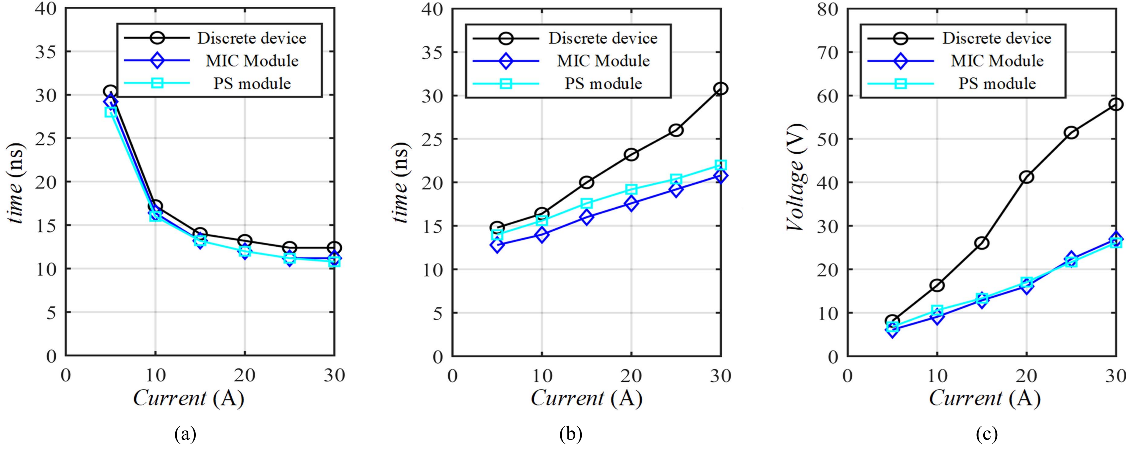


Fig. 23. Comparison of the switching characteristics of the SiC half-bridge module based on the PS structure and the aforementioned module at different currents. (a) Turn-OFF time. (b) Turn-ON time. (c) Overvoltage.

Since the change of parasitic capacitance in the SiC module has negligible influence on the interference source and DM conduction path, it can be predicted that the PS structure will not have a significant impact on the DM EMI of the converter compared to the MIC structure. Therefore, this article will only conduct a comparative study on CM EMI.

Fig. 26 shows the CM EMI produced by a buck converter based on the PS module, and it is compared to the discrete device and the MIC module. The following conclusions can be drawn from the comparison. For the part with noise frequency below 10 MHz, the CM EMI generated by the PS module is slightly higher than 110 dBμV, and the CM EMI generated by the discrete devices and the MIC module is about 120 and 114 dBμV, respectively. When the frequency is greater than 20 MHz, the inductive impedance in the conduction path increases rapidly, and then the CM EMI amplitude decreases rapidly. At this time, the difference between them is small.

Therefore, in the frequency range below 10 MHz, the parasitic capacitance optimization of the PS module reduces the CM EMI of the system by about 10 dB compared with the discrete device and dropped by 4 dB compared with the MIC module.

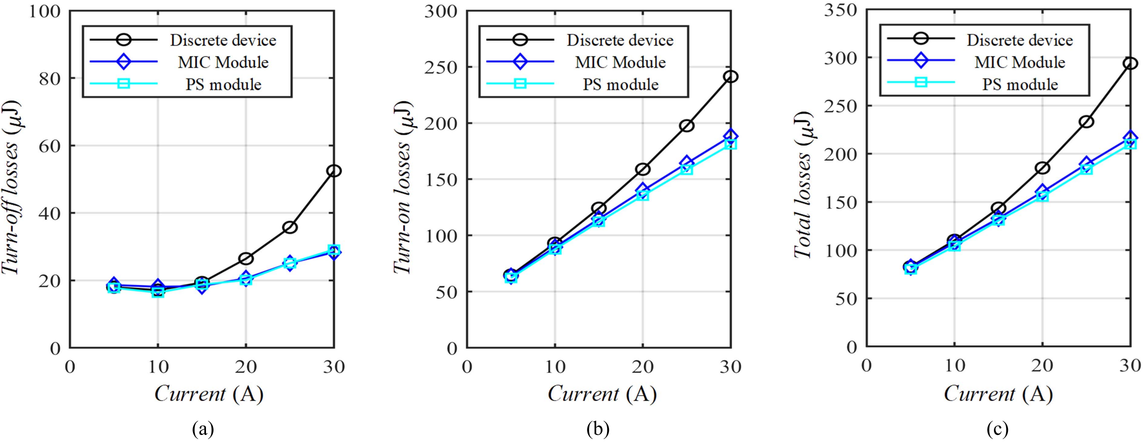


Fig. 24. Comparison of switching loss between the PS SiC half-bridge module and the aforementioned module at different currents. (a) Turn-OFF energy. (b) Turn-ON energy. (c) Total energy.

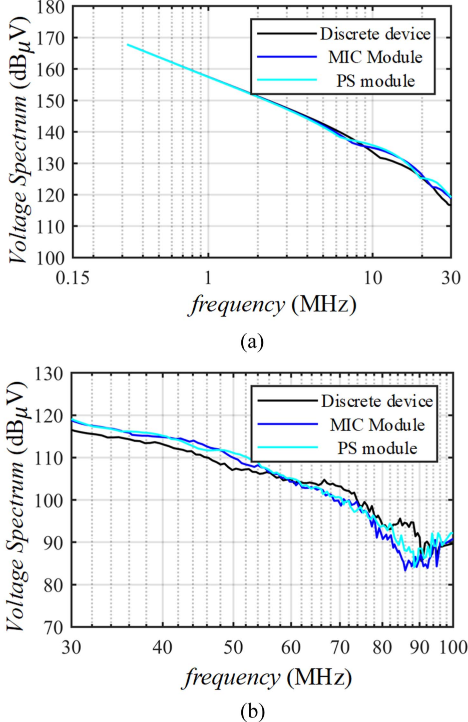


Fig. 25. Spectrum comparison of drain-source voltage v_{ds} of SiC half-bridge module with the PS structure. (a) 150 kHz–30 MHz. (b) 30–100 MHz.

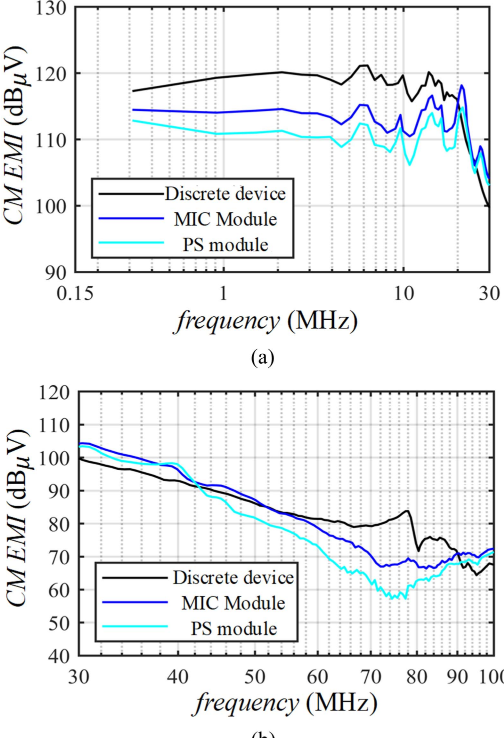
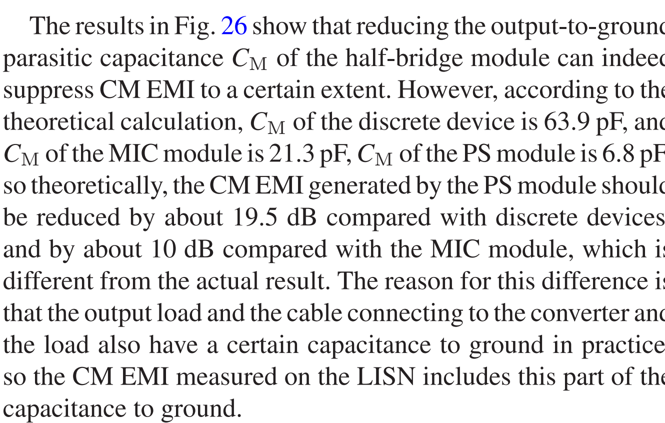


Fig. 26. Buck converter conducted CM EMI voltage comparison of PS modules. (a) 150 kHz–30 MHz. (b) 30–100 MHz.



The results in Fig. 26 show that reducing the output-to-ground parasitic capacitance C_{M} of the half-bridge module can indeed suppress CM EMI to a certain extent. However, according to the theoretical calculation, C_{M} of the discrete device is 63.9 pF, and C_{M} of the MIC module is 21.3 pF, C_{M} of the PS module is 6.8 pF, so theoretically, the CM EMI generated by the PS module should be reduced by about 19.5 dB compared with discrete devices, and by about 10 dB compared with the MIC module, which is different from the actual result. The reason for this difference is that the output load and the cable connecting to the converter and the load also have a certain capacitance to ground in practice, so the CM EMI measured on the LISN includes this part of the capacitance to ground.

To accurately compare the CM EMI contributed by the SiC module itself, a current probe (model LECROY CP030, bandwidth 50 MHz) was placed on the dc+ and dc– lines after LISN and before C_{dc} in Fig. 1 to measure the CM current flowing through the power lines. First, the CM current generated by the whole system is measured with one current probe under the condition that the converter heatsink is grounded. Then, with the heatsink ungrounded, the CM current generated by the part of the system other than the SiC half-bridge is measured in the same way. Next, subtract the CM currents measured by the two methods, and the CM current generated by the SiC half-bridge module can be obtained.

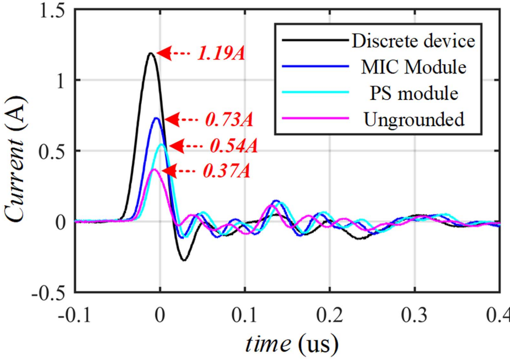


Fig. 27. Comparison of the total CM current of the system when the heat sink is grounded and ungrounded.

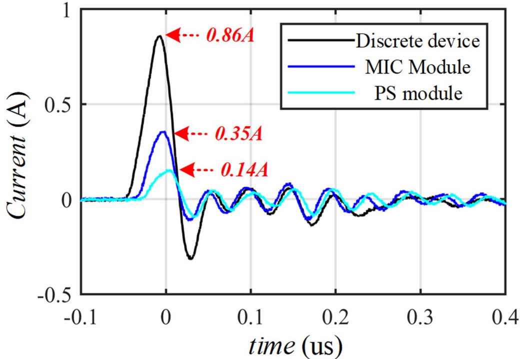


Fig. 28. Comparison of CM currents generated by PS modules, MIC modules, and discrete devices.

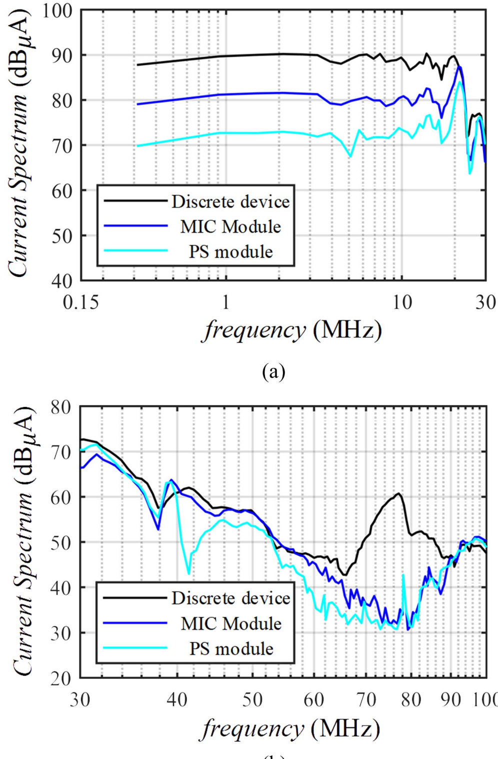


Fig. 29. CM current spectrum generated by PS modules, MIC modules, and discrete devices. (a) 150 kHz–30 MHz. (b) 30–100 MHz.

The CM current measured by the aforementioned method is shown in Fig. 27. This figure gives the total CM current of the system using the discrete device, the MIC module, and the PS module when the heatsink is grounded. Besides, the CM current of the system with the heat sink ungrounded is given for comparison. It can be seen from Fig. 27 that even when the heatsink of the SiC half-bridge is not grounded, there is still a certain CM current in the test system. Taking the turn-ON process as an example, the CM current peak in the system is 0.37 A. With the heatsink grounded, the test circuit based on the discrete device achieved a peak CM current of 1.19 A, the peak CM current of the circuit based on the MIC module was 0.73 A, and the peak CM current in the test circuit using the PS module is reduced to 0.54 A.

Subtract the CM currents under grounded and ungrounded conditions, and the results can be obtained in Fig. 28. Taking the turn-ON transient process of the SiC device as an example, the peak value of the CM current generated by the discrete device is about 0.86 A, the peak value of the CM current generated by the MIC module is reduced to 0.35 A, and the peak value of the CM current generated by the PS module is further reduced to 0.14 A.

These results show that reducing the parasitic capacitance C_{M} of the SiC half-bridge module to ground can effectively reduce the CM current generated by the SiC module. Furthermore, the frequency spectrum of the CM current generated by SiC devices in different packages can be obtained by FFT, as shown in Fig. 29. It can be seen from the figure that when the frequency is lower than 15 MHz, the amplitude of the CM current spectrum generated by the PS module is around 73 dBμA, the CM current generated by the discrete device is about 90 dBμA, and the CM current generated by the MIC module is about 82 dBμA. It can be seen that through the optimized design of the packaging structure, the CM current generated by the PS module is reduced by about 9 dB compared with the MIC module, and about 17 dB compared with the discrete device. This result is close to the theoretical value calculated according to the capacitance to ground.

The experiment verifies the feasibility of suppressing CM EMI by reducing the capacitance to ground C_{M}, and the effectiveness of the new low parasitic capacitance SiC packaging structure proposed in this article.

V. Conclusion

This work presents a hybrid-packaged SiC power module with low CM EMI and switching losses. To mitigate the adverse effects of high-speed switching-induced EMI, a shielding layer is added, which creates a low-resistance path for CM noise at high frequencies and reduces the module's equivalent capacitance to ground. The shielding layer significantly reduces the CM current flowing out of the power module. Furthermore, the optimized parasitic parameters increase the module's switching

rate, thus effectively reducing the switching losses in high-speed switching.

The proposed module is analyzed theoretically using an EMI model and switching model and validated through experimental verification. The simulation and experimental results confirm the good EMC performance and low loss performance of the module. The comprehensive optimization results in reduced system-level filtering and heat dissipation requirements, significantly improving power density and simplifying the design of power electronic systems. In addition, this article conducts research on the half-bridge structure, which is the basic structure of many circuit topologies. The conclusions of this article can be extended to other circuits accordingly based on the half-bridge structure after further verification.

Future work will involve analyzing multichip power modules and addressing current sharing issues resulting from parallel chip connections. These efforts will contribute to the development of more advanced and efficient power electronic systems.

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Yifan Zhang received the B.S. degree in electrical and electronic engineering in 2021 from the Huazhong University of Science and Technology, Wuhan, China, where she is currently working toward the Ph.D. degree in electrical engineering.

Her current research interests include wide bandgap devices packaging and electromagnetic interference issues.

Yue Xie received the B.S. and Ph.D. degrees in electrical and electronic engineering from the School of Electrical and Electronic Engineering, Huazhong University of Science and Technology, Wuhan, China, in 2016 and 2022, respectively.

He is currently an Engineer with BYD Company, Changsha, China. His research interests during the postgraduate period include wide bandgap devices packaging, electromagnetic interference issues, and switching behavior modeling.

Cai Chen (Member, IEEE) received the B.S. and Ph.D. degrees in electrical and electronic engineering from the Huazhong University of Science and Technology, Wuhan, China, in 2008 and 2014, respectively.

From March 2013 to December 2013, he was an Intern with GE Global Research Center, Shanghai, China. From 2014 to 2016, he was with the Advanced Semiconductor, Packaging and Integration Lab, Huazhong University of Science and Technology as a Postdoctoral Researcher. From 2016 to 2017, he was a Visiting Scholar with the Center for High Performance Power Electronics, The Ohio State University, Columbus, OH, USA. From 2017 to 2018, he was a Visiting Scholar with the College of Engineering, University of Arkansas, Fayetteville, AR, USA. In 2019, he joined the Huazhong University of Science and Technology, where he is currently an Associate Research Fellow. His research interests include WBG devices packaging, integration, packaging EMI issues, packaging reliability, and high-density applications.

Xinyue Guo received the B.S. degree in electrical engineering from Wuhan University, Wuhan, China, in 2020, and the M.S. degree in power electronics from the School of Electrical and Electronic Engineering, Huazhong University of Science and Technology, Wuhan, China, in 2023.

Her research interests include multilevel converters and WBG device packaging and applications.

Yiyang Yan received the B.S. degree in functional material and electrical and electronic engineering in 2018 and the M.S. degree in electrical engineering from the Huazhong University of Science and Technology, Wuhan, China, in 2021, where he is currently working toward the Ph.D. degree in electrical engineering with the School of Electrical and Electronic Engineering.

His current research interests include wide bandgap devices double-sided cooling package, high power density inverters, and package thermal modeling.

Lei Yang was born in Henan, China, in 1982. He received the Ph.D. degree in aerospace propulsion from the Beijing Institute of Technology, Beijing, China, in 2014.

He is currently a Senior Engineer with the Beijing Institute of Precision Mechatronics and Controls, Beijing, China. His research interest includes aerospace servo power technology.

Yong Kang (Fellow, IEEE) was born in Hubei, China, in 1965. He received the B.E., M.E., and Ph.D. degrees in electrical engineering from the Huazhong University of Science and Technology, Wuhan China, in 1988, 1991, and 1994, respectively.

In 1994, he joined the Huazhong University of Science and Technology as a Lecturer and was promoted to an Associate Professor in 1996 and to a Full Professor in 1998. He is the author of more than 60 technical papers. His research interests include power electronic converter, ac drivers, electromagnetic compatibility, their digital control techniques, WBG device packaging, and applications.