An Enhanced Adaptive Synchronous Rectification With Turn-ON Optimization for *LLC* Converters Based on Stepwise-Plus-Feedforward Control

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***Abstract*—Synchronous rectification (SR) is an essential aspect for *LLC* resonant converters to achieve high-efficiency design, and the mainstream SR method is the adaptive directly voltage-sensing-based method (ADVS-SR), where the drain–source voltage of the SR switch is sensed. However, due to the presence of parasitic capacitor of the transformer and output capacitors of SR switches, undeserved bode-diode conduction (BDC) caused by intricate voltage ringing across the SR switch will invalidate the conventional ADVS-SR turn-ON time tuning process under light-load condition, resulting in the dissipation of power efficiency. To solve this problem, in this article, the capacitive current spike, which is the main root of the voltage ringing in terms of turn-ON, is modeled and analyzed, and then different SR turn-ON candidates are compared. Based on that, this article proposes an enhanced adaptive SR strategy based on a novel stepwise-plus-feedforward (SPF) control to optimize SR turn-ON. The SPF-SR strategy can eliminate not only large reverse current caused by premature turn-ON but also large BDC interval caused by belated turn-ON over the whole operating range. On the basis of ADVS, the SPF-SR only need to sense extra $V_{\rm in}$, V_o, and I_o, which are easily sensed dc signals, and can be easily implemented in a cost-effective digital controller. Finally, a 300 W *LLC* prototype is built where experimental results show that the SR turn-ON issue is optimized by the SPF-SR strategy, and compared with commercial SR IC and conventional ADVS-SR, the SPF-SR strategy improves power efficiency up to 6.99% and 5.52%, respectively.**

***Index Terms*—Adaptive synchronous rectification (SR), light-load efficiency optimization, *LLC* resonant converter, turn-ON issue.**

I. Introduction

THE *LLC* resonant converter, as illustrated in Fig. 1, due to its excellent inherence of soft switching for both primary- and secondary-side switches over the whole operating range [1], has become a research hotspot [2], [3], [4], [5], [6]. For decades, *LLC* resonant converters have been widely used in electric vehicles, data center power supply, etc., where *LLC* converters are usually required to provide a low-voltage high-current output [7], thereby diode rectifiers will induce huge conduction losses, and synchronous rectification (SR) becomes critical to improve the efficiency [8].

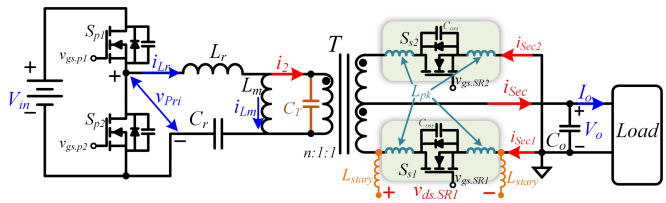

Fig. 1. Half-bridge *LLC* resonant converter with a full-wave rectifier.

Unfortunately, the SR control for *LLC* converters faces many challenges since the turn-ON/OFF instants of the SR switch are not only not identical to that of the primary switch but also seriously affected by the intricate parasitic parameters, especially as the switching frequency increases. For decades, various research articles have been carried out on *LLC* SR control [9], and some methods for bidirectional *CLLC* converters can also be applied to *LLC* converters due to their inherent similarity [10]. According to the type of sensing signal, *LLC* SR methods can be categorized into current-sensing-based SR (CS-SR), sensorless prediction-based SR (SLP-SR), indirectly voltage-sensing-based SR (IVS-SR), and directly voltage-sensing-based SR (DVS-SR).

The CS-SR control is one of the most primitive SR methods where rectifying current [11], [12] or primary-side current [13], [14], [15] are sensed by a current transformer. However, since CS-SRs all suffer from high sensing loss, bulky volume, and/or high cost, the focus of *LLC* SR control has shifted to the sensorless or the voltage-sensing-based method. SLP-SR methods omit the high-frequency sensing and predict SR time based on specific circuit model, e.g., specific constraints in [16] and [20], imprecise FHA model [17], [18], [19], or the ideal time-domain model (ITDM) [21], [22]. Although SLP-SRs have noisy immunity to parasitic parameter, such methods either have low accuracy of SR control or heavily rely on resonant parameters. IVS-SR methods tend to generate SR driver by

Manuscript received 17 March 2023; revised 30 May 2023; accepted 13 July 2023. Date of publication 17 July 2023; date of current version 22 September 2023. This work was supported by Shaanxi Science and Technology Innovation Team Program under Grant 2022TD-64. Recommended for publication by Associate Editor O. Lucia. *(Corresponding authors: Yunqing Pei; Laili Wang.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3296285.

Digital Object Identifier 10.1109/TPEL.2023.3296285

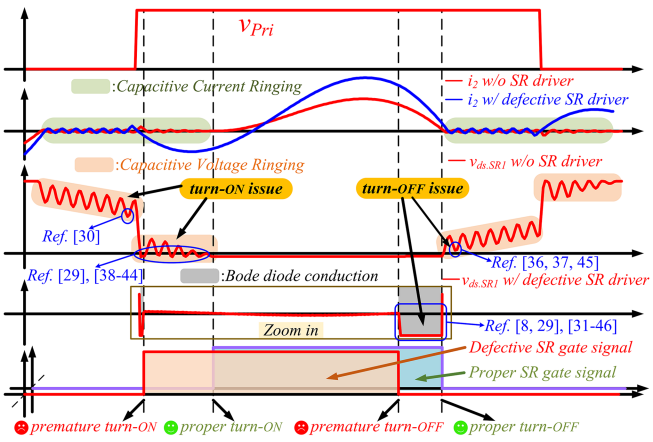


Fig. 2. Schematic waveform of *LLC* converters under light-load condition and the key turn-ON/OFF issues of DVS-SR.

employing some high-magnitude voltages, such as resonant capacitor voltage [23], inverter output voltage $v_{\rm pri}$ [24], resonant inductor voltage [25], [26], transformer voltage [24], [25], [26], or OFF-state SR drain–source voltage [27]. However, the control accuracy, which is the core advantage of the hardware-based SR method, will be sacrificed in the above IVS-SR methods as the resonant parameters deviated. Sun et al. [28] derived SR time from a noisy ripple of V_o, which reduces the reliability of this scheme.

Benefited from the small and lossless sensing circuit and the potential of accurate SR control, the DVS-SR has become the mainstream of *LLC* SR methods with the sensing of SR drain–source voltage ($v_{\rm ds}$), which can directly reflect the ON/OFF-state of SR body diode. However, the turn-ON/OFF issues of DVS-SR, as shown in Fig. 2, complicate the SR control. The key of the SR turn-OFF issue is that, impacted by the package inductance $L_{\rm pk}$ of SR and printed circuit board (PCB) stray inductance $L_{\rm stray}$, the sensed voltage will lead the voltage across $R_{\rm ds.on}$, resulting in premature turn-OFF [8], [29]. And the key of the SR turn-ON issue is that there will be remarkable voltage ringing after the SR current drops to zero due to the subresonance caused by the C_{oss} of SRs and the parasitic capacitance C_T of the transformer. Once this voltage ringing leads to extra body-diode conduction (BDC), the falsely triggered signal will result in premature turn-ON [29].

Originally, an RC or RCD [8], [29], [30] compensation network was carefully designed to deal with the issue of duty-cycle loss or voltage ringing; however, such methods require the exact value of parasitic inductance and $R_{\rm ds.on}$. Recently, the research hotspot of DVS-SR has focused on adaptive scheme (ADVS-SR) due to its immunity of duty-cycle loss, and several SR ICs [41], [42], [43], [44], [45], [46] adopting this concept have been released in industry.

The adaptive turn-OFF control was introduced in [31], where the SR turn-OFF time is stepwise tuned based on the BDC signals; however, it is only valid in the below-resonance region (BRR) ($f_s < f_r$, where f_s is the switching frequency and f_r is the resonant frequency of L_r and C_r), and at resonant point ($f_s = f_r$). Scholars in *CPES* [32], [33] further expanded this scheme in the above-resonance region (ARR) ($f_s > f_r$) and optimized its digital implementation on a low-cost controller. In [34], the turn-OFF time was tuned by sensing $v_{\rm ds}$ right before and after SR turns OFF, which complicates the voltage-sensing circuits. Amiri et al. [35] proposed an analytic–adaptive SR strategy based on the peak value of resonant current and zero-crossing instant of $v_{\rm ds}$; however, it is difficult to sense the zero-crossing point of $v_{\rm ds}$. Wang et al. [36] and the article presented in [45] pointed out that both early and belated turn-OFF will lead to BDC, so the conventional adaptive turn-OFF tuning process is in danger of losing control. In [36], an extra detecting window right after SR turns OFF was added to dissipate the BDC pulse caused by the belated turn-OFF. Another solution mentioned in [36] was implemented by Qian et al. [37] by setting an extra positive voltage threshold to detect the positive spike of $v_{\rm ds}$ when SR turns OFF late.

The adaptive schemes above have no mention of the SR turn-ON issue. In [38], the adaptive turn-OFF tuning process in [31] was simply introduced to tune the SR turn-ON time; however, it will be frozen by falsely triggered BDC signals at light load. A dual-edge tracking method for turn-OFF tuning was proposed in [39] and [42], where turn-ON delay at light load was suggested to prevent premature turn-ON, yet no solution was provided. In [40] and [43], an adjustable turn-OFF threshold was designed to tune the turn-OFF time, and the turn-ON delay will be increased if a positive $v_{\rm ds}$ right after SR turns ON was detected; however, the $v_{\rm ds}$ right after SR turns ON is so small and noisy to be detected accurately, especially in high-frequency application. In [41], the SR turn-ON delay was set to 155 ns under normal conditions, yet increased to 275 ns under light-load conditions. Similarly, the turn-ON delay in [44] was assumed a minimum value at high load and increased with decreasing load levels. However, SR turn-ON delay varies not only with load levels but also with voltage gain; consequently, a proper SR turn-ON strategy for the whole operating range is still worth looking forward to.

The state-of-the-art SR methods for *LLC* resonant converters are summarized and compared in Table I. ADVS-SR is adopted and optimized in this article. As aforementioned, the turn-OFF issue of DVS-SRs has been well studied; yet, the turn-ON issue of that is still a challenge, especially under light-load condition.

Motivated by this problem, in this article, the turn-ON issue of DVS-SRs is deeply analyzed in time domain, and an enhanced adaptive SR strategy based on novel stepwise-plus-feedforward (SPF) control is proposed to optimize SR turn-ON on the basis of ADVS-SR. In addition, the implementation of the proposed SPF-SR turn-ON optimization strategy using a cost-effective digital microcontroller and a few logic circuits is introduced in detail.

The rest of this article is organized as follows. The turn-ON issue of DVS-SRs is analyzed in Section II. The proposed SPF-SR strategy and its implementation are proposed in Sections III and IV, respectively. The experimental results are shown in Section V. Finally, Section VI concludes this article.

II. Turn-ON Issue of DVS-SRs

According to ITDM of *LLC*, at heavy load, *LLC* operates in *PO* mode in BRR where SR switch turns ON synchronously with primary switch and in *NP* mode in ARR where SR switch

TABLE I
SUMMARY AND COMPARISON TABLE OF SR METHODS FOR *LLC* CONVERTERS

Category	Sub-Group	Ref	Circuit Parameter Independence	Accuracy	Applicability	Cost	Sensing Circuit Volume	Extra Power Loss
CS-SR	Rectifying Current Sensing	[11,12]	★★★★★	★★★★★	★★★★★	★★★★★	★★★★★	★★★★★
	Primary-Side Current Sensing	[13-15]	★★★★★	★★★★★	★★★★★	★★★★★	★★★★★	★★★★★
SLP-SR	Specific Constraints Based	[16], [20]	★	★	★	None	None	None
	FHA Model Based	[17-19]	★	★★★	★★			
	Ideal Time-Domain Model Based	[21-22]	★	★★★★	★★★★★			
IVS-SR	Resonant Capacitor Voltage Sensing	[23]	★★	★★★★	★★★★★	★★★★	★★★	★
	Magnetic Voltage Sensing	[24-26]	★★	★★★★	★★★★★	★★★★	★★★★	★★★
	OFF-State v_{ds} Sensing	[27]	★★	★★★★	★★★★★	★	★	★
	V_o ripple & Load Current Sensing	[28]	★★★★	★★★	★★★★★	★	★	★
DVS-SR	Phase Compensation	[8], [29-30]	★	★★	★★	★	★	★
	Adaptive Turn-OFF	[31-37], [45]	★★★★★	★★★	★★★	★	★	★
	Adaptive Turn-ON/OFF	[38-44]	★★★★★	★★★★	★★★★	★	★	★
	The proposed SPF-SR		★★★★★	★★★★★	★★★★★	★	★	★

* "★" represents the unit of quantization.

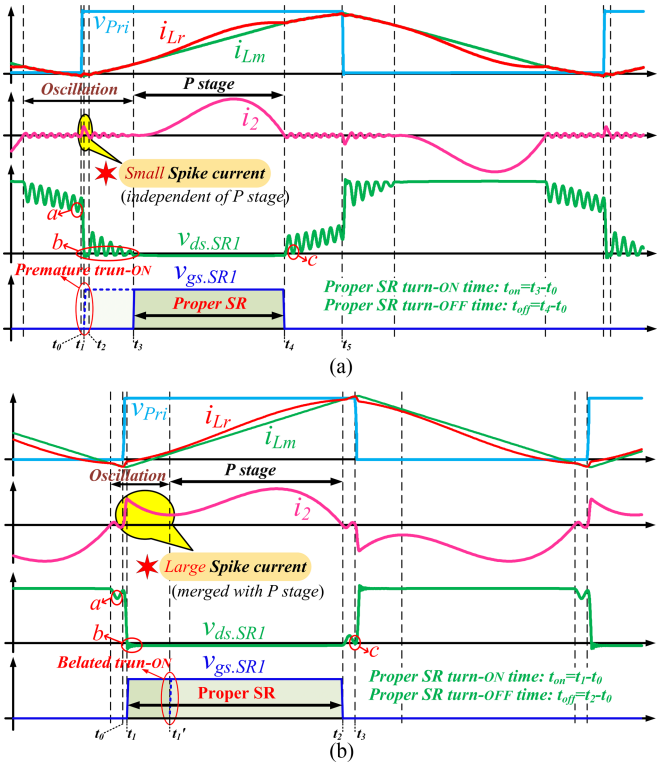


Fig. 3. Two typical scenarios of *LLC* converter under light-load condition. (a) Scenario one: Small spike current. (b) Scenario two: Large spike current.

turns ON behind primary switch, and there is no danger of early turn-ON. Ideally, *P* and *N* stages are the energy-delivery stages where the energy can be delivered from source to load; yet, *O* stage is the energy-blocking stage without any energy delivery.

At light load, ideally, *LLC* operates in *OPO* mode [2], where SRs should turn ON later than the primary switches. However, this situation is complicated by the equivalent parasitic capacitor C_T of the transformer and the C_{oss} of SRs. Fig. 3 shows two different scenarios of *LLC* under light-load condition. It can be seen that there is a capacitive spike in primary transformer current i_2 right after the primary switches act, where i_2 represents the reflected-to-primary-side drain current of all SRs. In scenario

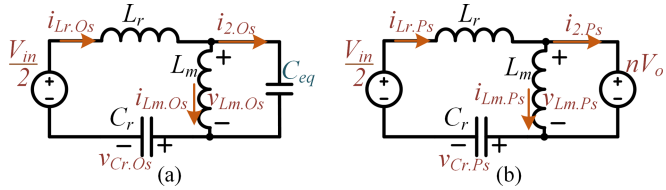


Fig. 4. Equivalent circuit of *LLC* resonant tank. (a) O_s stage. (b) P_s stage.

one, as shown in Fig. 3(a), the amplitude and duration of the spike current are small, and the SR body diode conducts several times (from t_2 to t_3) until the oscillation ends. Yet in scenario two, as shown in Fig. 3(b), the spike current is large and merged with *P* stage without any other following oscillation, and the SR body diode will conduct consecutively from t_1 to t_2 where *P* stage ends.

By and large, there are three harsh points, i.e., points *a*, *b*, and *c* of DVS-SR methods due to the voltage ringing, as shown in Fig. 3. However, SR switches should be limited to turn-ON not earlier than the primary switches according to the principle of *LLC*, and a small detecting window right after SR turns OFF is set in this article to avoid sensing the BDC signal caused by the belated turn-OFF. Therefore, points *a* and *c* have no mischief to SR control in this article. As for point *b*, the most influential issue is the current spike, while the oscillating current following this spike is relatively small or even absent, as shown in Fig. 3, and can be ignored for analysis. Therefore, in this section, the effect of spike current on SR control is deeply analyzed.

A. Time-Domain Analysis of Capacitive Spike Current

The spike current consists of two stages, as shown in Fig. 3, where stage 1 (from t_0 to t_1) is marked as O_s stage and stage 2 (from t_1 to t_2) is marked as P_s stage. Equivalent circuits of these two stages are shown in Fig. 4, and for the generality of analytic results, the following derivation is normalized based on the following equation:

$$V_{\text{base}} = V_{\text{in}}/2, \quad Z_{\text{base}} = Z_r = \sqrt{L_r/C_r}, \quad I_{\text{base}} = V_{\text{base}}/Z_{\text{base}},$$
$$f_{\text{base}} = f_r = \omega_r/2\pi = 1/\left(2\pi\sqrt{L_rC_r}\right). \tag{1}$$

Based on Kirchhoff's law, the four-order linear differential equation set of O_s stage can be derived as follows:

$$\begin{cases} V_{\text{in}}/2 = L_r di_{Lr.Os}(t)/dt + (v_{Cr.Os}(t) - V_{\text{in}}/2) \\ \qquad +v_{Lm.Os}(t) \\ i_{Lr.Os}(t) = C_r dv_{Cr.Os}(t)/dt, \\ i_{2.Os}(t) = C_{\text{eq}} dv_{Lm.Os}(t)/dt \\ v_{Lm.Os}(t) = L_m di_{Lm.Os}(t)/dt \\ i_{2.Os}(t) = i_{Lr.Os}(t) - i_{Lm.Os}(t) \end{cases} \tag{2}$$

where C_{eq} is the sum of the equivalent parasitic capacitor C_T of the transformer and the reflected-to-primary side C_{oss} of all SRs

$$C_{\text{eq}} = C_T + 2C_{oss}n_{\text{SR}}/n^2 \tag{3}$$

where n_{SR} is the number of SRs in parallel and n is the turns ratio of the transformer. Equation (2) can be further normalized based on (1)

$$\begin{cases} 1 = d\hat{i}_{Lr.Os}(\theta)\Big/d\theta + (\hat{v}_{Cr.Os}(\theta) - 1) + \hat{v}_{Lm.Os}(\theta) \\ \hat{i}_{Lr.Os}(\theta) = d\hat{v}_{Cr.Os}(\theta)/d\theta, \hat{i}_{2.Os}(\theta) = hd\hat{v}_{Lm.Os}(\theta)/d\theta \\ \hat{v}_{Lm.Os}(\theta) = d\hat{i}_{Lm.Os}(\theta)\Big/d\theta\Big/k \\ \hat{i}_{2.Os}(\theta) = \hat{i}_{Lr.Os}(\theta) - \hat{i}_{Lm.Os}(\theta) \end{cases} \tag{4}$$

where $\theta = \omega_r t$ is the electrical angle, $k = L_r/L_m$, and $h = C_{\text{eq}}/C_r$, and symbols with superscript "^" in this article represent normalized parameters based on (1). Solving equation set (4) yields

$$\begin{cases} \hat{i}_{2.Os}(\theta) = -\left(C_1 h\lambda_1^2/k\right)\cos(\lambda_1\theta) - \left(C_2 h\lambda_1^2/k\right)\sin(\lambda_1\theta) \\ \quad -\left(C_3 h\lambda_2^2/k\right)\cos(\lambda_2\theta) - \left(C_4 h\lambda_2^2/k\right)\sin(\lambda_2\theta) \\ \hat{v}_{Lm.Os}(\theta) = -\left(C_1\lambda_1/k\right)\sin(\lambda_1\theta) + \left(C_2\lambda_1/k\right)\cos(\lambda_1\theta) \\ \quad -\left(C_3\lambda_2/k\right)\sin(\lambda_2\theta) + \left(C_4\lambda_2/k\right)\cos(\lambda_2\theta) \end{cases} \tag{5}$$

where λ_1 and λ_2 are the characteristic roots of (4), representing the high-frequency component and low-frequency component of (5), respectively

$$\begin{cases} \lambda_1 = \sqrt{\left(1 + h + k + \sqrt{(1+h)^2 - 2(h-1)k + k^2}\right)/2h} \\ \lambda_2 = \sqrt{\left(1 + h + k - \sqrt{(1+h)^2 - 2(h-1)k + k^2}\right)/2h} \end{cases} \tag{6}$$

where C_1, C_2, C_3, and C_4 are the coefficients determined by the initial value of voltage and current in the resonant tank

$$\begin{cases} C_1 = -\left(\hat{i}_{2.Os}(0)k + \hat{i}_{Lm.Os}(0)h\lambda_2^2\right)/\left(h(\lambda_1^2 - \lambda_2^2)\right) \\ C_2 = \lambda_1\left(\hat{v}_{Lm.Os}(0)k + (\hat{v}_{Cr.Os}(0) - \hat{v}_{Lm.Os}(0)h - 2)\lambda_2^2\right)/ \\ \quad \left(\lambda_1^2 - \lambda_2^2\right) \\ C_3 = \left(\hat{i}_{2.Os}(0)k + \hat{i}_{Lm.Os}(0)h\lambda_1^2\right)/\left(h(\lambda_1^2 - \lambda_2^2)\right) \\ C_4 = \lambda_2\left(\hat{v}_{Lm.Os}(0)k + (\hat{v}_{Cr.Os}(0) - \hat{v}_{Lm.Os}(0)h - 2)\lambda_1^2\right)/ \\ \quad \left(\lambda_2^2 - \lambda_1^2\right). \end{cases} \tag{7}$$

Similarly, the second-order linear differential equation set of P_s stages can be derived as follows:

$$\begin{cases} V_{\text{in}}/2 = L_r di_{Lr.Ps}(t)/dt + (v_{Cr.Ps}(t) - V_{\text{in}}/2) + nV_o \\ nV_o = L_m di_{Lm.Ps}(t)/dt = v_{Lm.Ps}(t) \\ i_{Lr.Ps}(t) = C_r dv_{Cr.Ps}(t)/dt \\ i_{2.Ps}(t) = i_{Lr.Ps}(t) - i_{Lm.Ps}(t). \end{cases} \tag{8}$$

After normalizing, the general solution of P_s stage is derived based on (8) and can be expressed as follows:

$$\begin{cases} \hat{i}_{2.Ps}(\theta) = \hat{i}_{Lr.Ps}(0)\cos\theta - (\hat{v}_{Cr.Ps}(0) - 2 + M)\sin\theta \\ \qquad -\hat{i}_{Lm.Ps}(0) - kM\theta \\ \hat{v}_{Lm.Ps}(\theta) = M \end{cases} \tag{9}$$

where $M = 2nV_o/V_{\text{in}}$ is the voltage gain of the resonant tank, and it should be noticed that the general solution of P stage is identical with (9) of the P_s stage. Moreover, the normalized drain–source voltage $\hat{v}_{\text{ds.SR1}}(\theta)$ of S_{s1} can be derived from $\hat{v}_{Lm}(\theta)$

$$\hat{v}_{\text{ds.SR1}}(\theta) = M - \hat{v}_{Lm}(\theta). \tag{10}$$

Then, the normalized drain–source voltage $\hat{v}_{\text{ds.SR1}}(\theta)$ in the O_s stage can be derived by substituting (5) into (10)

$$\begin{aligned} \hat{v}_{\text{ds.SR1}.Os}(\theta) &= \left(C_1\lambda_1/k\right)\sin(\lambda_1\theta) - \left(C_2\lambda_1/k\right)\cos(\lambda_1\theta) \\ &\quad + \left(C_3\lambda_2/k\right)\sin(\lambda_2\theta) - \left(C_4\lambda_2/k\right)\cos(\lambda_2\theta) + M. \end{aligned} \tag{11}$$

Similarly, the normalized drain–source voltage $\hat{v}_{\text{ds.SR1}}(\theta)$ in P_s stage can be derived by substituting (9) into (10)

$$\hat{v}_{\text{ds.SR1}.Ps}(\theta) = M - M = 0. \tag{12}$$

It should be noticed that $v_{\text{ds.SR1}.Ps}$ in P_s stage is typically about -0.7 V when the SR body diode conducts and is millivolt level when channel resistor $R_{\text{ds.on}}$ of SR switch conducts, which is so small that it is reasonable to consider $v_{\text{ds.SR1}.Ps}$ as zero in (12).

According to Fig. 3, O_s stage, which is the first stage of spike current, starts at t_0 when primary switch acts (ignoring the deadtime of primary switches), and then i_2 begins to increase, while $v_{\text{ds.SR1}}$ begins to decrease due to the discharge of C_{eq}, and when $v_{\text{ds.SR1}}$ drops to zero at t_1, O_s stage ends and P_s stage begins. In P_s stage, the body diode of SR is conducted, so $v_{\text{ds.SR1}}$ is regarded as zero, and P_s stage ends when i_2 drops to zero at the first time or when primary switch acts the next time, which also means the end of the spike current. The duration t_{Os} of O_s stage and t_{Ps} of P_s stage can be expressed as follows:

$$\begin{cases} t_{Os} = t_1 - t_0 = \theta/\omega_r|_{\hat{v}_{\text{ds.SR1}.Os}(\theta)=0}, \theta \in (0, \pi/\lambda_1) \\ t_{Ps} = t_2 - t_1 = \min\{\theta/\omega_r\}|_{i_{2.Ps}(\theta)=0}, \theta > 0. \end{cases} \tag{13}$$

Fig. 5 shows the oscillation in O_s stage based on (5) and (11), and it can be seen that i_2 is mainly determined by its high-frequency component, yet its low-frequency component is very small. And due to the existence of low-frequency components of $v_{\text{ds.SR1}}$, t_{Os} is slightly larger than a quarter of the oscillation period in O_s stage, so the maximum spike current $I_{\text{spike.peak}}$ appears in O_s stage and can be derived based on (5) and denormalized as follows:

$$I_{\text{spike.peak}} \approx nI_{\text{base}}h\lambda_1^2\sqrt{C_1^2 + C_2^2}\Big/k. \tag{14}$$

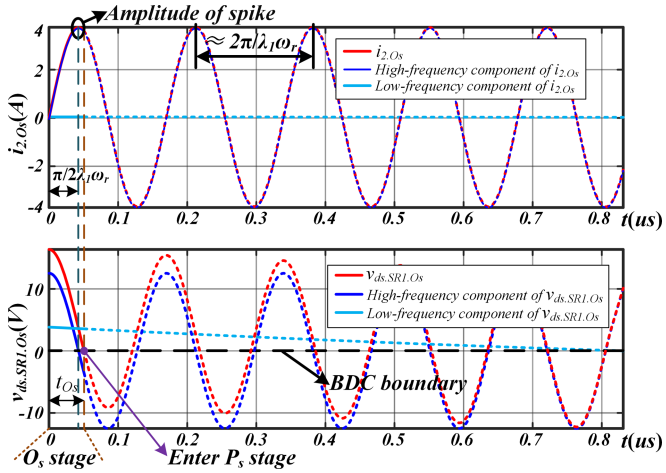


Fig. 5. Oscillation in O_s stage (including the high-frequency component and low-frequency component) and its extension without constraints.

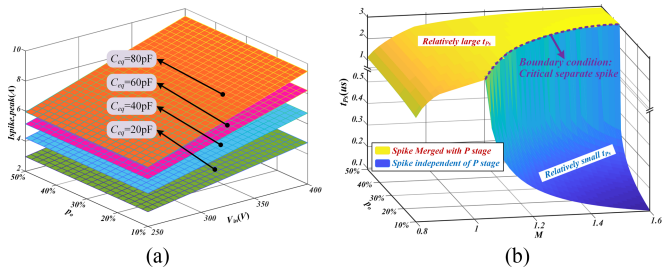


Fig. 6. (a) Amplitude $I_{\text{spike.peak}}$ of spike current versus M and p_o. (b) Duration t_{Ps} of P_s stage of spike current versus M and p_o at $C_{\text{eq}} = 60$ pF.

Since $\lambda_1 \gg \lambda_2$, (14) can be further simplified by substituting (1), (6), and (7) into it and can be represented as follows:

$$I_{\text{spike.peak}} \approx h\lambda_1\lambda_2^2 n V_{\text{in}}/(kZ_r). \tag{15}$$

Equation (15) indicates that, under a certain resonant tank, the amplitude of spike current is only determined by C_{eq} and V_{in}. To be specific, first, the greater the C_{eq}, the larger the $I_{\text{spike.peak}}$ due to the longer discharging time of C_{eq}, and that is, essentially, why the spike current can be regarded as capacitive. Second, under a certain C_{eq}, $I_{\text{spike.peak}}$ is independent of the load condition, yet is proportional to input voltage. Furthermore, the curve of $I_{\text{spike.peak}}$ versus V_{in} and p_o, which is the proportion of output power P_o in rated output power $P_{o.R}$ representing the degree of power load, based on (14) is plotted in Fig. 6(a), which further verifies the reliability of the simplification in (15).

Another dimension of concern is the duration of the spike current. Since O_s stage is the lossless $v_{\text{ds.SR1}}$ discharging stage, yet the BDC or the SR $R_{\text{ds.on}}$ conduction in P_s stage will result in SR conduction loss; consequently, only the duration t_{Ps} of P_s stage is worth analyzing. Based on (13), the curve of t_{Ps} versus M and p_o can be obtained, as shown in Fig. 6(b). It illustrates that, under light-load and high-voltage-gain conditions, the spike current is independent of P stage and t_{Ps} is very small, and with either the decrease of voltage gain or the increase of load, the t_{Ps} will increase until the spike current is merged with P stage. Once the merging occurs, P_s stage will be sustained until the end of P stage and t_{Ps} becomes much larger than that when the spike current is independent of P stage. The boundary condition, named critical separate spike, as shown in Fig. 6(b), actually occurs when i_2 in P_s stage drops to zero with exactly zero slope.

Finally, in order to intuitively reveal the law of spike current in different scenarios, based on (5), (9), and (11)–(13), a series of schematic waveforms of spike current and $v_{\text{ds.SR1}}$ is shown in Fig. 7, which is consistent with the analysis above.

TABLE II
SYSTEM SPECIFICATION OF *LLC* CONVERTERS

Parameters	Values
Input voltage V_{in}	250 V–400 V
Output voltage V_o	12 V
Rated output power $P_{o.R}$	300 W
Resonant inductor L_r	25 μH
Resonant capacitor C_r	25.33 nF
Magnetizing inductor L_m	125 μH
Switching frequency f_s	120–220 kHz

B. Comparison of Different Turn-ON Countermeasures

Theoretically, SR switch S_{s1} is conducted just in P stage, but as expounded above, due to the presence of spike current, there will be conduction of S_{s1} in P_s stage, which is prior to P stage, and that brings the confusion to determine the SR turn-ON time. To figure this issue out, different turn-ON countermeasures are analyzed and compared in this section based on the system specification in Table II. It should be noticed that the analysis in this article follows the principle of turning ON/OFF SR switch once in a switching cycle to minimize switching loss; therefore, only conduction loss should be considered for SR switches.

The most common turn-ON strategy among the existing methods is the radical turn-ON (RTO) strategy, that is, turning ON SRs as soon as the first BDC pulse is detected, which actually occurs at the beginning of P_s stage. Since the duration t_{Os} of O_s stage is much smaller than half switching cycle, from the perspective of ITDM, the operating mode of *LLC* is shifted from *OPO* mode to *PO* mode under light-load conditions; in that case, the reverse current will be present, increasing the conduction loss. On the basis of ITDM, the analysis of reverse current caused by RTO strategy under light-load conditions can be illustrated in Fig. 8. The comparison of resonant current i_{Lr} and SR current $i_{Sec} = n\cdot|i_2|$ between in *PO* mode and in *OPO* mode indicates that the reverse current is more dominant when the voltage gain is relatively high, e.g., $M = 1.536$, as shown in Fig. 8(a), than when the voltage gain is relatively low, e.g., $M = 0.96$, as shown in Fig. 8(b). Moreover, to further inspect the impact of reverse current on power loss, the square of rms value of i_{Lr} and i_{Sec}, which are expressed as $I^2_{Lr.\text{rms}}$ and $I^2_{Sec.\text{rms}}$ and represent unit-resistor loss in primary and secondary side respectively, can be solved based on ITDM, and then the increase ratio $j_{Lr.\text{rms2}}$ of $I^2_{Lr.\text{rms}}$ and $j_{Sec.\text{rms2}}$ of $I^2_{Sec.\text{rms}}$ in *PO* mode relative to that in *OPO* mode can be defined as $j_{Lr.\text{rms2}} = (I^2_{Lr.\text{rms}}|_{PO} - I^2_{Lr.\text{rms}}|_{OPO})/I^2_{Lr.\text{rms}}|_{OPO}$ and $j_{Sec.\text{rms2}} = (I^2_{Sec.\text{rms}}|_{PO} - I^2_{Sec.\text{rms}}|_{OPO})/I^2_{Sec.\text{rms}}|_{OPO}$. The curves of $j_{Lr.\text{rms2}}$ and $j_{Sec.\text{rms2}}$ versus M and p_o, as shown in Fig. 8(c) and (d), indicate that, first, either the lighter the

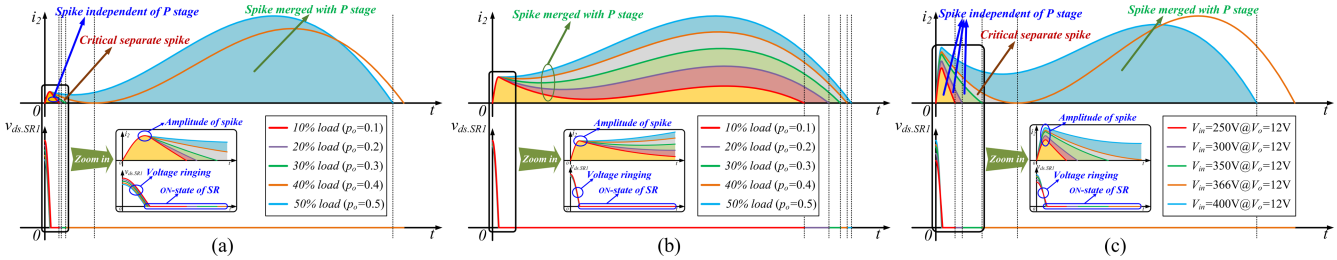


Fig. 7. Capacitive spike current and SR drain–source voltage at $C_{\rm eq} = 31.25$ pF. (a) In BRR: $M = 1.536$. (b) In ARR: $M = 0.96$. (c) Under different $V_{\rm in}$ at $p_o = 0.2$.

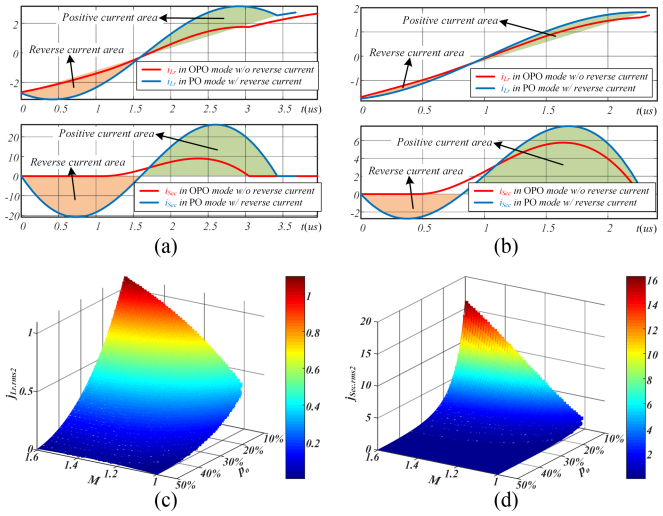


Fig. 8. Analysis of reverse current caused by RTO strategy under light-load conditions on the basis of ITDM, i.e., the comparison of i_{Lr} and i_{Sec} between in *PO* mode and *OPO* mode (a) at $M = 1.536$ and $p_o = 0.1$ and (b) at $M = 0.96$ and $p_o = 0.1$, and the increase ratio of square of rms value of (c) i_{Lr} and (d) i_{Sec} in *PO* mode relative to that in *OPO* mode.

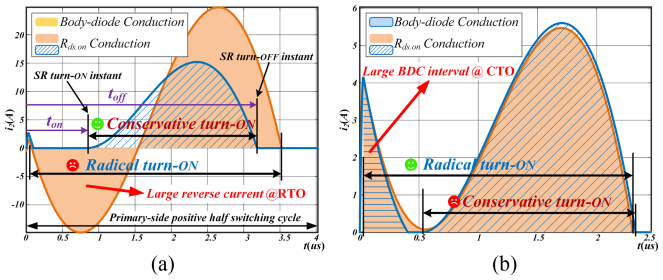


Fig. 9. Comparison between RTO and CTO during positive half switching cycle. (a) In BRR: $M = 1.536$, $p_o = 0.2$, and at $V_{\rm in} = 250$ V. (b) In ARR: $M = 0.96$, $p_o = 0.1$, and at $V_{\rm in} = 400$ V.

load or the higher the voltage gain, the greater the increase of conduction loss caused by the reverse current; second, the increase of conduction loss in the secondary side, as shown in Fig. 8(d), is more significant than that in the primary side, as shown in Fig. 8(c).

When considering the spike current ulteriorly, the remarkable reverse current caused by the RTO strategy under light-load and high-voltage-gain conditions can be shown in Fig. 9(a). Another serviceable countermeasure is the conservative turn-ON (CTO) strategy where SR switches are turned ON at the beginning of P stage, and the core idea of the CTO strategy is that the BDC pulses caused by spike current and a series of oscillations following this spike should be regarded as the false trigger and be ignored. However, there will be a large BDC interval before SR turns ON caused by a current spike under light-load and low-voltage-gain conditions, as shown in Fig. 9(b).

In addition to RTO and CTO strategies, the turn-ON instant of SR drivers should not be earlier than the beginning of P_s stage to prevent the hard turn-ON of SR switches and should not be later than the beginning of P stage to minimize the BDC interval before SR turn-ON instant. Moreover, theoretically, SR turn-ON instant can be anywhere between the beginning of P_s stage and the beginning of P stage, and in order to compare the impact of different turn-ON strategies on efficiency, the total conduction loss of all SR switches after being normalized based on output power P_o can be derived and expressed as the unit SR loss $p_{\rm cnt.SR}$ as follows:

$$p_{\rm cnt.SR} \approx \frac{2f_s}{p_o \cdot P_{o.R}} \left[\int_{t_{Os}}^{t_{\rm on}} i_2(t)dt \cdot nV_{Dth} + \int_{t_{\rm on}}^{t_{\rm off}} i_2^2(t)dt \cdot \frac{n^2 R_{\rm ds.on}}{n_{\rm SR}} \right] \tag{16}$$

where $R_{\rm ds.on}$ is the ON-state resistance of a single SR switch, V_{Dth} is the body-diode threshold voltage of SRs, $t_{\rm on}$ is the SR turn-ON time, i.e., the duration from the beginning of primary-side positive half switching cycle to the rising edge of the driver of S_{s1}, as shown in Fig. 9(a), and $t_{\rm off}$ is the SR turn-OFF time. The unit SR loss in (16) contains the loss caused by BDC in t_{Os}–$t_{\rm on}$, and by $R_{\rm ds.on}$ conduction in $t_{\rm on}$–$t_{\rm off}$, and it should be noticed that, since this article focuses on the SR turn-ON issue, the $t_{\rm off}$ in (16) is always considered to be optimal and there is no BDC signal after SR turns OFF. For a reasonable design of *LLC* converter, the maximum conduction losses of all SRs should normally not exceed 0.5% of the rated output power $P_{o.R}$. And in the occasion of *LLC* with a wide voltage-gain range, the maximum rms value of SR current is approximately associated with the switching frequency and load condition, and that is

$$P_{o.R} \times 0.5\% \geq \max \left\{ \left(\frac{\pi P_{o.R}}{2\sqrt{2f_{n.\min}} V_{o.\max}} \right)^2, \left(\frac{\pi P_{o.R}}{2\sqrt{2f_{n.\max}} V_{o.\min}} \right)^2 \right\} \times R_{\rm SR} \tag{17}$$

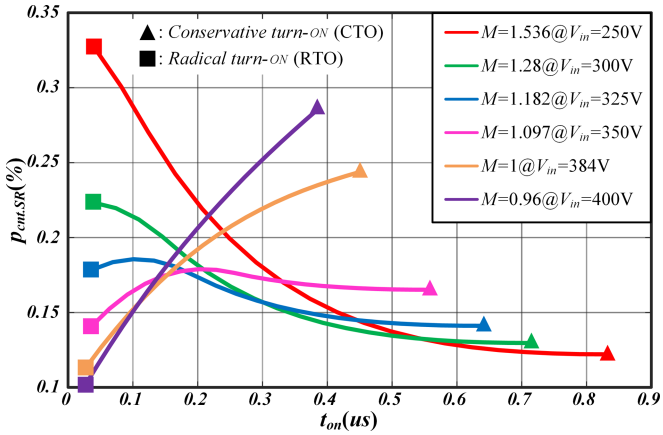


Fig. 10. Unit SR loss $p_{\mathrm{cnt.SR}}$ versus turn-ON time t_{on}. at $p_o = 0.2$, $C_{\mathrm{eq}} = 20$ pF, $n_{\mathrm{SR}} = 2$, $R_{\mathrm{ds,on}} = 2.2$ mΩ, and $V_{Dth} = 0.7$ V.

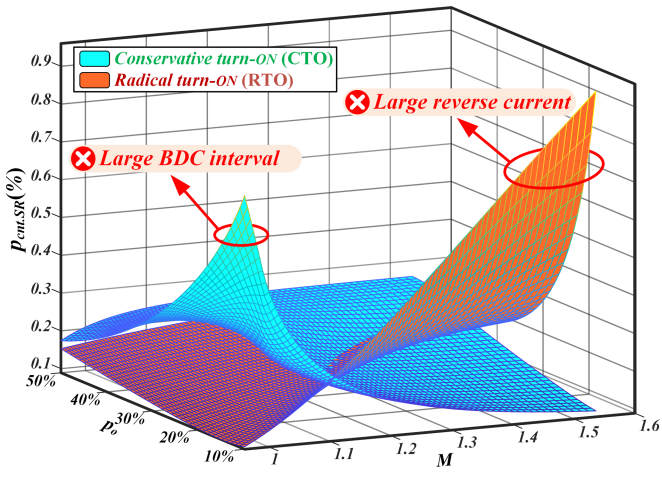


Fig. 11. Unit SR loss $p_{\mathrm{cnt.SR}}$ versus M and p_o under both RTO strategy and CTO strategy at $n_{\mathrm{SR}} = 2$, $C_{\mathrm{eq}} = 40$ pF, $R_{\mathrm{ds,on}} = 2.2$ mΩ, and $V_{Dth} = 0.7$ V.

where $f_{n.\mathrm{min/max}} = f_{s.\mathrm{min/max}}/f_r$, and $R_{\mathrm{SR}} = R_{\mathrm{ds.on}}/n_{\mathrm{SR}}$. According to the power level, output-voltage stress, and switching frequency range, the maximum R_{SR} can be determined by (17) and used to select SR switches and parallel number n_{SR}. Under the system specification in Table II, R_{SR} should be less than 1.1672 mΩ, and then two BSC022N04LS6 from Infineon in parallel ($n_{\mathrm{SR}} = 2$) are selected to constitute SR switches, where $R_{\mathrm{ds.on}}$≈1.8 mΩ at 25 °C–2.34 mΩ at 90 °C, V_{Dth}≈0.65–0.75 V, and C_{oss}≈1.365 nF at 24 V contributing 21.322 pF to C_{eq}.

After that, the unit SR loss $p_{\mathrm{cnt.SR}}$ versus t_{on} under different voltage gains can be plotted based on (16), as shown in Fig. 10, which illustrates that the minimum SR loss only occurs when either the RTO or CTO strategy is adopted. The essential reason is that turning ON SR drivers between the beginning of P_s stage and the beginning of P stage is inferior to the CTO strategy in eliminating reverse current, while inferior to the RTO strategy in eliminating BDC interval. As a result, only the RTO and CTO strategies deserved to be further analyzed.

Based on (16), the curve of $p_{\mathrm{cnt.SR}}$ versus M and p_o under both RTO and CTO strategy is shown in Fig. 11. It can be seen that, under light-load and high-voltage-gain condition, the minimum SR loss is guaranteed by the CTO strategy, while with the decrease of voltage gain or the increase of load, the minimum SR loss is guaranteed by the RTO strategy instead. Accordingly, the whole operating area can be categorized into CTO area and RTO area, where the CTO strategy is optimum in the CTO area, while the RTO strategy is optimum in RTO area. As a result, the core of the SR turn-ON optimization is that, to maintain the minimum SR loss over the whole operating area, using CTO strategy in CTO area yet RTO strategy in RTO area.

It should be noted that although the above analysis is performed under light-load condition, RTO area, in fact, can accommodate the whole heavy-load conditions. Moreover, conclusions in this section can be extended to other conditions of *LLC* converters.

III. Proposed SPF-SR Turn-ON Optimization Strategy

On the basis of analysis in Section II, the proposed SPF-SR turn-ON optimization strategy is described in this section, which consists of the dual identification of optimal SR turn-ON area and the determination of SR turn-ON time based on SPF control.

A. Dual Identification of Optimal SR Turn-ON Area

The first concept of the proposed SPF-SR strategy is identifying the optimal SR turn-ON area, i.e., identifying the boundary between RTO area and CTO area. As mentioned before, SPF-SR strategy is on the basis of ADVS-SR, so in addition to dc signals V_{in}, V_o, and I_o, only BDC signal is sensed for SR control. Especially, the first pulse of the BDC signal in each half switching cycle is caused by a spike current in P_s stage, and according to Figs. 6(b) and 11, the curves of t_{Ps} and $p_{\mathrm{cnt.SR}}|_{\mathrm{CTO}}$ versus M and p_o have similar characteristics. Therefore, V_{in}, V_o, I_o, and t_{Ps} can be used to identify the optimal SR turn-ON area, and for the generality of analysis, $M = 2nV_o/V_{\mathrm{in}}$ and $p_o = V_oI_o/P_{o.R}$ can be derived, and t_{Ps} can be normalized as D_{Ps}, that is

$$D_{Ps} = t_{Ps}/(T_s/8) = 8f_st_{Ps}, (0 \le D_{Ps} \le 1). \tag{18}$$

Based on the analysis above, different boundaries between RTO area and CTO area under different C_{eq} can be mapped into (M-p_o-D_{Ps}) space, as shown in Fig. 12(a), and then projected onto (M-p_o) plane, as shown in Fig. 12(b), and (M-D_{Ps}) plane, as shown in Fig. 12(c). In (M-p_o) plane, area boundaries under different C_{eq} can be conveniently obtained based on the sensed M and p_o. However, it can be seen that the area boundary in (M-p_o) plane changes dramatically with the deviation of C_{eq}, i.e., the greater the C_{eq}, the smaller the CTO area, and vice-versa. Since the C_{eq} is difficult to be obtained and varies with operating conditions, it is not sufficient to identify boundaries only in (M-p_o) plane.

In (M-D_{Ps}) plane, however, the area boundary changes much slightly with the deviation of C_{eq} compared with that in (M-p_o) plane, which is very beneficial for identifying the area boundary. However, the BDC pulse in the P_s stage can only be integrally sensed by CTO strategy, yet be destroyed by premature SR turn-ON under the RTO strategy, so that in RTO area, the SR turn-ON time should be first tuned to the beginning of P stage before the area identification. Since RTO area is usually the dominant

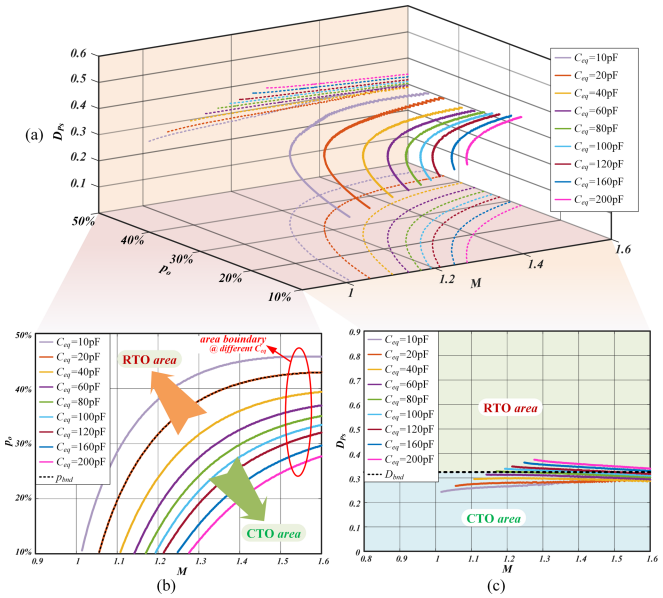


Fig. 12. Boundaries between RTO area and CTO area under different $C_{\rm eq}$. (a) at $n_{\rm SR} = 2$, $R_{\rm ds,on} = 2.2$ mΩ, and $V_{Dth} = 0.7$ V in (M-p_o-D_{Ps}) space and the projection of Fig. 12(a) onto (b) (M-p_o) plane and (c) (M-D_{Ps}) plane.

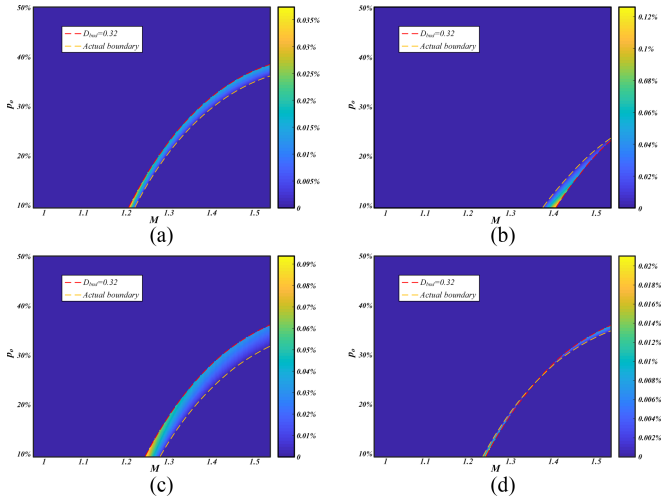


Fig. 13. Differences between actual unit SR loss and minimum unit SR loss caused by parameters mismatch at $n_{\rm SR} = 2$. (a) $R_{\rm ds,on} = 2.2$ mΩ, $V_{Dth} = 0.7$ V, and $C_{\rm eq} = 30$ pF. (b) $R_{\rm ds,on} = 2.2$ mΩ, $V_{Dth} = 0.7$ V, and $C_{\rm eq} = 120$ pF. (c) $R_{\rm ds,on} = 1.8$ mΩ, $V_{Dth} = 0.75$ V, and $C_{\rm eq} = 40$ pF. (d) $R_{\rm ds,on} = 2.34$ mΩ, $V_{Dth} = 0.65$ V, and $C_{\rm eq} = 40$ pF.

area that contains most of the heavy-load condition, the area boundary identification only in (M-D_{Ps}) plane will complicate the implementation of the identification process.

Aiming at the above issues, a novel dual-identification method, which combines the p_o-identification in (M-p_o) plane and the D_{Ps}-identification in (M-D_{Ps}) plane, is proposed in this article.

First, according to the selected SR switch, C_{oss} contributes about 21.322 pF to $C_{\rm eq}$. Therefore, based on a conservative area boundary $p_{\rm bnd}$ at $C_{\rm eq} = 20$ pF in (M-p_o) plane, p_o-identification is performed to preliminarily screen out most of the RTO areas, as shown in Fig. 12(b), where $p_{\rm bnd}$ can be established by a lookup table indexed by M. Hence, if the sensed p_o is not smaller than $p_{\rm bnd}$, it must be in RTO area; otherwise, the D_{Ps}-identification is performed in (M-D_{Ps}) plane to further identify the optimal area. At the beginning of D_{Ps}-identification, SR turn-ON time is first tuned by CTO strategy, and then D_{Ps} can be sensed and derived based on (18). As illustrated in Fig. 12(c), the area boundary under different $C_{\rm eq}$ in (M-D_{Ps}) plane can be approximately unified as a constant value $D_{\rm bnd}$, and that is

$$D_{\rm bnd} \approx 0.32 = \text{Constant}. \tag{19}$$

Actually, the reason why the area boundary in (M-D_{Ps}) plane changes slightly near constant $D_{\rm bnd}$ with the deviation of $C_{\rm eq}$ is that a certain degree of the D_{Ps} is always required to achieve the same $p_{\rm cnt.SR}|_{\rm CTO}$ and $p_{\rm cnt.SR}|_{\rm RTO}$. Based on (19), the optimal area can be further determined by comparing D_{Ps} with $D_{\rm bnd}$ when p_o is smaller than $p_{\rm bnd}$, and that is, if D_{Ps} is not smaller than $D_{\rm bnd}$, it is in RTO area; otherwise, it is in CTO area. In conclusion, the proposed dual identification of optimal SR turn-ON area can be summarized as follows:

$$\text{SR turn-on} \begin{cases} \text{CTO}, & p_o < p_{\rm bnd} \;\&\&\; D_{Ps} < D_{\rm bnd} \\ \text{RTO}, & p_o \geq p_{\rm bnd} || D_{Ps} \geq D_{\rm bnd}. \end{cases} \tag{20}$$

In order to further inspect the impact of parameter mismatch on the dual-identification method in (20), differences between the actual unit SR loss and minimum unit SR loss are illustrated in Fig. 13. It shows that, with the deviation of $C_{\rm eq}$, $R_{\rm ds.on}$, and/or V_{Dth}, in most areas away from the boundary $D_{\rm bnd}$, the minimum SR loss is always guaranteed by (20), yet in the area near $D_{\rm bnd}$, the actual unit SR loss increases inconsiderably compared with the minimum of that (e.g., up to about 0.12%). Therefore, the strategy in (20) has good immunity to the parameter mismatch.

In addition, it should be noticed that RTO strategy is natively the optimal one when the spike current is merged with P stage, and hence, the area boundary can only occur when the spike current is independent of P stage.

B. Determination of SR Turn-ON Time Based on SPF Control

On the basis of (20), RTO and CTO areas can be identified over the whole operating range, and the mission of step two is to determine the SR turn-ON time in these two areas.

As discussed above, in RTO area, SRs should turn ON at the beginning of P_s stage, i.e., the beginning of the first BDC pulse, which can be easily achieved by adaptive stepwise control. Yet in CTO area, SRs should turn ON at the beginning of P stage to eliminate large reverse current; in that case, the traditional adaptive stepwise tuning process is no longer operative due to the falsely triggered BDC pulses caused by current spike and the following oscillations. In conclusion, to optimize the SR turn-ON, a proper turn-ON time delay is essential in CTO area, while a deliberate premature turn-ON is necessary in RTO area.

Aiming at that, a novel SPF-SR strategy is proposed in this section for determining SR turn-ON time. To be specific, in RTO area, the single stepwise tuning process is sufficient and the output of the feedforward control is set as zero. While in CTO area, the feedforward control predetermines the beginning time of the P stage, and the adaptive stepwise tuning process fine

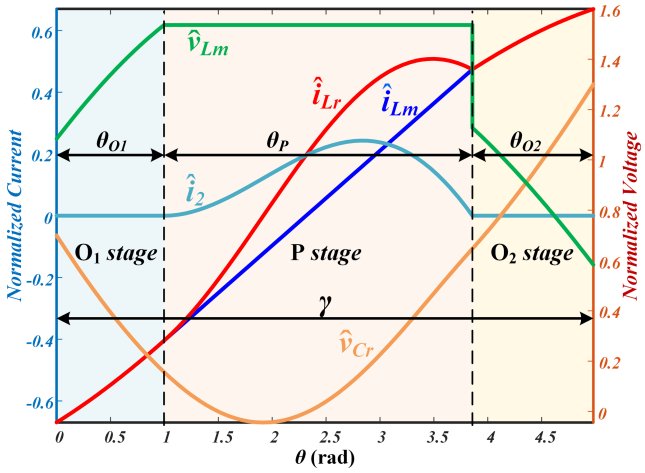


Fig. 14. Normalized waveforms of the *LLC* resonant tank in *OPO* mode during positive half switching cycle based on ITDM.

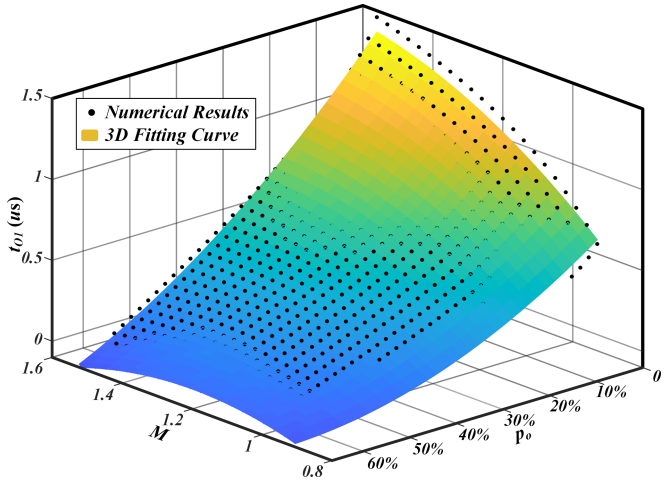


Fig. 15. Numerical solving results of t_{O1} in *OPO* mode based on ITDM and the 3-D polynomial fitting curve of t_{O1} where $R^2 = 0.9958$.

tunes the SR turn-ON time with a small step size to draw near the optimal point. According to Fig. 11, the CTO area only occurs under light-load condition, which is right contained in the *OPO* mode from the perspective of ITDM; therefore, the beginning time of *P* stage in CTO area can be preliminarily derived from the duration t_{O1} of the first *O* stage in the ideal *OPO* mode.

Based on ITDM, general solutions of state variables in *LLC* resonant tank in different stages can be obtained [2], and then the normalized waveforms of ideal OPO mode can be illustrated, as shown in Fig. 14, where $\theta_{O1} = \omega_r \cdot t_{O1}$ is the normalization of t_{O1}. And referring to Fig. 14, normalized constrain equations of the ideal *OPO* mode can be established to solve t_{O1}.

The total duration of O_1, *P*, and O_2 stages should be equal to half switching period, and that is

$$\theta_{O1} + \theta_P + \theta_{O2} = \gamma = \pi / f_n \tag{21}$$

where $f_n = f_s/f_r$. In steady state, the values of the inductor current and capacitor voltage at the beginning and end of the half switching period should be symmetrical to their dc component, that is

$$\begin{cases} \hat{i}_{Lr}(\theta_{O2})\Big|_{O2\text{stage}} = -\hat{i}_{Lr}(0)\Big|_{O1\text{stage}} \\ \hat{v}_{Cr}(\theta_{O2})|_{O2\text{stage}} = -\hat{v}_{Cr}(0)|_{O1\text{stage}} + 2. \end{cases} \tag{22}$$

At the joints of each two adjacent stages, the inductor current and capacitor voltage should be continuous, and that is

$$\begin{cases} \hat{i}_{Lr}(\theta_{O1})\Big|_{O1\text{stage}} = \hat{i}_{Lr}(0)\Big|_{P\text{stage}}, \hat{i}_{Lr}(\theta_P)\Big|_{P\text{stage}} \\ \quad = \hat{i}_{Lr}(0)\Big|_{O2\text{stage}} \\ \hat{i}_{Lm}(\theta_{O1})\Big|_{O1\text{stage}} = \hat{i}_{Lm}(0)\Big|_{P\text{stage}}, \hat{i}_{Lm}(\theta_P)\Big|_{P\text{stage}} \\ \quad = \hat{i}_{Lm}(0)\Big|_{O2\text{stage}} \\ \hat{v}_{Cr}(\theta_{O1})|_{O1\text{stage}} = \hat{v}_{Cr}(0)|_{P\text{stage}}, \hat{v}_{Cr}(\theta_P)|_{P\text{stage}} \\ \quad = \hat{v}_{Cr}(0)|_{O2\text{stage}}. \end{cases} \tag{23}$$

At the end of O_1 stage, normalized magnetizing voltage $\hat{v}_{Lm}$ should be exactly equal to the voltage gain *M*, and that is

$$\hat{v}_{Lm}(\theta_{O1})|_{O1\text{stage}} = M. \tag{24}$$

Since only *P* stage is the energy-delivery stage in *OPO* mode, normalized load current $\hat{I}_o$ can be expressed as the average of $\hat{i}_2$ in *P* stage, and that is

$$\begin{aligned} \gamma \hat{I}_o &= \int_0^{\theta_P} \left(\hat{i}_{Lr}\Big|_{P\text{stage}} - \hat{i}_{Lm}\Big|_{P\text{stage}} \right) d\theta \\ &= \hat{v}_{Cr}(0)|_{O2\text{stage}} - \hat{v}_{Cr}(0)|_{P\text{stage}} \\ &\quad - \hat{i}_{Lm}(0)\Big|_{P\text{stage}} \theta_P - \frac{1}{2} k M \theta_P^2. \end{aligned} \tag{25}$$

By combining (21)–(25), the normalized mode equation set of *OPO* mode, which contains transcendental equations, can be fully characterized. Similar to the idea in [22], t_{O1} is numerically solved using the *fsolve* function in MATLAB and expressed by the polynomial fitting method. The numerical solving result and the 3-D polynomial fitting curve of t_{O1} versus *M* and p_o are shown in Fig. 15, and the fitted expression of t_{O1} can be derived as a function of *M* and p_o, which can be expressed as follows:

$$\begin{aligned} t_{O1} &= \theta_{O1}/\omega_r = f(M, p_o) \\ &= (-2.092 + 4.085M - 0.343p_o \\ &\quad - 1.152M^2 - 1.985M \cdot p_o + 1.545p_o^2)(\mu\text{s}). \end{aligned} \tag{26}$$

Hence, only t_{O1} in (26) needs to be calculated online for the proposed feedforward control, and the feedforward signal $t_{\text{on.ffw}}$ is set as t_{O1} in CTO area based on (26), yet set as zero in RTO area, and that is

$$t_{\text{on.ffw}} = \begin{cases} 0, & \text{in RTO area} \\ t_{O1}, & \text{in CTO area.} \end{cases} \tag{27}$$

Moreover, the output of adaptive stepwise tuning, expressed as $t_{\text{on.spw}}$, will be decreased with a small step size Δt_{spw} from its value in the previous control cycle, expressed as $t'_{\text{on.spw}}$, if there

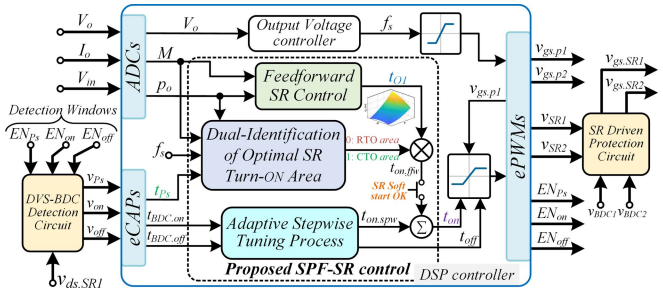


Fig. 16. System block diagram of *LLC* converters with the SPF-SR strategy.

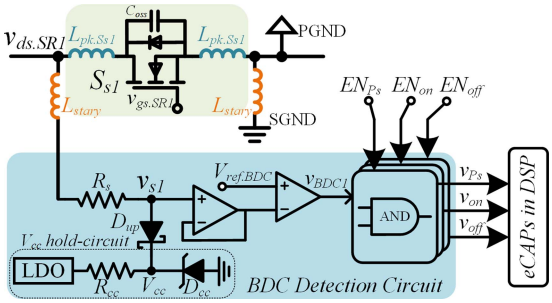


Fig. 17. Modified DVS-based BDC-signal detection circuit, which is very suitable for the low-output-voltage applications.

is an overlarge BDC interval right before SR turns ON, while be increased if a tiny or even no BDC interval is detected, that is

$$t_{\text{on.spw}} = \begin{cases} t'_{\text{on.spw}} - \Delta t_{\text{spw}}, & \text{overlarge BDC} \\ t'_{\text{on.spw}} + \Delta t_{\text{spw}}, & \text{tiny or no BDC.} \end{cases} \tag{28}$$

The SPF-SR strategy combines the adaptive stepwise tuning control and feedforward control to determine SR turn-ON time. As a result, based on (26)–(28), the optimal SR turn-ON time t_{on} can be expressed as follows:

$$t_{\text{on}} = t_{\text{on.spw}} + t_{\text{on.ffw}}. \tag{29}$$

IV. Implementation of the Proposed SPF-SR Strategy

The proposed SPF-SR turn-ON optimization strategy can be implemented with a cost-effective digital microcontroller and a few logic circuits, as illustrated in the system block diagram in Fig. 16, where output-voltage control and the proposed SPF-SR control are integrated into one microcontroller. Implementation of the SPF-SR strategy primarily contains the concept of directly voltage-sensing (DVS) based BDC detection method, SR soft start, digital control sequence, and driven-protection method.

A. DVS-Based BDC Detection Method

The SPF-SR strategy is on the basis of ADVS-SR, where BDC signal is the key SR signal. In this section, a modified DVS-based BDC detection circuit, which is suitable for the low-output-voltage application, is proposed, as shown in Fig. 17.

First, to accurately sense drain–source voltage $v_{\text{ds.SR1}}$ in the ON-state while reliably blocking that in the OFF-state, a resistor R_s in series to $v_{\text{ds.SR1}}$, a diode D_{up} pulled up to V_{cc}, and a

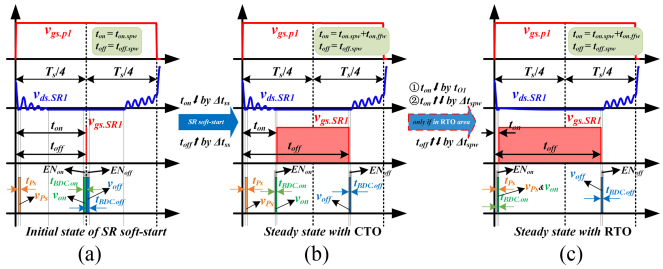


Fig. 18. Proposed SR soft-start process. (a) Initial state of SR soft-start process. (b) SR soft-start process reaches steady state under CTO strategy. (c) Steady state under RTO strategy when RTO area is identified.

V_{cc} hold circuit are utilized to form the DVS circuit. Hence, the sensed voltage v_{s1} captures the ON-state $v_{\text{ds.SR1}}$ with a high accuracy since the voltage drop across R_s is puny when S_{S1} is in the ON-state. Besides, v_{s1} is clamped to $V_{cc} + V_{D\text{up}}$ when S_{S1} is in the OFF-state, where $V_{D\text{up}}$ is the forward voltage of D_{up}. By contrast, antiseries diode or resistive voltage divider is always utilized to sense $v_{\text{ds.SR1}}$ in most of the conventional DVS methods where the sensing accuracy or the sensing noise immunity is sacrificed, respectively.

The v_{s1} will generate the BDC signal v_{BDC1} of S_{s1} through the impedance matching and the comparison to reference voltage $V_{\text{ref.BDC}}$. Furthermore, to obtain BDC signals, including v_{Ps} in P_s stage, v_{on} right before SR turns ON, and v_{off} right after SR turns OFF, which are required for the proposed SPF-SR control; three corresponding detecting-window signals EN_{Ps}, EN_{on}, and EN_{off}, which will be discussed later, are well designed. Finally, those three specialized BDC signals will be sent to eCAP submodule of the DSP microcontroller to perform the SPF-SR control.

B. SR Soft-Start Strategy

To reposefully launch the proposed SR control during the startup process of *LLC* converters, a matched SR soft-start strategy is proposed in this section. If *LLC* begins to startup, V_o soft-start program, which is associated with the primary-side drivers, is executed first, while SR control still remains blocked. Once the V_o soft-start program is terminated, V_o is basically established and then the proposed SR soft-start strategy begins to work.

According to the *LLC* ITDM, with the decrease of load, both t_{on} and t_{off} will approach $T_s/4$ at the boundary between *OPO* and *O* (no-load) mode, and thus, over the whole operating range, the SR turn-ON/OFF time satisfies that

$$t_{Os} \le t_{\text{on}} \le T_s/4 \le t_{\text{off}} \le 3T_s/4. \tag{30}$$

In consequence, the initial value of both t_{on} and t_{off} during SR soft-start process is set to $T_s/4$, as shown in Fig. 18(a). In the beginning, the single stepwise tuning control with step size Δt_{ss} is adopted, where t_{on} begins to decrease, yet t_{off} begins to increase. During this process, the BDC interval right before SR turns ON and right after SR turns OFF will be decreased. When both the pulsewidths of v_{on}, expressed as $t_{\text{BDC.on}}$, and of v_{off}, expressed as $t_{\text{BDC.off}}$, are within the designed hysteresis

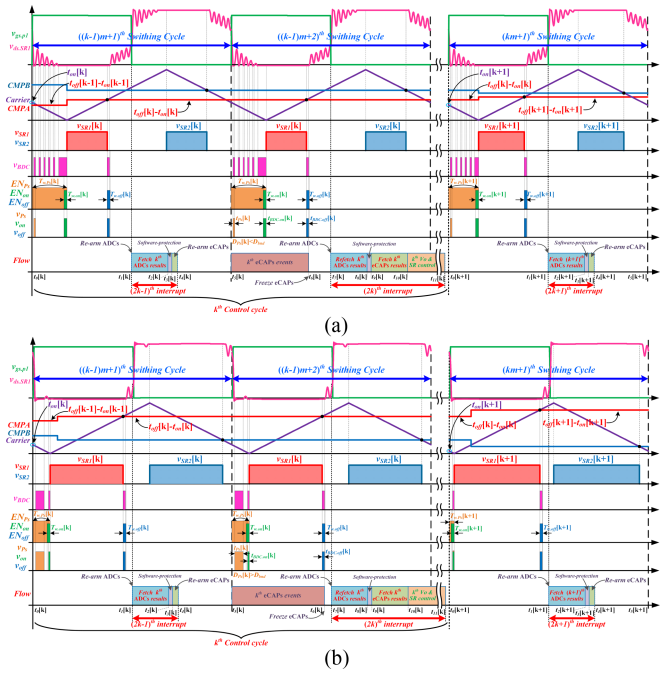


Fig. 19. Digital control sequence of SPF-SR strategy on switching-cycle scale in a cost-effective digital microcontroller. (a) In CTO area. (b) In RTO area.

zone, the steady state of SR is preliminarily reached based on the CTO strategy, as shown in Fig. 18(b); therefore, the steady state of adaptive SR stepwise tuning process can be expressed as follows:

$$T_{th.\min} \le t_{\mathrm{BDC.on}} \text{ and } t_{\mathrm{BDC.off}} \le T_{th.\max}. \tag{31}$$

where $T_{th.\min}$ and $T_{th.\max}$ are the lower and upper boundary of the designed hysteresis zone, respectively. Once (31) is satisfied, dual identification of optimal SR turn-ON area are launched, and subsequent SR turn-ON control is shifted to SPF control from a single stepwise tuning. If CTO area is identified, SR soft-start process is accomplished. If RTO area is identified; however, the feedforward control will be bypassed so that t_{on} is decreased by t_{O1} immediately according to (27), and then the SR time will be tuned by the SPF-SR control until SR steady state in RTO area is reached, as shown in Fig. 18(c), which means that SR soft-start process in RTO area is accomplished.

C. Digital Control Sequence

In order to implement the SPF-SR control in a cost-effective digital controller, multicycle control concept is utilized, that is, executing SR control once in every m switching cycles ($m = 2, 3, 4, \ldots$). The digital control sequence of the proposed SPF-SR strategy on switching-cycle scale is illustrated in Fig. 18, where number k represents the kth control cycle ($k = 1, 2, 3, \ldots$).

In each control cycle, as shown in Fig. 19, dual interrupts are adopted to guarantee minimum eCAP time delay. To be specific, in each kth control cycle, the $(2k-1)$th and the $(2k)$th interrupts are responded in the first and second switching cycle, respectively. In the $(2k-1)$th interrupt, the kth ADC results are first fetched for software protection, and then the

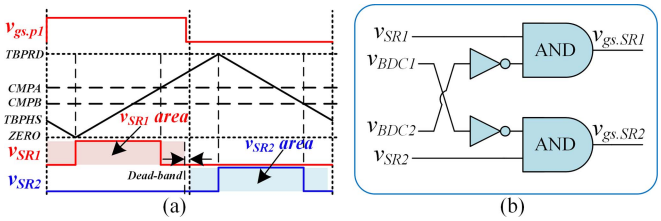


Fig. 20. SR-driven-protection method. (a) Digital protection of PWM signals for SR switches. (b) BDC-signal-based driver interlock circuit.

eCAP submodule is rearmed so that BDC signals in the second switching cycle are captured in the kth eCAP events, then eCAP will be frozen automatically. In the $(2k)$th interrupt, the kth ADC results are refetched for the protection and the kth V_o control, the kth eCAP results are fetched for the kth SR control, and finally, the $(2k)$th interrupt is finished in the mth switching cycle until the kth control is accomplished.

In order to capture the desired BDC pulses v_{Ps}, v_{on}, and v_{off}, three detecting-window signals EN_{Ps}, EN_{on}, and EN_{off} should be well designed. EN_{on} and EN_{off} are right before SR turns ON and right after SR turns OFF, respectively, and the pulsewidth of them is smaller than half oscillating period in O_s stage. EN_{Ps} starts at the rising edge of the primary driver $v_{gs.p1}$ of S_{p1} and ends at the rising edge of pulsewidth modulation (PWM) signal v_{SR1} of S_{s1}. Benefiting from one-shot eCAP configuration, v_{Ps} in P_s stage can be easily captured.

Moreover, in order to avoid frequent SR turn-ON oscillation in steady state caused by D_{Ps}-identification in RTO area, in this article, if the difference between p_o and that when the last D_{Ps}-identification is executed, expressed as $p_{o.\mathrm{pre}}$, is less than 2%, D_{Ps}-identification will be prohibited, and the last optimal turn-ON area will be on hold until a new D_{Ps}-identification is rebooted.

Fig. 19(a) shows SR time tuning process in CTO area, where $v_{\mathrm{SR1}}[k+1]$ and $v_{\mathrm{SR2}}[k+1]$, which are PWM signals for S_{s1} and S_{s2}, respectively, can be properly tuned based on $t_{\mathrm{BDC.on}}[k]$, $t_{\mathrm{BDC.off}}[k]$, $t_{Ps}[k]$, and the kth M, p_o, and f_s. Fig. 19(b) shows the SR time tuning process in RTO area, where the p_o-identification in the $(k-1)$th control cycle cannot screen out the optimal area, and $t_{\mathrm{on}}[k]$ will be tuned by CTO strategy, and then D_{Ps}-identification will be executed in the kth control cycle. Since $D_{Ps}[k] > D_{\mathrm{bnd}}$ is satisfied in Fig. 19(b), $t_{\mathrm{on}}[k+1]$ will be tuned by RTO strategy.

D. SR-Driven-Protection Method

In most cases, SR shoot-through condition is destructive to *LLC* converters; therefore, it is critical to prevent the simultaneous conduction of SR switches S_{s1} and S_{s2}, especially in the transient process. To this end, in this article, SR-driven protection consists of two aspects.

1) SR drivers for S_{s1} and S_{s2} should not be high level simultaneously.
2) SR driver for S_{s1}/S_{s2} should not be high level when the body diode of S_{s2}/S_{s1} is conducted.

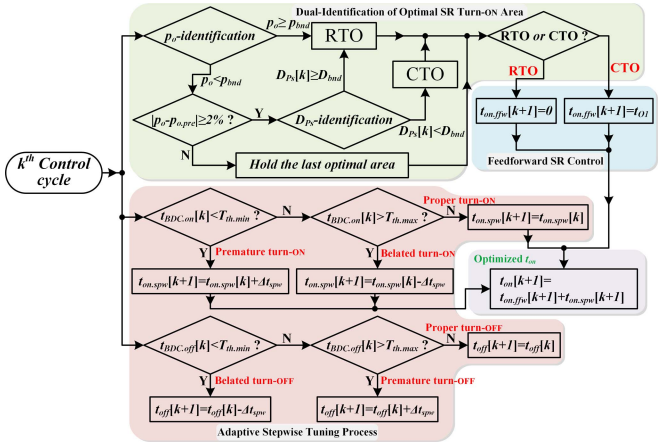
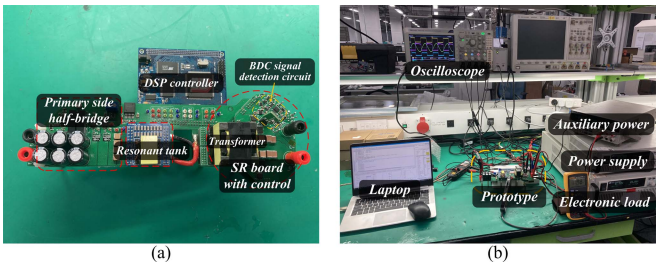


Fig. 21. Digital control diagram of the proposed SPF-SR control strategy.



(a) (b)

Fig. 22. Experimental environments. (a) Prototype of *LLC* converter with the proposed SPF-SR control. (b) Experimental test platform.

First, as shown in Fig. 20(a), based on the up–down-count configuration of the DSP ePWM submodule, PWM signals $v_{\rm SR1}$ and $v_{\rm SR2}$ are generated in the up-count stage and the down-count stage, respectively, with proper deadtime. Therefore, $v_{\rm SR1}$ and $v_{\rm SR2}$ are natively symmetry and cannot be high level simultaneously.

Second, in terms of aspect 2), BDC-signal-based driver interlock circuit, consisting of a few AND gates and NOT gates, is designed, as shown in Fig. 20(b), where the SR driver $v_{gs.\rm SR1}$ of S_{s1} will be disabled once $v_{\rm BDC2}$ is at high level, even if $v_{\rm SR1}$ is at high level, and similarly does the $v_{gs.\rm SR2}$ of S_{s2}. Actually, this is essential for SR-driven protection of *LLC* converters in ARR.

The digital control diagram of the SPF-SR strategy is shown in Fig. 21, and the analysis in this section can indicate that the implementation of SPF-SR strategy hardly increases hardware cost, loss, and online computational complexity compared with that of the available ADVS-SR methods.

V. Experimental Results

The proposed SPF-SR control strategy is verified on a 300-W *LLC* prototype with DSP microcontroller TMS320F28335 from Texas Instruments, as shown in Fig. 22(a). It illustrates that the *LLC* prototype consists of a primary-side half-bridge, a resonant tank, and an SR daughterboard with the integrated transformer. Operation specifications and parameters of key components of the designed *LLC* prototype are listed in Tables II and III,

TABLE III
Parameters of Key Components of *LLC* Prototype With SR Control

Key Components	Parameters
Resonant inductor L_r	PQ2020, PC95 ferrite core 25 μH, 0.1 mm*80, 19 turns
Resonant capacitor C_r	CGA5H4C0G2J562J115AA 5.6nF/2*9, 630VDC, C0G-MLCC
Transformer T	PQ3230, PC95 ferrite core L_m=125 μH, 16:1:1 with center-tap Primary-side coil: 0.1 mm*80 Secondary-side coil: 0.1 mm*200*4
Primary switches S_{p1}–S_{p2}	GaN System GS66504B
SR switches S_{s1}–S_{s2}	2 Infineon BSC022N04LS6 in parallel

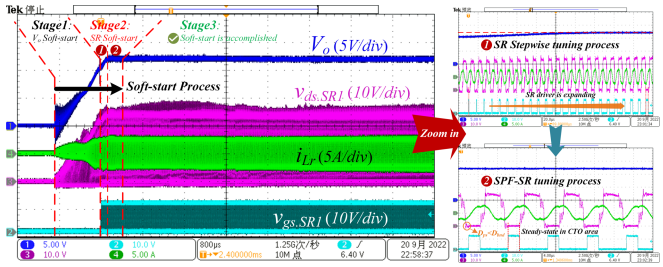


Fig. 23. Soft-start process of the *LLC* prototype in CTO area that consists of V_o soft-start process and SR soft-start process.

respectively, and the experimental test platform of the *LLC* prototype is established, as shown in Fig. 22(b).

Fig. 23 shows the result of *LLC* soft-start process in the CTO area consisting of two stages, where stage 1 is the V_o soft-start process and stage 2 is the SR soft-start process. In stage 1, the SR driver remains blocked and the duty cycle of $v_{\rm pri}$, which is the input voltage of the resonant tank, is increased from 0% to 50% with proper deadband time for the power delivery, and thus, V_o is increased from zero. In stage 2, SR driver is unblocked and there are two substages, as shown in the enlarged view of Fig. 23, where SR driver is expanded based on the stepwise tuning control in substage 1 until the steady state under CTO strategy is reached, and in substage 2, SPF-SR control begins to work together with the V_o closed-loop control since the sensed D_{ps} is smaller than $D_{\rm bnd}$, the SR soft-start process is accomplished, and *LLC* operates stably in CTO area.

To verify the reliability and accuracy of the proposed SPF-SR strategy, some steady-state results are exhibited in Figs. 24–26. Fig. 24 shows results in CTO area under the light-load condition at $V_{\rm in}$ = 250 V, V_o = 12 V, M = 1.536, and p_o = 20%. It can be seen that, when using the conventional ADVS-SR strategy in CTO area, as shown in Fig. 24(a), premature turn-ON will be produced caused by a false trigger and there will be a large reverse current, while SPF-SR strategy will generate proper SR drivers without reverse current, as shown in Fig. 24(b), and compared with that in Fig. 24(a), the rms value of i_{Lr} is smaller and the power efficiency of the *LLC* prototype is improved by 1.59%.

Fig. 25 shows results in RTO area under light-load condition at $V_{\rm in}$ = 400 V, V_o = 12 V, M = 0.96, and p_o = 10%. It can be seen that, if a single CTO strategy is utilized or a rough SR turn-ON delay is imposed constrainedly, as shown in Fig. 25(a), there will be a large BDC interval in P_s stage, which causes dissipative

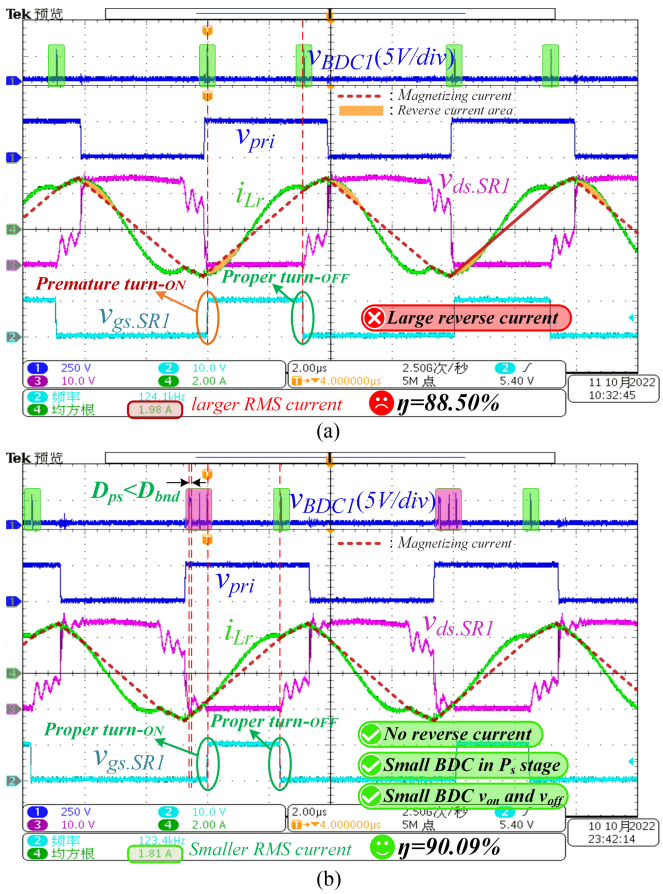


Fig. 24. Steady-state results in CTO area under light-load condition at V_{in} = 250 V, V_o = 12 V, M = 1.536, and p_o = 20%. (a) Large reverse current caused by the premature turn-ON based on the conventional ADVS-SR strategy. (b) Proper SR control without reverse current based on the proposed SPF-SR strategy.

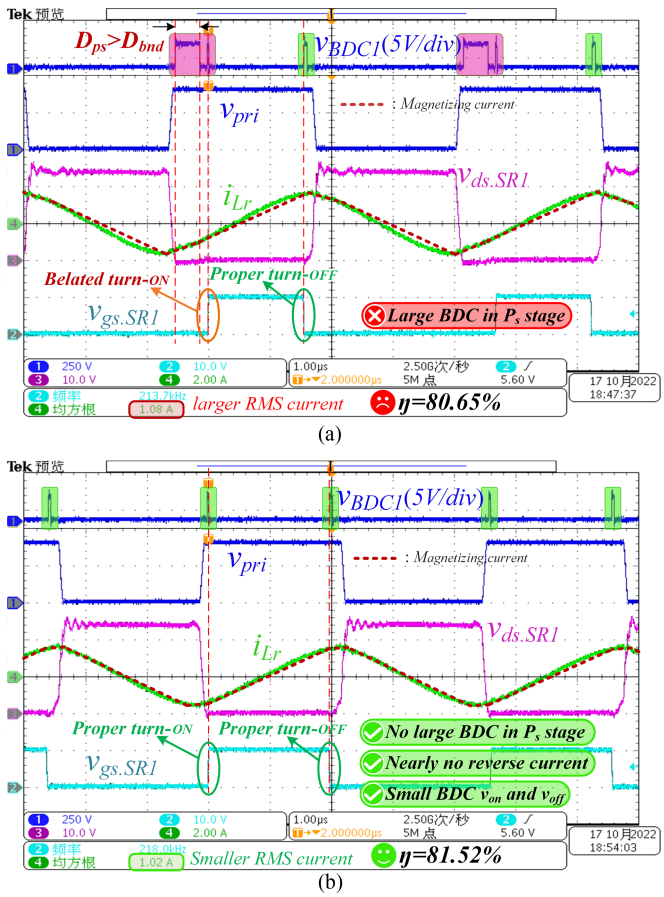


Fig. 25. Steady-state results in RTO area under light-load condition at V_{in} = 400 V, V_o = 12 V, M = 0.96, and p_o = 10%. (a) Large BDC interval in P_s stage caused by belated turn-ON when single CTO strategy is utilized or a rough turn-ON delay is imposed constrainedly. (b) Proper SR control without large BDC interval in P_s stage based on the proposed SPF-SR strategy.

power efficiency, while the SPF-SR strategy will generate proper SR drivers without large BDC interval in P_s stage, as shown in Fig. 25(b), and compared with that in Fig. 25(a), the rms value of i_{Lr} is smaller and power efficiency of *LLC* is improved by 0.87%.

Fig. 26 shows the steady-state results of SPF-SR strategy under heavy-load conditions, where Fig. 26(a) shows the result in BRR at V_{in} = 300 V, V_o = 12 V, M = 1.28, and p_o = 100%, and Fig. 26(b) shows the result in ARR at V_{in} = 400 V, V_o = 12 V, M = 0.96, and p_o = 100%. It can be seen that under heavy-load condition, *LLC* operates stably in RTO area based on SPF-SR strategy, either in BRR or in ARR.

The steady-state results in Figs. 24–26 indicate that, under light-load condition, the SPF-SR strategy cannot only eliminate large reverse current in CTO area but also eliminate large BDC interval in P_s stage in RTO area, and under heavy-load condition, SPF-SR strategy tunes SR turn-ON time based on the RTO strategy to eliminate large BDC interval. Consequently, compared with the existing ADVS-SR methods, the proposed SPF-SR strategy can produce proper SR turn-ON/OFF time over the whole operating range, and the steady-state results above verify the analysis in Sections II and III.

Moreover, the steady-state result of commercial SR control IC NCP4308 from ON Semiconductor under light-load condition in BRR is shown in Fig. 27. To avoid multiple SR turn-ON/OFF caused by the false trigger, minimum ON/OFF blanking time is provided in NCP4308. It can be seen that the premature turn-ON effected by the false trigger of BDC will cause large reverse current, and the premature turn-OFF affected by parasitic inductor will cause large BDC interval v_{off}. Therefore, compared with the proposed SPF-SR strategy, the power efficiency when utilizing this SR IC will be declined dramatically.

Ulteriorly, in order to verify the dynamic performance of the proposed SPF-SR strategy, some transient results are captured, as shown in Figs. 28–31. Fig. 28 shows the dynamic result of the load step-up process (i.e., from 20% load to 100% load) in BRR at V_{in} = 250 V, V_o = 12 V, and M = 1.536. It can be seen that, in the steady state before the load steps up, *LLC* prototype operates in CTO area, where $D_{ps} < D_{\text{bnd}}$, and thus, reverse current is eliminated, during the load step-up process, the optimal SR turn-ON area is gradually shifted from CTO area to RTO area to eliminate the large BDC interval in P_s stage, and the enlarged view of a typical point in the load step-up process shows the proper SR driver in RTO area where $p_o > p_{\text{bnd}}$, and in the steady state after load steps up, *LLC* operates stably in RTO where $p_o > p_{\text{bnd}}$.

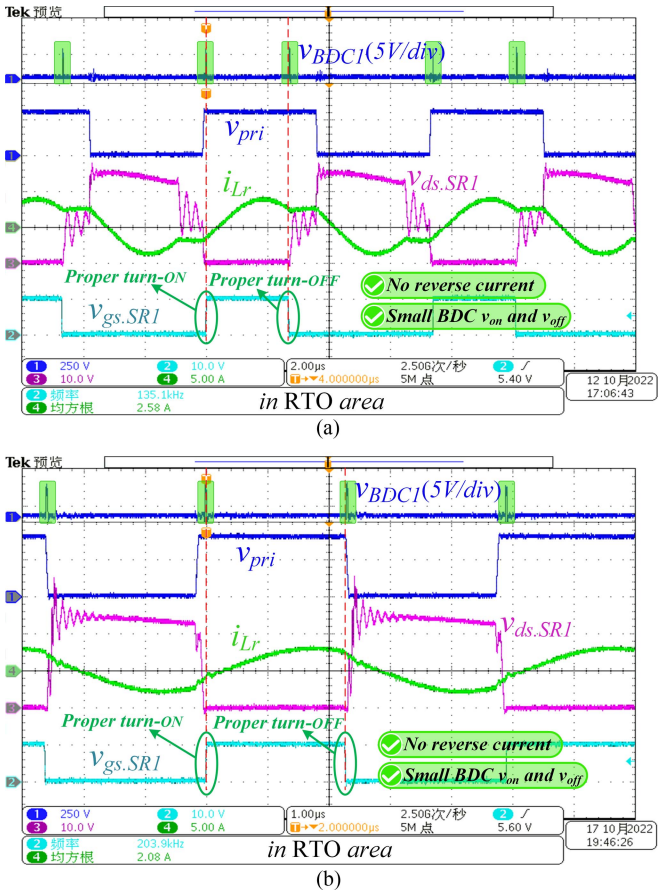


Fig. 26. Steady-state results of the proposed SPF-SR strategy under heavy-load conditions. (a) In BRR at $V_{\text{in}} = 300$ V, $V_o = 12$ V, $M = 1.28$, and $p_o = 100\%$. (b) In ARR at $V_{\text{in}} = 400$ V, $V_o = 12$ V, $M = 0.96$, and $p_o = 100\%$.

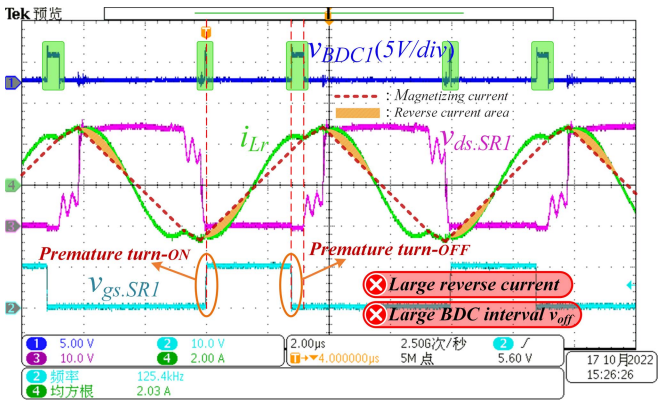


Fig. 27. Typical steady-state result of the commercial smart SR IC NCP4308 under light-load condition in BRR at $V_{\text{in}} = 250$ V, $V_o = 12$ V, $M = 1.536$, and $p_o = 10\%$.

Fig. 29 shows the dynamic result of the load step-down process (i.e., from 100% load to 20% load) in BRR at $V_{\text{in}} = 250$ V, $V_o = 12$ V, and $M = 1.536$. It can be seen that, in the steady state before the load steps down, *LLC* prototype operates in RTO area, where $p_o > p_{\text{bnd}}$, during the load step-down process, the optimal SR turn-ON area is gradually shifted from RTO area to CTO area to eliminate the large reverse current, the enlarged view of a typical point in the load step-down process shows

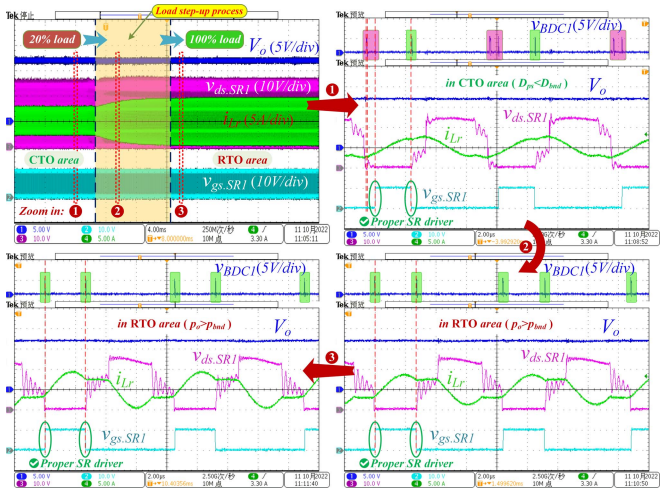


Fig. 28. Dynamic result of the load step-up process of the proposed SPF-SR strategy in BRR at $V_{\text{in}} = 250$ V, $V_o = 12$ V, and $M = 1.536$, where the load is stepped up from 20% to 100% and the optimal area is shifted from CTO to RTO area.

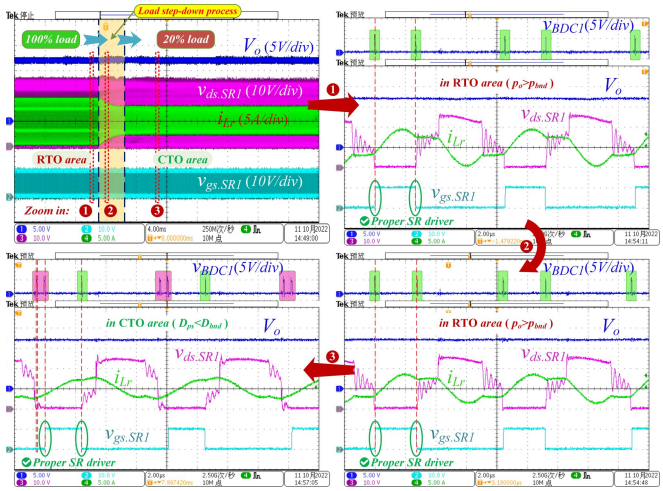


Fig. 29. Dynamic result of load step-down process of the proposed SPF-SR strategy in BRR at $V_{\text{in}} = 250$ V, $V_o = 12$ V, and $M = 1.536$, where the load is stepped down from 100% to 20% and the optimal area is shifted from RTO to CTO area.

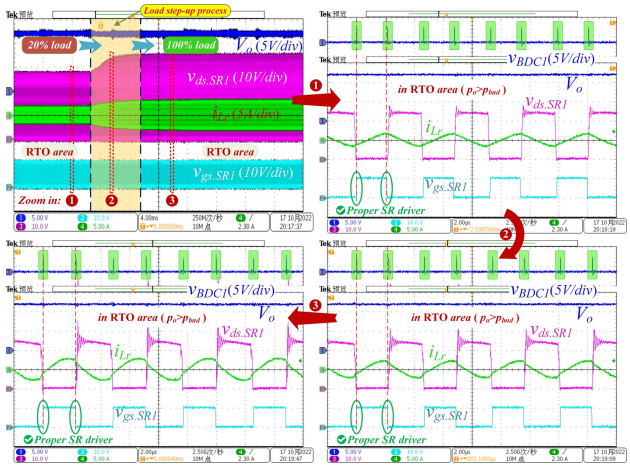


Fig. 30. Dynamic result of the load step-up process of the proposed SPF-SR strategy in ARR at $V_{\text{in}} = 400$ V, $V_o = 12$ V, and $M = 0.96$, where the load is stepped up from 20% to 100% and the optimal area is maintained in RTO area.

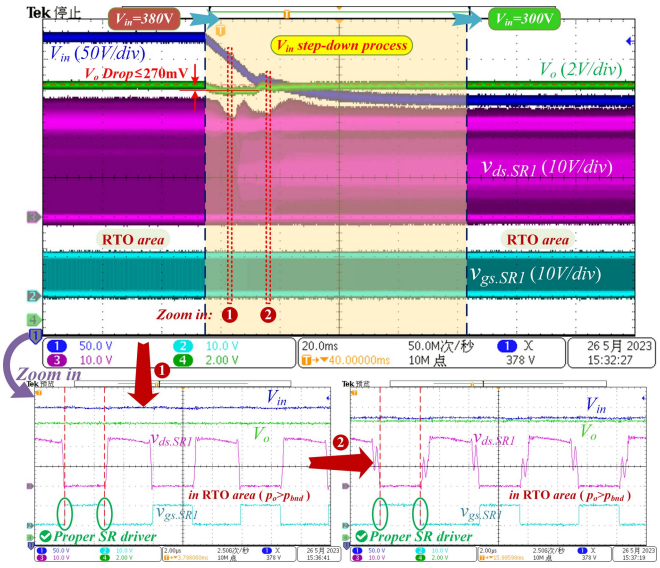


Fig. 31. Dynamic result of the V_{in} step-down process of the proposed SPF-SR strategy in ARR at $V_o = 12$ V and $R_{\text{load}} = 0.48\ \Omega$, where V_{in} is stepped down from 380 to 300 V and the optimal area is maintained in RTO area.

the proper SR driver in RTO area where $p_o > p_{\text{bnd}}$, and in the steady state after load steps down, the *LLC* operates stably in CTO where $D_{ps} < D_{\text{bnd}}$.

Fig. 30 shows the dynamic result of the load step-up process (i.e., from 20% load to 100% load) in ARR at $V_{\text{in}} = 400$ V, $V_o = 12$ V, and $M = 0.96$. It can be seen that the *LLC* prototype always operates in RTO area whether before, during, or after the load step-up process since $p_o > p_{\text{bnd}}$ is always satisfied. Fig. 31 shows the dynamic result of V_{in} step-down process (i.e., from 380 to 300 V) at $V_o = 12$ V and $R_{\text{load}} = 0.48\ \Omega$. It can be seen that the SPF-SR can always produce the proper SR drivers during the V_{in} step-down process.

In consequence, the experimental results in Figs. 23–31 fully indicate that the proposed SPF-SR strategy can produce proper SR drivers over the whole operating range whether in the steady state or during the dynamic process; therefore, the reliability, accuracy, and dynamic performance of SPF-SR are verified.

Finally, efficiency comparisons between the proposed SPF-SR, the conventional ADVS-SR, and the SR IC NCP4308 are illustrated, as shown in Fig. 32, where Fig. 32(a) shows the 3-D curve of power efficiency versus V_{in} and power load, and Fig. 30(b) and (c) shows the curves of power efficiency versus power load at $V_{\text{in}} = 250$ V and $V_o = 12$ V, and at $V_{\text{in}} = 400$ V and $V_o = 12$ V, respectively. It can be seen that the SPF-SR strategy can always maintain maximum power efficiency over the whole operating range. Compared with the conventional ADVS-SR, SPF-SR increases the power efficiency under light-load condition up to 5.52% due to the elimination of both large reverse current and large BDC interval in P_s stage, and compared with the commercial SR IC NCP4308, SPF-SR increases power efficiency over the whole operating range due to the elimination of both the large reverse current and the large BDC interval v_{off}, and the power efficiency improvement is up to 6.99%.

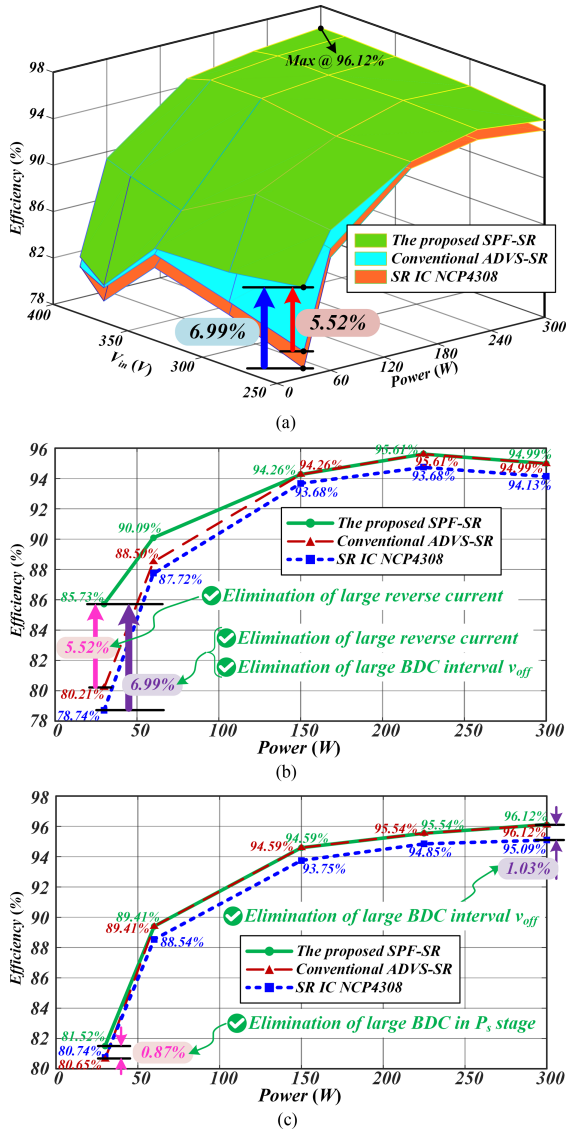


Fig. 32. Power efficiency comparisons between the proposed SPF-SR, the conventional ADVS-SR, and SR IC NCP4308. (a) Three-dimensional surface of efficiency versus V_{in} and power load. (b) Efficiency curves versus power at $V_{\text{in}} = 250$ V and $V_o = 12$ V. (c) Efficiency curves versus power at $V_{\text{in}} = 400$ V and $V_o = 12$ V.

VI. Conclusion

This article proposes a novel SPF-SR control strategy for *LLC* converters on the basis of ADVS-SR technology. First, the turn-ON issue of DVS-SRs is analyzed in detail based on the time-domain analysis of the capacitive spike current. And then based on the comparison of different SR turn-ON countermeasures, the SPF-SR strategy, which consists of the dual identification of optimal SR turn-ON area and the determination of turn-ON time, is proposed. Finally, the implementation of the proposed SPF-SR strategy is introduced with four key aspects.

Compared with the conventional ADVS-SR methods, the proposed SPF-SR designs a novel SR turn-ON time calculation model and optimizes the SR turn-ON, especially under light-load condition. SPF-SR strategy can eliminate not only the large

reverse current but also the large BDC interval; therefore, light-load efficiency is dramatically increased. The SPF-SR strategy can be digitally implemented with a cost-effective digital microcontroller and a few logic circuits. The experimental results verify that the SPF-SR strategy maintains excellent performance whether in the steady state or the dynamic process. Compared with the conventional ADVS-SR and commercial SR IC, SPF-SR strategy improves efficiency up to 5.52% and 6.99%, respectively. As a result, the proposed SPF-SR strategy provides an effective optimization solution to the adaptive SR control for *LLC* resonant converters.

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