An Efficient Interleaved Bidirectional DC–DC Converter With Shared Soft-Switching Auxiliary Circuit

Jianghu Wan, Fang Liu, *Member, IEEE*, Yong Li, *Senior Member, IEEE*, and Kang-Zhi Liu, *Senior Member, IEEE*

***Abstract*—A soft-switching interleaved bidirectional dc–dc converter, which is the combination of the conventional one and the introduced auxiliary circuit, is proposed in this article. The auxiliary branch composed of a capacitor, an inductor and two switches connected in series, is attached to the switching nodes of the two phases and serves them in a shared manner. Due to voltage continuity of the auxiliary capacitor, the zero-voltage switching (ZVS) condition is realized nearly for primary switches at turn-OFF. With the designed driving sequences, the current gradually flows through auxiliary inductor ahead of primary switches turn-ON, which is key to realizing ZVS condition for the switches. Moreover, the limited current slope guarantees the zero-current switching condition for auxiliary switches. Operating principle in buck mode is elaborated and design guideline is presented. Considering the parasitic resonance between the auxiliary inductor and the output capacitors of auxiliary switches, a clamping structure is given. A 1.2-kW prototype of the proposed converter is built and tested. The experimental results show the high performance.**

***Index Terms*—Interleaved bidirectional dc–dc converter, soft switching, zero-current switching (ZCS), zero-voltage switching (ZVS).**

I. Introduction

AS THE systems with energy storage elements, such as uninterrupted power supplies [1], hybrid/electric vehicles [2], renewable power generation [3], supercapacitor or battery balance systems [4], and dc microgrids [5], rapidly grows, the bidirectional dc–dc converters are extensively employed and researched to manage power flow and match voltage. To reduce the input and output current ripple and improve the power handling capability, the converter formed by two phases of conventional counterparts connected in parallel and operated with interleaved principle is established. Thanks to current sharing, many advantages, such as reliability improved [6], thermal well distributed [7], ohmic conduction losses reduced subsequently efficiency improved, are also achieved. Besides, the diode freewheeling is feasible to be replaced by synchronous rectifying, which enhances efficiency further.

In spite of those fine features, the converter operates under hard switching condition, which causes severe electromagnetic noise and great switching losses and reverse recovery losses. These problems get more serious with switching frequency increasing needed by high power density [8]. To overcome the identified defects, many soft-switching techniques featuring zero-voltage switching (ZVS) and zero-current switching (ZCS) were proposed and widely introduced into the regular interleaved bidirectional dc–dc converter. The triangular current mode or critical conduction mode for single converter also applies to the interleaved one [9], [10], [11]. Although ZVS condition is achieved without any change of topology, current ripple is inevitably high and accurate current control is necessary [9]. Complicated schemes, such as pulse frequency modulation [10], [11], and variable inductor with special core [12], must be adopted to extend soft switching range.

Moreover, soft switching can be obtained by replacing the two independent filter inductors with a coupled inductor [13], [14], [15]. Any additional device is not necessary and simplicity of the topology is maintained. The duty cycle must be limited otherwise high circulating current would be caused [14]. Since the mutual inductor acts as the effective filter, the output current is actually transferred from one phase to another under interleaved operation but does not flow through both phases evenly, which induces more conduction loss. To suppress the parasitic resonance caused by the reverse recovery of diode, extra auxiliary circuit is introduced [16], [17].

To overcome the abovementioned shortcomings, interleaved converter with soft-switching auxiliary circuit assisted can realize ZVS or ZCS under continuous conduction mode (CCM) over a wide load range [18], [19], [20], [21], [22], [23], [24]. It

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is easy to apply the circuit proposed for the single converter to the interleaved converter, but too many auxiliary elements are involved [18], [19]. Thus, soft-switching methods with simple and shared auxiliary branch are more attractive. In [20], [21], and [22], ZVS conditions are realized only for boost mode and the duty cycle should be above 0.5 to avoid duty cycle loss. In [23] and [24], auxiliary inductor is attached directly to the two switching nodes of the interleaved boost converter. This concept is applicable to the bidirectional one [25]. Pahlevaninezhad et al. [26] replaced this inductor with a *LC* resonant network. Since the magnetizing time of the auxiliary inductor is not actively controllable, it is hard to make a good trade-OFF between soft switching range and current stress. As a result, the weighted efficiency improvement is not evident.

In [27] and [28], the center-tapped inductor is designed to replace the aforementioned inductor. The other auxiliary circuit is connected with the center terminal. By replacing the diode in auxiliary circuit with power switch, bidirectional operation can be obtained. High current flowing through auxiliary branch is not solved because the duration of voltage placed on this inductor depends on main circuit, which will degrade efficiency at light load. To make matters worse, the auxiliary switch suffers from hard switching during both turn-ON and turn-OFF transient [28]. In [29], the bidirectional switch formed by two power switches connected in series in back-to-back form is employed to excite auxiliary inductor. However, the switches are not shared, which increases the complexity of driver and control. In [30], the auxiliary circuit is based on the active clamped concept and connected in series with the main power flow. Soft switching realization is at the expense of excessive voltage and current stresses. High conduction losses are caused and auxiliary inductor in large size is needed.

To address the problems abovementioned, this article proposes a soft switching interleaved bidirectional dc–dc converter with active auxiliary circuit assisted. The auxiliary branch is shared by the two phases of the primary circuit and connected in parallel with main power flow, which makes the conduction loss low and topology simple. Driven by designed sequences, ZVS condition for main switches and ZCS operation for auxiliary switches are realized. Considering the output capacitors of the auxiliary switches resonate with the auxiliary inductor, a clamping branch of two diodes is given to avoid any extra voltage across the switches and alleviate oscillation. A 1.2-kW prototype is built and tested. The efficiency curves show the high performance. Soft switching operation is realized over a wide power in both power flow direction.

II. Analysis of the Proposed Converter

The topology of the proposed ZVS interleaved bidirectional dc–dc converter is depicted Fig. 1. It consists of two identical traditional bidirectional dc–dc converters connected in parallel and the ZVS auxiliary branch, which is highlighted in gray shadow. Therefore, the inductances of the two main inductors L_1 and L_2 satisfy $L_1 = L_2 = L$. The parasitic output capacitors of primary power switches are equivalently parallel with C_a. So, quantity C_a is enlarged slightly by output capacitance. It is

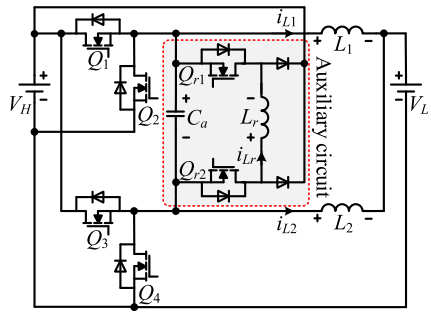

Fig. 1. Proposed soft-switching interleaved DC–DC converter.

acceptable to represents the summation of C_a and the output capacitance with C_a. The output capacitors of the auxiliary switches resonate with auxiliary inductor for a short while, which hardly has impact on the soft switching condition. They are ignored in the fundamental operation.

The switches of primary circuit are switched in the regular manner regardless of auxiliary circuit switching state. That is, Q_1 and Q_2 are driven with the complementary pulses, so are the switches Q_3 and Q_4. The phase between the driver signals of Q_1 and Q_3 is shifted 180° to achieve interleaved operation. In buck mode, Q_1 and Q_3 are main switches, Q_2 and Q_4 are synchronous rectification (SR) switches. While in boost mode the roles of these switches exchange. To share the same controller in both modes, the proportion of Q_1 and Q_3 ON time versus switching period is defined as duty cycle (D).

According to power flow direction, the operation is divided into buck and boost modes. In buck mode, power flows from high-side voltage (V_H) source to low-side voltage (V_L) source, In boost mode power flows in the opposite direction. Excited by designed pulses, L_r current gradually approaches main inductor current before main switch turn-ON, which provides the ZVS condition for the switch and eliminates the reverse recovery problem of SR switch body diode.

To simplify the analysis, the ON-state resistance of the power switch and the forward voltage drop across the switch body diode are ignored since they are quite low. According to the current loop, one switching cycle is further subdivided into 12 time intervals. Owing to the symmetry of the interleaved topology and the similarity of the operation in buck and boost mode, only 6 intervals in buck mode are analyzed in detailed. Since the operating process under $D \leq 0.5$ is distinct from that under $D > 0.5$, the operating principles under both conditions are, respectively, analyzed in the following text.

A. Condition I: $D > 0.5$

The driver signals and the related theoretical waveforms under $D > 0.5$ are presented in Fig. 2. Although half a switching cycle is divided into 6 intervals, there are only four different circuit states, as illustrated in Fig. 3. The operation principle is analyzed in detailed as follows.

Interval 1[t_0~t_1, Fig. 2(a)]: This interval begins at t_0, when the main switch Q_1 is turned OFF. Thereafter, C_a resonates with L_r and L_1 connecting in parallel, as illustrated in Fig. 3(a).

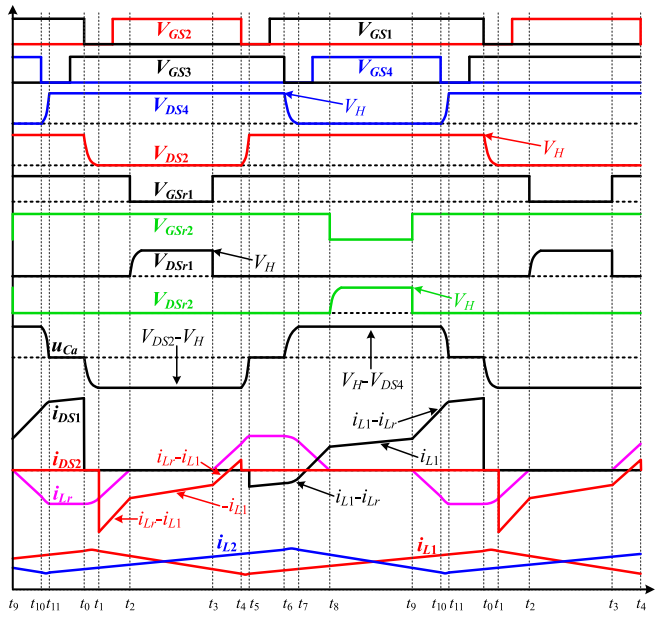

Fig. 2. Theoretical waveform of the proposed converter under $D > 0.5$.

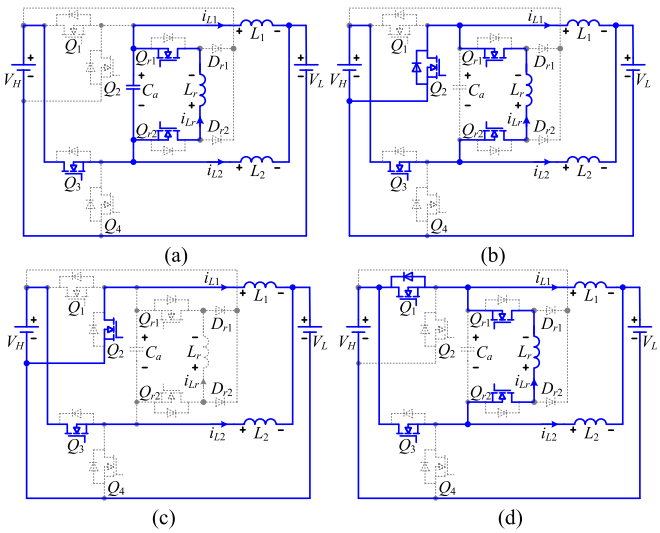

Fig. 3. Circuit states for each operation interval in buck mode under $D > 0.5$. (a) Interval 1, Interval 5. (b) Interval 2, Interval 4. (c) Interval 3. (d) Interval 6.

Applying the Kirchhoff's Current Law, the difference current i_{Lr}-i_{L1} flows through C_a in the direction opposite to its reference direction, causing the voltage across C_a starts to get more negative slowly from zero. This way, C_a voltage changes slightly during the short turn-OFF transient of Q_1. So, the near ZVS turn-OFF is realized for Q_1. As Q_3 maintains ON during this interval, the voltage imposed on L_2 is (V_H-V_L), which causes i_{L2} to increase linearly

$$u_{Ca}(t) = [i_{Lr}(t_0) - i_{L1}(t_0)]\sin\omega_1(t-t_0)/(\omega_1 C_a) + [\cos\omega_1(t-t_0) - 1](V_H - V_L)L_r/(L_r + L_1) \quad (1)$$

$$i_{Lr}(t) = \frac{V_H - V_L}{L_r + L_1}(t-t_0) - \frac{V_H - V_L}{\omega_1(L_r + L_1)}\sin\omega_1(t-t_0) + \frac{i_{Lr}(t_0) - i_{L1}(t_0)}{\omega_1^2 C_a L_r}[\cos\omega_1(t-t_0) - 1] + i_{Lr}(t_0) \quad (2)$$

$$i_{L1}(t) = \frac{V_H - V_L}{L_r + L_1}(t-t_0) + \frac{L_r(V_H - V_L)}{\omega_1 L_1(L_r + L_1)}\sin\omega_1(t-t_0) - \frac{i_{Lr}(t_0) - i_{L1}(t_0)}{\omega_1^2 C_a L_1}[\cos\omega_1(t-t_0) - 1] + i_{L1}(t_0) \quad (3)$$

$$i_{L2}(t) = i_{L2}(t_0) + (V_H - V_L)(t-t_0)/L_2 \quad (4)$$

$$\omega_1 = 1\Big/\sqrt{L_{p1}C_a},\ L_{p1} = L_r L_1/(L_r + L_1). \quad (5)$$

Interval 2[t_1~t_2, Fig. 2(b)]: At t_1, C_a voltage grows to be slightly more negative than -V_H, which causes Q_2 body diode to be forward biased and naturally turn ON to conduct the difference current i_{Lr}-i_{L1}. Thus, Q_2 can be turned ON under the ZVS condition throughout this interval. The voltages imposed on L_1 and L_r are, respectively, -V_L and V_H. As a result, i_{L1} drops linearly while i_{Lr} ramps up towards zero. Equivalent circuit for this operating state is shown in Fig. 3(b)

$$i_{L1}(t) = i_{L1}(t_1) - V_L(t-t_1)/L_1 \quad (6)$$

$$i_{Lr}(t) = i_{Lr}(t_1) + V_H(t-t_1)/L_r. \quad (7)$$

Interval 3[t_2~t_3, Fig. 2(c)]: This interval starts exactly when the current flowing through L_r reaches zero. To prevent i_{Lr} from continuing ramping up from zero, Q_{r1} must be turned OFF at or ahead of this instant. Under this condition, ZCS turn-OFF is obtained for Q_{r1}. Subsequently, i_{Lr} maintains zero and the auxiliary circuit does not participate in the primary topology operating throughout this interval. The converter is equivalent to the traditional interleaved counterpart, as shown in Fig. 3(c).

Interval 4[t_3~t_4, Fig. 2(b)]: When the auxiliary switch Q_{r1} is turned ON at t_3, this interval begins. Immediately, i_{Lr} increases from zero with the limited slope V_H/L_r. For this reason, the current through Q_{r1} is just slightly above zero during the short turn-ON transient, which guarantees the near ZCS condition for Q_{r1} turn-ON. Since the states of the primary circuit switches are not changed, the rate of change in i_{L1} and i_{L2} maintain the same values as in the last interval. The circuit state for this stage is the same with that in *interval 2*, i.e., Fig. 3(b)

$$i_{Lr}(t) = V_H(t-t_3)/L_r. \quad (8)$$

Interval 5[t_4~t_5, Fig. 2(a)]: The main switch Q_2 is turned OFF at t_4, which is the beginning of this interval. C_a thereupon resonates with the two inductors L_1 and L_r connecting in parallel. The difference current i_{Lr}-i_{L1} flows through C_a in the same direction with its voltage reference direction, causing C_a voltage to increase slowly from -V_H towards zero. During the short turn-OFF transient, the voltage change is almost zero. Thereby, the near ZVS turn-OFF is achieved for Q_2 due to this clamping function of C_a, which is similar to what happened in *interval 1*.

The operating state is presented Fig. 3(a)

$$u_{Ca}(t) = [i_{Lr}(t_4) - i_{L1}(t_4)]\sin\omega_1(t-t_4)/(\omega_1 C_a) - V_H - (L_1V_H + L_rV_L)[\cos\omega_1(t-t_4)-1]/(L_r+L_1) \quad (9)$$

$$i_{Lr}(t) = i_{Lr}(t_4) + \frac{i_{Lr}(t_4)-i_{L1}(t_4)}{\omega_1^2 C_a L_r}[\cos\omega_1(t-t_4)-1] + \frac{L_1V_H+L_rV_L}{(L_r+L_1)\omega_1 L_r}\sin\omega_1(t-t_4) + \frac{V_H-V_L}{L_r+L_1}(t-t_4) \quad (10)$$

$$i_{L1}(t) = i_{L1}(t_4) - \frac{i_{Lr}(t_4)-i_{L1}(t_4)}{\omega_1^2 C_a L_1}[\cos\omega_1(t-t_4)-1] - \frac{L_1V_H+L_rV_L}{(L_r+L_1)\omega_1 L_1}\sin\omega_1(t-t_4) + \frac{V_H-V_L}{L_r+L_1}(t-t_4). \quad (11)$$

Interval 6[t_5∼t_6, Fig. 2(d)]: The interval starts as C_a voltage reaches the forward voltage drop of Q_1 body diode at t_5. Thus, the body diode naturally turns ON and the difference current i_{Lr}-i_{L1} flows through it, which means the ZVS condition for Q_1 turn-ON is realized. In this interval, the voltage imposed on L_r and L_1 are 0 and V_H-V_L, respectively. So, i_{Lr} remains constant and i_{L1} slopes up. The circuit state is shown in Fig. 3(d)

$$i_{L1}(t) = i_{L1}(t_5) + (V_H - V_L)(t-t_5)/L_1. \quad (12)$$

At t_6, *interval 7* starts with Q_3 turn-OFF under near ZVS condition. There are also 6 intervals in the rest half cycle during t_6∼t_0. Based on the topology symmetry, the operation in these intervals is similar to the aforementioned process. It will not be analyzed in detailed to avoid duplication description.

B. Condition II: $D \leq 0.5$

The driver sequences under $D \leq 0.5$ and the corresponding theoretical waveforms for voltage and current are shown in Fig. 4. During the 6 intervals for a half switching cycle, there are still four distinct circuit states, as presented in Fig. 5. The detailed steady-state operating principle is analyzed as follows.

Interval 1[t_0∼t_1, Fig. 2(a)]: At t_0, Q_2 body diode is forward biased and turns ON, which provides freewheeling path for the difference current i_{L1}-i_{Lr}. Thus, Q_2 obtains the ZVS condition to be turned ON as the conventional converter does, as shown in Fig. 4(a). Since the voltage across L_r constantly equals to zero, i_{Lr} does not change and L_r maintains its stored energy. L_1 and L_2 are demagnetized and releasing energy to load

$$i_{L1}(t) = i_{L1}(t_0) - (t-t_0)V_L/L_1 \quad (13)$$

$$i_{L2}(t) = i_{L2}(t_0) - (t-t_0)V_L/L_2 \quad (14)$$

$$i_{Lr}(t) = i_{Lr}(t_0). \quad (15)$$

Interval 2[t_1∼t_2, Fig. 2(b)]: This interval starts at t_1, when Q_4 is turned OFF. i_{L2} plus i_{Lr} immediately flows through C_a and a resonance between C_a, L_2, and L_r begins. The circuit state for this process is illustrated in Fig. 4(b). Since i_{Lr} is practically negative and -i_{Lr} is higher than i_{L2}, C_a is reversely charged by the surplus current -i_{Lr}-i_{L2}, causing C_a voltage to slowly grow

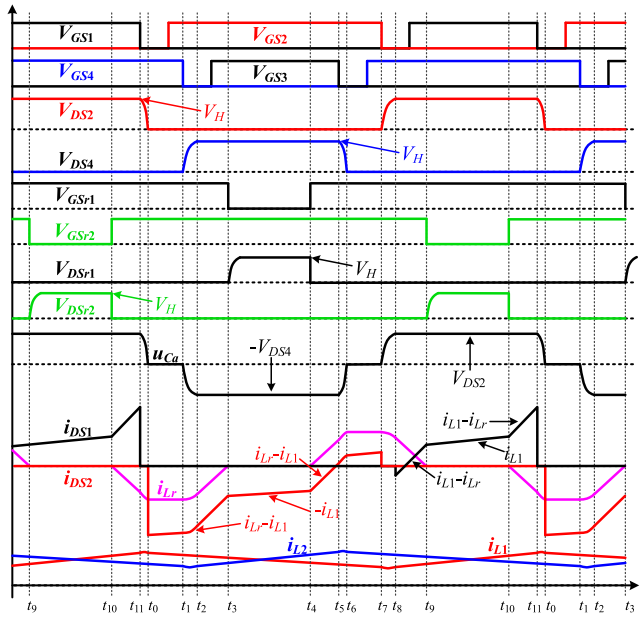

Fig. 4. Theoretical waveform of the proposed converter under $D \leq 0.5$.

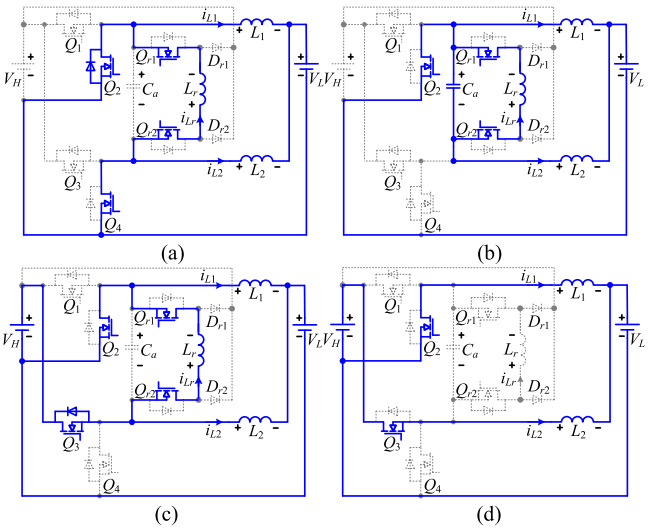

Fig. 5. Circuit states for each operation interval in buck mode under $D \leq 0.5$. (a) Interval 1. (b) Interval 2, Interval 6. (c) Interval 3, Interval 5. (d) Interval 4.

more negative from zero. It means the slew rate of Q_4 drain-source voltage is significantly reduced. Consequently, the near ZVS condition is guaranteed during the short turn-OFF transient

$$u_{Ca}(t) = [\cos\omega_2(t-t_1)-1]V_L L_r/(L_r+L_2) + \sin\omega_2(t-t_1)[i_{Lr}(t_1)+i_{L2}(t_1)]/(\omega_2 C_a) \quad (16)$$

$$i_{L2}(t) = \frac{-V_L L_r}{\omega_2 L_2(L_r+L_2)}\sin\omega_2(t-t_1) - \frac{V_L(t-t_1)}{L_r+L_2} + \frac{i_{Lr}(t_1)+i_{L2}(t_1)}{\omega_2^2 L_2 C_a}[\cos\omega_2(t-t_1)-1] + i_{L2}(t_1) \quad (17)$$

$$i_{Lr}(t) = \frac{-V_L}{\omega_2(L_r+L_2)}\sin\omega_2(t-t_1) + \frac{V_L(t-t_1)}{L_r+L_2} + \frac{i_{Lr}(t_1)+i_{L2}(t_1)}{\omega_2^2 L_r C_a}[\cos\omega_2(t-t_1)-1] + i_{Lr}(t_1) \tag{18}$$

$$\omega_2 = 1\Big/\sqrt{L_{p2}C_a}, L_{p2} = L_rL_2/(L_r+L_2). \tag{19}$$

Interval 3[t_2∼t_3, Fig. 2(c)]: When C_a voltage grows slightly more negative than -V_H and Q_3 body diode is forward biased, this interval begins. Both i_{L2} and i_{Lr} flow through Q_3 body diode. Shortly afterwards Q_3 is turned ON under ZVS condition. The equivalent circuit for this operating state is shown in Fig. 4(c). Throughout this interval, L_2 is energized by positive voltage V_H-V_L, causing i_{L2} to increase linearly. i_{Lr} approaches zero gradually with constant positive slope

$$i_{L2}(t) = i_{L2}(t_2) + (t-t_2)(V_H - V_L)/L_2 \tag{20}$$

$$i_{Lr}(t) = i_{Lr}(t_2) + V_H(t-t_2)/L_r. \tag{21}$$

Interval 4[t_3∼t_4, Fig. 2(d)]: This interval starts at t_3, when i_{Lr} falls to zero and the auxiliary switch Q_{r1} is turned OFF. So, the ZCS condition is obtained Q_{r1}. Practically, since it is difficult to turn OFF Q_{r1} exactly when i_{Lr} reaches zero, Q_{r1} is turned OFF ahead of t_3 to avoid the annoyance of i_{Lr} decreasing to negative. Owing to the current continuity of L_r, the decline gradient of the current flowing through Q_{r1} body diode is quite low. There is hardly reverse recovery current caused by this diode even it conducts for a while. For this reason, the turn-OFF loss of Q_{r1} is roughly zero. As i_{Lr} drops to zero, the operating state is identical to the conventional counterpart, as shown in Fig. 4(d).

Interval 5[t_4∼t_5, Fig. 2(c)]: This interval starts by turning on the auxiliary switch Q_{r1} at t_4. Subsequently, both i_{L2} and i_{Lr} flow through Q_3. The operating state for this stage is the same with that in *interval 3*, as shown in Fig. 4(c). Similarly, Q_{r1} obtains the near ZCS condition because of connecting with L_r. Thus, i_{Lr} slopes up from zero with gradient V_H/L_r

$$i_{Lr}(t) = V_H(t-t_4)/L_r. \tag{22}$$

Interval 6[t_5∼t_6, Fig. 2(b)]: This interval begins at t_5 when Q_3 gate drive signal goes low. Instantly, the current through Q_3 falls towards zero steeply while the surplus current flows to C_a during the turn-OFF transient. As C_a is large, the voltage across it is nearly unchanged for the short duration. In other words, the ZVS condition is achieved for Q_3. After the transient, i_{L2} plus i_{Lr} flows through C_a, causing C_a to resonate with L_2 and L_r. So, C_a voltage keeps increasing towards zero in a resonance manner in the rest of this interval. The operating state is the same with that in *interval 2*, as shown in Fig. 4(b)

$$u_{Ca}(t) = [V_LL_r/(L_r+L_2) - V_H][\cos\omega_2(t-t_5)-1] + [i_{Lr}(t_5)+i_{L2}(t_5)]\sin\omega_2(t-t_5)/(\omega_2C_a) - V_H \tag{23}$$

$$i_{L2}(t) = \frac{1}{\omega_2L_2}\left(V_H - \frac{V_LL_r}{L_r+L_2}\right)\sin\omega_2(t-t_5) + i_{L2}(t_5) - \frac{V_L(t-t_5)}{L_r+L_2} + \frac{i_{Lr}(t_5)+i_{L2}(t_5)}{\omega_2^2L_2C_a}[\cos\omega_2(t-t_5)-1] \tag{24}$$

$$i_{Lr}(t) = \frac{1}{\omega_2L_r}\left(V_H - \frac{V_LL_r}{L_r+L_2}\right)\sin\omega_2(t-t_5) + i_{Lr}(t_5) + \frac{V_L(t-t_5)}{L_r+L_2} + \frac{i_{Lr}(t_5)+i_{L2}(t_5)}{\omega_2^2L_rC_a}[\cos\omega_2(t-t_5)-1]. \tag{25}$$

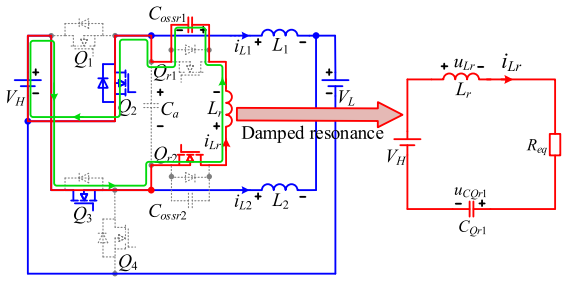

Fig. 6. Resonance process caused by parasitic parallel capacitors.

Next, there are also 6 time intervals in the latter half cycle starting at t_6 and ending at t_0. Similarly, due to the symmetry between the upper and the under bidirectional converter of the interleaved topology, the operation in the latter half of the switching cycle is symmetric with that in the former. It will not be described in the following to avoid repetition. As for boost mode, both the operating principle analysis and the theoretical waveforms are similar to these in buck mode except that the current flows in the opposite direction.

III. Parasitic Resonance Analysis and Depression

As stated previously, the output capacitors of the auxiliary switches are not taken into consideration because it hardly affects the soft-switching condition for main switches. But they cause additional voltage stress to the auxiliary switches, which increases with the capacitance. As shown in datasheet, the output capacitance is nonlinear and extremely high at low drain-source voltage. Consequently, the resonating duration is long and the amplitude is high. It is necessary to take action to suppress the parasitic resonance.

The output capacitor seriously resonates with the auxiliary inductor for a period of time in the early time of *interval 3* under $D > 0.5$ and *interval 4* under $D \le 0.5$. Taking the operation under $D > 0.5$ as an example, the resonating loop and equivalent circuit are shown in Fig. 6 with red line, where C_{ossr1} and C_{ossr2} are, respectively, the output capacitors of Q_{r1} and Q_{r2}. In the equivalent circuit, R_{eq} represents the stray series resistor. Since i_{Lr} is negative in *interval 2*, u_{Cossr1} is basically zero. Thus, at the beginning of *Interval 3*, both i_{Lr} and u_{Cossr1} are zero while u_{Lr} equals to V_H, causing i_{Lr} to rise up from zero. That means the auxiliary circuit is not in steady state and L_r resonates with C_{ossr1} subsequently. The resonating voltage obeys zero state

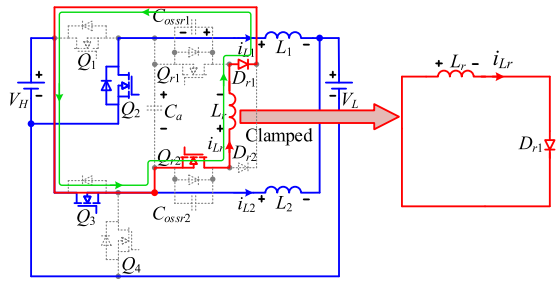

Fig. 7. Clamping protection theory.

response, which is expressed as

$$u_{Cossr1}(t)=V_H-V_He^{-\frac{R_{eq}}{2L_r}t}\left(\cos\omega_{pa}t+\frac{R_{eq}}{2\omega_{pa}L_r}\sin\omega_{pa}t\right) \tag{26}$$

where $\omega_{pa}=\sqrt{4L_r/C_{ossr1}-R_{eq}^2}/(2L_r)$.

Since L_r is almost thousand times greater than C_{ossr1} and R_{eq} is close to zero, the theoretical maximum voltage across auxiliary switch is basically $2V_H$, which excessively increases the stress. More seriously, the maximum is much higher than $2V_H$ since the output capacitance is inversely proportional to the square root of the drain-source voltage. The stray resistance R_{eq} is the only damping to force the resonance to decay. As a result, the resonance will last for a long time and the auxiliary switch will experience severe voltage overshoot.

To avoid extra voltage stress across auxiliary switches, two diodes D_{r1} and D_{r2} are added, as shown in Fig. 7. Taking D_{r1} as an example, it will be forward biased and conducting once u_{Cossr1} reaches V_H. Then, the resonating current flows through D_{r1} and Q_{r1} voltage is clamped. As the energy in L_r is wasted by D_{r1} completely, the auxiliary circuit reaches steady state.

IV. Parameter Design Guideline

A. Inductance Design

Based on $L_1=L_2=L$, it can be derived that $L_{p1}=L_{p2}=L_p$ and consequently $\omega_1=\omega_2=\omega$. To facilitate the following analysis, it is assumed that the total power of the interleaved converter is P and the average power is balanced between the two phases. Thus, the filter inductor design for this converter accords with that for the single converter. The inductor current ripple is

$$\Delta I_L=(V_H-V_L)DT/2L \tag{27}$$

where T is the switching period corresponding to frequency f. Obviously, ΔI_L gets maximum $\Delta I_{L,\max}$ as D is equal to 0.5

$$\Delta I_{L,\max}=V_HT/8L. \tag{28}$$

Generally, $\Delta I_{L,\max}$ is expected to be less than one fifth of $I_{ave,\max}$ to realize low current ripple ratio, where $I_{ave,\max}$ is the maximum of average inductor current I_{ave}. Thus, L satisfies

$$L>5V_HT/(8I_{ave,\max}). \tag{29}$$

As analyzed in Section II, the ZVS condition for primary switches is provided by exciting L_r with designed pulse. And the lower the inductance of L_r is, the shorter the conduction time of the auxiliary circuit will be, which contributes to less current increment and conduction loss in primary circuit. So, L_r is designed to be less one fifth of L, i.e., $L_r<L/5$.

B. ZCS Condition for Auxiliary Switches

Since auxiliary switches are connected in series with the auxiliary inductor L_r, the rate of change in current through the switches is restrained evidently. The current through auxiliary switches keeps close to zero during the short turn-ON transient. Thus, the near ZCS turn-ON is realized for auxiliary switches. At the turn-OFF instant, the current through auxiliary switches naturally reaches zero owing to L_r. The body diodes of auxiliary switches do not suffer from evident reverse recovery current. Thereby, the turn-OFF is also under near ZCS condition.

C. Near ZVS Turn-Off Condition for Main Switches

As presented in Section II, the two operating processes under $D>0.5$ and $D\le 0.5$ are similar to each other. The former is taken as an example to analyze the soft switching condition for main switches and current stress. The same results are suitable for operation under $D\le 0.5$.

The current flowing through all inductors can be regarded as unchanged during the turn-OFF transient since this duration is quite short. So, the following expressions are derived:

$$i_{Lr}(t_0)\approx i_{Lr}(t_1), \tag{30}$$

$$i_{L1}(t_0)\approx i_{L1}(t_1)=I_{ave}+(V_H-V_L)D/(2Lf) \tag{31}$$

$$i_{L1}(t_5)\approx i_{L1}(t_4)=I_{ave}-(V_H-V_L)D/(2Lf). \tag{32}$$

As the current flowing through the power switch declines approximately linearly to zero after turn-OFF [31], the voltage increment across C_a during Q_1 turn-OFF transient is

$$\Delta u_{Ca,f}\approx[i_{L1}(t_0)-i_{Lr}(t_0)]t_f/2C_a \tag{33}$$

where t_f is the fall time corresponding to the turn-OFF transient. To guarantee the near ZVS condition for Q_1 turn-OFF, the voltage change across C_a must be low enough (generally less than one fifth of V_H) to be ignored. So, the quantity C_a satisfies

$$C_a>5[i_{L1}(t_0)-i_{Lr}(t_0)]t_f/2V_H. \tag{34}$$

At t_4, Q_2 is turned OFF. Then, C_a is charged by the resonance between L_r, L_1, and C_a. Due to the freewheeling of Q_2 body diode, the minimum $i_{Lr}(t_4)$ is equal to $i_{L1}(t_4)$. It means $i_{Lr}(t_4)$ is not less than $i_{L1}(t_4)$. To achieve the lowest conduction loss, $i_{Lr}(t_4)$ must be designed as minimum, i.e.,

$$i_{Lr}(t_4)=i_{L1}(t_4). \tag{35}$$

Even though there may be reverse recovery current caused by Q_2 body diode, Q_2 can still obtain the near ZVS condition based on (9) because the reverse recovery current is quite low and (35) hold approximately. Based on (30)–(35), the near ZVS condition for Q_1 turn-OFF leads to

$$C_a>5I_{ave,\max}t_f/V_H. \tag{36}$$

The duration from Q_{r1} turn-ON to Q_2 turn-OFF is defined as $D_{aux}T$. It is given by

$$D_{aux}T = L_r i_{L1}(t_4)/V_H. \tag{37}$$

D. ZVS Turn-On Condition for Main Switches and Dead Zone

Considering that L_r is far smaller than L_1, the second term of (1) can be ignored. It obtains the following approximation:

$$u_{Ca}(t) \approx [i_{Lr}(t_0) - i_{L1}(t_0)]\sqrt{L_r/C_a}\sin\omega_1(t-t_0). \tag{38}$$

Apparently, u_{Ca} gets maximum as $\omega_1(t\text{-}t_0)$ is around $\pi/2$, so, the sufficient dead zone from Q_1 turn-OFF to Q_2 turn-ON is

$$t_{dz} \approx \pi/2\omega_1. \tag{39}$$

The magnitude of sine function is 1. By combining (30)–(32) and (38), the ZVS turn-ON condition for Q_2 leads to

$$I_{ave} > \frac{V_H}{2\sqrt{L_r/C_a}}. \tag{40}$$

By combining (9) with (35) and equating $u_{Ca}(t)$ to zero, it obtains the ZVS turn-ON condition for Q_1

$$\cos\omega_1(t-t_4) = 1 - \frac{1}{\frac{L_1}{L_r+L_1} + \frac{L_r}{L_r+L_1}\frac{V_L}{V_H}}. \tag{41}$$

Since L_1 is far greater than L_r and V_L is less than V_H, it derives

$$-L_r/L_1 < \cos\omega_1(t-t_4) < 0. \tag{42}$$

Obviously, $\cos\omega_1(t\text{-}t_4)$ is negative but extremely close to zero. Thus, $\omega_1(t\text{-}t_4)$ is roughly $\pi/2$. Solution for this dead zone yields the result consistent with (39). Equation (42) shows ZVS condition for Q_1 turn-ON can always be achieved in spite of the load condition and low-side voltage. Although the proportion of L_r to L_1 definitely affects the soft switching of Q_1, it is quite close to zero and has little impact on the soft switching condition. Likewise, the above analyses and results for ZVS turn-ON condition under $D > 0.5$ are applicable to these under $D \le 0.5$.

E. Current Stress

To minimize the conduction loss, the maximum magnitude of the current flowing through L_r is basically equal to the valley value of i_{L1} or i_{L2}. Assuming that the current stress of auxiliary switch is I_{CS_aux}, it is obtained according to (32) as

$$I_{CS\_aux} = I_{ave} - (V_H - V_L)D/(2Lf). \tag{43}$$

Since the current ripple is relatively low compared to the average inductor current, it can be neglected and I_{CS_aux} is close to I_{ave}. As shown in Fig. 2, the current flowing through main switches reaches maximum at t_1. Defining the current stress of main switch as I_{CS_m}, it is determined by $i_{L1}(t_1)$ plus $i_{Lr}(t_1)$ in magnitude, i.e.,

$$I_{CS\_m} = i_{L1}(t_1) - i_{Lr}(t_1) = 2I_{ave}. \tag{44}$$

V. Experimental Analysis

To demonstrate the validity and the aforementioned features of the proposed soft-switching interleaved bidirectional dc–dc converter, a prototype with 1.2-kW power rating operating at 50 kHz switching frequency is developed in the laboratory, as presented in Fig. 8. The detailed parameters of the elements and the operating condition are listed in Table I. Measured with mixed domain oscilloscope MDO3014 from Tektronix, the voltage and current waveforms of Q_1 and Q_2 in buck mode are presented in Figs. 9 –11. The waveforms in boost mode are shown in Figs. 12 –14. Additionally, the zoon-in versions during switching transient are also presented.

As shown in experimental waveforms, the ZVS turn-ON is realized strictly for all switches in both modes. The near ZVS turn-OFF is obtained well for Q_2 in buck mode and Q_1 in boost mode. But, the near ZVS condition at Q_1 turn-OFF is not met well in buck mode as the power increases, which is the same at Q_2

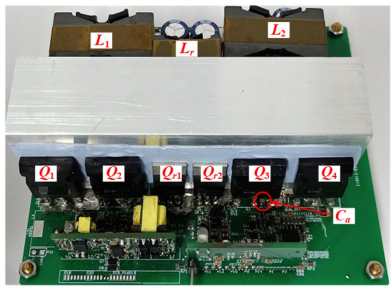

Fig. 8. Experimental prototype of the proposed converter.

TABLE I
Parameters of Prototype

Parameters	Value	Parameters	Value
Q_1–Q_4	IRFP90N20DPBF	C_a	22 nF
Q_{r1} and Q_{r2}	IPP110N20N3	L_1 and L_2	50 μH
D_{r1} and D_{r2}	VSSA310A	L_r	5 μH
V_L	12~48V	V_H	60 V
C_{oss} *of* Q_1	1070 pF	C_{oss} of Q_{r1}	401 pF

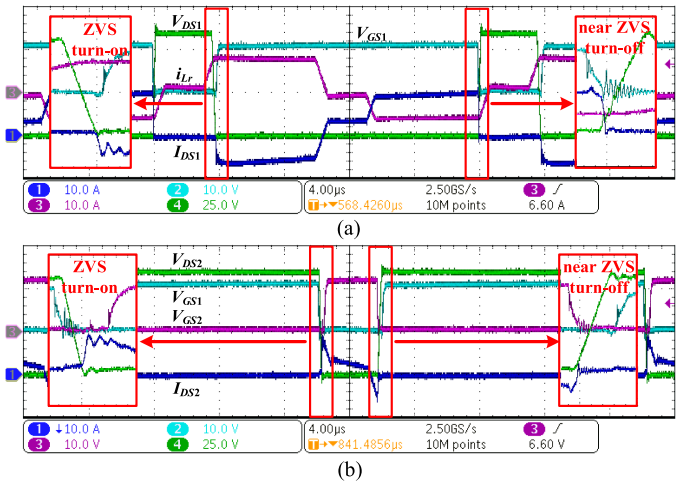

Fig. 9. Soft switching operation for Q_1 and Q_2 in buck mode at $V_L = 48$ V and 5 A average current. (a) Q_1. (b) Q_2.

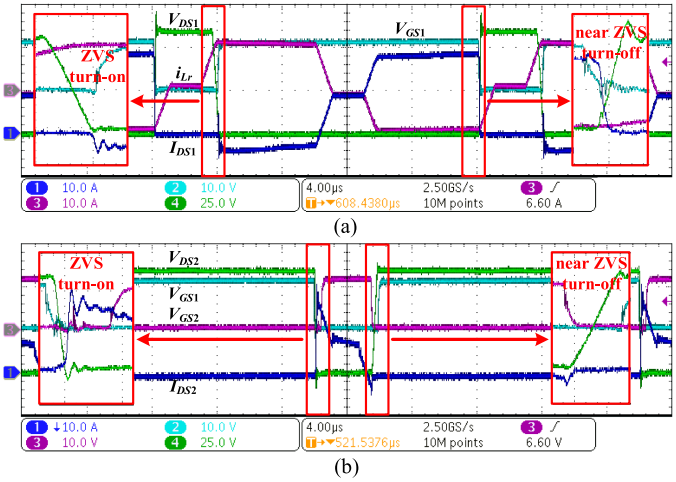

Fig. 10. Soft switching operation for Q_1 and Q_2 in buck mode at $V_L = 48$ V and 15 A average current. (a) Q_1. (b) Q_2.

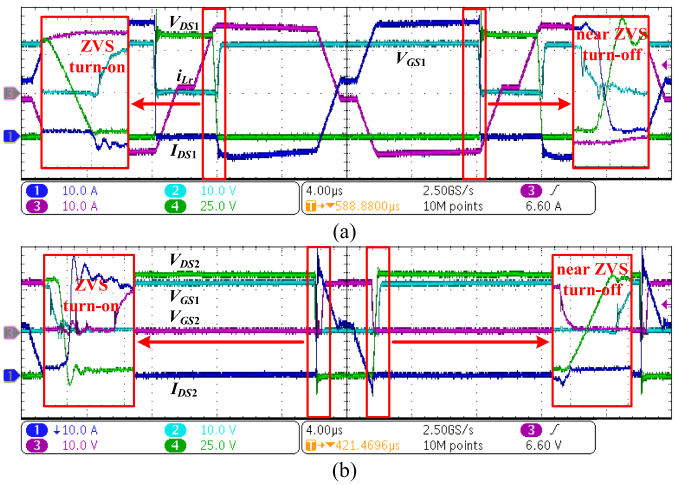

Fig. 11. Soft switching operation for Q_1 and Q_2 in buck mode at $V_L = 48$ V and 25 A average current. (a) Q_1. (b) Q_2.

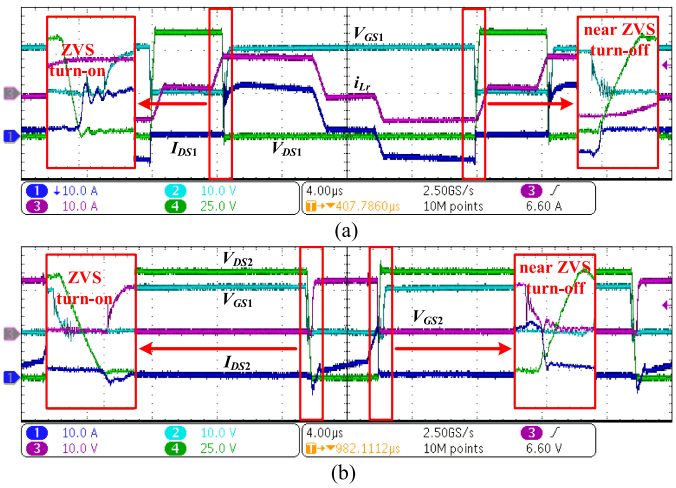

Fig. 12. Soft switching operation for Q_1 and Q_2 in boost mode at $V_L = 48$ V and 5 A average current. (a) Q_1. (b) Q_2.

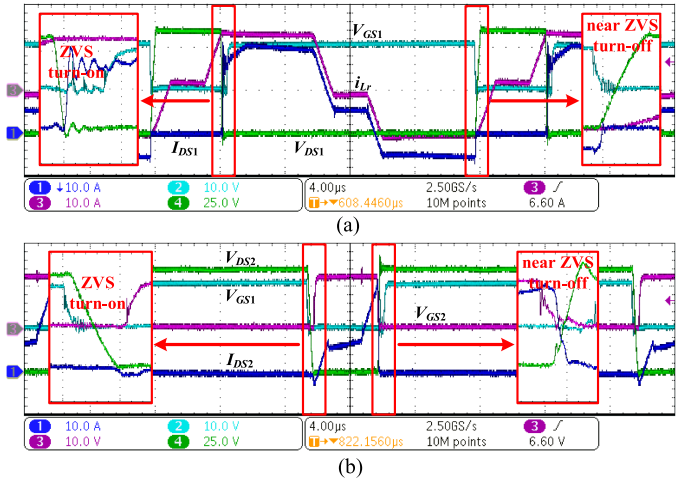

Fig. 13. Soft switching operation for Q_1 and Q_2 in boost mode at $V_L = 48$ V and 15 A average current. (a) Q_1. (b) Q_2.

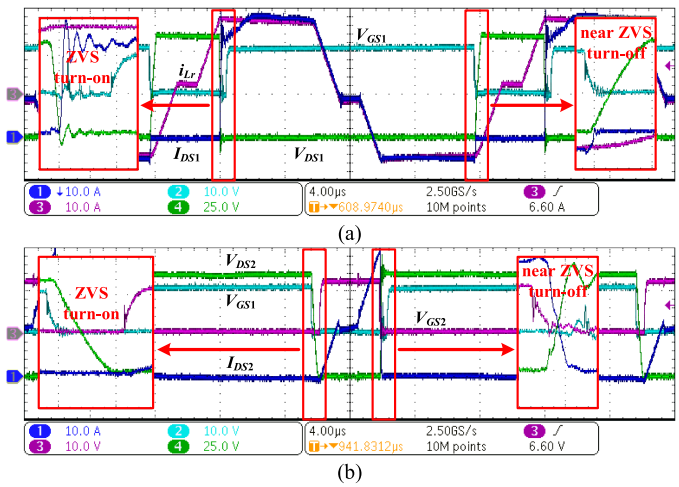

Fig. 14. Soft switching operation for Q_1 and Q_2 in boost mode at $V_L = 48$ V and 25 A average current. (a) Q_1. (b) Q_2.

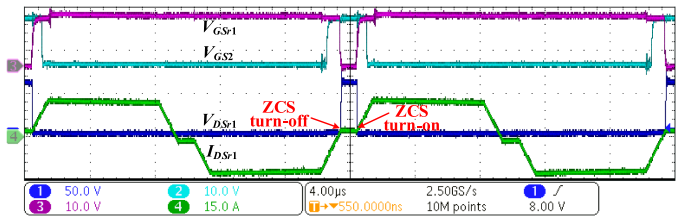

Fig. 15. Soft switching operation for Q_{r1} in buck mode.

turn-OFF in boost mode. It is because the fall time of the switch is not as short as assumed in abovementioned analysis, causing C_a voltage to change evidently. So, C_a with larger capacitance and switch with shorter fall time would facilitate better results.

Since the ZCS condition for Q_{r1} and Q_{r2} is independent of the power, the waveforms under $I_{ave} = 12.5$ A are taken to show the soft switching operation, as presented in Figs. 15 and 16. It is

TABLE II
COMPARISON OF THE PROPOSED CONVERTER WITH PREVIOUS METHODS

Features \ References		Ref [28]	Ref [29]	Ref [30]	Ref [32]	Ref [33]	Proposed converter
Auxiliary devices	Switches	2	4	1	2	2	2
	Diodes	0	0	0	0	4	2
	Inductors	1	1	1	2	2	1
	Coupled	Yes	No	No	Yes	Yes	No
	Capacitors	2	0	1	1	4	1
Protecting structure		Not needed	Not designed	Not designed	Not needed	Not designed	2 diodes
Total components of the topology		11	11	9	9	16	12
Voltage stress on auxiliary switch (diode)		V_H	$>V_H$	V_H+V_{CC}	V_H+V_{CC}	V_H+V_{CC}	V_H
Voltage stress on main switch		V_H	V_H	$>V_H$+V_{CC}	V_H+V_{CC}	V_H+V_{CC}	V_H
Current stress of main switch		$>2I_{ave}$	I_{ave}	$2I_{ave}$	I_{ave}	I_{ave}	$2I_{ave}$
Current stress of auxiliary switch		$>2I_{ave}$	I_{ave}	$2I_{ave}$	I_{ave}	I_{ave}	I_{ave}
Floating driving voltage		3	4	3	4	2	2
Soft switching condition for main switch	Turn-on	ZVS	ZVS	ZVS	ZVS	ZVS	ZVS
	Turn-off	Hard	Hard	Hard	Hard	Hard	Near ZVS
Soft switching condition for auxiliary switch	Turn-on	Near ZCS	Near ZCS	ZVS	Near ZCS	ZVS	Near ZCS
	Turn-off	Near ZCS	Near ZCS	Near ZVS	Hard	Hard	Near ZCS
Soft switching range		Wide	Wide	Wide	Wide	Narrow	Wide

TABLE III
LOSS COMPARISON OF THE PROPOSED CONVERTER WITH THE CONVENTIONAL COUNTERPART

Type of loss	Conventional converter			Proposed converter			
	Formula	Value (full load)	Value (40% load)	Formula		Value (full load)	Value (40% load)
				Main circuit	Auxiliary circuit		
Turn-on loss	$2V_H[i_{L1}(t_4)+I_{rr}]t_{rr}f+V_H i_{L1}(t_4)t_r f$	32.91 W	13.8 W	0	$C_{ossr}V_H^2 f$	0.07 W	0.07 W
Turn-OFF loss	$V_H i_{L1}(t_0)t_f f$	1.5 W	0.6 W	$(I_{ave}t_f)^2 f/(3C_a)$	0	0.2	0.08
Conduction loss	$2I_{ave}^2 R_{ON}$	7.24 W	1.2 W	$(12D-4+8D_{aux}/3)I_{ave}^2 R_{ON}$	$(4D-2+8D_{aux}/3)I_{ave}^2 R_{ON}$	38.8 W	5.5 W
Core loss	$2K_{fe0}f^{\alpha}\left(\frac{V_H(1-D)D}{N_L A_L f}\right)^{\beta}V_{e\_L}$	5.2 W	5.2 W	$2K_{fe0}f^{\alpha}\left(\frac{V_H(1-D)D}{N_L A_L f}\right)^{\beta}V_{e\_L}$	$K_{fe0}f^{\alpha}\left(\frac{2L_r I_{ave}}{N_{Lr}A_{Lr}}\right)^{\beta}V_{e\_Lr}$	7.2 W	5.6 W
Total loss	-	46.9 W	20.9 W	-	-	46.27 W	11.3 W

Note: t_r is the rise time of the power switch. t_{rr} is the reverse recovery time of the body diode, I_{rr} is the corresponding reverse recovery current. R_{ON} represents the effective ON-resistance of the switch. K_{fe0}, α and β are all constant parameters related to the ferrite material. N_L, A_L, and V_{e_L} are respectively the winding turns, sectional area and core volume of the main inductor. N_{Lr}, A_{Lr}, and V_{e_Lr} are, respectively, the winding turns, sectional area and core volume of the auxiliary inductor.

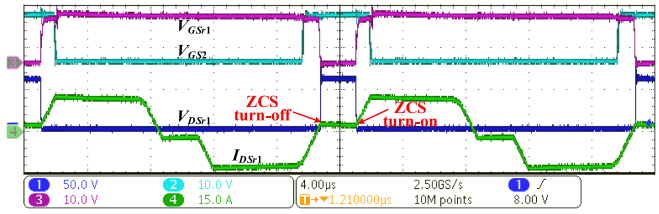

Fig. 16. Soft switching operation for Q_{r1} in boost mode.

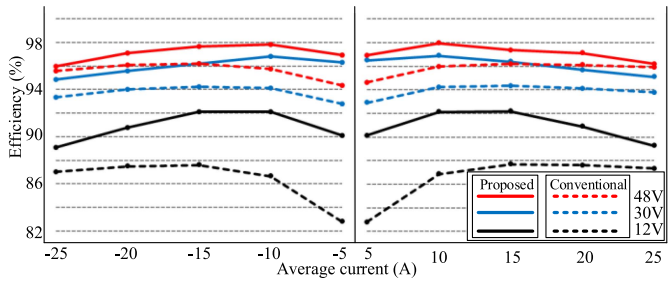

Fig. 17. Efficiency comparison between the proposed soft-switching interleaved bidirectional DC–DC converter and the conventional counterpart.

clear that Q_{r1} realizes the near ZCS turn-ON and turn-OFF in both modes. Topology symmetry can guarantee the ZCS operation for Q_{r2}. And extra voltage stress across the auxiliary switches is avoided due to the clamping effect provided by the two auxiliary diodes D_{r1} and D_{r2}, which improves reliability.

Apart from excellent soft switching operation, the proposed converter has other advantages over the previous methods. A comparison between them is carried out in terms of auxiliary devices, current stress, soft switching range, and so on, as shown in Table II. It shows with relatively small number of extra components and simple driving power, the proposed converter retains soft switching operation for all switches over a wide range. The protecting design is considered and then both the voltage stress and current stress are low, which makes the converter more reliable.

To further prove the high performance, the loss of this converter is analyzed and compared to that of its conventional counterpart. Loss breakdown under rated operating condition is listed in Table III. Also, the efficiency of the two converters is measured. The curves of efficiency versus power at V_L = 12 V, 30 V, and 48 V are plotted in Fig. 17. It can be seen from this table that the switching loss is mainly eliminated by the proposed method. But the conduction loss is increased heavily. The dominant loss in the two converters is distinct from each

other. And the increment of conduction loss is less than the decrement of the switching loss. So, the proposed converter shows higher efficiency than its regular counterpart over a wide power range and wide voltage gain range in both modes. Since the total current practically flows through one phase of the proposed converter for a quite long time, the conduction loss is then multiplied. The gradient of the conduction loss increment is greater than that of the switching loss decrement. So, the efficiency of the proposed converter gradually drops as the power exceeds a certain value. The soft switching feature of this converter is mainly at the cost of higher conduction loss.

VI. Conclusion

In this article, a high efficiency interleaved bidirectional dc–dc converter is proposed. This converter is on the basis of the conventional counterpart and the introduced auxiliary circuit. Composed of two switches, an inductor and a small capacitor, the auxiliary circuit is connected with the two switching nodes of the basic topology to realize sharing. This concept facilitates simple structure and hardware design as the source of auxiliary switch is attached to that of main switch. The two auxiliary switches are connected in series with the inductor and driven by designed sequences, which is key to realizing ZVS turn-ON for primary switches. Due to the voltage continuity, the capacitor provides the near ZVS condition for main switches to turn OFF. Meanwhile, the near ZCS condition for auxiliary switches is achieved naturally as the current slope is limited significantly by auxiliary inductor. To prove the validity of the proposed converter, a 1.2-kW laboratory prototype operating at 50 kHz switching frequency is built and tested. The efficient curves versus power under various voltage gain show the high performance compared to the primary converter. With the soft switching assisted, the converter efficiency is up to 98% at 40% of the full power, where the improvement is more than 2%.

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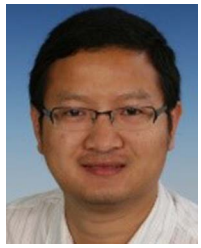

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