A Three-Phase Five-Level Unidirectional Rectifier With Reduced Components

Wenyuan Zhang, Xiaonan Zhu, *Member, IEEE*, Hongliang Wang, *Senior Member, IEEE*, Qing Li, Xiaojun Deng, Hanzhe Wang, and Xiumei Yue

***Abstract*—Owing to the advantages of simple structure, higher power density, and reliability, unidirectional five-level rectifiers are attractive solutions for high-power medium-voltage nonregenerative applications such as electric vehicle charging pile, telecommunication power, and laser power. However, the existing five-level unidirectional rectifiers use more switching devices or flying capacitors (FCs). This will reduce the power density and increase the complexity of the system. To address this issue, this article presents a three-phase five-level unidirectional rectifier with reduced components. It uses only three active switches and one FC per phase. Compared with most similar rectifiers, the number of active switching devices and floating capacitors has been reduced by 25% and 50%, respectively. Consequently, the proposed rectifier has the comprehensive merits in terms of simple structure and higher power density of the system. The operating principles of the proposed topology, control strategy, modulation scheme, and comparison study are presented in depth. Finally, a 3 kW three-phase experimental prototype is built to verify the validity and flexibility of the proposed topology.**

***Index Terms*—Five-level unidirectional rectifier, multilevel converter, pulsewidth modulation (PWM), three-phase system, unity power factor.**

I. Introduction

With the development of power electronics technology, pulsewidth modulation (PWM) rectifiers have been widely used in high power ac/dc conversion systems [1], [2]. It is more beneficial compared to the passive diode rectifiers since they present low harmonic distortion [3]. Particularly, the power flow is unidirectional in higher power applications, such as electric vehicle (EV) charging pile, telecommunication power, and laser power [4], [5]. Unidirectional three-phase PWM rectifiers become more attractive in these applications, due to the advantages of higher reliability, fewer active switches and lower the total cost [6], [7].

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The authors are with the College of Electrical and Information Engineering, Hunan University, Changsha 410082, China (e-mail: wenyuanzhang@hnu.edu.cn; zhuxn@hnu.edu.cn; wanghl123@hnu.edu.cn; liqing@hnu.edu.cn; xiaojundeng@hnu.edu.cn; hanzhewang@hnu.edu.cn; yuexm@hnu.edu.cn).

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In the last few decades, the rectifier topologies have been developed from two-level to three-level for industrial applications [8]. Among the traditional three-phase PWM rectifier topologies, the VIENNA rectifier is a well-known unidirectional three-level structure. Owing to its compact size, simple structure, and low voltage stress, it has been mostly used in industrial products [8], [9]. However, following the increase of the voltage rating and power level, the high-voltage rating devices must be applied to stand the voltage stress. Note that the high-voltage devices have low switching speed and large saturation voltage drop between the collector and the emitter [10]. Meanwhile, the cost of high-voltage devices and their gate drivers is higher. These factors will lead to the larger volume of input filter, higher cost, and lower efficiency of converter [11]. It is well recognized that a five or higher level topology has some distinctive merits, such as 1) further reducing the semiconductor voltage ratings for a given dc bus voltage, 2) superior harmonic performance for a given switching frequency, and 3) reducing switching losses.

The most popular multilevel topologies used in industrial applications mainly include the following categories: neutral point clamped (NPC) converter [12], flying capacitor (FC) converter [13], and cascaded H-bridge converter [39]. As the number of voltage level increases, the distinctive merits mentioned above are prominent. At the same time, the complexity of the system regarding the structure and control technique for multilevel converters also increase dramatically [11]. The five-level inverter based on FC structure with high utilization rate of dc voltage is presented in [29], in which the FCs have self-balancing capacity. However, the additional current-limiting inductor is required. Note that the power flows in both directions for the traditional multilevel topologies. In contrast, the unidirectional multilevel rectifiers, which use fewer active switching devices, are attractive options for nonregenerative applications [19].

To date, several five-level unidirectional rectifier topologies [14], [15], [16], [17] are derived from NPC types. In [14], a unidirectional five-level rectifier is obtained by replacing some active switches with diodes in conventional NPC. It requires six active switches and eight diodes per phase, as shown in Fig. 1(a). In order to further reduce the number of active switches, two other topologies have been proposed in [15] and [16], which use four active switches in Fig. 1(b) and (c), respectively. The five-level multiple-pole VIENNA rectifier topology has been presented in [17] and it uses two active switches per phase. However, these topologies require extra circuits for balancing

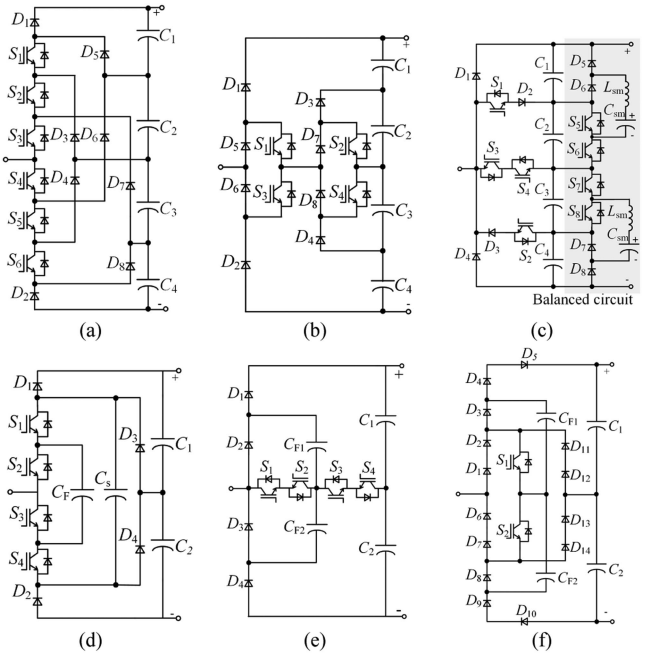

Fig. 1. Phase leg of the existing five-level unidirectional rectifiers. (a) Classical NPC [14]. (b) Multipole NPC [15]. (c) Hybrid T-type [16]. (d) Topology in [18]. (e) Topology in [19]. (f) Topology in [20].

the dc-link capacitor voltages, which increases the cost, volume and reduces reliability [18].

Following another approach, two unidirectional five-level rectifiers in [18] and [19] are developed from the bidirectional hybrid multilevel topologies, as shown in Fig. 1(d) and (e), respectively. Among them, the topology in Fig. 1(d) is derived from the five-level FC-ANPC and the topology in Fig. 1(e) is derived from the five-level stacked multicell converter, which combine the features of FC and NPC types. Thus, their dc neutral point (NP) voltages are easier to be balanced, without extra hardware circuits. They all present four switches and two FCs per phase. In [20], another unidirectional hybrid rectifier is derived from the dual FC active NPC converter, as shown in Fig. 1(f). It uses only two active switches per phase, which is the minimum required for a five-level rectifier. This will reduce the driver requirement and hardware complexity. In [21], an SiC and Si hybrid five-level unidirectional rectifier is proposed, in which the application of SiC devices improves the power density and efficiency of the system.

From the aforementioned topologies, it is concluded that it should be made a tradeoff between the numbers of switching devices and capacitors, the cost, and voltage stress of devices. To improve this issue, this article presents a new three-phase five-level unidirectional rectifier topology structure, in which the number of switching devices and floating capacitors has been further reduced. This feature will simplify the hardware structure of the system and reduce the complexity of the control system [27], [28].

The rest of the article is organized as follows. Section II introduces the basic idea and the operating principles of the proposed rectifier. Section III presents the control system of the

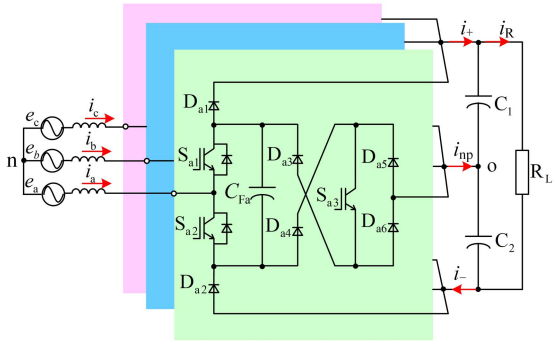

Fig. 2. Proposed three-phase five-level rectifier topology.

proposed rectifier. In Section IV, a comprehensive analysis and comparison is given. Section V presents the experimental results. Finally, Section VI concludes the article.

II. Operation Principles of the Proposed Three-Phase Five-Level Rectifier

A. Introduction of the Proposed Rectifier

The schematic of the proposed three-phase five-level rectifier in this article is shown in Fig. 2. The phase leg consists of three active switches (S_{X1}–S_{X3}), six diodes (D_{X1}–D_{X6}), and one FC C_{Fx} (X∈ (a, b, c) phases). The output dc voltage is defined as V_{dc}. The dc link consists of two series-connected capacitors (C_1, C_2), whose voltages are controlled at half of the dc-link voltage ($V_{dc}/2$), and the FCs are at $V_{dc}/4$. Through the voltage combination of dc-link capacitors and the FC, five input voltage levels $+V_{dc}/2$, $+V_{dc}/4$, 0, $-V_{dc}/4$, and $-V_{dc}/2$ can be obtained, which are defined as +2, +1, 0, –1, and –2 level, respectively.

Some features of the proposed rectifier are as follows.

1) The number of active switches is three per phase, and their voltage stress is $V_{dc}/4$. Compared with the most existing five-live rectifiers, the number is reduced by 25%.
2) Only three FCs are required, hence balancing the FC voltages is simple and then three voltage sensors for FCs are also cut down, which will reduce the complexity and increase the reliability of the control system [27], [28].
3) No extra hardware circuit, which usually contains additional switch devices and passive components, is needed to balance the dc-link capacitors voltage.
4) Using less devices and FCs will simplify the hardware structure and improve the power density of the system.

B. Operation Principle Analysis

The proposed rectifier has eight switching states, as shown in Fig. 3, which are named from A to H. Here, the red line represents the grid current path. The influence of the existing wiring inductance can be reduced by the low-cost snubber circuits [37] or the application laminated busbar [38]. When all the controlled switches are OFF, input point A gets connected to the dc-link midpoint through C_1 or C_2. Then, the rectifier generates +2 or –2 levels in Fig. 3(a) and (h), respectively. Similarly, when S_{a2} or S_{a1} is turned ON, the rectifier generates +1 or –1 level in

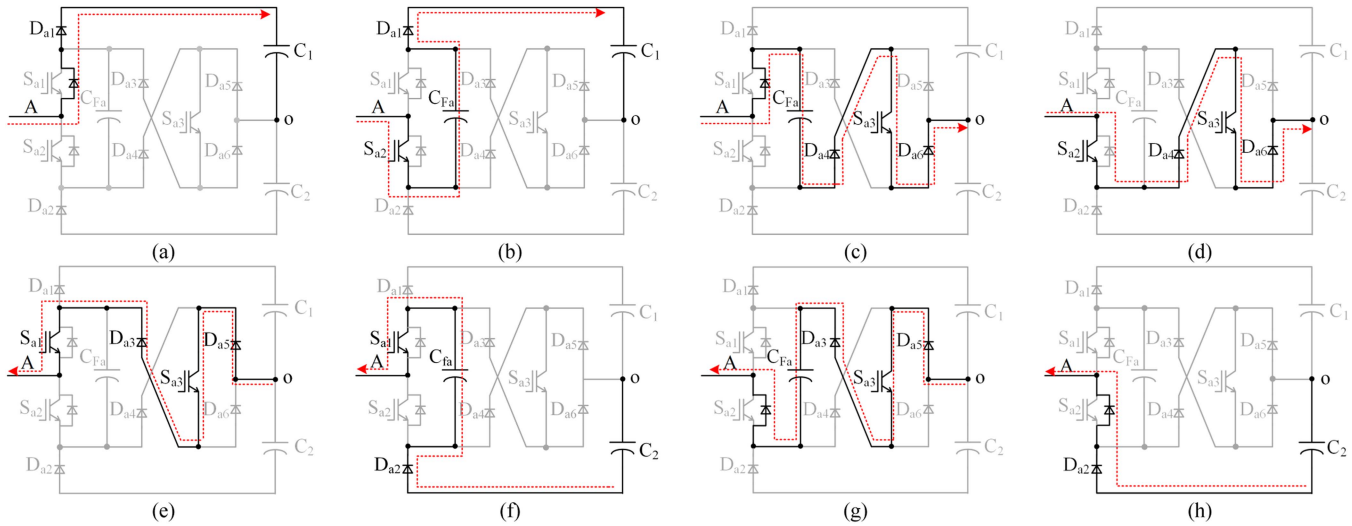

Fig. 3. Eight switching states for the proposed three-phase five-level rectifier. (a) State A: $+V_{\rm dc}/2$. (b) State B: $+V_{\rm dc}/4$. (c) State C: $+V_{\rm dc}/4$. (d) State D: $+0$. (e) State E: -0. (f) State F: $-V_{\rm dc}/4$. (g) State G: $-V_{\rm dc}/4$. (h) State H: $-V_{\rm dc}/2$.

TABLE I
SWITCHING STATES, BRIDGE VOLTAGES, AND IMPACT ON THE FCS

State	$V_{\rm AO}$	$S_{\rm x1}$	$S_{\rm x2}$	$S_{\rm x3}$	$i_{\rm x}$	Impact of $i_{\rm x}$ to $C_{\rm FX}$
A	$V_{\rm dc}/2$	0	0	0		–
B	$V_{\rm dc}/4$	0	1	0	+	discharge
C	$V_{\rm dc}/4$	0	0	1		charge
D	0	0	1	1		–
E	0	1	0	1		–
F	$-V_{\rm dc}/4$	0	0	1	–	charge
G	$-V_{\rm dc}/4$	1	0	0		discharge
H	$-V_{\rm dc}/2$	0	0	0		–

Fig. 3(b) and (f). As can be observed, these switching states are only discharging the FC. Therefore, two other switching states are required to balance the FC voltage by charging the FC. In Fig. 3(c) and (g), when $S_{\rm a3}$ is ON, the rectifier also generates $+1$ and -1 levels, which are called redundant switching states. When ($S_{\rm a2}$, $S_{\rm a3}$) or ($S_{\rm a1}$, $S_{\rm a3}$) are turned ON, the rectifier generates $+0$ or -0 level in Fig. 3(d) and (e). During the positive half-cycle of grid current, the used states are from A to D. States from E to H are used during the negative half-cycle of grid current.

Table I lists all eight switching states and their impact on FC voltage. "+" represents that the direction of grid current is from A to o and "–" is from o to A. As can be seen from Table I, two pairs of redundant switching states (+1: B and C) and (–1: F and G) have the opposite impacts on FC voltage regulation. Therefore, the regulation of FC voltage can be achieved by proper selection of redundant switching states.

III. MODELING AND CONTROL STRATEGY

A. Average Model of the Proposed Rectifier

Based on the operation principle of the rectifier, the pole voltages to the dc midpoint $u_{\rm xo}$ (x ∈a, b, c) can be given in (1), and $S_{\rm x1}$, $S_{\rm x2}$, and $S_{\rm x3}$ are defined as (2)

$$u_{\rm xo} = \frac{V_{\rm dc}}{4}\left(2 - S_{\rm x1} - S_{\rm x2} - S_{\rm x3}\right)\mathrm{sgn}(i_{\rm x}) \tag{1}$$

$$S_{\rm x1,x2,x3} = \begin{cases} 1, & \text{if } S_{\rm x1,x2,x3} \text{ is turned on} \\ 0, & \text{if } S_{\rm x1,x2,x3} \text{ is turned off.} \end{cases} \tag{2}$$

Assuming that the three-phase grids and dc NP are balanced, the modes of the proposed rectifier are obtained. When the rectifier system is oriented in the synchronous reference (d–q frame) of the grid voltage vector and the d-axis of the reference frame is aligned with grid voltage vector, the model of the rectifier can be described in (3) [23], [24], where L and R are the inductance and resistance of input inductor, respectively, and ω is the angular speed of the grid voltage vector

$$\begin{cases} e_{\rm d} = |e| = u_{\rm d} + Ri_{\rm d} + L\dfrac{di_{\rm d}}{dt} - \omega L i_{\rm q} \\ e_{\rm q} = 0 = u_{\rm q} + Ri_{\rm q} + L\dfrac{di_{\rm q}}{dt} + \omega L i_{\rm d}. \end{cases} \tag{3}$$

For the dc output side, the model is given by

$$\begin{cases} C_0\dfrac{dV_{\rm dc1}}{dt} = i_+ - \dfrac{V_{\rm dc}}{R_L} \\ C_0\dfrac{dV_{\rm dc2}}{dt} = i_- - \dfrac{V_{\rm dc}}{R_L} \end{cases} \tag{4}$$

where i_+ and i_- represent the currents flowing through the positive dc bus and the negative dc bus, respectively, and C_0 is the capacitance of upper and lower capacitors in dc link.

B. Control Strategy

The control strategy must meet the following requirements.

1) The dc output voltage should be regulated.
2) The NP voltage and FC voltage should be balanced.
3) The unity power factor as well as minimizing the current distortion at the rectifier terminal should be realized.

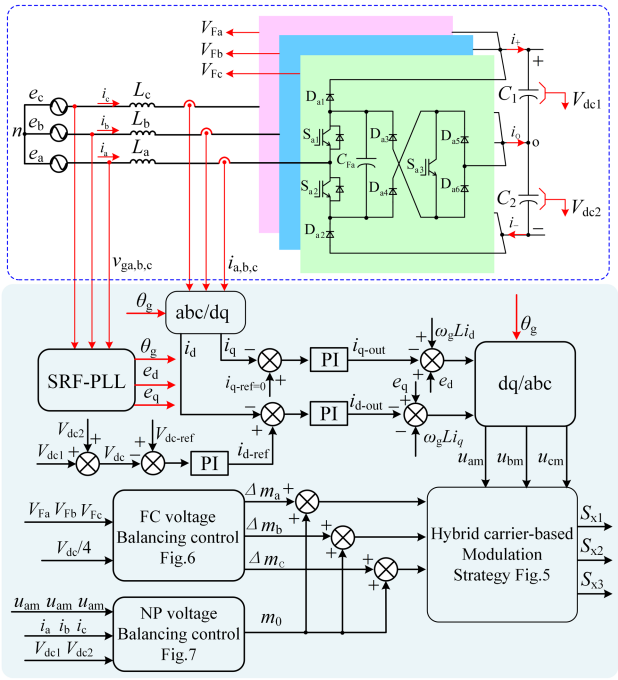

Fig. 4. Overall control strategy of the proposed rectifier.

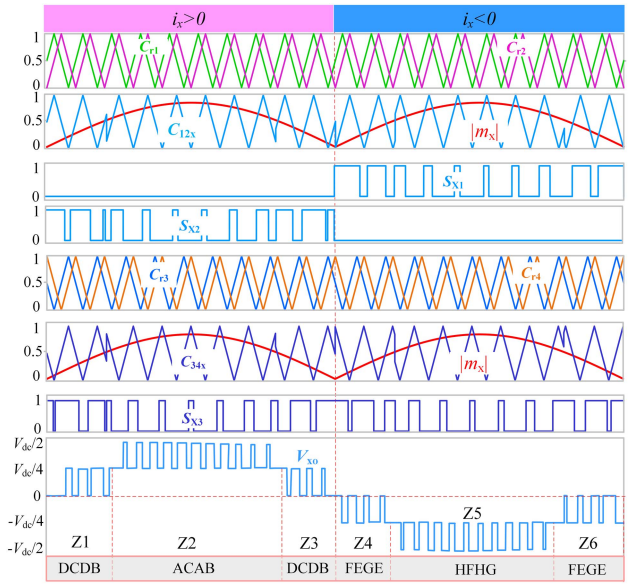

Fig. 5. Hybrid modulation for the proposed rectifier.

Based on the model of the rectifier in (3), the grid voltage oriented vector control strategy for the proposed rectifier is shown in Fig. 4.

The dc output voltage and the input current are controlled by a proportional and integral (PI) controller on a *d–q* rotating frame, which is the same as that in a conventional three-level converter [9], [22]. It should be noted that this control strategy is mainly used for normal grid condition. Combining the injected the zero-sequence component and a PI controller is implied to control the dc NP voltage, which is analyzed in detail. Additionally, the FC voltages are controlled by proportional controller to modify the reference modulation signal. The hybrid phase shift PWM modulation is adopted to realize the smaller grid current distortion and allocate the two pairs of redundant switching states (B, C and E, F) for ± 1 voltage levels. The detailed implementation method is discussed later. The excellent control scheme with "input current-oriented" in [26] can be also implied to improve the performance of the proposed rectifier, such as the utilization of dc-link voltage.

C. Modulation Scheme

For this application, a hybrid modulation strategy is used in this article because of its best performance in terms of both lower harmonic of input current and the overall converter efficiency [20]. Fig. 5 shows the diagram of the PWM scheme for the proposed rectifier. It is implemented with four carrier signals (C_{r1}, C_{r2}, C_{r3}, C_{r4}) shown in Fig. 5 and there is a phase shift of 90° among these carrier signals. According to the direction of the phase current (i_{x}) and the magnitude of the modulation signals (m_{x}), the carrier signal $C_{12\mathrm{x}}$ is selected from C_{r1} and C_{r2} and $C_{34\mathrm{x}}$ is from C_{r3} and C_{r4}. The generation principle of $C_{12\mathrm{x}}$ and $C_{34\mathrm{x}}$ is as follows:

$$C_{12\mathrm{x}} = \begin{cases} C_{\mathrm{r1}}, & \text{for } (\, i_{\mathrm{x}} > 0\,) \text{ xor } (\, |m_{\mathrm{x}}| > 0.5\,) = 1 \\ C_{\mathrm{r2}}, & \text{for } (\, i_{\mathrm{x}} > 0\,) \text{ xor } (\, |m_{\mathrm{x}}| > 0.5\,) = 0 \end{cases} \tag{5}$$

$$C_{34\mathrm{x}} = \begin{cases} C_{\mathrm{r3}}, & \text{for } (\, i_{\mathrm{x}} > 0\,) \text{ xor } (\, |m_{\mathrm{x}}| > 0.5\,) = 1 \\ C_{\mathrm{r4}}, & \text{for } (\, i_{\mathrm{x}} > 0\,) \text{ xor } (\, |m_{\mathrm{x}}| > 0.5\,) = 0. \end{cases} \tag{6}$$

During positive fundamental period, the gate pulses for switches S_{x2} and S_{x3} are obtained by comparing the absolute value of m_{x} ($|m_{\mathrm{x}}|$) with the carrier $C_{12\mathrm{x}}$ and $C_{34\mathrm{x}}$, respectively; S_{x1} is "OFF." For the negative fundamental period, gate pulses for S_{x1} and S_{x3} are obtained by comparing the $|m_{\mathrm{x}}|$ with the carrier $C_{12\mathrm{x}}$ and $C_{34\mathrm{x}}$, respectively; S_{x2} is "OFF." Note that the carrier signals $C_{12\mathrm{x}}$ and $C_{34\mathrm{x}}$ have 180° phase shifted property. This will be used to balance the FC voltages as well as generating the five-level voltage waveforms in the pole voltage. For example, the pole voltage V_{xo} is switched between $+2$ and $+1$ in zone Z2. For $+1$ voltage level, the switching states B and C are required to balance the FC voltages. Therefore, the rotation sequence of (A, C, A, B) is achieved in zone Z2. In addition, the applied modulation functions can be easily realized by the field-programmable gate array (FPGA) card or digital logic circuits.

D. FC Voltage Balancing Control

Under normal operating conditions, the redundant switching states (B, C) and (F, G) are evenly selected during the positive period and the negative period, respectively. Thus, the charging time and discharging time of FC are equally distributed in a carrier period and FC voltages are naturally balanced at 0.25 V_{dc}. However, considering the effects of the nonidealities and dynamic conditions, a simple proportional compensator is utilized for feedback regulation, Δm_{a} is calculated by feedback

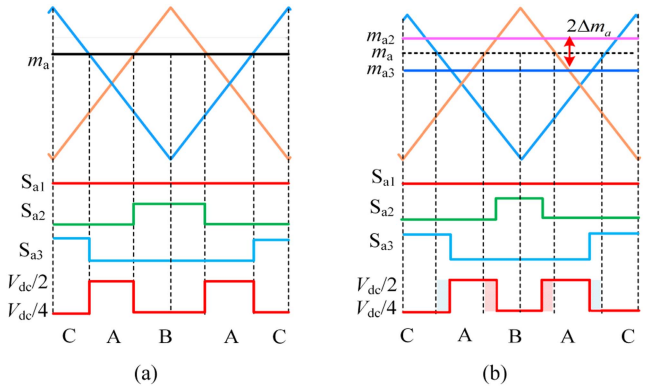

Fig. 6. Effects of addition/subtraction of a constant to the modulating signal on the rectifier input voltage and switching signals (a) before modification and (b) after modification.

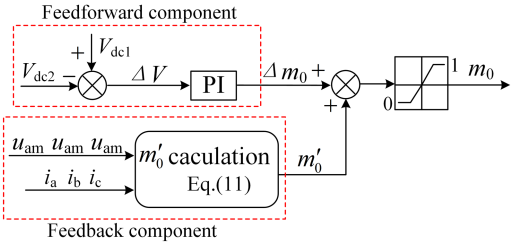

Fig. 7. Control block diagram of the NP voltage.

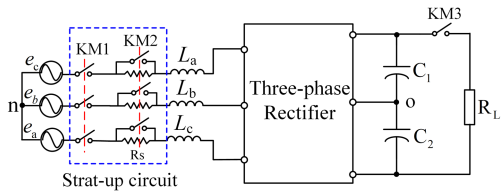

Fig. 8. Simplified schematic diagram of the three-phase rectifier system.

controller in the real system. For "a" phase, the modulation waves m_a of S_{a2} and S_{a3} can be modified slightly with Δm_a. Defining the modified modulation waves of S_{a2} and S_{a3} as m_{a2} and m_{a3}, respectively. In a positive fundamental period, they can be given as

$$\begin{cases} m_{a2} = m_a + \Delta m_a \\ m_{a3} = m_a - \Delta m_a. \end{cases} \tag{7}$$

Taking zone Z2 for example, Fig. 6 shows the effect of adding/subtracting a positive constant (Δm_a) to m_a. It can be proved that switching states B and C have same duration without FC regulators in Fig. 6(a). In Fig. 6(b), the duration of state C is increased, whereas it is decreased for state B. Reverse will happen when Δm_a is negative. This modified process will not inflect the average value of the rectifier pole voltage. Note that the charging time and discharging time of FC are regulated. Thus, the FC voltages are controlled to their rated value. Based on the same principle, in negative fundamental period, the modified modulation waves m_{a1} and m_{a3} can be written as

$$\begin{cases} m_{a1} = m_a - \Delta m_a \\ m_{a3} = m_a + \Delta m_a. \end{cases} \tag{8}$$

E. NP Voltage Balancing Control

From (4), the dc NP voltage is modeled as follows:

$$C_0 \frac{d(V_{dc2} - V_{dc1})}{dt} = i_{np} = i_- - i_+. \tag{9}$$

According to the operation characteristics of the proposed rectifier and the derivation procedures given in [25], the average current through NP can be expressed as

$$-i_{np} = |i_a|\, u_{am} + |i_b|\, u_{bm} + |i_c|\, u_{cm} + m'_0(|i_a| + |i_b| + |i_c|) \tag{10}$$

where u_{am}, u_{bm}, and u_{cm} are the original reference modulation signal, and $m'_0$is injected the zero-sequence component. In order to keep the NP balanced, the average NP current should be controlled to zero within the pulse interval. Therefore, according to (10), the injected zero-sequence component (m'_0) can be calculated as

$$m'_0 = -\frac{|i_a|\, u_{am} + |i_b|\, u_{bm} + |i_c|\, u_{cm}}{|i_a| + |i_b| + |i_c|}. \tag{11}$$

Theoretically, with the injected m'_0, the NP voltage can be balanced. However, considering the influence of nonideal factors on the NP voltage, such as the sampling error of sensors, and the asymmetry of system parameters in real system, only using the calculated m'_0 cannot balance the NP voltage accurately [20], [25]. Especially, for the dual-port applications, this method cannot balance the unbalanced loads. Hence, the feedback controller (PI) is added to compensate these effects in the real system. The controller generates a feedback compensation component Δm_0. The m'_0 acts as the feedforward component to compensate the key NP current. Then, the control block diagram of the NP voltage is illustrated in Fig. 7, and final zero-sequence component m_0 is equal to the sum of m'_0 and Δm_0.

F. Startup Procedure for FCs and DC-Link Capacitors

The simplified circuit configuration of the three-phase rectifier system is illustrated in Fig. 8.

The start-up circuit is commonly used for ac/dc converter system [35]. The voltage buildup procedure for the capacitors of the rectifier consists of the following four stages.

Stage I: Preliminary voltage buildup for C_1 and C_2. KM1 is closed and the S_{a3}, S_{b3}, S_{c3} are turned OFF. After this stage, C_1 and C_2 are charged to $V_{set1}/2$. $V_{set1}/2$ is approximately equal to the amplitude of grid line voltage.

Stage II: Preliminary voltage buildup for the C_{Fa}, C_{Fb}, and C_{Fc}. In this stage, the S_{a3}, S_{b3}, S_{c3} are turned ON and the FCs are initially charged to the preset value of $V_{set1}/4$. When the voltage of FCs reaches to $V_{set1}/4$, all switches are turned OFF.

Stage III: Further voltage buildup for C_1, C_2, C_{Fa}, C_{Fb}, and C_{Fc} with closed-loop control. After the first two stages, dc-link capacitors are charged to $V_{set1}/2$ and FCs are charged to $V_{set1}/4$.

TABLE II
VOLTAGE STRESS AND SELECTED DEVICES FOR LOSS CALCULATION

Switches	Voltage stress	Current stress	Switching frequency	Selected devices
S_{x1}-S_{x1}	$V_{dc}/4$	I_m	f_s for half line cycle	IXFH70N30Q3
S_{x3}	$V_{dc}/4$	I_m	f_s for line cycle	IXFH70N30Q3
D_{x1}-D_{x2}	$3V_{dc}/4$	I_m	f_s for half line cycle	DSEI60-06A
D_{x3}-D_{x4}	$V_{dc}/2$	I_m	f_s for half line cycle	DPG60I400HA
D_{x5}-D_{x6}	$V_{dc}/4$	I_m	f_s for half line cycle	DPG60I300HA

TABLE III
DUTY RATIO OF EACH DEVICE

Switches	Duty ratio (d_{sw})	
	Positive cycle (i_{ga}>0)	Negative cycle (i_{ga}<0)
D_{a1}	$M\sin(\omega t)$	0
S_{a1}	$M\sin(\omega t)$	1-$\lvert M\sin(\omega t)\rvert$
S_{a2}	1-$M\sin(\omega t)$	$\lvert M\sin(\omega t)\rvert$
D_{a2}	0	$\lvert M\sin(\omega t)\rvert$
D_{a3}, D_{a5}	0	1-$\lvert M\sin(\omega t)\rvert$
D_{a4}, D_{a6}	1-$M\sin(\omega t)$	0
S_{a3}	1-$M\sin(\omega t)$	1-$\lvert M\sin(\omega t)\rvert$

The closed-loop control strategy is shown in Fig. 4. Different from normal operation control stage, the reference value of the dc-link voltage controller is linearly increased to the rated value with a relatively small step (V_{step}).

Stage IV: Normal operation closed-loop control. When Stage III is completed, the rectifier begins its normal operation stage and KM2 and KM3 are closed.

IV. COMPREHENSIVE ANALYSIS AND COMPARISON

A. Analysis of Power Loss and Stress in Devices

The voltage stress and switching frequency are summarized in Table II, where f_s is the switching frequency. The current stress of devices is the peak value of grid current (I_m).

In order to theoretically evaluate the power losses of each device in the rectifier for practical applications, the power module used in parallel in the EV charger system is taken as an example. In the module, the front-end rectifier creates the dc power source for the back-end power conversion, in which the rated power is set to 15 kW, grid line voltage is 380 V, and the dc-link voltage is set to 650 V. The rating of selected devices is chosen in accordance with their voltage stress and current stress, in which a safety margin for the switches and diodes is considered. The main selected devices for loss calculation are listed in Table II.

As for the switches in this topology, their conduction losses can be divided into two parts. One part is the loss of the switch itself, the other part is its body diode loss. Commonly, the conduction loss is related to the modulation strategy and the currents flowing through it. The average duty ratios of the active switches and diodes are given in Table III.

According to the modulation strategy, M is the modulation depth index and ω is the angular frequency of grid voltage. The average conduction loss of the MOSFET during the grid period could be given as [30]

$$P_{C\_SW} = \frac{1}{2\pi}\int_0^{2\pi} u_{ds}(t)i(t)d_{sw}(t)d(\omega t) \tag{12}$$

where $u_{ds}(t) = i(t)R_{ds}$, $i(t) = I_m\sin(\omega t)$, I_m is the peak value of the grid current, and R_{ds} is the drain-source resistance of the MOSFET during the ON-state operation. Similarly, the average conduction loss of the diode could be given by [36]

$$P_{C\_d} = \frac{1}{2\pi}\int_0^{2\pi} u_F(t)i(t)d_{sw}(t)d(\omega t) \tag{13}$$

where $u_F(t) = V_{FO} + i(t)R_F$, V_{FO} is the diode fixed voltage drop under zero-current condition, and R_F is the diode ON-drop resistance. By combining (12)–(13) and Table III, the conduction loss of S_{a1}, S_{a2} can be calculated as

$$P_{C\_Sa1} = \frac{I_m^2 R_{ds}}{4} - \frac{2MI_m^2 R_{ds}}{3\pi} + \frac{MI_m V_{FO}}{4} + \frac{2MI_m^2 R_F}{3\pi}. \tag{14}$$

Differently, the conduction loss for S_{a3} has no body diode loss and can be given by

$$P_{C\_Sa3} = \frac{I_m^2 R_{ds}}{2} - \frac{4MI_m^2 R_{ds}}{3\pi}. \tag{15}$$

Similarly, the conduction loss for D_{a1}, D_{a2} can be obtained as follows:

$$P_{C\_Da1} = \frac{V_{FO}MI_m}{4} + \frac{2MI_m^2 R_F}{3\pi}. \tag{16}$$

The conduction loss for D_{a3}, D_{a4}, D_{a5}, and D_{a6} can be obtained as follows:

$$P_{C\_Da3} = \frac{R_F I_m^2}{4} + \frac{V_{FO}I_m}{\pi} - \frac{V_{FO}MI_m}{4} - \frac{2I_m^2 MR_F}{3\pi}. \tag{17}$$

As it has been discussed in [31], the switching losses P_{sw} of the switch can be obtained as

$$P_{sw} = \frac{1}{2\pi}\frac{V_{off}(t_{on}+t_{off})}{2T}\int_0^{2\pi} i(\theta)d\theta \tag{18}$$

where V_{off} is the OFF-state voltage, t_{on} and t_{off} are turn-ON and turn-OFF times, respectively, and $i(\theta)$ is the current flowing across switches. The reverse recovery loss of diode during reverse recovery period could be approximated as [32]

$$P_{rev\_d} = \frac{1}{2\pi}\frac{Q_{rr}V_R}{\sqrt{2}I_F T_s}\int_0^{2\pi} i_F(\theta)d\theta \tag{19}$$

where Q_{rr} is the reverse recovery charge, V_R is the voltage across the diode, and I_F is the test condition of Q_{rr} in the datasheet.

According to the designed circuit parameters and the selected devices listed in Table II, using (12)–(19), the calculated losses for the devices in one phase are obtained and the distributions of power losses among the devices are depicted in Fig. 9 and theoretical efficiency of the rectifier is estimated to be 98.87% at 15 kW, where the loss of filter inductors and capacitors is ignored. The percentage of power losses at switches S_{a3} is lower than S_{a1} and S_{a2} since it has no power loss of the body diode. The average conduction time of D_{a3}–D_{a6} is lower than that of other devices. Hence, the distributed power loss of them is low. The uneven loss distribution among the devices can be further improved by optimized modulation methods [33], [34].

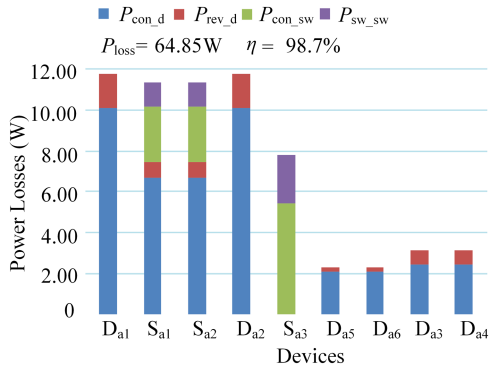

Fig. 9. Power losses of devices for the proposed rectifier.

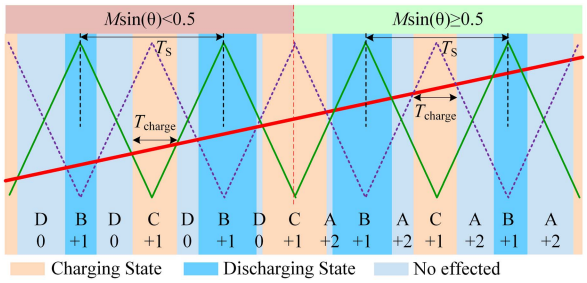

Fig. 10. Diagram of the modulation in a positive half-cycle.

B. FC Design

The FC design is usually decided by its voltage ripple requirement, and the maximum voltage ripple depends on the charging and discharging times during one carrier period. Here, the charging time is used to calculate the FC voltage ripple.

From Fig. 10, it is obtained that the charging time of FC ($T_{\rm charge}$) during one switching cycle ($T_{\rm S}$) can be written as

$$\begin{cases} T_{\rm charge} = T_{\rm S} M \sin\theta & (M\sin\theta > 0.5) \\ T_{\rm charge} = T_{\rm S}(1 - M\sin\theta) & (M\sin\theta \le 0.5)\,. \end{cases} \tag{20}$$

From (20), it is obtained that $T_{\rm charge}$ reaches its peak value when $M\sin\theta = 0.5$. With the FC charging time $T_{\rm charge}$, the FC voltage variation $\Delta V_{\rm FC}$ can be calculated as

$$\Delta V_{\rm FC} = \frac{\Delta Q_{\rm FC}}{C_{\rm FC}} = \frac{T_{\rm charge} I_{\rm m} \sin\theta}{C_{\rm FC}}. \tag{21}$$

Combining (20) and (21), the FC voltage ripple can be written as

$$\begin{cases} \Delta V_{\rm FC} = \dfrac{I_{\rm m} T_{\rm s} M \sin^2\theta}{C_{\rm FC}} & (M\sin\theta \le 0.5) \\ \Delta V_{\rm FC} = \dfrac{I_{\rm m} T_{\rm s}}{C_{\rm FC}} \left(\sin\theta - M\sin^2\theta\right) & (M\sin\theta > 0.5)\,. \end{cases} \tag{22}$$

From (22), it is obtained that $\Delta V_{\rm FC}$ reaches its peak value when $\sin\theta = 1/2M$. Generally, $\Delta V_{\rm FC}$ is limited to 2% of FC voltage in practice [14]. Therefore, the minimum capacitance value $C_{\rm FC}$ can be calculated as

$$C_{\rm FC,min} \ge \frac{I_{\rm m} T_{\rm S}}{4\Delta V_{\rm FC} M}. \tag{23}$$

A certain margin should be taken into consideration in practice.

C. Comparison With Different Topologies

Table IV presents a detailed comparison of several key features of the proposed rectifier with other similar existing rectifiers. Compared with unidirectional NPC five-level rectifier in [14], the number of switches and their drivers are markedly reduced. Compared with rectifiers in [15] and [16], the number of switches and drivers are also cut down and the voltage stress of some switches is lower. Compared with the rectifier in [17], the peak inverse voltage of some switches is also lower. Furthermore, the proposed rectifier does not require extra hardware circuit for balancing the dc-link capacitor voltages, compared with the rectifier in [15], [16], and [17].

The topologies in [18], [19], and [20] and the proposed topology have the similar structure, in which FCs are engaged to achieve $\pm V_{\rm dc}/4$ levels. Hence, in addition to comparing the number of capacitors, it is also necessary to compare the other parameters, such as the capacitance, rms current, and voltage. Considering the operation principles of the topologies and the function of the capacitors, the theoretical capacitance of FCs and dc link capacitors in these topologies are the same with the same working conditions. Table V presents a detailed comparison of capacitors in these topologies. The rms current of each FC in [19] and [20] is lower, which is the advantage. Note that three additional clamping capacitors in [18] are required. In terms of the total volumes of all capacitors, the proposed rectifier has advantages over the other similar topologies, which will improve the power density of system.

Compared with the hybrid five topologies in [18] and [19], the number of active devices and floating capacitors has been reduced by 25% and 50%, respectively. The rectifier in [20] uses the least active switches and corresponding driver circuits for the five-level rectifiers, which is beneficial. Compared with [20], the proposed rectifier uses less diodes and FCs. This will simplify the structure of the rectifier and reduce the complexity of the control system [27], [28].

In short, the proposed rectifier has a comprehensive merit in terms as the comments count, simple topology structure and then simple control system, and higher power density of the system. Some of the diodes with high-voltage stress can be improved by series-connected low-voltage diodes for medium-voltage applications.

V. Experimental Verification

The experimental tests have been carried out to verify the effectiveness of the proposed rectifier. The control schematic of the system is consistent with Fig. 4. The experimental setup and its corresponding specifications are shown in Fig. 11 and Table VI, respectively. For the control circuit, a Texas Instruments TMS320F28335 DSP plus Altera EP2C8Q208 FPGA

TABLE IV
COMPARISON OF DIFFERENT THREE-PHASE TOPOLOGIES

Parameter		Pro.	[14]	[15]	[16]	[17]	[18]	[19]	[20]
No. of switches	$V_{dc}/4$	9	18	6	10	7	12	12	6
	$3V_{dc}/8$	0	0	6	0	0	0	0	0
	$V_{dc}/2$	0	0	0	6	3	0	0	0
	$3V_{dc}/4$	0	0	0	0	0	0	0	0
No. of diodes	$V_{dc}/4$	6	12	12	4	12	0	0	42
	$3V_{dc}/8$	0	0	6	0	0	0	0	0
	$V_{dc}/2$	6	6	0	6	0	12	12	0
	$3V_{dc}/4$	6	6	6	6	0	0	0	0
No. of DC capacitors		2	4	4	4	4	2	2	2
No. of flying capacitors		3	0	0	0	0	6	6	6
No. of drivers		9	18	12	16	10	12	12	6
PIV		$V_{dc}/4$	$V_{dc}/4$	$3V_{dc}/8$	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/4$	$V_{dc}/4$	$V_{dc}/4$
Extra hardware circuit for voltage balancing		Not needed	Not needed	Needed	Needed	Needed	Not needed	Not needed	Not needed

PIV represents the peak inverse voltage of switches in a topology.

TABLE V
COMPARISONS FOR THE PARAMETER OF DIFFERENT CAPACITORS

	Parameters	Pro.	[18]	[19]	[20]
DC-link capacitor	Number	2	2	2	2
	Rated voltage	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$
	RMS current	$I_{rms,bus}$	$I_{rms,bus}$	$I_{rms,bus}$	$I_{rms,bus}$
Flying capacitor	Number	3	3	6	6
	Rated voltage	$V_{dc}/4$	$V_{dc}/4$	$V_{dc}/4$	$V_{dc}/4$
	RMS current	$\sqrt{2}I_{rms,FC}$	$\sqrt{2}I_{rms,FC}$	$I_{rms,FC}$	$I_{rms,FC}$

$I_{rms,bus}$ represents the rms current of dc-link capacitors ; $I_{rms,FC}$ represents the rms current of flying capacitors in [20] and [21].

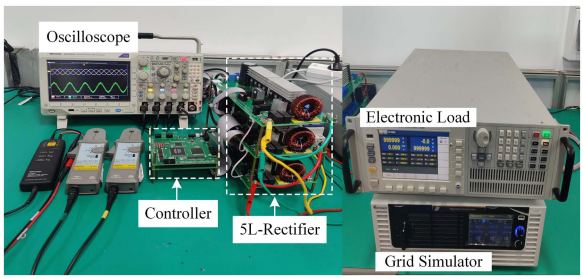

Fig. 11. Photograph of the experimental setup of the proposed rectifier.

TABLE VI
SYSTEM PARAMETERS

Description	Symbol	Value
Output voltage	V_{dc}	650 V
Grid line voltage	V_{gab}	380 V @ 50 Hz
FC capacitance	C_{Fa}, C_{Fb}, C_{Fc}	220 uF
DC-link capacitance	C_1, C_2	390 uF
Filter inductance	L_a, L_b, L_c	1.5 mH
Switching frequency	f_s	5 kHz
Power	P	3.0 kW

digital platform is used. The experimental results of the proposed rectifier are shown in Figs. 12–16.

Fig. 12 shows the experimental waveforms of the rectifier in the steady state. Its input line voltage is 380 V, 50 Hz, the output rated power is 3 kW, and the dc output voltage command is set to 650 V. Fig. 12(a) shows the three-phase grid currents (i_a, i_b, and i_c) and the terminal line voltage (V_{ab}). The three currents are purely sinusoid and balanced, and V_{ab} is seen to have nine levels, which is the feature of a three-phase five-level converter. In Fig. 12(b), it can be seen that the three terminal line voltages are all with nine levels, and the measured total harmonic distortion (THD) of i_a is 2.71%. Fig. 12(c) shows the waveforms of i_a, the grid phase voltage with respect to the grid neutral (e_{an}), and rectifier side phase a voltage (V_{ao}). The grid current is controlled to be in phase with the grid voltage and the measured power factor is 0.999. A five-step voltage waveform is observed in phase voltage, which agrees with the expectation. Fig. 12(d) exhibits the waveforms of output dc-link voltage (V_{dc}), two dc-link capacitors voltage (V_{c1}, V_{c2}), and one FC voltage (V_{Fa}): channel 1 is V_{dc}, which is controlled to 650 V; channel 2 and channel 3 are V_{c1} and V_{c2}, and they are stabilized at about 325 V; Channel 4 is V_{Fa}, which is stabilized at about 162 V. The measured peak-to-peak FC voltage ripple is 3 V (3 V/162 V = 1.8%) and two dc-link capacitors voltage ripple is 11 V (11 V/325 V = 3.4%). They verify the effectiveness of the dc-link midpoint voltage controller and the FC voltage controllers. The voltage waveforms on some of the devices are shown in Fig. 12(e) and (f); the maximum voltages on S_{a1}, S_{a2}, and S_{a3} are around 162.5 V in Fig. 12(e), which is one-fourth of dc output voltage; Fig. 10(f) shows the voltages on D_{a1}, D_{a3}, and D_{a5}.

Transient responses of the rectifier were conducted to verify the stability of the control strategy. Fig. 13(a) and (b) shows transient responses with the input grid voltages perturbed by ±40%. As can be seen, the terminal line voltage (V_{ab}) keeps stability during grid disturbance. This also indicates that the voltages of FCs maintain balance. In addition, the grid current can be obtained well, and no large current spikes occur during the transient process. Fig. 13(c) shows the transient responses with step change of the load power by±50%. The load power suddenly changes from 1.5 to 3.0 kW and then, again changes back to 1.5 kW. It is observed that the two dc-link voltages and FC voltage can be balanced at their rating value after the transient time.

To further validate the ability of the method for NP voltage balance, the response of the rectifier with unbalanced dc load

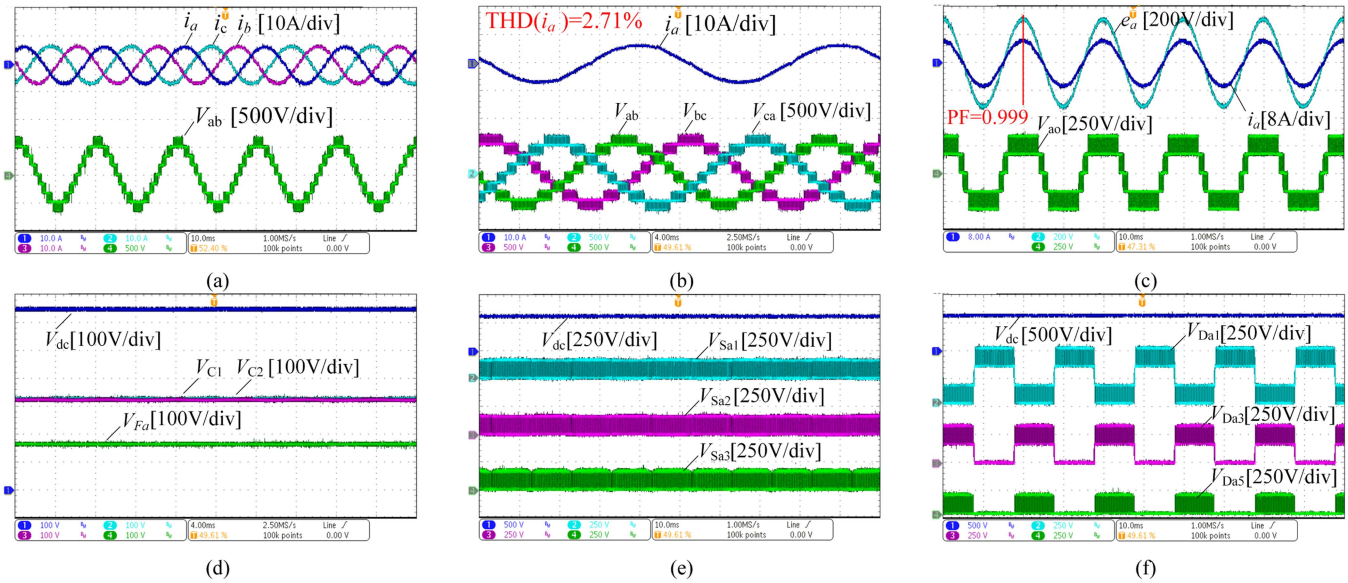

Fig. 12. Experimental results exhibiting steady-state waveforms (input voltage: 380 V, 50 Hz, output DC-link voltage: 650 V, load: 3 kW).

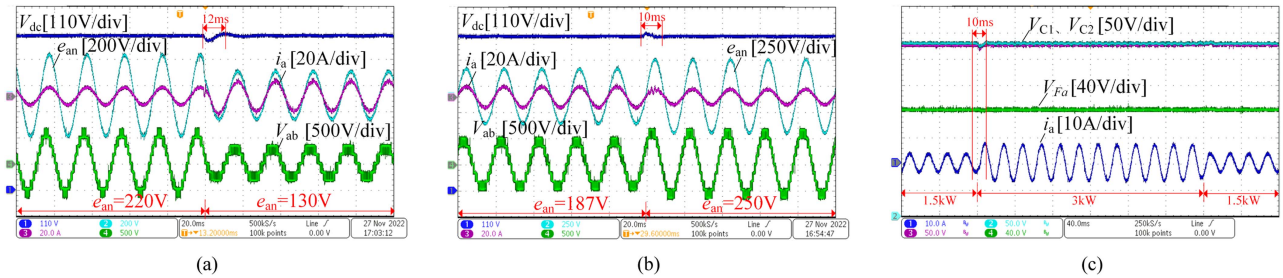

Fig. 13. Experimental results exhibiting transient state waveforms. (a) Input phase voltage steps from 220 to 130 V. (b) Input phase voltage steps from 187 to 250 V. (c) Output power steps from 1.5 to 3.0 kW.

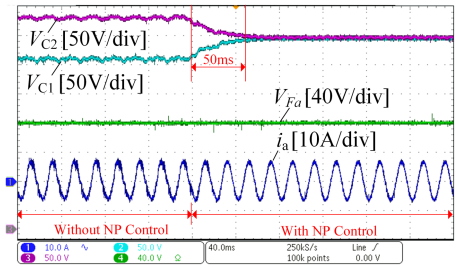

Fig. 14. NP voltage-balance control for the proposed rectifier under unbalanced load condition: $R1 = 60\ \Omega$, $R2 = 80\ \Omega$.

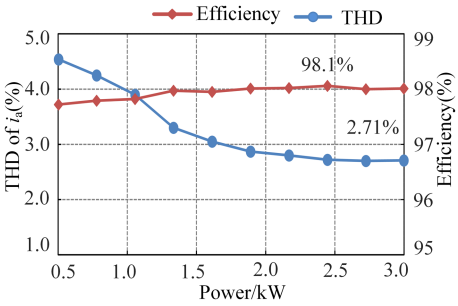

Fig. 15. Measured efficiency curve and THD curve of grid current.

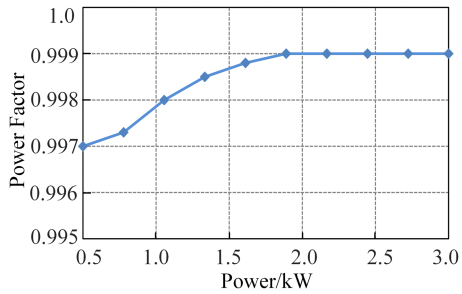

Fig. 16. Measured power factor curve of the rectifier.

was conducted, in which C_1 is connected to the resistor with 60 Ω and C_2 is connected to the resistor with 80 Ω. Fig. 14 shows the transient responses of V_{c1}, V_{c2}, V_{Fa}, and i_a, when the NP voltage-balance control is added. It is observed that the two dc-link capacitor voltages can be balanced rapidly after the addition of NP voltage-balance control.

Overall, the effectiveness of the control strategy for the proposed five-level rectifier is verified by the obtained steady state and dynamic performances. By the power analyzer, the measured efficiency and THD as a function of power for the

proposed rectifier are shown in Fig. 15. Noted that the maximum efficiency is around 98.1% and the THD of grid current is 2.71% (the 40th or less order component harmonics were considered) at rating power, which is complying with IEC61000-3-2 standards. Fig. 16 shows the power factor with the out power and it is always maintained about 0.999 over the load range of 2 kW.

VI. Conclusion

A three-phase five-level unidirectional rectifier is proposed in this study. It uses only three active switches and one FC per phase and their voltage-ratings are all one-fourth of the dc-link voltage. Compared with most existing similar five-level rectifiers, the number of active switching devices and floating capacitors has been reduced by 25% and 50%, respectively. Furthermore, the rectifier has the comprehensive merits in terms of the simple structure and higher power density of the system, because it uses less switch devices and FCs, which can be an attractive solution for the industry. All the mentioned advantages have been compared with the existing rectifiers. The 3 kW experimental prototype has been used to verify the effectiveness of the proposed rectifier. The power factor at the grid is found to be more than 0.997, and the efficiency more than 97.5%. Therefore, authors believe that these features make it a suitable topology for nonregenerative applications, such as EV charging pile systems, telecommunication power systems, and laser power systems.

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Wenyuan Zhang received the M.Sc. degree in electrical engineering from Guangxi University, Nanning, China, in 2017. He is currently working toward the Ph.D. degree in electrical engineering with the College of Electrical and Information Engineering, Hunan University, Changsha, China.

From 2017 to 2019, he was an Electrical Engineer with the CRRC Dalian R&D Company, Ltd. His research interests include digital control techniques, modulation strategies, topology research of multilevel converters, and renewable energy systems.

Xiaonan Zhu (Member, IEEE) was born in Henan, China, in 1995. He received the B.S. degree in electrical engineering from China University of Petroleum, Qingdao, China, in 2017, and the Ph.D. degree in electrical engineering from the College of Electrical and Information Engineering, Hunan University, Changsha, China, in 2022.

He is currently a Postdoctoral Researcher in electrical engineering with Hunan University. His research interests include the power converter design, analysis and modulation techniques, grid integration of renewable energy, and control algorithms in power electronics.

Hongliang Wang (Senior Member, IEEE) received the B.Sc. degree in electrical engineering from Anhui University of Science and Technology, Huainan, China, in 2004, and the Ph.D. degree in electrical engineering from Huazhong University of Science and Technology, Wuhan, China, in 2011.

From 2004 to 2005, he was an Electrical Engineer with the Zhejiang Hengdian Thermal Power Plant. From 2011 to 2013, he was a Senior System Engineer with the Sungrow Power Supply Company, Ltd. From 2013 to 2018, he was a Postdoctoral Fellow with Queen's University. Since 2018, he has been with Hunan University, Changsha, China, where he is currently a Full Professor with the College of Electrical and Information Engineering. He has authored more than 90 technical papers in the journals and conferences. He is the inventor/coinventor of 62 China issued patents and 14 U.S. issued patents. His research interests include multilevel topology, high-gain topology, parallel technology and virtual synchronous generator technology for photovoltaic application and microgrids application, resonant converters and server power supplies, and LED drivers.

Qing Li was born in Hunan, China, in 1998. She received the B.S. degree in electrical engineering and automation from Changsha University of Science and Technology, Changsha, China, in 2020. She is currently working toward the M.S. degree in electrical engineering with the College of Electrical and Information Engineering, Hunan University, Changsha, China.

Her research interests include multilevel converter topology, modulation techniques, control algorithms and design of converters in ac–dc and dc–dc fields.

Xiaojun Deng was born in Hunan, China, in 1997. He received the B.S. degree in electrical engineering from China University of Mining and Technology, Xuzhou, China, in 2019. He is currently working toward the Ph.D. degree in power electronics with the College of Electrical and Information Engineering, Hunan University, Changsha, China.

His research interests include multilevel converter topology, modulation techniques, and control algorithms for photovoltaic application and renewable energy system.

Hanzhe Wang received the B.S and M.S. degrees in electrical engineering from China University of Mining and Technology, Xuzhou, China, in 2016 and 2019, respectively. He is currently working toward the Ph.D. degree in power electronics with Hunan University, Changsha, China.

His research interests include digital control techniques, modulation strategies, multilevel topology of inverter for photovoltaic application and renewable energy systems control.

Xiumei Yue received the B.Sc. degree in electrical engineering from Anhui University of Science and Technology, Huainan, China, in 2004, and the M.Sc. degree in electrical engineering from Huazhong University of Science and Technology, Wuhan, China, in 2007.

From 2007 to 2011, she was with Hubei Polytechnic University. From 2011 to 2014, she was a Senior Intellectual Property Engineer with the Sungrow Power Supply Company, Ltd. From 2014 to 2017, she was with Queen's University, Kingston, ON, Canada. Since 2018, she has been with Hunan University, Changsha, China. Her research interests include converter topology and control technology and dc/ac converter.