A Parallel Resonant DC Link Inverter With Low Current Stress on Main Switch

Enhui Chu, Jiaxiang Song, and Hongquan Ni

***Abstract*—The resonant current of the resonant dc link inverter is superimposed on the main switch in periods of the zero-voltage notch creation, which increases the current stress as well as the conduction loss of the main switch, and inevitably escalates the selection cost of the main circuit. To solve these problems, a parallel resonant dc link inverter with low current stress on main switch is proposed in this article. The main switch of this inverter does not need parallel resonant capacitors, and it also ensures that the current of the main switch remains at the load current value during the whole resonance process or the zero-voltage notch, thus effectively reduces the current stress of the main switch, and thereby the hardware cost of the main circuit can be further diminished. At the same time, the conduction loss of the main switch is significantly decreased since the resonant current is no longer considered, thus improving the efficiency of the inverter. The operation principle of this circuit is analyzed and compared with existing literatures and the design method is also given in the article. Finally, the effectiveness of this resonant dc link inverter is experimentally verified.**

***Index Terms*—Auxiliary resonant circuit, current stress, main switch, parallel resonant dc link inverter, resonant capacitor.**

I. Introduction

INVERTERS occupy an important position in the fields of photovoltaic power generation and motor drive, etc. With the maturity of new energy technologies and the fast-speed advancement of power electronics, improving the waveform quality of inverters, improving system efficiency, and reducing system cost have received more and more attention. The soft-switching technology is applied extensively in the field of inverters for its advantages to effectively realize the reduction of switching losses of power electronic devices, the improvement of the harmonics for the inverter system output waveform, and the enhancement of the system efficiency [1], [2], [3]. Currently, there are two main types of soft-switching inverters that are more commonly utilized: auxiliary resonant poles [4], [5], [6], [7], [8], [9], [10], [11], [12] and auxiliary resonant dc link [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26]. The resonant dc link (Rdc-link) inverter has been the current focal research direction for experts in this field due to its characteristics of simpler structure, lower hardware cost, and higher system efficiency.

The Rdc-link soft-switching inverter was first introduced byDivan of the University of Wisconsin (now Georgia Tech) in 1989 [13], which has the advantages of low topological complexity and simple modulation strategy, but the higher voltage stress limits the reduction of switching losses, and the method is not compatible with the conventional pulsewidth modulation (PWM) inverter control strategy. Divan subsequently presented the active clamped Rdc-link inverter [14], which solved the mentioned problems, and since then the research of Rdc-link inverter has become a hot topic.

Due to the simplicity of the active clamped Rdc-link inverter topology, which is used in different applications, and many experts and scholars have proposed various improved modulation strategies based on this topology [15], [16]. However, its resonant inductor is present in the main circuit, and this not only increases the inductor losses, but also the resonant inductor tends to resonate with the parasitic parameters of the main circuit, thereby increasing the parasitic oscillation of the system. In order to remove the resonant inductor from the main circuit, a new Rdc-link inverter was proposed in [17] and [18], which adds an additional split capacitor on the dc side to achieve the purpose of eliminating the resonant inductor from the main circuit, but it leads to the dc side neutral point unbalance during the resonance process. The auxiliary resonant circuit proposed in [19] and [20] uses a coupled inductor and transformer, which also removes the resonant inductor out from the main circuit, while this auxiliary circuit is simpler. However, it should be noted that the design difficulty of the coupling inductor and the size and magnetic saturation of the transformer cannot be ignored. During soft switching, the resonant current is able to flow past the switch of the main circuit, which can contribute to increasing current stress as well as conduction losses of the main switch, and also bring about harmonic problems of the output waveform. With the aim of reducing the control complexity of the circuit and the design difficulty, the auxiliary resonant circuit proposed in [21] has neither coupling inductor nor transformer, and also its dc side has no split capacitor, but the capacitance of its auxiliary resonant circuit is still large, and its capacitance voltage needs to reach more than 1/2 to participate in resonance. To solve the drawbacks of the above literature, the auxiliary resonant circuit proposed in [22] avoids both the splitting capacitor and the coupling inductor, so its applications are more

Manuscript received 26 April 2023; revised 19 July 2023; accepted 19 August 2023. Date of publication 28 August 2023; date of current version 22 September 2023. This work was supported by the National Natural Science Foundation of China under Project 51977028. Recommended for publication by Associate Editor F. Azcondo. *(Corresponding author: Jiaxiang Song.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3308611.

Digital Object Identifier 10.1109/TPEL.2023.3308611

widespread, and the authors of this literature propose a variety of modulation strategies on this basis [23], [24], which makes the efficiency of the inverter improved. The Rdc-link inverters proposed in the above literatures all utilize the auxiliary circuit to create zero-voltage notch, as well as all of main switches are capable of completing switching during the zero-voltage notch. Nevertheless, during the resonance process and the holding of the zero-voltage notch, the resonant current is superimposed on the main switch, which leads to the current stress and the conduction loss increase for the main switch, and inevitably reduces the efficiency of the Rdc-link inverter and increases the hardware selection cost for the main circuit.

To address the above problems, the improved auxiliary circuit proposed in [25] solves the current stress problem within the period of the zero-voltage notch. However, it ignores the resonant current generated within its resonance period, since its main switch is in parallel with the resonant capacitor, so it cannot completely solve the main switch current stress problem because there is still part of the resonant current. For solving the current stress problem of the main switch for the Rdc-link inverter completely, this article proposes the Rdc-link inverter with low current stress of the main switch, which has the following advantages.

1) The main switch of the Rdc-link inverter proposed in this article does not require parallel resonant capacitors. The main circuit is identical to the traditional hard-switching inverter, and this auxiliary resonant circuit can be plug-and-play.
2) This Rdc-link inverter can solve the current stress problem of the main switch. Whether in the period of the zero-voltage notch or in the resonant process, the resonant current of this inverter does not flow pass the switch of the main circuit, so the current stress on the main switch always maintains the value as the load current, which can reduce the selection cost for the main switch.
3) The reduction of the current stress also decreases the conduction loss for the main switch during resonance process, which helps to further improve the efficiency of the Rdc-link inverter.
4) The inverter can not only ensure the soft switching operation of all switches, but also eliminates the need for high-capacity split capacitors, coupling inductors, and transformers in its auxiliary resonant circuit.

The rest of this article is organized as follows. The working principle of the parallel Rdc-link inverter is given in Section II. The characteristics analysis of the inverter is given in Section III. The design method and design principles are given in Section IV. Feasibility of the above principle is experimentally verified is given in Section V. Finally, Section VI concludes this article.

II. Circuit Topology and Working Principle

A. Circuit Topology and Basic Characteristics

Fig. 1 presents the parallel Rdc-link inverter proposed in this article, and the inverter mainly includes the auxiliary resonant circuit and the conventional PWM inverter. The main switch of this inverter does not require the parallel resonant capacitor.

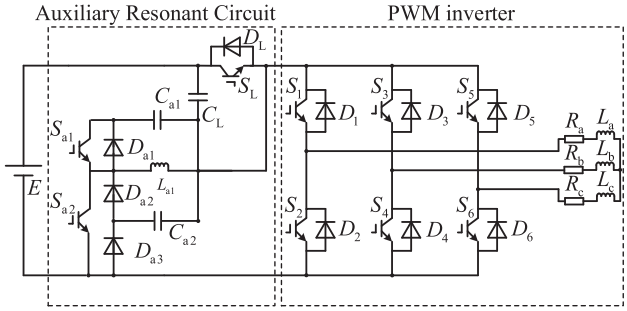

Fig. 1. RDC-link inverter of this article.

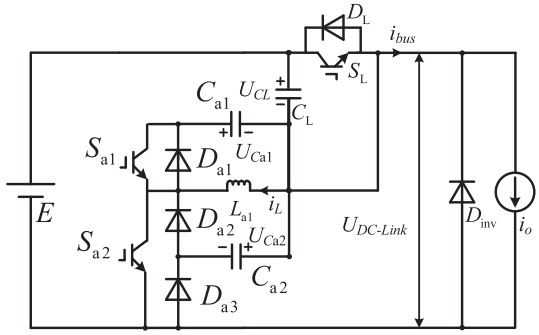

Fig. 2. Equivalent circuit of this RDC-link inverter.

The auxiliary resonant circuit mainly consists of three auxiliary switch, four diodes, three resonant capacitors and one resonant inductor. The auxiliary switches are: bus switch S_L; auxiliary switch S_{a1}; and auxiliary switch S_{a2}. Diodes are: diode D_{a1}; diode D_{a2}; diode D_{a3}; and diode D_L. Resonant components include: resonant capacitor C_{a1}; resonant capacitor C_L; resonant capacitor C_{a2}; and resonant inductor L_{a1}. Fig. 2 gives the equivalent circuit of this Rdc-link inverter, and the assumed direction for each component is marked. In Fig. 2, all diodes of the main circuit are equated to diode D_{inv} and the load is equated to D_{inv} and the others are equated to the current source i_{o}. $U_{\text{DC-Link}}$ denotes the dc-bus voltage and i_{bus} denotes the dc bus current.

B. Working Principles of This Resonant DC Link Inverter

Fig. 3 gives the operation waveforms of the component for the auxiliary circuit. In Fig. 3, t_{dead} is the dead time, at t_1 the bus switch S_L is turned OFF and the main switches start switching after T_1, at t_3 the auxiliary switch S_{a2} is turned OFF and the auxiliary switch S_{a1} is turned ON after T_2. at t_6 the auxiliary switch S_{a1} is turned OFF and the bus switch S_L is turned ON after T_3. Fig. 4 gives the corresponding equivalent circuit. Before analyzing the working principle of the inverter, it can be assumed in advance that all devices (switches, diodes) are ideal, while the current i_o of the inverter remains constant in the period of the zero- voltage notch, and the value of the resonant inductor L_{a1} is L, i.e., $L_{a1} = L$. The whole resonant process is as below.

1) *Process 0 [$\sim t_0$]:* The inverter bus switch S_L is always ON until the moment of t_0, and the load current of the inverter

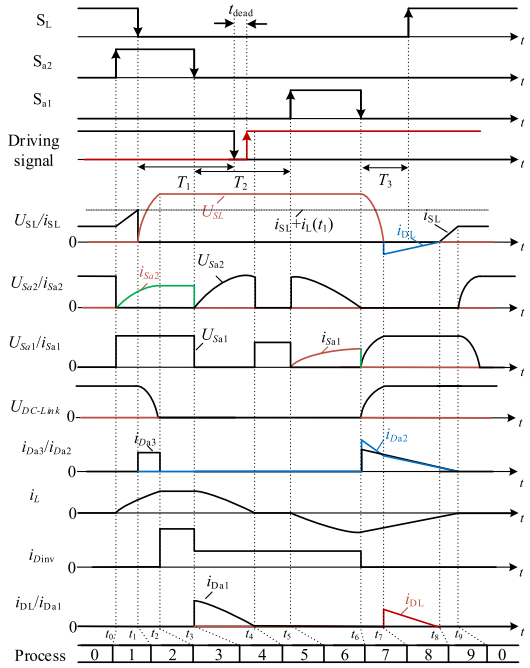

Fig. 3. Operation waveforms of auxiliary circuit switching devices.

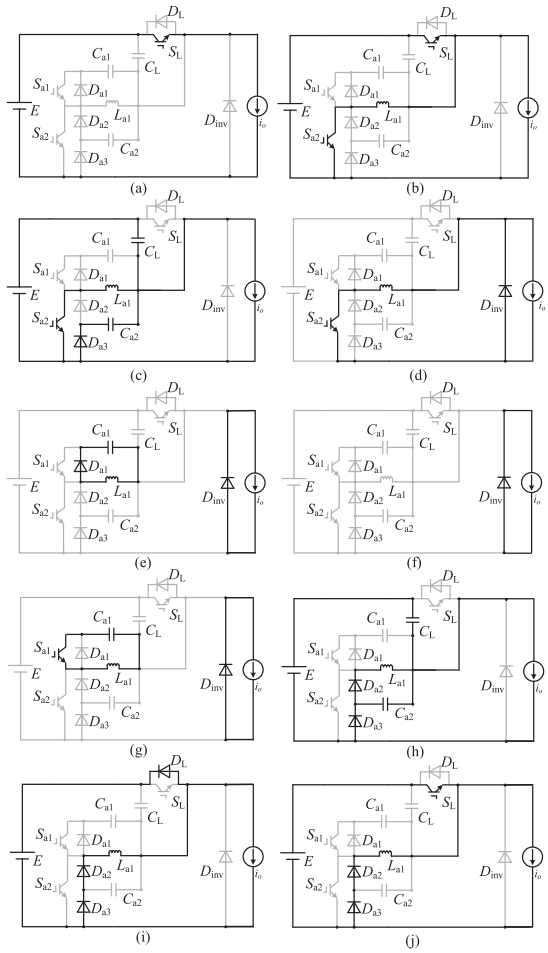

Fig. 4. Equivalent circuits of the whole resonant process. (a) Process 0. (b) Process 1. (c) Process 2. (d) Process 3. (e) Process 4. (f) Process 5. (g) Process 6. (h) Process 7. (i) Process 8. (j) Process 9.

flows via the main inverter through the bus switch S_L. The initial states of each resonant capacitor as well as resonant inductor in the auxiliary resonant circuit are $U_{CL}(t_0) = 0$, $U_{Ca1}(t_0) = 0$, $U_{Ca2}(t_0) = E$, and $i_L(t_0) = 0$. The bus current is $i_{bus} = i_o$.

2) *Process 1 [t_0, t_1]:* This process is an energy storage process. At the moment of t_0, the auxiliary switch S_{a2} is ON as well as the inductor L_{a1} absorbs energy, so the inductor current increases linearly. Under the influence of the resonant inductor L_{a1}, S_{a2} realizes quasi-zero current switching (QZCS) turn-ON. The process ends when the inductor current rises to $i_L(t_1)$. Under this process, currents flowing through the resonant inductor L_{a1} and the bus switch S_L are

$$i_L(t) = \frac{E}{L} \cdot t \tag{1}$$

$$i_{SL}(t) = \frac{E}{L} \cdot t + i_o. \tag{2}$$

The bus current i_{bus} under process 1 is

$$i_{\text{bus}} = i_{SL} - i_L = i_o \tag{3}$$

3) *Process 2 [t_1, t_2]:* At t_1, the inductor current rises to $i_L(t_1)$ and bus switch S_L is OFF, diode D_{a3} conducts. the resonant inductor L_{a1} resonates with resonant capacitors C_L and C_{a2}, C_L is charged, capacitor C_{a2} is discharged. S_L can realize quasi-zero voltage switching (QZVS) turn-OFF under the influence of capacitor C_L. and When capacitor C_L is charged to E, resonance ends. The currents flowing through inductor L_{a1} and capacitors C_L and C_{a2} in this mode are as follows:

$$i_{CL}(t) = C_L \omega E \sin \omega t + C_L \omega^2 L \left(i_L(t_1) + i_{\text{o}}\right) \cos \omega t \tag{4}$$

$$i_{Ca2}(t) = -C_{a2} \left(\omega E \sin \omega t + \omega^2 L (i_L(t_1) + i_{\text{o}}) \cos \omega t\right) \tag{5}$$

$$i_L(t) = \frac{E}{\omega L} \sin \omega t + \left(i_L(t_1) + i_{\text{o}}\right) \cos \omega t - i_{\text{o}}. \tag{6}$$

The voltages of capacitors C_L and C_{a2} in this mode are as follows:

$$U_{Ca2}(t) = E \cos \omega t - \omega L \left(i_L(t_1) + i_{\text{o}}\right) \sin \omega t \tag{7}$$

$$U_{CL}(t) = E - E \cos \omega t + \omega L \left(i_L(t_1) + i_{\text{o}}\right) \sin \omega t. \tag{8}$$

At t_2, the voltage across the resonant capacitor C_L is charged to E, process 2 is done. The value of inductor current at t_2 is

$$i_L(t_2) = \sqrt{\left(\frac{E}{\omega L}\right)^2 + \left(i_{\text{o}} + i_L(t_1)\right)^2} - i_{\text{o}}. \tag{9}$$

From (8), the duration $t_{1\text{-}2}$ of this process is

$$t_{1-2} = \frac{1}{\omega} \cdot \arctan \frac{E}{\omega L \left(i_L(t_1) + i_o\right)} \tag{10}$$

where the resonant angular frequency is

$$\omega = \frac{1}{\sqrt{L(C_L + C_{a2})}}.$$

This process provides energy to the load to ensure the constant load current i_o, and while at the same time the bus current i_{bus} remains the load current i_o in this process.

4) *Process 3 [t_2, t_3]:* This process is the circulating process. At t_2, the capacitor C_L is charged to E, the inductor current reaches its maximum value, the diode D_{a3} is OFF, D_{inv} turns ON and the resonance ends. The inductor current in this mode circulates within S_{a2}- D_{inv}- L_{a1}, while the load current i_o is freewheeling via D_{inv}. Until S_{a2} is turned OFF, process 3 ends.

The bus current i_{bus} in this process is

$$i_{\text{bus}} = -\sqrt{\left(\frac{E}{\omega L}\right)^2 + \left(i_o + i_L(t_1)\right)^2} + i_o. \tag{11}$$

5) *Process 4 [t_3, t_4]:* At t_3, the auxiliary switch S_{a2} is turned OFF, D_{a1} conducts, the resonant inductor L_{a1} is in resonance with the resonant capacitor C_{a1}, and the residual energy stored in L_{a1} is transferred to C_{a1}. Under the influence of C_{a1}, S_{a2} can achieve QZVS turn-OFF. The process ends when the residual energy of L_{a1} is 0. That is, once the resonant current drops to zero, the diode D_{a1} is naturally OFF. The mathematical expressions for the current i_L of $L_{a1}$and the voltage of capacitor C_{a1} during this process are

$$i_L(t) = i_L(t_2)\cos\omega_1 t \tag{12}$$

$$U_{Ca1}(t) = \omega_1 L i_L(t_2)\sin\omega_1 t \tag{13}$$

where the resonant angular frequency of the circuit is

$$\omega_1 = \frac{1}{\sqrt{LC_{a1}}}.$$

The duration of the process $t_{3\text{-}4}$ is

$$t_{3-4} = \frac{\pi}{2\omega_1}. \tag{14}$$

The bus current i_{bus} is 0 in this process, and the load current is continued through D_{inv}.

6) *Process 5 [t_4, t_5]:* At t_4, the residual energy of the inductor is 0, and all components of the auxiliary circuit are inactive at this time. The bus current i_{bus} is 0 in this process, and the load current i_o is continued through D_{inv}. This process ends when S_{a1} is ON. According to (13), the voltage across the resonant capacitor C_{a1} is $\omega_1 L i_L(t_2)$ at t_4.

7) *Process 6 [t_5, t_6]:* At the moment of t_5, S_{a1} is turned ON and the resonant inductor L_{a1} is in resonance with the resonant capacitor C_{a1}. The remaining energy in the resonant capacitor is transferred to L_{a1} to ensure that there is enough energy is available in the resonant inductor for the subsequent resonance. The inductor L_{a1} absorbs energy, so the current of inductor L_{a1} rises from zero in this process, S_{a1} can achieve QZCS turn-ON. The mathematical expressions for the current through L_{a1} and the voltage across capacitor C_{a1} during this process are as follows:

$$U_{Ca1}(t) = \omega_1 L i_L(t_2)\cos\omega_1 t \tag{15}$$

$$i_L(t) = -C_{a1}\omega_1^2 L i_L(t_2)\sin\omega_1 t. \tag{16}$$

The bus current i_{bus} is 0 in this process. This process ends until the capacitor C_{a1} is discharged to 0.

The duration of this process $t_{5\text{-}6}$ is

$$t_{5-6} = \frac{\pi}{2\omega_1}. \tag{17}$$

It is worth noting that the dc-bus voltage $U_{\text{DC-link}}$ is always 0 between processes 3 and 6, so the main switch can accomplish switching in either process. The main switch can realize ZVS switching.

8) *Process 7 [t_6, t_7]:* At t_6, S_{a1} is OFF, diodes D_{a2} and D_{a3} conduct. The resonant inductor L_{a1} starts resonating with resonant capacitors C_L and C_{a2}, while C_L is discharged, C_{a2} is charged. Under the influence of resonant capacitor, S_{a1} achieves QZVS turn-OFF. When capacitor C_L is discharged to 0, resonance ends. The currents flowing through inductor L_{a1} as well as capacitors C_L and C_{a2} in this process are as follows:

$$i_L(t) = \left(i_o - C_{a1}\omega_1^2 L i_L(t_2)\right)\cos\omega t - i_o \tag{18}$$

$$i_{Ca2}(t) = C_{a2}L\omega^2\left(i_o - C_{a1}\omega_1^2 L i_L(t_2)\right)\cos\omega t \tag{19}$$

$$i_{CL}(t)\cdot C_L = L\omega^2\left(i_o - C_{a1}\omega_1^2 L i_L(t_2)\right)\cos\omega t. \tag{20}$$

The voltages across capacitors C_L and C_{a2} in this process are as follows:

$$U_{Ca2}(t) = -L\omega\left(i_o - C_{a1}\omega_1^2 L i_L(t_2)\right)\sin\omega t \tag{21}$$

$$U_{CL}(t) = E + L\omega\left(i_o - C_{a1}\omega_1^2 L i_L(t_2)\right)\sin\omega t. \tag{22}$$

The duration of this process $t_{6\text{-}7}$ is

$$t_{6-7} = \frac{1}{\omega}\arcsin\frac{E}{L\omega\left(i_o - C_{a1}\omega_1^2 L i_L(t_2)\right)}. \tag{23}$$

This process is similar to process 2 and this process provides energy to the load to ensure that the load current i_o remains constant, while at the same time the bus current i_{bus} remains i_o in this process.

9) *Process 8 [t_7, t_8]:* This process is the energy return process. At t_7, the capacitor C_L is discharged to 0 and the resonance ends. At this time, L_{a1} feeds the remaining energy back to E through D_L, so the inductor current decreases linearly. During this process, bus switch S_L is ON, and S_L can achieve ZVS turn-ON. This process ends until the inductor current drops to -i_o. The inductor current in this process is

$$i_L(t) = i_L(t_7) - \frac{E}{L}t. \tag{24}$$

It should be noted that the inductor energy in this process is not only supplied to the power supply E, but also to the load to keep i_o constant, thus the bus current $i_{\rm bus}$ in this process is always i_o. This process ends when i_L drops to -i_o, and the duration of this process $t_{7\text{-}8}$ is

$$t_{7-8} = L\frac{i_L(t_7) - i_o}{E}. \tag{25}$$

10) *Process 9 [t_8, t_9]:* At t_8, i_L drops to -i_o, and the residual energy in the inductor L_{a1} is no longer fed back to the power supply E, but flows to the load. The current of bus switch S_L increases slowly in this process, and the inductor energy continues to drop, and when the residual energy of L_{a1} drops to 0, the diodes D_{a2} and D_{a3} turn OFF naturally, and process 9 ends. The currents flowing through S_L and the resonant inductor L_{a1} in this process are as follows:

$$i_L(t) = -i_{\rm o} + \frac{E}{L}t \tag{26}$$

$$i_{\rm SL}(t) = \frac{E}{L}t. \tag{27}$$

According to (26) and (27), the bus current $i_{\rm bus}$ in this process is

$$i_{\rm bus} = i_{SL} - i_L(t) = i_o. \tag{28}$$

Therefore, the duration of this process $t_{8\text{-}9}$ is

$$t_{8-9} = \frac{Li_{\rm o}}{E}. \tag{29}$$

At the moment of t_9, the residual energy of L_{a1} drops to 0, diodes D_{a2} and D_{a3} turn OFF naturally, and the operating process for the full switching cycle ends.

C. Discussion of Main Switch Current Stress

From the above theoretical analysis, it can be recognized that the current that flows past the main switch remains at the load current value in period of the whole soft-switching process for the proposed Rdc-link inverter in this article.

For the proposed Rdc-link inverter in this article, processes 2 and 7 are resonant process, and process 3– process 6 are the holding of zero-voltage notch. Combined with the above-mentioned mode analysis, the current of the main switch is constantly equal to the load current, both in the resonant process and the holding of zero-voltage notch

$$i_{S1} = i_o. \tag{30}$$

The resonance process of different circuits is given in Fig. 5. As shown in Fig. 5(a), process 7 is its resonant process, because the inductor L_{r1} resonates with the shunt resonant capacitor of the main switch, so its resonant current will flow past the switch, and the current flowing through S_1 at this time is

$$i_{S1} = i_o + (i_{Lr\rm MAX} - i_0)\cos\omega_2(t - t_6) \tag{31}$$

where $i_{Lr\rm MAX}$ is the maximum resonant current in [25] and ω_2 is the corresponding angular resonant frequency. i_o is the load current, $i_{Lr\rm MAX}$ is higher than the maximum load current, i.e.,: $i_{Lr\rm MAX} > i_{o\rm MAX}$.

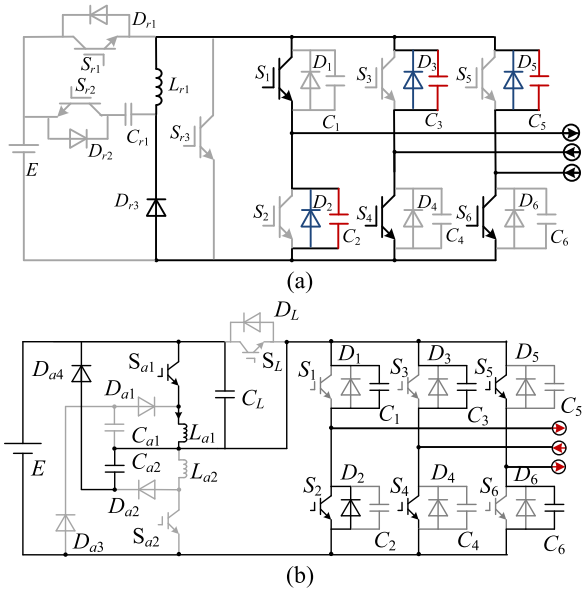

Fig. 5. Resonant process in different circuits. (a) Process 7 in [25]. (b) Process 6 in [24].

The main switch of the inverter proposed in [24] also needs to be connected in parallel with the resonant capacitor [see Fig. 5(b)], so the current in the main switch during resonance is the superposition of the load current and the resonant current

$$i_{S1} = i_o + \frac{C_a}{2C_a + C_b} \cdot \frac{E}{\omega_1 L}\sin\omega_1 t \tag{32}$$

where L is the resonant inductor in [24], ω_1 is the resonant angular frequency, C_a and C_b are the resonant capacitors, respectively.

Therefore, the current flowing through the main switch is constantly equal to the load current, the current flowing through the main switch in [24] and [25] is the superposition of the load current and the resonant current. it is concluded that the proposed resonant dc link inverter solves the current stress problem of the main switch (which exists in the existing literature).

III. Characterization of Resonant DC Link Inverter

A. Soft-Switching Boundary Conditions of Switches

Soft switching of all the switches must be ensured by the soft switching inverter before it makes sense, so this section combines the above analysis of the working principle with the soft-switching conditions of the switches.

1) To ensure the ZVS turn-ON of the main switch, the delay time T_1 should be greater than the maximum charging time of the bus capacitor C_L in process 2, and should not exceed the minimum energy release time of the inductor in process 4. T_1 should satisfy

$$t_{1-2(\max)} + t_{2-3(\min)} + t_{3-4(\min)} > T_1 \geq t_{1-2(\max)}. \tag{33}$$

TABLE I
CHARACTERISTIC COMPARISON OF DIFFERENT CIRCUITS

Auxiliary resonant circuit	[19]		[22]		[25]		This paper	
Auxiliary switch	2		3		3		3	
Diode	2		5		3		4	
Resonant capacitor	2		9		7		3	
Resonant inductor	2 (Coupling inductor)		2		1		1	
Total	8		19		14		11	
Soft-switching	Turn-on	Turn-off	Turn-on	Turn-off	Turn-on	Turn-off	Turn-on	Turn-off
Main switch	ZVS	ZVS	ZVS	ZVS	ZVS	ZVS	ZVS	ZVS
Auxiliary switch	QZCS	QZVS	QZCS	QZVS	QZCS	QZVS	QZCS	QZVS
Current stress	Maximum Current		Maximum Current		Maximum Current		Maximum Current	
Auxiliary switch	I_{omax}+I_{res}		I_{omax}+I_{res}		I_{omax}+I_{res}		I_{omax}+I_{res}	
Main switch	I_{omax}+I_{res}		I_{omax}+I_{res}		I_{omax}+I_{res}		I_{omax}	

2) To ensure that the bus switch S_L achieves ZVS turn-ON, the delay time T_3 should be greater than the maximum discharge time of the bus capacitor C_L, and it should also be less than the time of the minimum release of energy from the inductor in process 8. T_3 should satisfy

$$t_{6-7(\max)} + t_{7-8(\min)} > T_3 > t_{6-7(\max)}. \tag{34}$$

B. Di/Dt *and* Dv/Dt *of Switches*

The auxiliary switch S_{a2} is connected in series with the resonant inductor, so when S_{a2} is turned ON, the resonant inductor current is the current flowing through S_{a2}. From (1), it can be seen that the changing rate of current *di/dt* when S_{a2} is turned ON is

$$\frac{di_{Sa2}}{dt} = \frac{E}{L}. \tag{35}$$

From (2), it can be seen that the changing rate of current *di/dt* flowing through bus switch S_L when S_{a2} is turned ON is

$$\frac{di_{SL}}{dt} = \frac{E}{L}. \tag{36}$$

From (16), it can be seen that the changing rate of current *di/dt* when S_{a1} is turned ON is

$$\frac{di_{Sa1}}{dt} = -C_{a1}\omega_1^3 L i_L(t_2)\cos\omega_1 t. \tag{37}$$

As the resonant capacitor C_L is connected in parallel with bus switch S_L, the changing rate of voltage *dU/dt* when the bus switch S_L is turned OFF can be seen from (8) as

$$\frac{dU_{SL}}{dt} = \omega E\sin\omega t + \omega^2 L\left(i_L(t_1) + i_o\right)\cos\omega t. \tag{38}$$

When the auxiliary switch S_{a1} is turned OFF, the changing rate of voltage *dU/dt* can be seen from (21) as

$$\frac{dU_{Sa1}}{dt} = L\omega^2\left(i_o - C_{a1}\omega_1^2 L i_L(t_2)\right)\cos\omega t. \tag{39}$$

When the auxiliary switch S_{a2} is turned OFF, the changing rate of voltage *dU/dt* can be seen from (13) as

$$\frac{dU_{Sa2}}{dt} = L\omega_1^2 i_L(t_2)\cos\omega_1 t. \tag{40}$$

According to the (35), (36), (37), (38), (39), and (40) can be seen, When the voltage E, load current i_o and the changing rate of the voltage and current are given, the parameters of the resonant element can also be determined simultaneously.

Table I compares the soft-switching inverter proposed in this article with those in [19], [22], and [25]. $I_{o\max}$ is the maximum load current, $I_{\rm res}$ is the maximum resonant current. From Table I, it is apparent that this soft-switching inverter and the soft-switching inverters of [19], [22], and [25] can realize soft switching for all switches, however, they differ in terms of topology and loss and stress. In terms of the auxiliary resonant circuit, the soft-switching inverter of [19] has fewer switches, but its auxiliary switch needs to be operated twice during a single zero-voltage notch. Meanwhile, the voltage stress of its auxiliary switch is higher, so the losses of the auxiliary resonant circuit are not dominant. It is worth noting that its auxiliary resonant circuit contains coupling inductors, and the size, design difficulty, and losses of the coupling inductors also limit the application of this inverter. The auxiliary resonant circuits of [22] and [25] use more devices, both of them require resonant capacitors connected in parallel to the main switch. In relation to the main circuit, Wang et al. [19] and Chu et al. [22] indicate that the main switch carries resonant current not only during the resonant process but also during the zero-voltage notch, which increases the current stress and the conduction loss for the main switch. The resonant current flows through the main switch during resonance in [25], which cannot completely address the current stress problem of the main switch. The soft-switching inverter proposed in this article has no resonant current flowing through the main switch either during the zero-voltage notch or resonance process, which reduces the current stress and conduction loss of the main switch and can further improve the efficiency of the inverter.

IV. Parameter Design

A. Design Principles of This Inverter

When designing system parameters, it is crucial to take into stresses, losses, and other factors, so the parameter design for the circuit should meet the following points.

1) The operation of auxiliary switch Sa2 should satisfy (33).
2) The operation of the main switch should satisfy (33).
3) The duration of process 8 should satisfy (34).
4) Selection of resonant capacitors CL, Ca1, Ca2.

With the aim of reducing the turn-OFF loss of S_L, the changing rate of the voltage $(dU_{SL}/dt)_{\text{set}}$ after S_L is turned OFF should satisfy

$$\omega E \sin \omega t + \omega^2 L(i_L(t_1) + i_o) \cos \omega t \le \left(\frac{dU_{SL}}{dt}\right)_{\text{set}}. \quad (41)$$

With the aim of reducing the turn-OFF loss of S_{a1}, the changing rate of the voltage $(dU_{Sa1}/dt)_{\text{set}}$ after S_{a1} is turned OFF should satisfy

$$L\omega^2 \left(i_o - C_{a1}\omega_1^2 L i_L(t_2)\right) \cos \omega t \le \left(\frac{dU_{Sa1}}{dt}\right)_{\text{set}}. \quad (42)$$

With the aim of reducing the turn-OFF loss of S_{a2}, the changing rate of the voltage $(dU_{Sa2}/dt)_{\text{set}}$ after S_{a2} is turned OFF should satisfy

$$L\omega_1^2 i_L(t_2) \cos \omega_1 t \le \left(\frac{dU_{Sa2}}{dt}\right)_{\text{set}}. \quad (43)$$

5) Selection of the inductor L_{a1}

With the aim of reducing the turn-ON loss of S_{a2}, the changing rate of its current $(di_{Sa2}/dt)_{\text{set}}$ should satisfy

$$\frac{E}{L} \le \left(\frac{di_{Sa2}}{dt}\right)_{\text{set}}. \quad (44)$$

With the aim of reducing the turn-ON loss of S_{a1}, the changing rate of its current $(di_{Sa1}/dt)_{\text{set}}$ should satisfy

$$-C_{a1}\omega_1^3 L i_L(t_2) \cos \omega_1 t \le \left(\frac{di_{Sa1}}{dt}\right)_{\text{set}}. \quad (45)$$

B. Design Example of This Inverter

In order to conduct experimental tests to verify the above theoretical analysis, the inverter dc supply voltage $E = 400$ V and the maximum output load current $I_{o\max} = 50$ A are used as an example for equipment parameter selection. Set the voltage rise rate $(dU/dt)_{\text{set}} = 2000$ V/μs after the switch is turned OFF and the current rise rate $(di/dt)_{\text{set}} = 50$ A/μs after the switch is turned ON.

Substituting $E = 400$ V, $(di/dt)_{\text{set}} = 50$ A/μs into (44), it is evident that the resonant inductor L_{a1} should satisfy: $L \ge 8$ μH, so take $L = 10$ μH. To ensure the smooth operation of the whole resonance, let the duration time of process 1 be 1.5 us, according to (1): $i_L(t_1) = 60$ A. Substituting $(dU/dt)_{\text{set}} = 2000$ V/μs, $i_L(t_1) = 60$ A into (41), it can be seen that $C_L + C_{a2} \ge 51.77$ nF, so take $C_L = C_{a2} = 30$ nF. Substituting the above parameters into (9), it can see that $i_L(t_2) = 60.4$ A. According to (42), it can see that $C_{a1} \ge 152$ nF, so take $C_{a1} = 200$ nF.

TABLE II
Devices and Parameters of the Experimental Circuit

Components	Parameters of the inverter
Control Panel	FPGA- EP4CE10E22C8
Driver board	2SC0108T2G0-17
Input DC voltage E	400V
Switching frequency f_s	20 kHz
S_1-S_6	FF100R06ME3 (100 A)
S_L, S_{a1}, S_{a2}	FF200R06ME3 (200 A)
D_{a2}~D_{a3}	DSEI2X101-06A (2*96A)
C_L, C_{a1}	30 nF
C_{a2}	200 nF
L_{a1}	10 μH

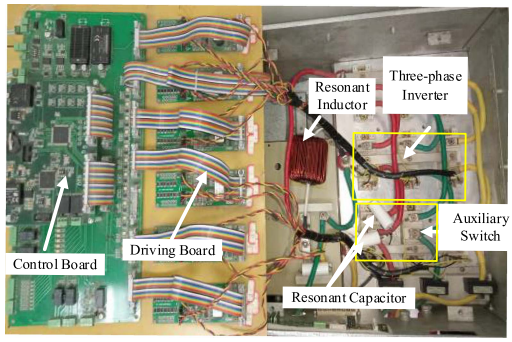

Fig. 6. Photograph of this experimental circuit.

V. Experimental Results

To verify the analysis results of this Rdc-link inverter, a 5 kW/20 kHz soft switching inverter prototype was built for experimental verification. Table II gives the prototype devices and parameters. Fig. 6 shows the photo of this experimental circuit.

Fig. 7 gives the experimental waveforms of bus switch S_L. From Fig. 7, it is clear that the bus switch S_L can realize ZVS turn-ON as well as QZVS turn-OFF. Fig. 8 gives the experimental waveform of the main switch. From Fig. 8, it can be seen that the main switch is switched during the zero-voltage notch, so that ZVS turn-ON and ZVS turn-OFF can be achieved. Fig. 9 gives the experimental waveform of the auxiliary switch S_{a1}. From Fig. 9, it is clear that the auxiliary switch S_{a1} achieves QZCS turn-ON and QZVS turn-OFF. Fig. 10 gives the experimental waveform of auxiliary switch S_{a2}. From Fig. 10, it is clear that the auxiliary switch S_{a2} achieves QZCS

A. Experimental Waveforms

Turn-ON and QZVS turn-OFF. Figs. 7–10 verify the above operating principle, so all the switches of this inverter can achieve

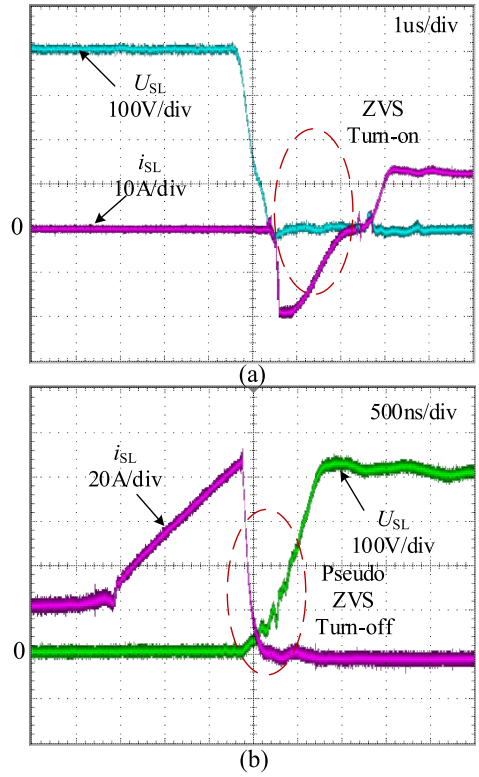

Fig. 7. Experimental waveforms of the bus switch S_L. (a) Turn-ON waveform of S_L. (b) Turn-OFF waveform of S_L.

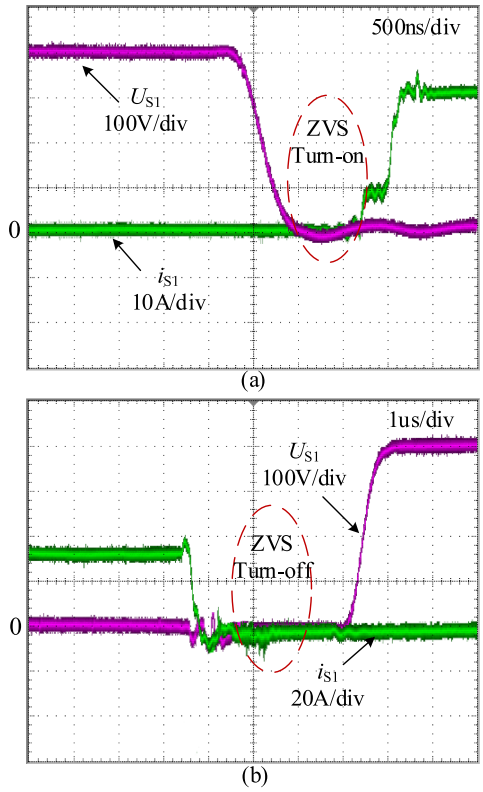

Fig. 8. Experimental waveforms of the main switch S_1. (a) Turn-ON waveform of S_1. (b) Turn-OFF waveform of S_1.

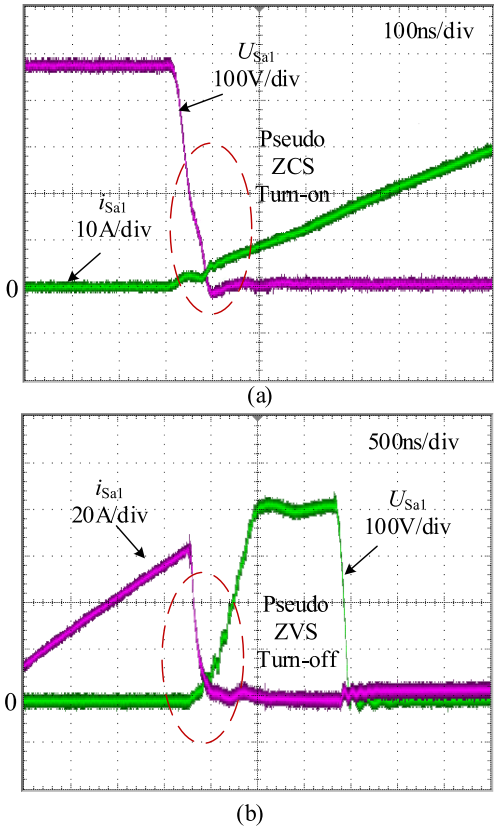

Fig. 9. Experimental waveforms of the auxiliary switch S_{a1}. (a) Turn-ON waveform of S_{a1}. (b) Turn-OFF waveform of S_{a1}.

soft switching. Fig. 11 gives the bus current waveform and the waveform of the zero-voltage notch. Combining the above theoretical analysis and Fig. 11, it is clear that the $U_{\mathrm{DC\text{-}Link}}$ voltage resonance drops to zero in process 2, however, the bus current i_{bus} is constant at this time, the energy of the resonant element is supplied to the load in this process to keep the current i_o constant. The bus current i_{bus} is negative in process 3, so it does not flow through the switch. During process 4–process 6, the bus current is 0. The main switch completes switching in this phase. During process 7–process 9, the bus current remains at the load current i_o, so there is no resonant current flowing through the main switch in the whole soft switching process, and the current of the main switch is always i_o.

The current waveforms of the main switch under the inverter proposed in this article and the inverter proposed in [25] are given in Fig. 12. Combining Fig. 5 and (31), it can be obtained that during the resonance process of the Rdc-link inverter proposed in [25], the resonant current still flows through the main switch when the resonant inductor resonates with the resonant capacitor because the main switch is connected in parallel with the resonant capacitor. As the maximum load current is 50 A, the resonant current is about 52 A, the current for the main switch at this time is 102 A, which is about twice the load current. The increase in current stress leads to higher losses in the main switch and higher hardware costs.

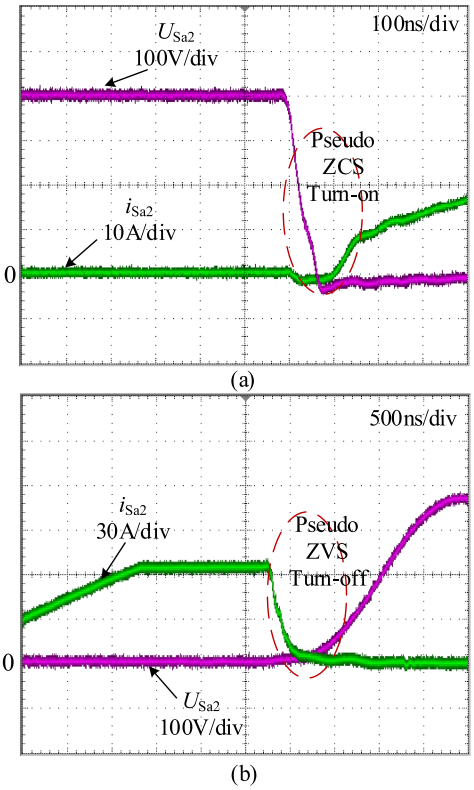

Fig. 10. Experimental waveforms of the auxiliary switch S_{a2}. (a) Turn-ON waveform of S_{a2}. (b) Turn-OFF waveform of S_{a2}.

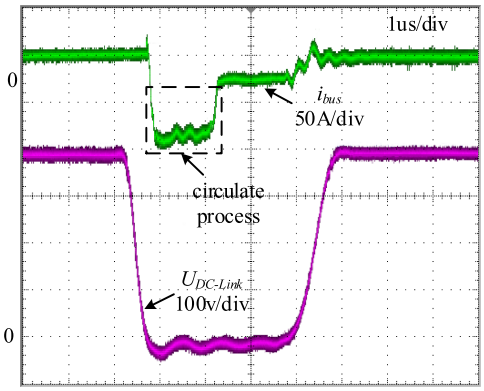

Fig. 11. Waveforms of the bus current and the zero-voltage notch.

Combining with the above theoretical analysis, it is clear that the main switch of this inverter does not require parallel resonant capacitors, thus the current of the main switch remains at i_o. In Fig. 12, although there is resonant current flowing through the main circuit, it is in the circulating process in process 3, with negative current flowing past the anti-parallel diode of the main circuit rather than past the main switch (see process 3). Therefore, this main switch does not flow through the resonant current. Compared with [25], this inverter greatly reduces the main switch current stress, reduces the main circuit conduction loss, and reduces the hardware cost of the switch.

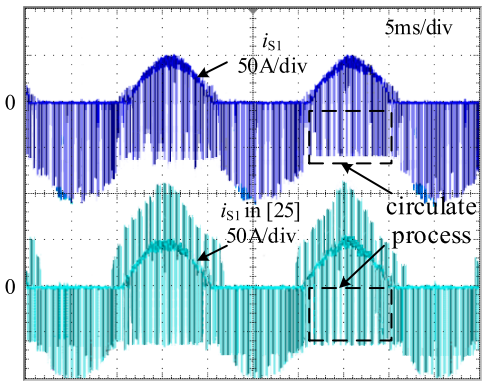

Fig. 12. Main switch current of the inverter proposed in this article and [25].

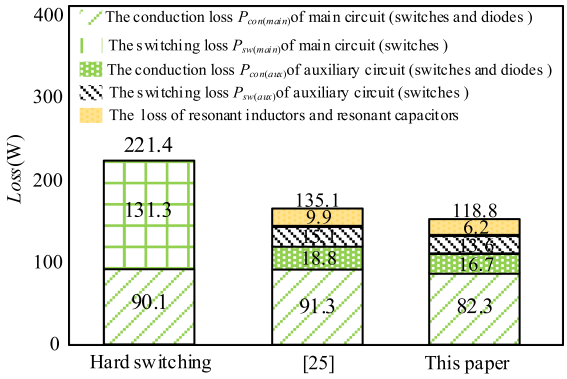

Fig. 13. Theoretical loss distribution.

B. *Efficiency Evaluation*

Theoretical loss calculation formulas are given in [23], [24], and [25], and in this experiment, the theoretical loss calculation formula given in [25] is used for comparison with [25]. Fig. 13 shows the theoretical loss distribution for different inverters at rated output of 5 kW. According to Fig. 13, the losses for the hard-switching inverter at 5 kW are 221.4 W, with the conduction losses of 90.1 W and switching losses of 131.3 W. The efficiency is 95.57%. It is important to note that the conduction loss for the switch does not diminish by the soft switching technique, the conduction loss is related to the power device itself. The loss distribution given in [25] ignores the loss of the resonant element, and since the main switch of this inverter does not require parallel resonant capacitors, the loss of the relevant resonant element is added in this article. From [25], It is well known that during resonance, its resonant current flows past the main switch, thus increasing the conduction loss for the main switch, so the conduction loss under [25] is 1.2 W higher than hard-switching inverter. The main switch can realize ZVS turn-ON and ZVS turn-OFF, so the switching loss for the switch is 0. However, the auxiliary resonant circuit also generates losses, and the switching loss of the auxiliary switch is 15.1 W, the conduction loss is 18.8 W, and the loss of the resonant element is 9.9 W. The total loss of [25] is 135.1 W, and the output efficiency is 97.29%. This inverter reduces the number of capacitors of

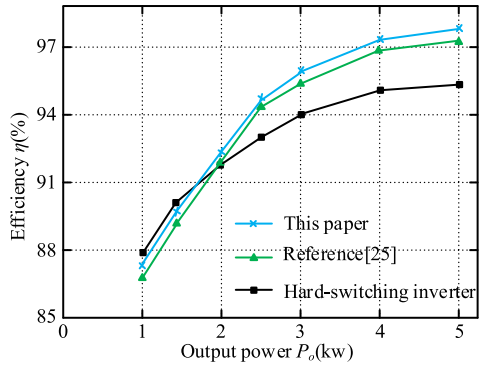

Fig. 14. Efficiency curves of the inverters.

the main switch, and therefore also reduces the losses of the resonant elements in the resonance process. However, there is still a small loss in the main circuit as the resonant current will flow past the diode during process 3. The total loss for this inverter is 118.8 W, the switch conduction loss is 82.3 W, the conduction loss for auxiliary switch is 16.7 W, the switching loss for auxiliary switch is 13.6 W, the loss for the resonant element is 6.2 W. The efficiency is 97.62%.

The experimental efficiencies of the inverters are given in Fig. 14, where the blue line indicates the inverter proposed in this article, the red line is the inverter proposed in [25], and the black line is the hard-switching inverter. At a rated output power of 5 kW, the actual output efficiency for the hard- switching inverter is 95.56%, basically consistent with the above theoretical calculation. The actual output efficiency of [25] is 97.27%. The actual efficiency of this soft-switching inverter is 97.575%, which is 0.305% more than that of [25] and 2.015% higher than hard-switching inverter. At light load output, the actual output efficiency for the Rdc-link inverter is lower than hard-switching inverter, which is because at low power output, the current for the inverter is lower and the corresponding switching losses are also lower. At this point, the losses for the auxiliary resonant circuit are higher than the switching losses of the switch, so the efficiency is slightly lower than hard-switching inverter. However, this inverter can decrease the switch current stress and reduce the hardware cost as well as conduction losses, so the efficiency for this inverter is still superior than the Rdc-link inverter proposed in [25], reflecting the advantage of this inverter under full load.

VI. Conclusion

In this article, a parallel Rdc-link inverter is proposed with low main switch current stress. Combining the above theoretical analysis and experimental results, the following conclusions can be drawn.

1) This parallel Rdc-link inverter can realize the soft switching of all switches, while there are no coupling inductors or transformers in auxiliary circuit, and no large-capacity split capacitors at dc side, so that the soft-switching process does not cause the midpoint voltage unbalance problem.
2) In this inverter, the current of the main switch remains always the load current, and the resonant current of this inverter does not flow to the main switch either the resonance process or in the period of the zero-voltage notch. So, the main switch current stress is reduced.
3) The reduction of the switch current stress can further reduce the switch conduction loss, thus improving the system efficiency of the inverter.
4) The main switch of this inverter does not require parallel resonant capacitors, so no resonant current passes through the main switch during resonance, which solves the problem of current stress on the switch caused by the resonance process.

In the future, the inverter can be used in motor drives as well as photovoltaic grid-connections, etc. Although this inverter solves the superposition relationship between the resonant current of the auxiliary circuit and the load current of the main switch. However, how to further reduce the cost and loss of auxiliary circuits on this basis is the key to research.

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