# Letters

## A Dynamic Smooth Transition Control Integrated With Hybrid Modulation for Wide Output Voltage Range Bidirectional CLLC Resonant Converters

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***Abstract*—The objective of this letter is to propose a dynamic smooth transition control (DSTC) integrated with hybrid modulation for wide output voltage range bidirectional *CLLC* resonant converters. Traditionally, the pulse frequency modulation (PFM) technique is adopted for *CLLC* resonant converters. However, under the low output voltage and light load condition, the PFM control might be failed because of the parasitic effect under high-frequency operation. To solve this issue, the phase-shift modulation (PSM) can be included to achieve wide output voltage range and full load operation. Therefore, the hybrid modulation integrated with PFM and PSM is utilized in this letter. Moreover, in order to suppress the voltage fluctuation and to reduce the response time during the mode switching transient, a DSTC is proposed in this letter. The proposed control can be implemented by the digital signal processor without adding extra circuit and components. Finally, a 2-kW prototype *CLLC* resonant converter is built to verify the performance and feasibility of the proposed circuit and control strategy. Experimental results show that the peak circuit conversion efficiency is 96.7%, whereas the improvement of the voltage fluctuation and the transient response time during the mode switching are equal to 50% and 42%, respectively.**

***Index Terms*—Bidirectional power flow, CLLC resonant converter, hybrid modulation, smooth transition.**

### I. Introduction

IN ORDER to achieve carbon neutral and net zero emission, electric vehicles (EVs) have been rapidly developed in recent years. The battery charger is an essential component in the EV system, whereas it is realized by power electronic technologies [1]. Generally, the battery charger consists of a two-stage structure, including a front-end ac–dc power factor corrector (PFC) and a rear-end dc–dc converter. The PFC circuit should be installed between the power grid and the dc-link. Main purposes of PFCs are to convert the power from ac to dc, and to correct the power factor. On the other hand, the dc–dc converter is included between the dc-link and the load/battery. Under normal condition, the dc–dc converter transfers the power from the dc-link and control the voltage and current of the load/battery. In this case, the battery charger achieves grid-to-vehicle (G2V) scenario. However, in order to regulate the power quality of the electric grid, the dc–dc converter can deliver the active/reactive power from the EV battery to the grid. In this situation, the battery charger achieves vehicle-to-grid (V2G) scenario. That is to say, the bidirectional power flow is necessary for the dc–dc converter. It should be noticed that the galvanic isolation feature is usually considered for the dc–dc converter.

Several types of power converters provide the ability of bidirectional power flow and the galvanic isolation, such as the dual active bridge (DAB) converter [2], the phase-shift full-bridge (PSFB) converter [3], and the *LLC/CLLC* resonant converter [4], [5]. For the DAB and the PSFB converter, there is no need to include extra resonant tanks. Therefore, the number of circuit components can be reduced. However, due to linear current feature, the switching losses might be increased. On the other hand, two individual resonant tanks are included in the *CLLC* converter, whereas it provides better bidirectional power flow capability. In addition, with *CLLC* converter, it will be easier to achieve the zero-voltage switching (ZVS) or the zero-current switching (ZCS) under the full load operation. Consequently, the switching frequency and power density of the *CLLC* resonant converter can be increased.

In general, the pulse frequency modulation (PFM) is adopted for the *CLLC* resonant converter. The switching frequency will dynamically be modified to regulate the output voltage/current. However, the range of the switching frequency will be increased to achieve wide output voltage range and full load operation. As a result, there will be challenges when designing the magnetizing components [6]. Moreover, under a high-frequency operation, the input/output voltage gain might be diverged with PFM because of the parasitic effect [7].

To solve this issue, the integration of PFM and phase-shift modulation (PSM) was introduced and developed [8], [9], [10], [11], [12]. First, the hybrid modulation of PFM and PSM was proposed in [8] and [9] to achieve the wide output voltage range of the *LLC* resonant converter. Besides, operating principles of PSM were also presented in these two works. In [10], a synchronous rectification advance on-time method was proposed. With this method, the lagging leg switches can achieve ZVS when the *LLC* resonant converter operates in PSM. In addition, a loss optimization method for phase-shifted *LLC* resonant

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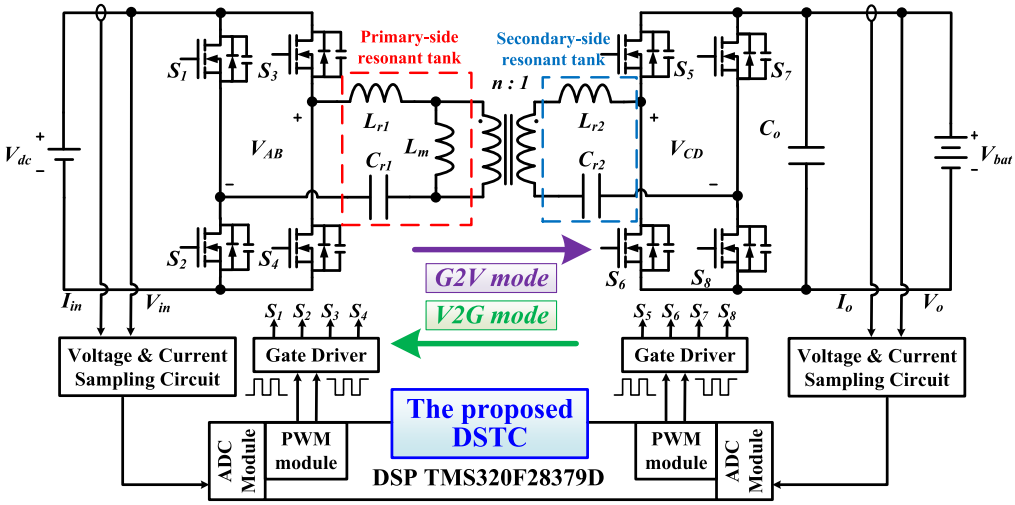


Fig. 1. Circuit diagram of the CLLC resonant converter.

converters was presented in [11]. This approach can reduce the circuit losses according to different circuit specifications and parameters. In [12], an interleaved *LLC* resonant converter with PSM was proposed to achieve the output voltage range from 10 to 420 V. Although these methods are effective, the optimization of the switching between PFM and PSM are not considered and revealed.

In this letter, the hybrid modulation is adopted for the *CLLC* resonant converter. The PFM and PSM can be switched according to different output voltage and load levels. Moreover, in order to suppress the voltage fluctuation and to improve the transient response during the mode switching, the dynamic smooth transition control (DSTC) is proposed in this letter. Besides, a feedforward voltage controller is developed in the DSTC to enhance the circuit performance. Finally, 2-kW prototype *CLLC* circuits with experiments will be presented to verify the performance and feasibility of the proposed DSTC. Experimental results show that the peak efficiency of the converter is 96.7%, whereas the improvement of the voltage fluctuation and the transient response time during the mode switching are equal to 50% and 42%, respectively.

## II. CLLC Resonant Converter With PFM and PSM

Fig. 1 shows the circuit diagram of the full-bridge type *CLLC* resonant converter. It can be seen that two individual resonant tanks are included in the circuit. The transformer provides the galvanic isolation feature between the input and output. The dynamic smooth transition control (DSP) TMS320F28379D is utilized as the system controller, whereas the proposed DSTC can be realized by the DSP.

Generally, the *CLLC* resonant converter is controlled with PFM. The switching frequency will be regulated to control the output voltage/current. Fig. 2 shows gain curves of the *CLLC* resonant converter. From Fig. 2, it can be confirmed that the slopes of gain curves with PFM will be flat under high switching frequency. Therefore, it will be difficult to regulate the output voltage/current under low output voltage and light load

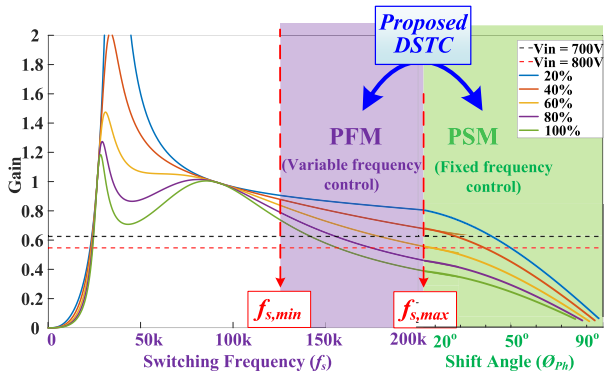


Fig. 2. Gain curves of the CLLC resonant converter with the hybrid modulation.

condition. To solve this issue, the PSM was introduced [13], [14]. With the integration of PFM and PSM, the converter can be well regulated under the wide output voltage and the full load operation.

Fig. 3 shows theoretical waveforms of PSM. $V_{gs1}$, $V_{gs2}$, $V_{gs3}$ and $V_{gs4}$ represent gate signals of $S_1$, $S_2$, $S_3$, and $S_4$, respectively. In Fig. 3, the phase of $V_{gs3}$ and $V_{gs4}$ leads the phase of $V_{gs1}$ and $V_{gs2}$. Therefore, $S_3$ and $S_4$ are defined as the leading leg while the $S_1$ and $S_2$ are defined as the lagging leg. Different from the PFM, the switching frequency of the PSM is fixed. Besides, the phase-shift angle $\emptyset_{Ph}$ between the leading leg switches and the lagging leg switches should be controlled. With the regulation of $\emptyset_{Ph}$, the output voltage/current can effectively be controlled under low output voltage and light load condition. However, lagging leg switches will be harder to achieve ZVS because of the resonant current reduction. Therefore, the hybrid modulation is adopted in this letter. Under high output voltage and heavy load condition, the converter operates in PFM mode. On the contrary, the converter operates in PSM mode under low output voltage and light load condition.

The voltage gain function of PFM and PSM are expressed in (1) and (2) shown at the bottom of the next page, respectively.

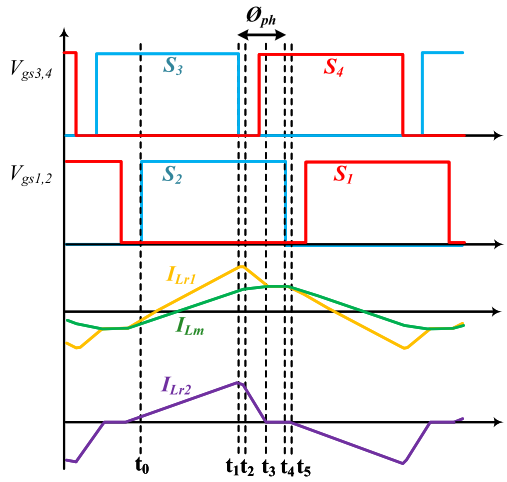


Fig. 3. Theoretical waveforms of the PSM.

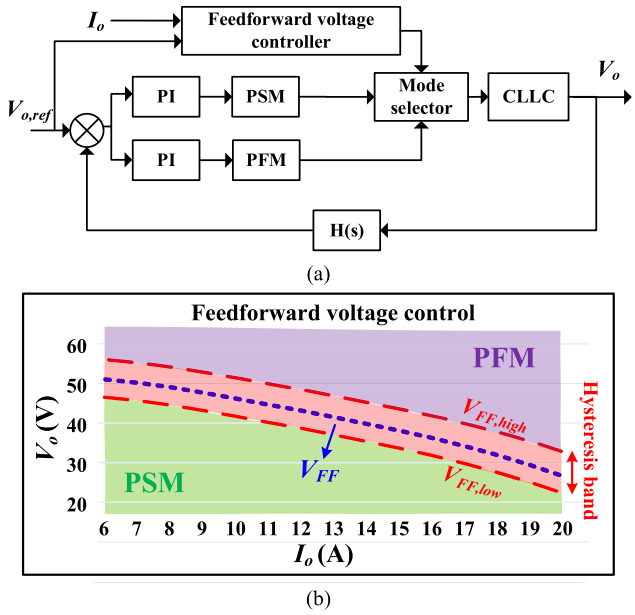


Fig. 4. (a) Control block diagram of the proposed DSTC. (b) Conceptual diagram of the feedforward voltage controller.

The quality factor $Q$, the $K$ factor, the first resonant frequency $f_{r1}$, the coefficients $a$ and $b$, the resonance angular frequency $\omega_r$, and the characteristic impedance $Z_r$ are defined in (3) shown at the bottom of this page. $L_{r1}$ and $C_{r1}$ represent the high voltage side resonant inductance and resonant capacitance, respectively. $L_{r2}$ and $C_{r2}$ are the low voltage side resonant inductance and the resonant capacitance, respectively. $n$ is the transformer turns ratio. $R_o$ is the load resistance. $L_m$ is the magnetizing inductance. $D_1$ is the overlapped conducting period of $S_2$ and $S_3$. $D_2$ represents the current conducting period of the low voltage side.

## III. Proposed Dynamic Smooth Transition Control

The hybrid modulation can achieve wide output voltage range and full load operation. Unfortunately, a certain response time and unavoidable voltage fluctuations will be occurred during the switching transient between the PFM and PSM. In order to suppress the voltage fluctuation and to improve the transient response during the mode switching, the DSTC is proposed.

Fig. 4(a) shows the control block diagram of the proposed DSTC. First, the reference output voltage, $V_{o,\mathrm{ref}}$, should be defined. Then, the selection of PFM or PSM will be determined by the mode selector according to different output voltage levels and load conditions. It is worth mentioning that two proportional–integral (PI) controllers are adopted for PFM and PSM. H(s) is the feedback sensor gain. Moreover, in order to achieve the proposed DSTC, a feedforward voltage controller is included in the control loop. Both $V_{o,\mathrm{ref}}$ and $I_o$ will be fed into the feedforward voltage controller. The conceptual diagram of the feedforward voltage controller is illustrated in Fig. 4(b). It can be seen that a feedforward voltage line ($V_{FF}$) is depicted in Fig. 4(b). A hysteresis band of $V_{FF}$ is included to prevent the mode switching bounces. $V_{FF,\mathrm{high}}$ and $V_{FF,\mathrm{low}}$ represent the upper and the lower bound of the hysteresis band, respectively. It is worth mentioning that the boundary $V_{FF,\mathrm{high}}$ and $V_{FF,\mathrm{low}}$ are determined by the tolerance of the resonant inductance and the resonant capacitance. In this letter, the tolerance of the resonant inductance and the resonant capacitance are set as 5%. However, $V_{FF,\mathrm{high}}$ and $V_{FF,\mathrm{low}}$ and the tolerance can be adjusted according to different considerations.

The flowchart of the hybrid modulation without the proposed DSTC is presented in Fig. 5(a). From Fig. 5(a), it can be confirmed that there will be three stages of the mode switching procedure. For instance, if the circuit is operated from PFM to PSM, the switching frequency is increased to the maximum switching frequency (200 kHz). After $T$ times counting, the

$$\frac{nV_o}{V_{dc}} = \left\{ \sqrt{\left(\frac{1}{K}+1-\frac{f_{r1}^2}{f_s^2 K}\right)^2 + \left[\frac{f_s}{f_{r1}}Q\left(1+\frac{a}{K}+a\right) - \frac{f_{r1}Q}{f_s}\left(1+\frac{1}{b}+\frac{1}{bK}+\frac{a}{K}\right) + \frac{f_{r1}^3 Q}{f_s^3 bK}\right]^2} \right\}^{-1} \quad \text{(PFM)} \tag{1}$$

$$\frac{nV_o}{V_{dc}} = \frac{R_o \cdot \frac{K}{1+2K}}{\frac{Z_r}{\sin(\omega_r \cdot D_1 T_S)\cdot D_2} - \frac{T_s}{4\cdot C_{r2}} + R_o \cdot \left(1-\frac{K}{1+2K}\right)} \quad \text{(PSM)} \tag{2}$$

$$Q = \frac{\sqrt{\frac{L_{r1}}{C_{r1}}}}{\frac{8n^2}{\pi^2}\cdot R_o},\ K = \frac{L_m}{L_{r1}},\ f_{r1} = \frac{1}{2\pi\sqrt{L_{r1}\cdot C_{r1}}},\ a = \frac{n^2 L_{r2}}{L_{r1}},\ b = \frac{C_{r2}}{n^2 C_{r1}},\ \omega_r = \frac{1}{\sqrt{L_{r1}C_{r1}}},\ Z_r = \sqrt{\frac{L_{r1}}{C_{r1}}}. \tag{3}$$

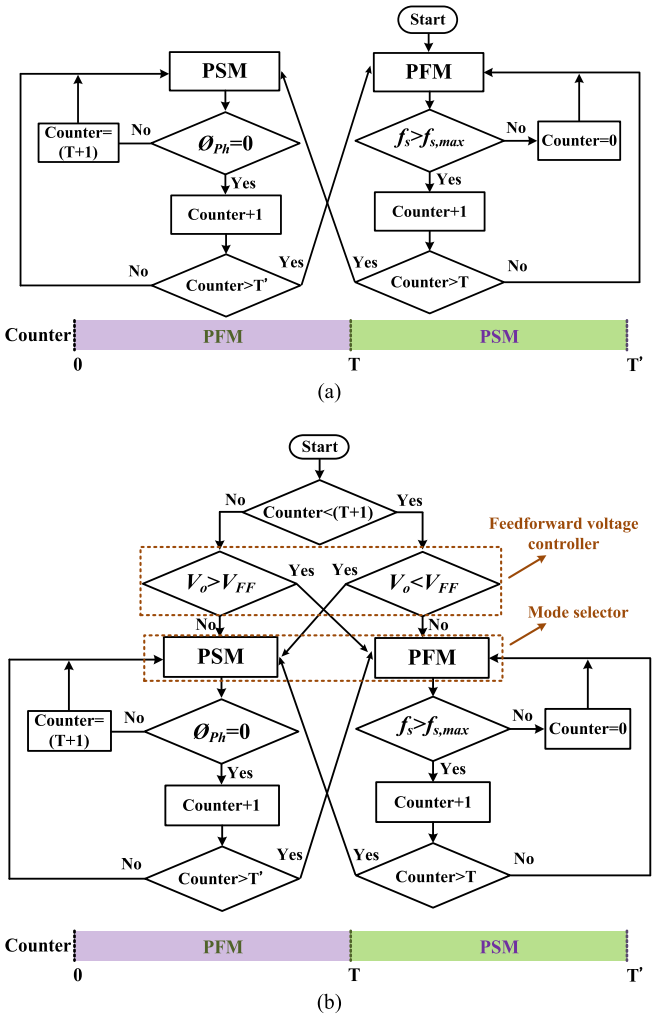


Fig. 5. Flowchart of the hybrid modulation. (a) Without the proposed DSTC. (b) With the proposed DSTC.

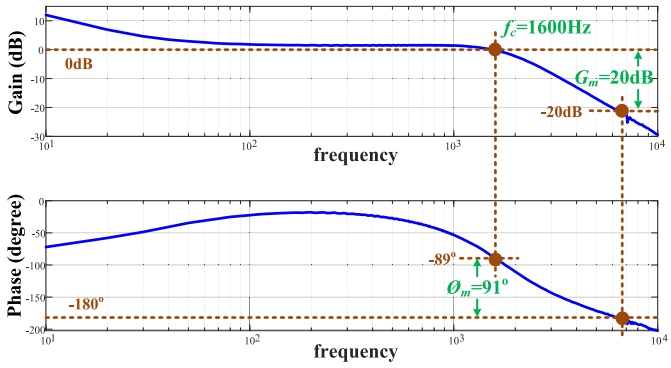


Fig. 6. Frequency response Bode plots of the system controller under the full load operation.

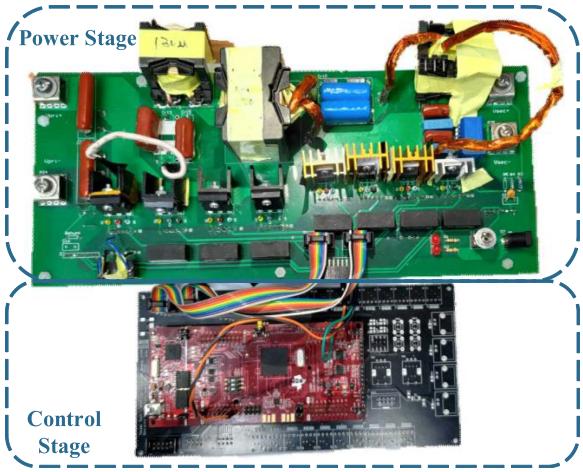


Fig. 7. CLLC prototype circuit figure.

operating mode can be switched to PSM. A certain period of the mode switching is required, whereas the mode switching period increases not only the response time but also the voltage fluctuation.

In order to solve this issue, the DSTC is proposed. The flowchart of the hybrid modulation with the proposed DSTC is shown in Fig. 5(b). With the DSTC, a feedforward voltage controller and the mode selector are included. If $V_o$ is greater than $V_{FF}$, the converter operates in PFM mode. On the contrary, if $V_o$ is smaller than $V_{FF}$, the converter operates in PSM mode. If the condition of $V_o$ and $I_o$ remain unchanged, the operating mode will not be changed. However, the mode will be switched when $V_o$ and $I_o$ conditions are changed. If $V_o$ is decreased and $f_s$ is lower than the maximum switching frequency limitation, $f_{s,\max}$, the converter remains operating in PFM. However, if $f_s$ is higher than $f_{s,\max}$, the operating mode should be switched from PFM to PSM. On the other hand, if $V_o$ is increased and $\emptyset_{Ph}$ is not zero, the converter remains operating in PSM. However, if $\emptyset_{Ph}$ is equal to zero, the operating mode should be switched from PSM to PFM. It is worth mentioning that a counter is included for preventing bounces during the mode switching transient. With the DSTC, $V_o$ and $I_o$ will be sensed and controlled in advance before the mode switching. Therefore, the mode switching period can be reduced while the transient response can be improved.

It should be noticed that the selection of PFM or PSM is not based on the power flow direction. Instead, the operating of PFM and PSM is determined by $V_o$, $I_o$, and the switching frequency. For instance, if the calculated switching frequency is higher than the predefined maximum switching frequency (200 kHz), the operating mode will be changed from PFM mode to PSM mode. It is independent of the power flow direction. That is to say, the hybrid modulation (PFM+PSM) and the proposed strategy can be utilized for both G2V and V2G scenarios. Therefore, Fig. 5 can be adopted for different power flow directions.

Finally, the frequency response Bode plots of the system controller under the full load operation are shown in Fig. 6. The PI controller gains have been included. It can be confirmed that the bandwidth is 1600 Hz. The gain margin and phase margin are 20 dB and 91°, respectively.

## IV. Experimental Results

In order to verify the performance and feasibility of the proposed circuit and DSTC strategy, a 2-kW prototype circuit with

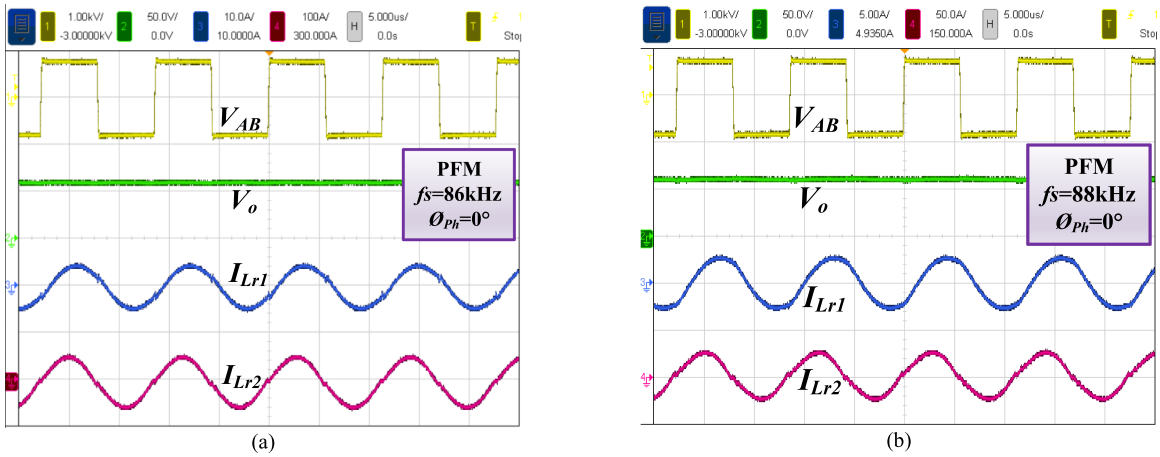


Fig. 8. Steady-state experimental waveforms of the PFM mode under $V_o = 60$ V. (a) 100% load condition. (b) 50% load condition.

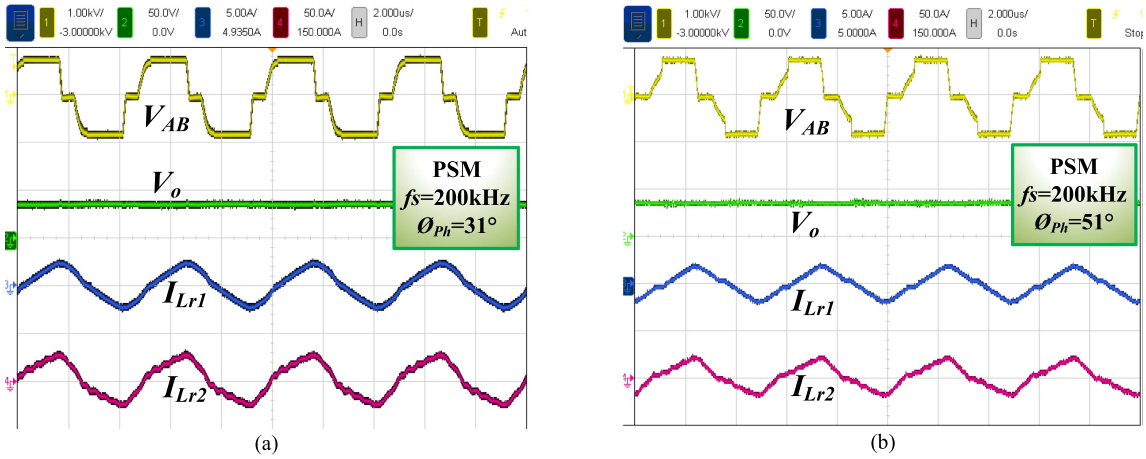


Fig. 9. Steady-state experimental waveforms of the PSM mode under $V_o = 35$ V. (a) 25% load condition. (b) 15% load condition.

experimental results will be presented in this section. Circuit specifications are shown in Table I. The prototype circuit figure is shown in Fig. 7.

Fig. 8 shows the steady-state experimental waveforms of the PFM mode under $V_o = 60$ V. Waveforms of the high-voltage side voltage $V_{AB}$, the output voltage $V_o$, the high-voltage side resonant current $I_{Lr1}$, and the low-voltage side resonant current $I_{Lr2}$ are presented. Fig. 8(a) shows waveforms of the 100% load condition when $V_o$ is 60 V. In this case, $I_o$ is 33 A and $f_s$ is 86 kHz. Fig. 8(b) shows waveforms of the 50% load condition when $V_o$ is 60 V. In this case, $I_o$ is 16.5 A and $f_s$ is 88 kHz. It is worth mentioning that only PFM mode is selected in Fig. 8. Therefore, $\emptyset_{Ph}$ is set as 0° in these two scenarios.

Fig. 9 shows the steady-state experimental waveforms of the PSM mode under $V_o = 35$ V. Waveforms of $V_{AB}$, $V_o$, $I_{Lr1}$, and $I_{Lr2}$ are presented. Fig. 9(a) shows waveforms of the 25% load condition when $V_o$ is 35 V. In this case, $I_o$ is 15 A and $\emptyset_{Ph}$ is 31°. Fig. 9(b) shows waveforms of the 15% load condition when $V_o$ is 35 V. In this case, $I_o$ is 10 A and $\emptyset_{Ph}$ is 51°. It should be noticed that only PSM mode is adopted in Fig. 9. Therefore, $f_s$ is fixed at 200 kHz in these two scenarios.

TABLE I
CIRCUIT SPECIFICATIONS OF THE CLLC RESONANT CONVERTER

| Parameters | Value or type |
|---|---|
| Rated power, $P_o$ | 2000 W |
| DC-link voltage, $V_{DC}$ | 700 – 800 V |
| Output voltage, $V_o$ | 35 – 60 V |
| Rated load current, $I_o$ | 33.3 A |
| Dominate resonant frequency, $f_{rl}$ | 86 kHz |
| Switching frequency, $f_s$ | 70 – 200 kHz |
| Phase-shift angle, $\emptyset_{Ph}$ | 10° – 80° |
| Transformer turns ratio, $n$ | 12.5 |
| Primary-side resonant inductance, $L_{rl}$ | 153 $\mu$H |
| Primary-side resonant capacitance, $C_{rl}$ | 22.4 nF |
| Magnetizing inductance, $L_m$ | 803 $\mu$H |
| Secondary-side resonant inductance, $L_{r2}$ | 920 nH |
| Secondary-side resonant capacitance, $C_{r2}$ | 3.4 $\mu$F |
| Switches of $S_1$, $S_2$, $S_3$, $S_4$ | SCT3040KL |
| Switches of $S_5$, $S_6$, $S_7$, $S_8$ | IPP051N15N5 |
| System controller | DSP TMS320F28379D |

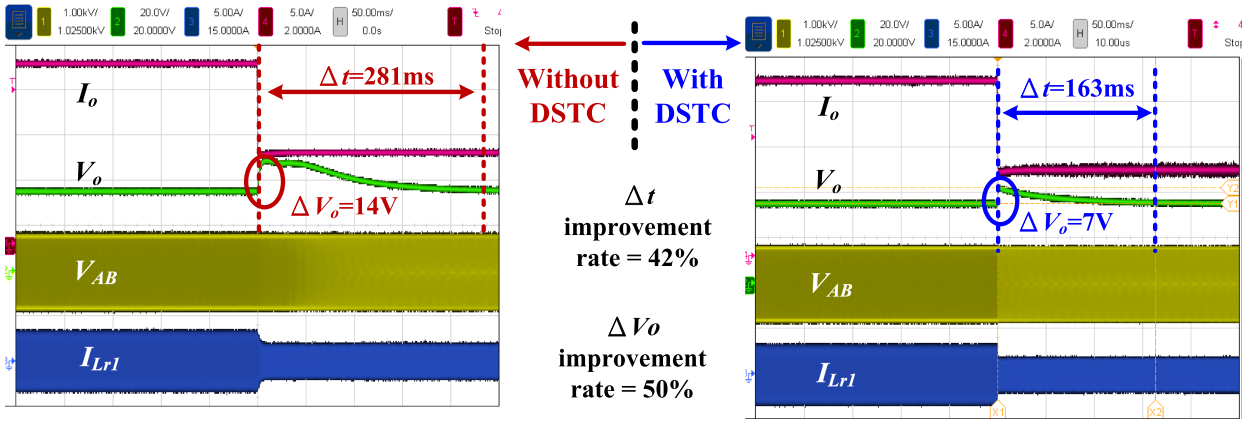


Fig. 10. Experimental waveforms of the load decreasing scenario.

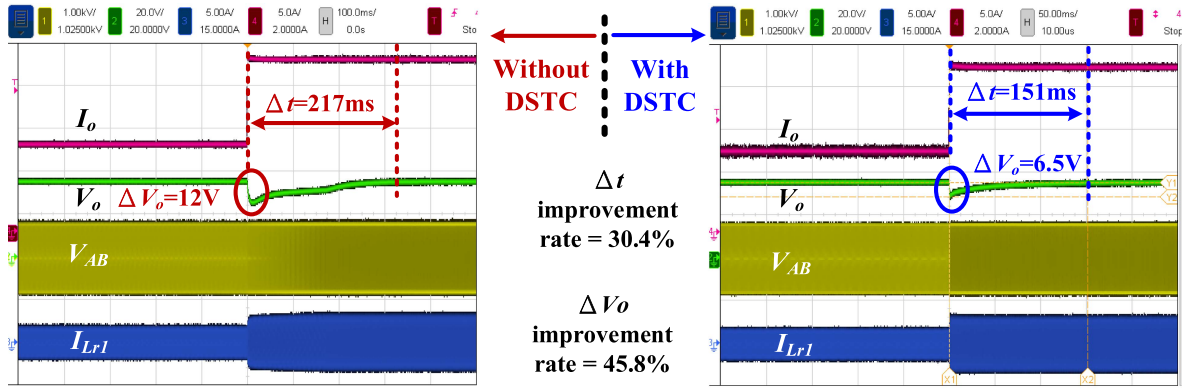


Fig. 11. Experimental waveforms of the load increasing scenario.

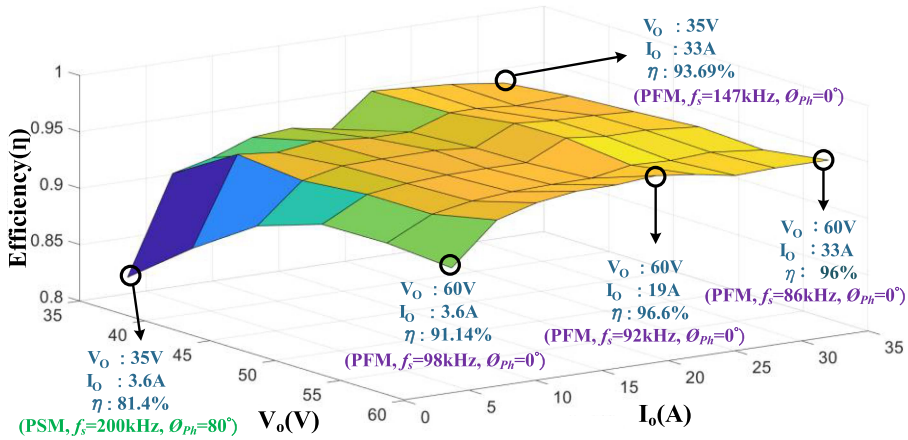


Fig. 12. Overall circuit efficiency under different output voltages and load conditions.

Fig. 10 demonstrates the experimental results of the load decreasing scenario. It can be seen that the load-changing transient response time and the overshoot voltage without the DSTC are measured as 281 ms and 14 V, respectively. On the contrary, with the proposed DSTC, the load-changing transient response time and the overshoot voltage are supresssed with 163 ms and 7 V, respectively. Under this scenario, the transient response is improved with 42% while the overshoot voltage is eliminated with 50%.

On the other hand, experimental results of the load increasing scenario are shown in Fig. 11. It can be confirmed that the load-changing transient response time and the undershoot voltage

without the DSTC are measured as 217 ms and 12 V, respectively. However, the load-changing transient response time and the undershoot voltage are supresssed with 151 ms and 6.5 V with the proposed DSTC. Under this scenario, the transient response is improved with 30.4% while the undershoot voltage is eliminated with 45.8%.

In Figs. 10 and 11, the period between the load changing instant and the $V_o$ recovery instant is captured and calculated to measure the transient response time $\Delta t$. On the other hand, under the condition of constant output current, $V_o$ will be changed when the load is varied. Under this situation, the overshoot/undershoot phenomenon of $I_o$ will occur and a certain transient response time is required. Theoretically, the proposed strategy is still effective to suppress the overshoot/undershoot of $I_o$ and to reduce the transient response time. However, the battery is considered for the low voltage side in this letter. For the characteristic of the battery, the battery voltage will not be changed instantaneously. Therefore, only conditions of constant output voltage with variable load currents are considered and realized in the experiments.

Eventually, the overall circuit efficiency under different output voltages and load conditions is shown in Fig. 12. The maximum circuit efficiency is 96.7% with $V_o = 60$ V/$I_o = 19$ A. In this case, the circuit is operated in PFM and $f_s$ is 92 kHz. The circuit efficiency under the full load operation is 96%.

## V. Conclusion

In this letter, the hybrid modulation integrated with PFM and PSM is considered for bidirectional *CLLC* resonant converters. Besides, a DSTC strategy is proposed to suppress the voltage fluctuation and to reduce the response time during the mode switching transient. A feedforward voltage controller is developed in the DSTC to enhance the circuit performance. The proposed control strategies can be realized by DSPs without adding extra circuit and components. Finally, experimental results obtained from a 2-kW prototype circuit verify the performance and feasibility of the proposed DSTC. From the experimental validations, the voltage fluctuation and the transient response time can be improved with 42% and 50%, respectively. The peak circuit conversion efficiency is 96.7%.

## References


[1] Y. Cao, M. Ngo, N. Yan, D. Dong, R. Burgos, and A. Ismail, "Design and implementation of an 18-kW 500-kHz 98.8% efficiency high-density battery charger with partial power processing," *IEEE J. Emerg. Sel. Topics Ind. Electron.*, vol. 10, no. 6, pp. 7963–7975, Dec. 2022.

[2] J. Hu, S. Cui, and R. W. De Doncker, "Natural boundary transition and inherent dynamic control of a hybrid-mode-modulated dual-active-bridge converter," *IEEE Trans. Power Electron.*, vol. 37, no. 4, pp. 3865–3877, Apr. 2022.

[3] G. Liu et al., "An improved zero-voltage and zero-current-switching phase-shift full-bridge PWM converter with low output current ripple," *IEEE Trans. Power Electron.*, vol. 38, no. 3, pp. 3419–3432, Mar. 2023.

[4] Y. Cao, M. Ngo, R. Burgos, A. Ismail, and D. Dong, "Switching transition analysis and optimization for bidirectional CLLC resonant DC transformer," *IEEE Trans. Power Electron.*, vol. 37, no. 4, pp. 3786–3800, Apr. 2022.

[5] C. - Y. Tang, H. - J. Wu, C. - Y. Liao, and H. - H. Wu, "An optimal frequency-modulated hybrid MPPT algorithm for the LLC resonant converter in PV power applications," *IEEE Trans. Power. Electron.*, vol. 37, no. 1, pp. 944–954, Jan. 2022.

[6] Y. Wei, Q. Luo, X. Sun, and H. Alan Mantooth, "An LLC converter with multiple operation modes for wide voltage gain range application," *IEEE Trans. Ind. Electron.*, vol. 68, no. 11, pp. 11111–11124, Nov. 2021.

[7] J.-H. Kim, C.-E. Kim, J.-K. Kim, and G. - W. Moon, "Analysis for LLC resonant converter considering parasitic components at very light load condition," in *Proc. 8th Int. Conf. Power Electron. Asia*, 2011, pp. 1863–1868.

[8] Y. Zhansen, W. Jun, M. Hao, and D. Jianhua, "A wide output voltage LLC series resonant converter with hybrid mode control method," in *Proc. IEEE 2nd Int. Future Energy Electron. Conf.*, 2015, pp. 1–5.

[9] B. McDonald and F. Wang, "LLC performance enhancements with frequency and phase shift modulation control," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2014, pp. 2036–2040.

[10] J. - Y. Lin, H.-Y. Yueh, Y.-F. Lin, and P. - H. Liu, "Variable-frequency and phase-shift with synchronous rectification advance on-time hybrid control of LLC resonant converter for electric vehicles charger," *IEEE J. Emerg. Sel. Topics Ind. Electron.*, vol. 4, no. 1, pp. 348–356, Jan. 2023.

[11] U. Mumtahina and P. J. Wolfs, "Multimode optimization of the phase shifted LLC series resonant converter," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10478–10489, Dec. 2018.

[12] B. Xue, H. Wang, J. Liang, Q. Cao, and Z. Li, "Phase-shift modulated interleaved LLC converter with ultrawide output voltage range," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 493–503, Jan. 2021.

[13] Y. Xiao, Z. Zhang, S. You, and M. Xingkui, "New hybrid control for wide input full-bridge LLC resonant DC/DC converter," in *Proc. 3rd Int. Conf. Intell. Green Building Smart Grid*, 2018, pp. 1–4.

[14] L. Shi, B. Liu, X. Sun, and S. Duan, "Burst-mode and phase-shift hybrid control method of LLC converters for wide output range applications," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 1013–1023, Feb. 2020.